NEC

MOS INTEGRATED CIRCUIT
μPD705102

V832™
32-BIT MICROPROCESSOR

DESCRIPTION

The μPD705102 (V832) is a 32-bit RISC microprocessor for embedded control applications, with a high-performance 32-bit V830™ processor core and many peripheral functions such as an SDRAM/ROM controller, 4-channel DMA controller, real-time pulse unit, serial interface, interrupt controller, and power management.

In addition to a high interrupt response speed and optimized pipeline structure, the V832 offers sum-of-products operation instructions, concatenated shift instructions, and high-speed branch instructions to realize multimedia functions, and therefore can provide high performance in multimedia systems such as Internet/intranet systems, car navigation systems, digital still cameras, and color faxes.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V832 User's Manual Hardware:	**U13577E**
V830 Family™ User's Manual Architecture:	**U12496E**

FEATURES

- CPU function
  - V830-compatible instructions
  - Instruction cache: 4 KB
  - Instruction RAM: 4 KB
  - Data cache: 4 KB
  - Data RAM: 4 KB
  - Minimum instruction execution cycle number : 1 cycle
  - Number of general-purpose registers: 32 bits × 32
  - Memory space and I/O space: 4 GB each
- Interrupt/exception processing function
  - Non-maskable: External input: 1
  - Maskable: External input: 8 (of which 4 are multiplexed with internal sources)
    Internal source: 11 types
- Bus control function
- Wait control function
- Memory access control function
- On-chip DMA controller: 4 channels
- Serial interface function
  - Asynchronous serial interface (UART): 1 channel
  - Clocked serial interface (CSI): 1 channel
  - Dedicated baud rate generator (BRG): 1 channel
- Timer/counter function
  - 16-bit timer/event counter: 1 channel
  - 16-bit interval timer: 1 channel
- Port function: 21 (I/O) ports
- Clock generation function: PLL clock synthesizer (×6 or ×8 multiplication)
- Standby function (HALT, STOP, and power management modes)
- Debug function
  - Debug-dedicated synchronous serial interface: 1 channel
  - Trace-dedicated interface: 1 channel

Document No. U13675EJ4V0DS00 (4th edition)
Date Published February 2001 N CP(K)
Printed in Japan

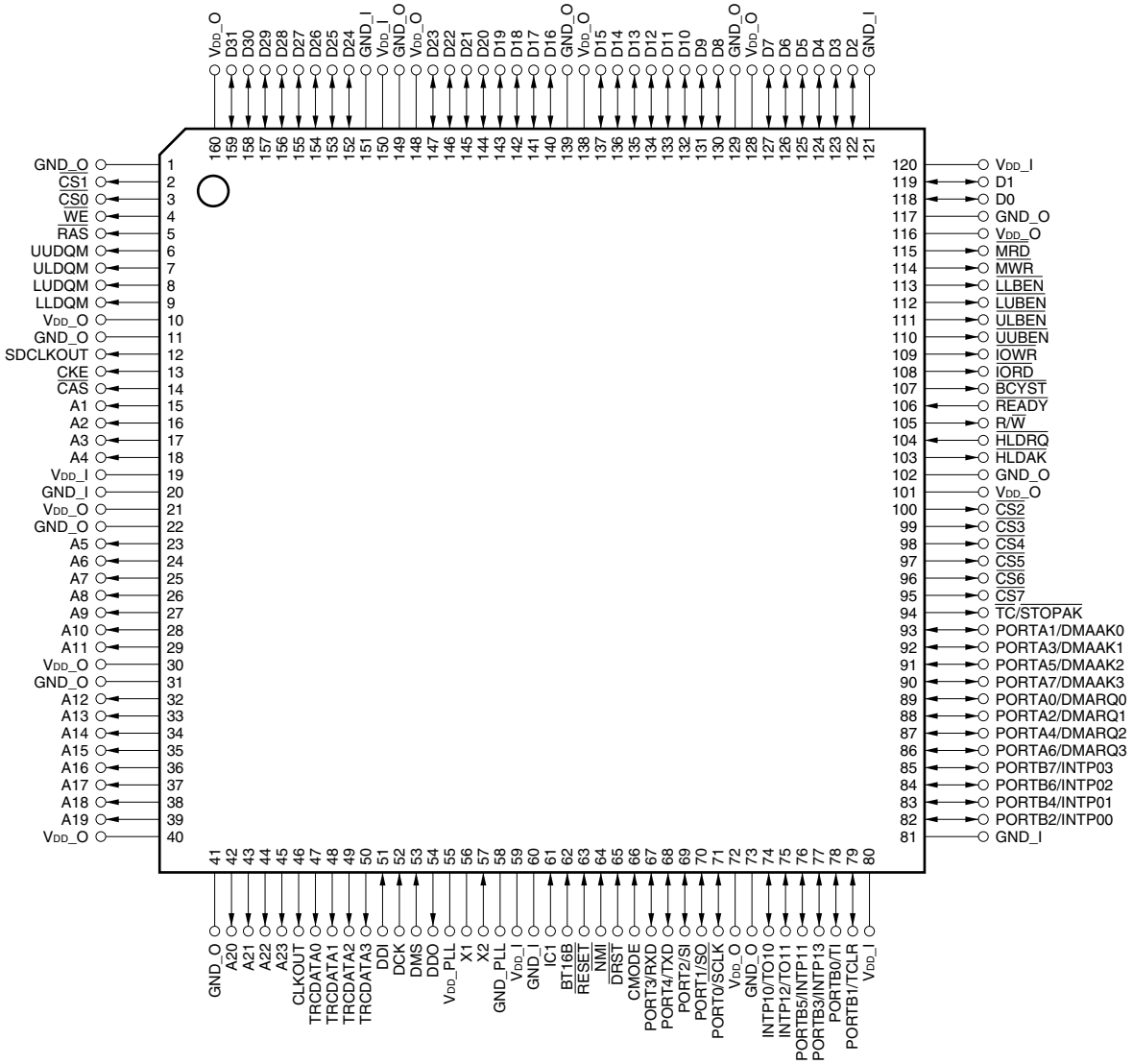
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD705102GM-143-8ED	160-pin plastic LQFP (fine pitch) (24 × 24)
μPD705102GM-133-8ED	160-pin plastic LQFP (fine pitch) (24 × 24)

PIN CONFIGURATION (TOP VIEW)

- 160-pin plastic LQFP (fine pitch) (24 × 24)
  μPD705102GM-143-8ED
  μPD705102GM-133-8ED

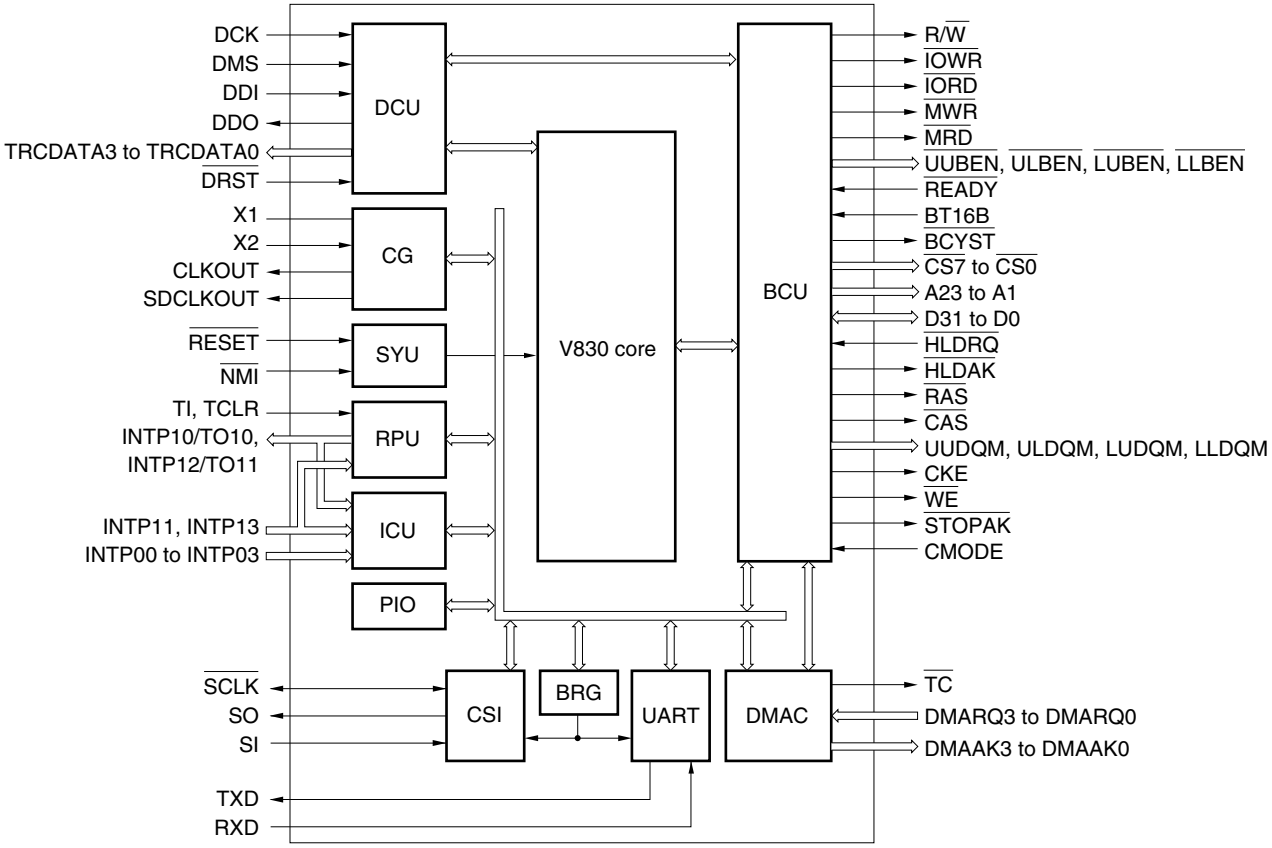


Caution Directly connect the IC1 (Internally connected 1) pin to GND_O.

PIN NAMES

A1 to A23: Address bus
$\overline{BCYST}$: Bus cycle start
BT16B: Boot bus size 16-bit
$\overline{CAS}$: Column address strobe
CKE: Clock enable
CLKOUT: Clock out
CMODE: Clock mode
$\overline{CS0}$ to $\overline{CS7}$: Chip select
D0 to D31: Data bus
DCK: Debug clock
DDI: Debug data input
DDO: Debug data output
DMAAK0 to DMAAK3: DMA acknowledge
DMARQ0 to DMARQ3: DMA request
DMS: Debug mode select
$\overline{DRST}$: Debug reset
GND_I: Ground
GND_O: Ground
GND_PLL: PLL ground
$\overline{HLDAK}$: Hold acknowledge
$\overline{HLDRQ}$: Hold request
IC1: Internally connected
INTP00 to INTP03, INTP10 to INTP13: Interrupt request from peripheral
$\overline{IORD}$: I/O read
$\overline{IOWR}$: I/O write
$\overline{LLBEN}$: Lower lower byte enable
LLDQM: Lower lower DQ mask enable
$\overline{LUBEN}$: Lower upper byte enable
LUDQM: Lower upper DQ mask enable
$\overline{MRD}$: Memory read
$\overline{MWR}$: Memory write
$\overline{NMI}$: Non-maskable interrupt request
PORT0 to PORT4, PORTA0 to PORTA7, PORTB0 to PORTB7: Port
R/$\overline{W}$: Bus read or write status
$\overline{RAS}$: Row address strobe
$\overline{READY}$: Ready
$\overline{RESET}$: Reset
RXD: Receive data
$\overline{SCLK}$: Serial clock
SDCLKOUT: SDRAM clock out
SI: Serial input
SO: Serial output
$\overline{STOPAK}$: Stop acknowledge
$\overline{TC}$: Terminal count
TCLR: Timer clear
TI: Timer input
TO10, TO11: Timer output
TRCDATA0 to TRCDATA3: Trace data
TXD: Transmit data
$\overline{ULBEN}$: Upper lower byte enable
ULDQM: Upper lower DQ mask enable
$\overline{UUBEN}$: Upper upper byte enable
UUDQM: Upper upper DQ mask enable
V_{DD}_I: Power supply (2.5 V)
V_{DD}_O: Power supply (3.3 V)
V_{DD}_PLL: PLL power supply (2.5 V)
$\overline{WE}$: Write enable
X1, X2: Crystal oscillator

INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

Pin Name	I/O	Function	Alternate Function
PORT0	Schmitt I/O	PORT 5-bit I/O port. Input/output can be specified in 1-bit units.	$\overline{SCLK}$
PORT1	I/O		SO
PORT2	Schmitt I/O		SI
PORT3			RXD
PORT4	I/O		TXD
PORTA0	I/O	PORTA 8-bit I/O port. Input/output can be specified in 1-bit units.	DMARQ0
PORTA1			DMAAK0
PORTA2			DMARQ1
PORTA3			DMAAK1
PORTA4			DMARQ2
PORTA5			DMAAK2
PORTA6			DMARQ3
PORTA7			DMAAK3
PORTB0	I/O	PORTB 8-bit I/O port. Input/output can be specified in 1-bit units.	TI
PORTB1			TCLR
PORTB2			INTP00
PORTB3			INTP13
PORTB4			INTP01
PORTB5			INTP11
PORTB6			INTP02
PORTB7			INTP03

1.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
D0 to D31	3-state I/O	Data bus	—
A1 to A23	3-state output	Address bus	—
$\overline{\text{READY}}$	Input	End of bus cycle enable	—
$\overline{\text{HLDRQ}}$	Input	Bus hold request	—
$\overline{\text{HLDAK}}$	Output	Bus hold enable	—
$\overline{\text{MRD}}$	3-state output	Memory read strobe	—
$\overline{\text{UUBEN}}$		Byte enable output (most significant byte: D31 to D24)	—
$\overline{\text{ULBEN}}$		Byte enable output (enables second byte: D23 to D16)	—
$\overline{\text{LUBEN}}$		Byte enable output (enables third byte: D15 to D8)	—
$\overline{\text{LLBEN}}$		Byte enable output (enables least significant byte: D7 to D0)	—
$\overline{\text{IORD}}$		I/O read strobe	—
$\overline{\text{IOWR}}$		I/O write strobe	—
$\overline{\text{MWR}}$		Memory write strobe	—
BT16B	Input	$\overline{\text{CS7}}$ space bus size setting	—
$\overline{\text{BCYST}}$	3-state output	Bus cycle start output	—
R/$\overline{\text{W}}$		R/W output	—
$\overline{\text{RESET}}$	Input	Reset input	—
X1	—	Crystal resonator connection (left open when external clock input)	—
X2	Schmitt input	Crystal resonator connection/external clock input	—
CLKOUT	Output	Bus clock output	—
CMODE	Input	PLL multiplication factor setting (×6, ×8)	—
$\overline{\text{CS2}}$, $\overline{\text{CS7}}$	3-state output	Memory chip select output	—
$\overline{\text{CS3}}$ to $\overline{\text{CS6}}$		Memory I/O chip select output	—
$\overline{\text{STOPAK}}$	Output	STOP mode report output	$\overline{\text{TC}}$
INTP10	Input	Maskable interrupt inputs	TO10
INTP11			PORTB5
INTP12			TO11
INTP13			PORTB3
INTP00			PORTB2
INTP01			PORTB4
INTP02			PORTB6
INTP03			PORTB7
$\overline{\text{NMI}}$		Non-maskable interrupt input	—
$\overline{\text{RAS}}$	3-state output	SDRAM $\overline{\text{RAS}}$ strobe	—
UUDQM		DQ mask enable (most significant byte: D31 to D24)	—
ULDQM		DQ mask enable (second byte: D23 to D16)	—
LUDQM		DQ mask enable (third byte: D15 to D8)	—
LLDQM		DQ mask enable (least significant byte: D7 to D0)	—

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{WE}$	3-state output	SDRAM write strobe	—
$\overline{CAS}$		SDRAM $\overline{CAS}$ strobe	—
$\overline{CS0}$		SDRAM chip select	—
$\overline{CS1}$		SDRAM/SRAM (ROM) chip select	—
CKE		SDRAM clock enable	—
SDCLKOUT	Output	SDRAM clock output	—
★ DMARQ0	Input	DMA requests (CH0 to CH3)	PORTA0
★ DMARQ1			PORTA2
★ DMARQ2			PORTA4
★ DMARQ3			PORTA6
★ DMAAK0	Output	DMA enable (CH0 to CH3)	PORTA1
★ DMAAK1			PORTA3
★ DMAAK2			PORTA5
★ DMAAK3			PORTA7
$\overline{TC}$		DMA transfer end output	$\overline{STOPAK}$
TO10		Timer 1 output	INTP10
TO11			INTP12
TCLR	Input	Timer 1 clear, start input	PORTB1
TI		Timer 1 count clock input	PORTB0
RXD	Schmitt input	UART data input	PORT3
TXD	Output	UART data output	PORT4
$\overline{SCLK}$	Schmitt I/O	CSI clock I/O	PORT0
SI	Schmitt input	CSI data input	PORT2
SO	Output	CSI data output	PORT1
DCK	Schmitt input	Debug clock input	—
DDI	Input	Debug data input	—
DDO	Output	Debug data output	—
DMS	Input	Debug mode select	—
$\overline{DRST}$		DCU reset input	—
TRCDATA0 to TRCDATA3	Output	Trace data output	—
V_{DD}_I	—	Positive power supply (2.5 V)	—
V_{DD}_O		Positive power supply (3.3 V)	—
GND_I		Ground potential (2.5 V)	—
GND_O		Ground potential (3.3 V)	—
V_{DD}_PLL		PLL (internal clock generator) positive power supply (2.5 V)	—
GND_PLL		PLL (internal clock generator) ground potential (2.5 V)	—

2. INTERNAL UNITS

(1) Bus control unit (BCU)

Controls the address bus, data bus, and control bus pins. The major functions of BCU are as follows:

(a) Bus arbitration

Arbitrates the bus mastership among bus masters (CPU, SDRAMC, DMAC, and external bus masters). The bus mastership can be changed after completion of the bus cycle under execution, and in an idle state.

(b) Wait control

Controls eight areas in the 16 MB space corresponding to eight chip select signals ($\overline{CS0}$ to $\overline{CS7}$). Generates chip select signals, controls wait states, and selects the type of bus cycle.

(c) SDRAM controller

Generates commands and controls access to SDRAM. CAS latency is 2 only.

(d) ROM controller

Accessing ROM with page access function is supported. The bus cycle immediately before is compared with addresses and wait states are controlled in the normal access (off-page) or page access (on-page) modes. A page width of 8 bytes to 16 bytes can be supported.

(2) Interrupt controller (ICU)

Services maskable interrupt requests (INTP00 to INTP03 and INTP10 to INTP13) from internal peripheral hardware and external sources. The priorities of these interrupt requests can be specified in units of four groups, and edge-triggered or level-triggered interrupts can be nested.

(3) DMA controller (DMAC)

Transfers data between memory and I/O in place of the CPU. The transfer type is 2-cycle transfer. Two transfer modes, single transfer and demand transfer, are available.

(4) Serial interface (UART/CSI/BRG)

One asynchronous serial interface (UART) channel and one clocked serial interface (CSI) channel are provided. As the serial clock source, the output of the baud rate generator (BRG) and the bus clock can be selected.

(5) Real-time pulse unit (RPU)

Provides timer/counter functions. The on-chip 16-bit timer/event counter and 16-bit interval timer can be used to calculate pulse intervals and frequencies, and to output programmable pulses.

(6) Clock generator (CG)

A frequency six or eight times higher than that of the resonator connected to the X1 and X2 pins is supplied as the operating clock of the CPU. In addition, both a bus clock, which functions as the operating clock of the peripheral units, and SDCLKOUT, which functions as an operating clock, are supplied from the CLKOUT pin. An external clock can be also input instead of connecting a resonator. For reducing the power consumption, a function to switch the frequencies of the CPU clock and bus clock via power management control (PMC) is provided.

(7) Port (PIO)

Provides port functions. Twenty-one I/O ports are available. The pins of these ports can be used as port pins or other function pins.

(8) System control unit (SYU)

A circuit that eliminates noise on the $\overline{\text{RESET}}$ signal (input)/$\overline{\text{NMI}}$ signal (input) is provided.

(9) Debug control unit (DCU)

A circuit to realize mapping and trace functions is provided to implement basic debugging functions.

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
3.3 V operation supply voltage	V_{DDO}			–0.5 to +4.0	V
2.5 V operation supply voltage	V_{DDI}			–0.5 to +3.6	V
	V_{DDPLL}			–0.5 to +3.6	V
Input voltage**Note**	V_I	$V_{DDO} \geq 3.7$ V		–0.5 to +4.0	V
		$V_{DDO} < 3.7$ V		–0.5 to V_{DDO} + 0.3	
Clock input voltage	V_K			–0.5 to V_{DDO} + 0.3	V
Operating ambient temperature	T_A	μPD705102-143	CPU core frequency ≤ 143 MHz	–40 to +85	°C
			CPU core frequency ≤ 144 MHz	–40 to +70	°C
		μPD705102-133	CPU core frequency ≤ 133 MHz	–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note Includes output pins.

Cautions 1. Do not directly connect the output (or input/output) pins of an IC device to each other, and do not connect them directly to V_{DD}, V_{CC} or GND. However, these restrictions do not apply to the high-impedance pins of an external circuit whose timing has been specifically designed to avoid output collision.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. For IC products, normal operation and quality are guaranteed only when the ratings and conditions described under the DC and AC characteristics are satisfied.

Operating Conditions

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
3.3 V operation supply voltage	V_{DDO}			3.0	3.6	V
2.5 V operation supply voltage	V_{DDI}			2.3	2.7	V
Operating ambient temperature	T_A	μPD705102-143	CPU core frequency ≤ 143 MHz	–40	+85	°C
			CPU core frequency ≤ 144 MHz	–40	+70	°C
		μPD705102-133	CPU core frequency ≤ 133 MHz	–40	+85	°C

Caution The V832 has two types of power supply, and there are no restrictions on the order that the voltage is to be applied. However, be sure not to maintain a state whereby only one power supply is applied voltage for 1 second or more.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator for manufacturer for evaluation.

DC Characteristics (V_{DDO} = 3.0 to 3.6 V, V_{DDI} = 2.3 to 2.7 V)

(μPD705102-143 (CPU core frequency ≤ 143 MHz): T_A = –40 to +85°C
μPD705102-143 (CPU core frequency ≤ 144 MHz): T_A = –40 to +70°C
μPD705102-133: T_A = –40 to +85°C)

Parameter		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Clock input voltage, low		V_{KL}	**Note 1**		–0.5		+0.2V_{DDO}	V
Clock input voltage, high		V_{KH}	**Note 1**		0.8V_{DDO}		V_{DDO} + 0.3	V
Input voltage, low		V_{IL}			–0.5		+0.6	V
Input voltage, high		V_{IH}			2.0		V_{DDO} + 0.3	V
Schmitt input voltage, low		V_{SL}	**Note 2**		–0.5		+0.2V_{DDO}	V
Schmitt input voltage, high		V_{SH}	**Note 2**		0.8V_{DDO}		V_{DDO} + 0.3	V
Output voltage, low		V_{OL}	I_{OL} = 3.2 mA				0.4	V
Output voltage, high		V_{OH}	I_{OH} = –400 μA		0.85V_{DDO}			V
Input leakage current, low		I_{LIL}	V_{IN} = 0 V				–10	μA
Input leakage current, high		I_{LIH}	V_{IN} = V_{DDO}				10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V				–10	μA
Output leakage current, high		I_{LOH}	V_O = V_{DDO}				10	μA
Supply current**Note 3**	2.5 V	I_{DDI}	Normal operation (PLL mode)	Clock division ratio 1/1		115	160	mA
				Clock division ratio 1/2		60		mA
				Clock division ratio 1/4		33		mA
			Normal operation (Direct mode)	Clock division ratio 1/1		15		mA
				Clock division ratio 1/2		7.5		mA
			In HALT mode			20	29	mA
			In STOP mode**Note 4**			25	450	μA
	3.3 V	I_{DDO}	Normal operation (PLL mode)	Clock division ratio 1/1		19	28	mA
				Clock division ratio 1/2		10		mA
				Clock division ratio 1/4		6		mA
			Normal operation (Direct mode)	Clock division ratio 1/1		4		mA
				Clock division ratio 1/2		3		mA
			In HALT mode			12	20	mA
			In STOP mode**Note 4**			5	10	μA

Notes 1. X2 pin, DCK pin, and $\overline{SCLK}$ pin at external clock input

2. PORT0/$\overline{SCLK}$, PORT2/SI, PORT3/RXD

3. Supply current at input clock: 17.85 MHz with output pins open, PLL 8×

4. External clock mode when clock input is stopped.

Capacitance

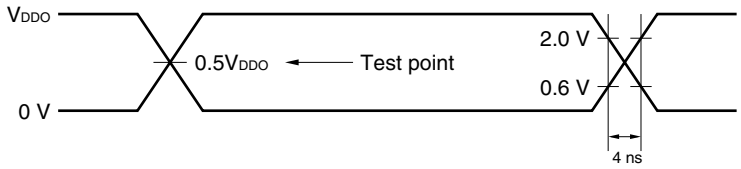
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}			10	pF

Remark These parameters are sample values, not the values actually measured.

AC Characteristics (V_{DDO} = 3.0 to 3.6 V, V_{DDI} = 2.3 to 2.7 V, C_L = 50 pF)

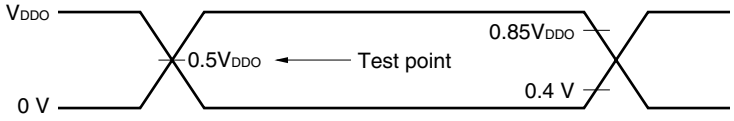
(μPD705102-143 (CPU core frequency ≤ 143 MHz): T_A = –40 to +85°C
μPD705102-143 (CPU core frequency ≤ 144 MHz): T_A = –40 to +70°C
μPD705102-133: T_A = –40 to +85°C)

AC test input waveform

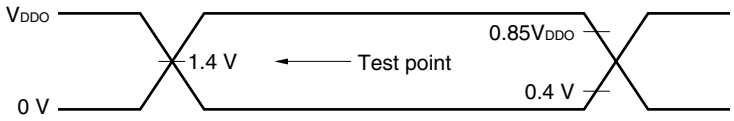


AC test output waveform

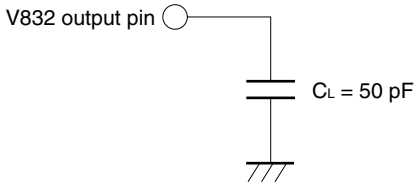
(a) $\overline{CS0}$, $\overline{CS1}$, $\overline{WE}$, $\overline{RAS}$, UUDQM, ULDQM, LUDQM, LLDQM, CKE, $\overline{CAS}$, SDCLKOUT, CLKOUT, A1 to A23, D0 to D31



(b) Other than above (a)



Test load



(1) Clock input (X2) timing (when external clock input used)

- **μPD705102-143**

Parameter	Symbol		Conditions	PLL Magnification				Unit
				×6 Mode		×8 Mode		
				MIN.	MAX.	MIN.	MAX.	
External clock cycle	<1>	t_{CYX}	**Note 1**	42	60	56	80	ns
			Note 2		45		60	ns
			Note 3	41.6	60	55.5	80	ns
			Note 4		45		60	ns
External clock high-level time	<2>	t_{XXH}	**Note 1**	16		23		ns
			Note 3	15.8		22.75		ns
External clock low-level time	<3>	t_{XXL}	**Note 1**	16		23		ns
			Note 3	15.8		22.75		ns
External clock rise time	<4>	t_{XR}			5		5	ns
External clock fall time	<5>	t_{XF}			5		5	ns

Notes 1. T_A = –40 to +85°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (default) = 100 to 143 MHz)

2. T_A = –40 to +85°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 to 35.8 MHz)

3. T_A = –40 to +70°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (default) = 100 to 144 MHz)

4. T_A = –40 to +70°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 to 36 MHz)

Remark The stability of the input clock is 0.1% of t_{CYX} or lower.

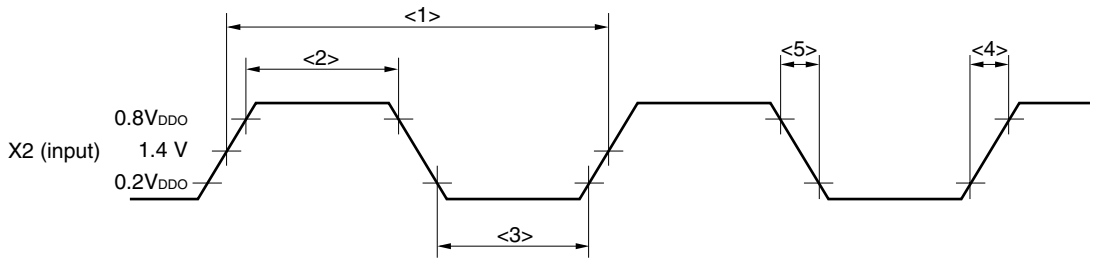
- **μPD705102-133**

Parameter	Symbol		Conditions	PLL Magnification				Unit
				×6 Mode		×8 Mode		
				MIN.	MAX.	MIN.	MAX.	
External clock cycle	<1>	t_{CYX}	**Note 1**	45	60	60	80	ns
			Note 2		45		60	ns
External clock high-level time	<2>	t_{XXH}		17.5		25		ns
External clock low-level time	<3>	t_{XXL}		17.5		25		ns
External clock rise time	<4>	t_{XR}			5		5	ns
External clock fall time	<5>	t_{XF}			5		5	ns

Notes 1. T_A = –40 to +85°C, when other than 1/4 is selected as the division ratio of the input clock (CPU core frequency (default) = 100 to 133 MHz)

2. T_A = –40 to +85°C, when 1/4 is selected as the division ratio of the input clock (CPU core frequency = 33.3 MHz)

Remark The stability of the input clock is 0.1% of t_{CYX} or lower.



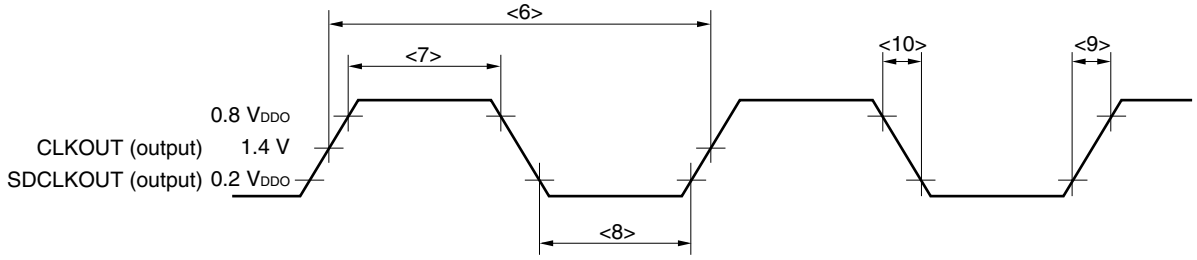
(2) Clock output timing (CLKOUT, SDCLKOUT)

Parameter	Symbol		Conditions	PLL Magnification				Unit
				×6 Mode		×8 Mode		
				MIN.	MAX.	MIN.	MAX.	
External clock cycle	<6>	t_{CYK}	**Note 1**	21		28		ns
			Note 2	20.8		27.75		ns
			Note 3	22.5		30		ns
External clock high-level time	<7>	t_{KKH}		$t_{CYK}/2 - 5$		$t_{CYK}/2 - 5$		ns
External clock low-level time	<8>	t_{KKL}		$t_{CYK}/2 - 5$		$t_{CYK}/2 - 5$		ns
External clock rise time	<9>	t_{KR}			5		5	ns
External clock fall time	<10>	t_{KF}			5		5	ns

Notes 1. μPD705102-143, T_A = –40 to +85°C

2. μPD705102-143, T_A = –40 to +70°C

3. μPD705102-133, T_A = –40 to +85°C



(3) Reset timing

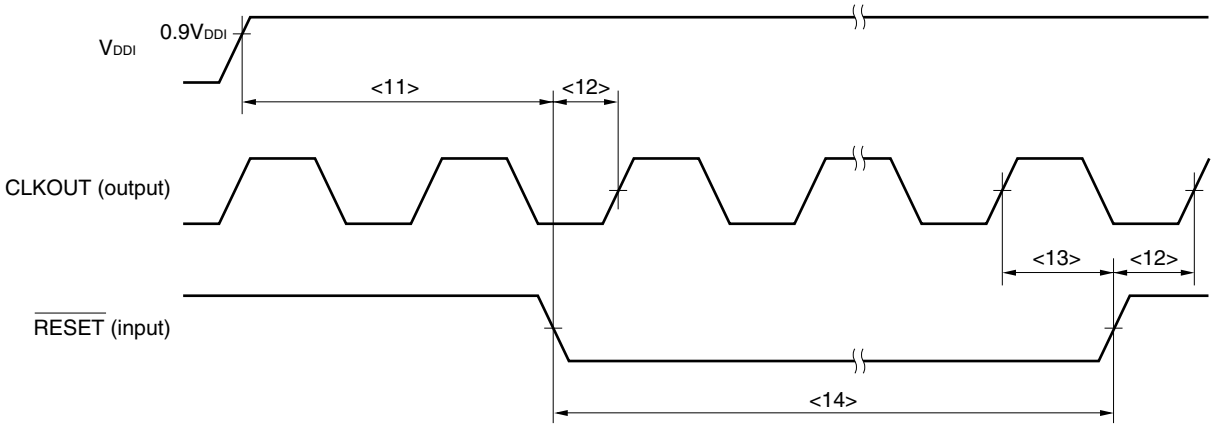
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ hold time (from V_{DDI} VALID)	<11>	t_{HVR}			2	μs
$\overline{\text{RESET}}$ setup time (to CLKOUT↑)	<12>	t_{SRK}		7		ns
$\overline{\text{RESET}}$ hold time (from CLKOUT↑)	<13>	t_{HKR}		7		ns
$\overline{\text{RESET}}$ pulse low-level width	<14>	t_{WRL}	**Note 1**	20		ms
			Note 2	10		ms
			Note 3	15		t_{CYX}

Notes 1. At power on or when returned from STOP mode, and the internal clock is generated.

2. At power on or when returned from STOP mode, and the external clock is generated, after the clock has stabilized.

3. When clock has stabilized under conditions other than Notes 1 and 2.

Remark It is not necessary to satisfy t_{SRK} and t_{HKR} if the reset occurs during the period of t_{HVR}. In such a case, however, the reset acknowledgement timing may be shifted.

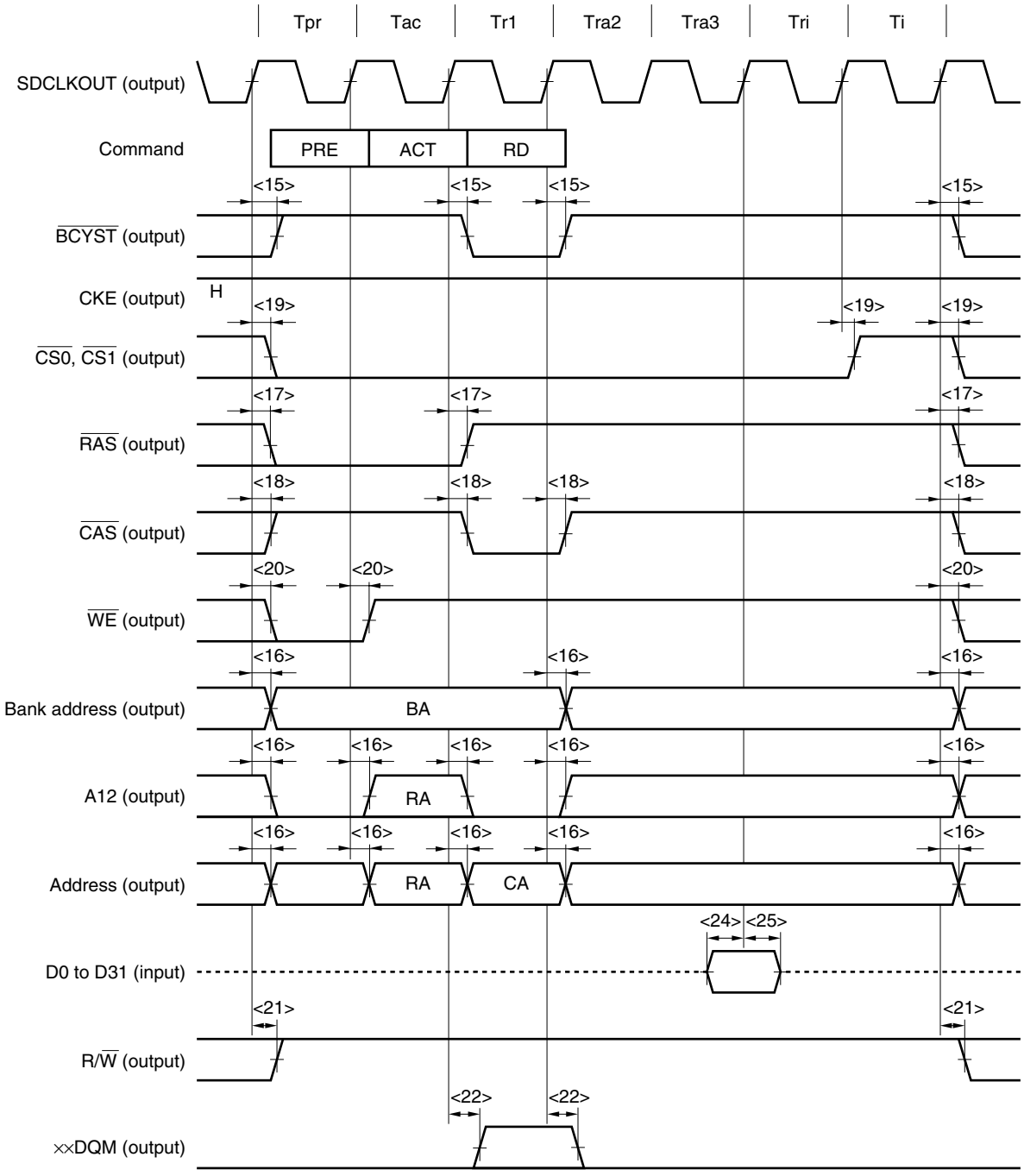


(4) SDRAM access timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{BCYST}$ delay time (from SDCLKOUT↑)	<15>	t_{DKBC}		2	12.5	ns
Address delay time (from SDCLKOUT↑)	<16>	t_{DKA}		2	12.5	ns
$\overline{RAS}$ delay time (from SDCLKOUT↑)	<17>	t_{DKRAS}		2	12.5	ns
$\overline{CAS}$ delay time (from SDCLKOUT↑)	<18>	t_{DKCAS}		2	12.5	ns
$\overline{CS0}$, $\overline{CS1}$ delay time (from SDCLKOUT↑)	<19>	t_{DKCS}		2	12.5	ns
$\overline{WE}$ delay time (from SDCLKOUT↑)	<20>	t_{DKWE}		2	12.5	ns
R/$\overline{W}$ delay time (from SDCLKOUT↑)	<21>	t_{DKRW}		2	12.5	ns
××DQM delay time (from SDCLKOUT↑)	<22>	t_{DKDQM}		2	12.5	ns
CKE delay time (from SDCLKOUT↑)	<23>	t_{DKCKE}		2	12.5	ns
Data input setup time (SDRAM read, to SDCLKOUT↑)	<24>	t_{SDRMK}		5		ns
Data input hold time (SDRAM read, from SDCLKOUT↑)	<25>	t_{HKDRM}		2		ns
Data output delay time (from active, from SDCLKOUT↑)	<26>	t_{DKDT}		2	12.5	ns
Data output delay time (from float, from SDCLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from SDCLKOUT↑)	<28>	t_{HZKDT}		3	20	ns

Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

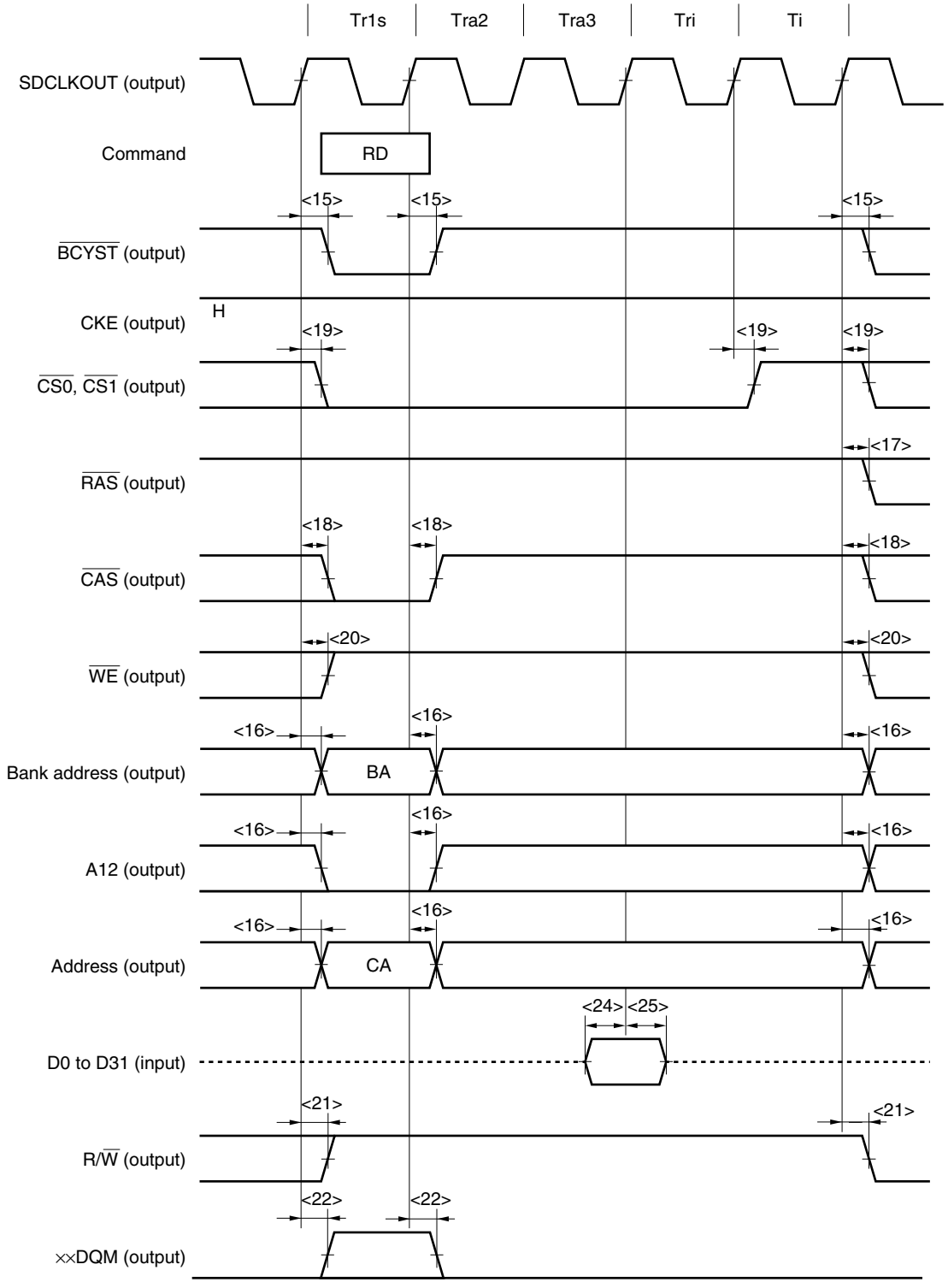
SDRAM single read cycle (off-page) (TRP = 0, TRCD = 0): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

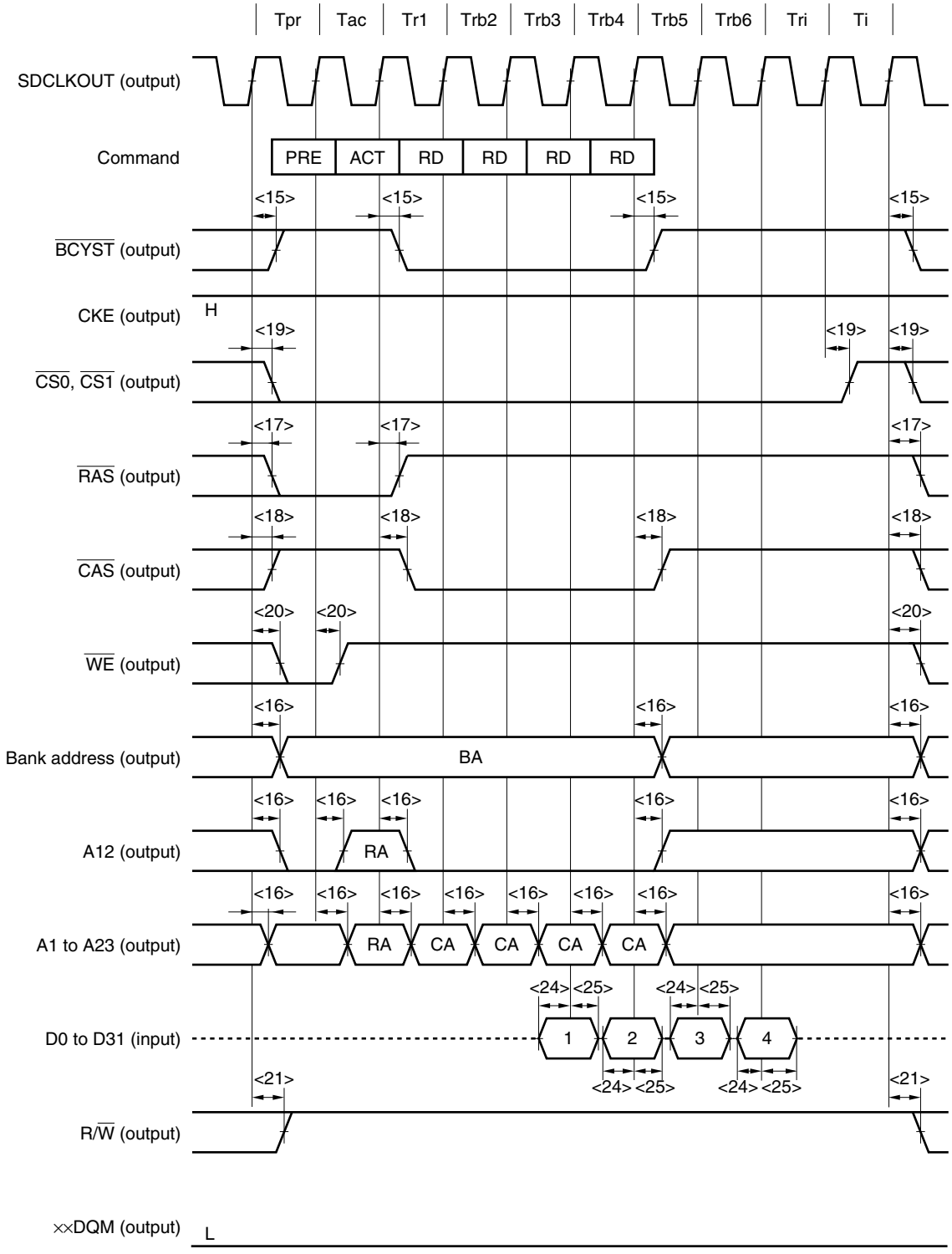
SDRAM single read cycle (on-page): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

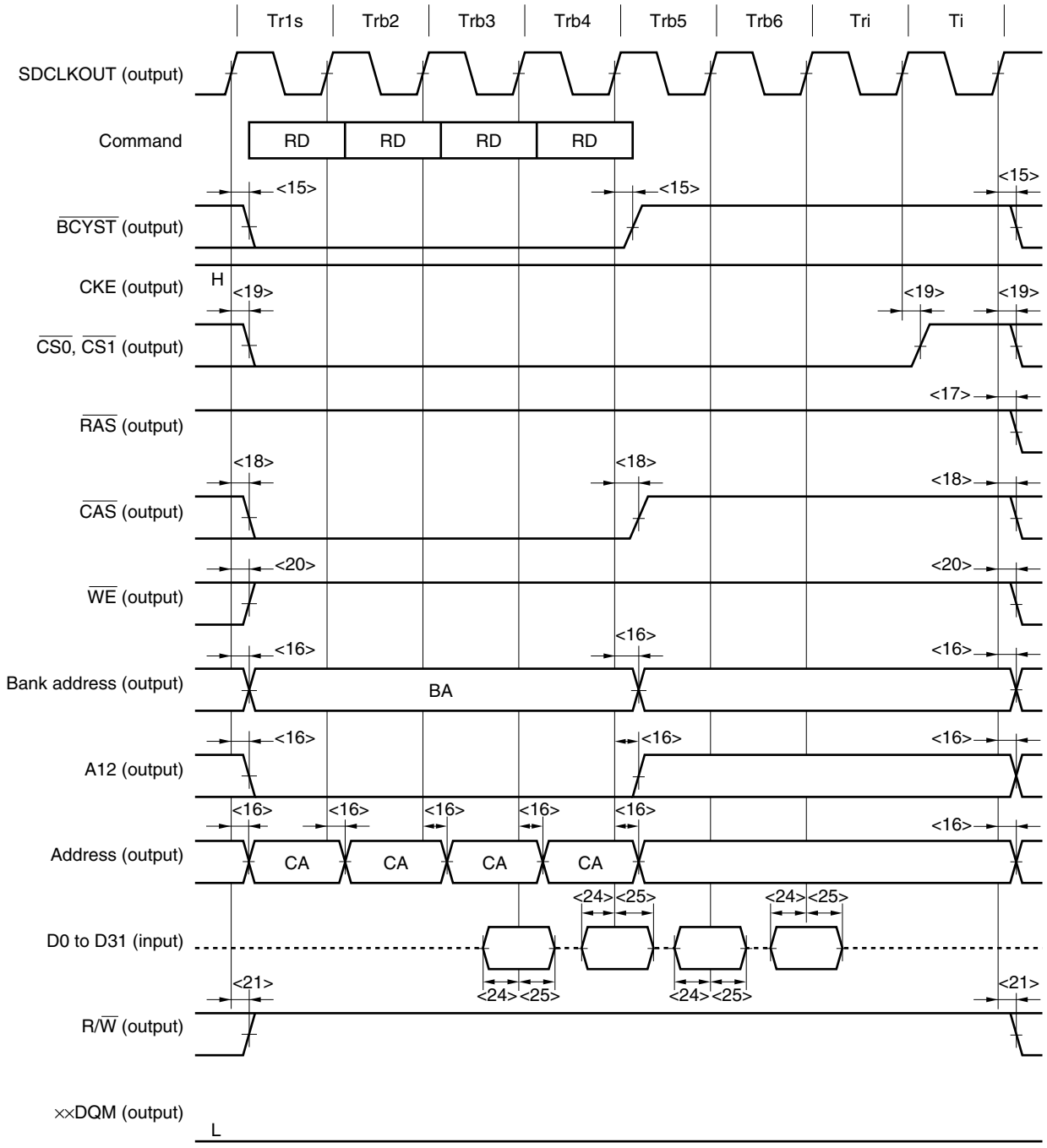
SDRAM burst read cycle (off-page) (TRP = 0, TRCD = 0): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

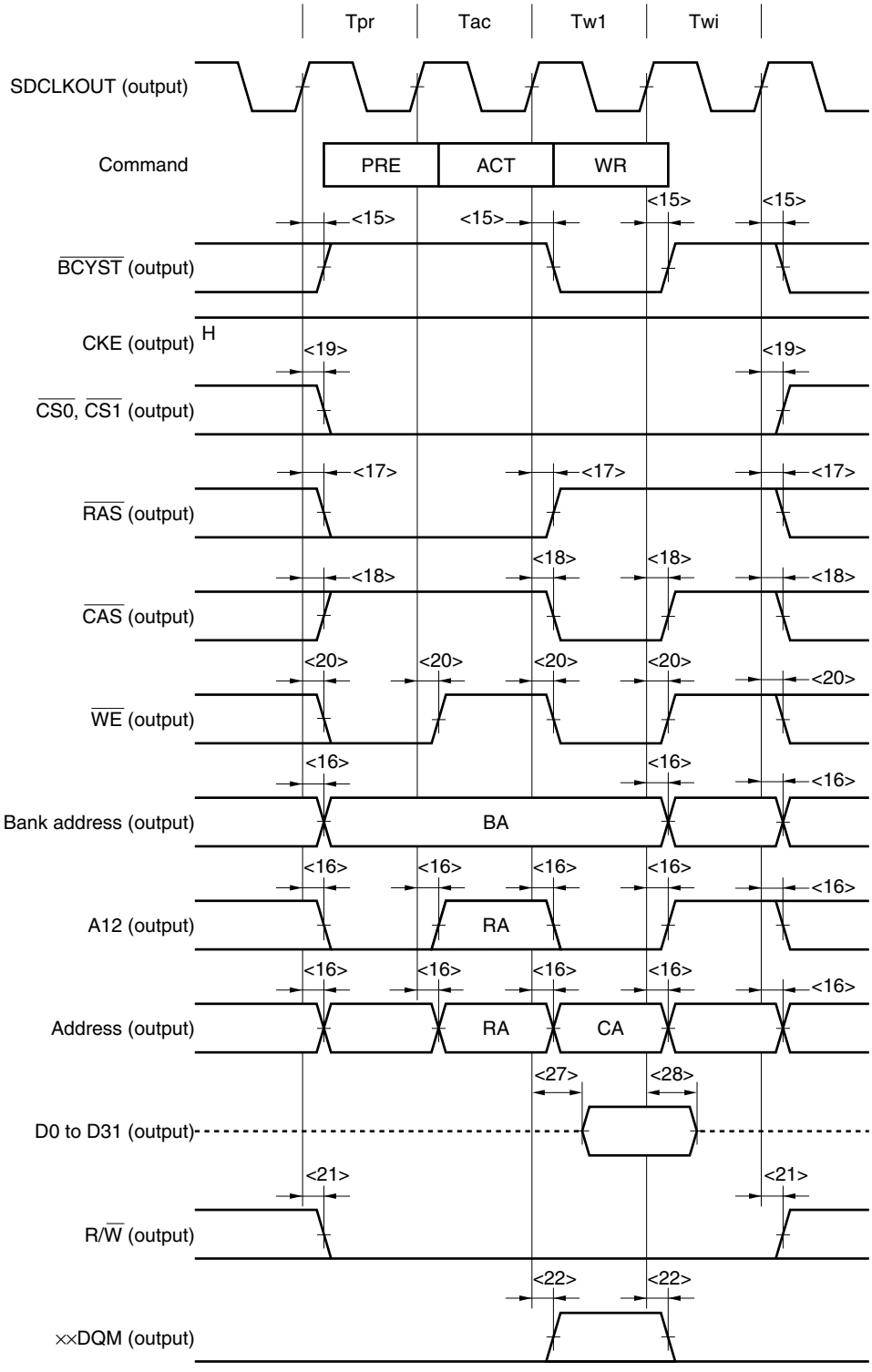
SDRAM burst read cycle (on-page): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

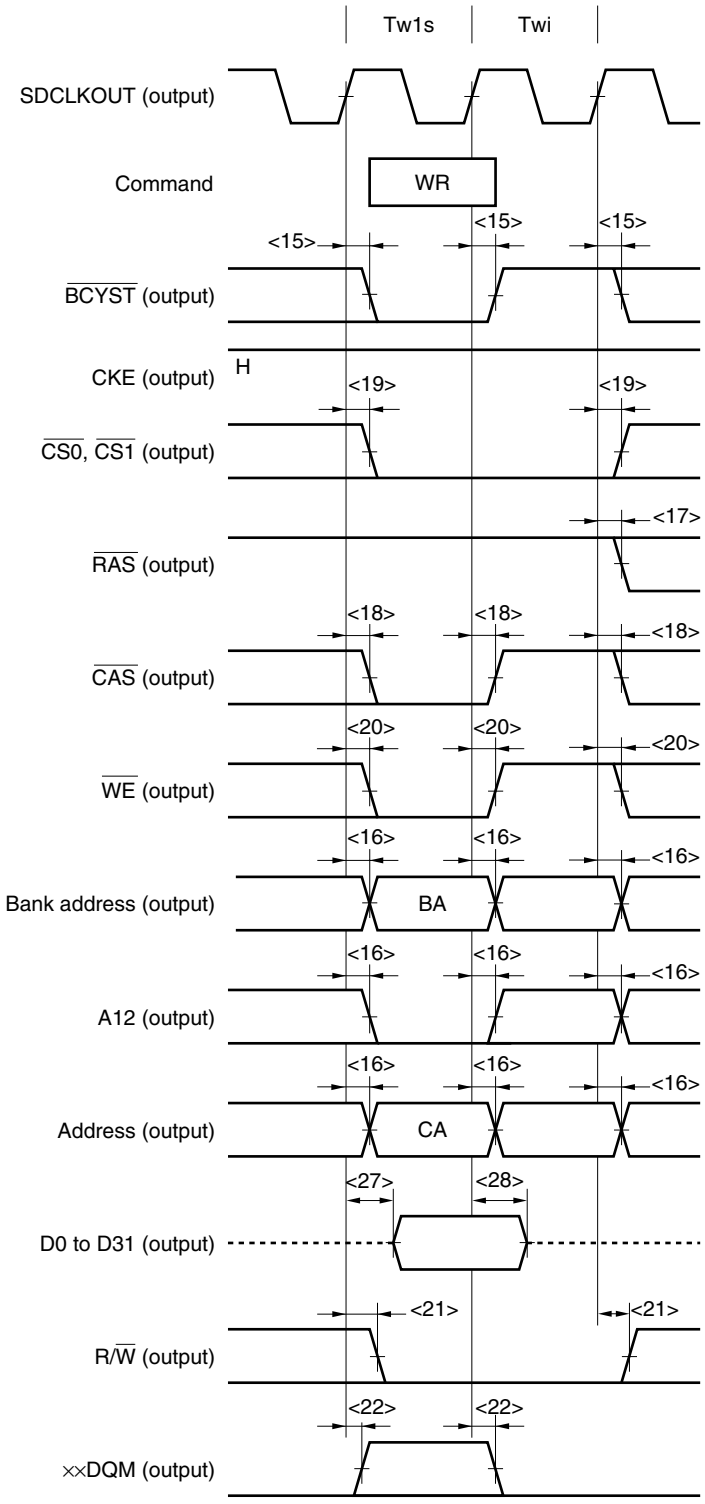
SDRAM single write cycle (off-page) (TRP = 0, TRCD = 0): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

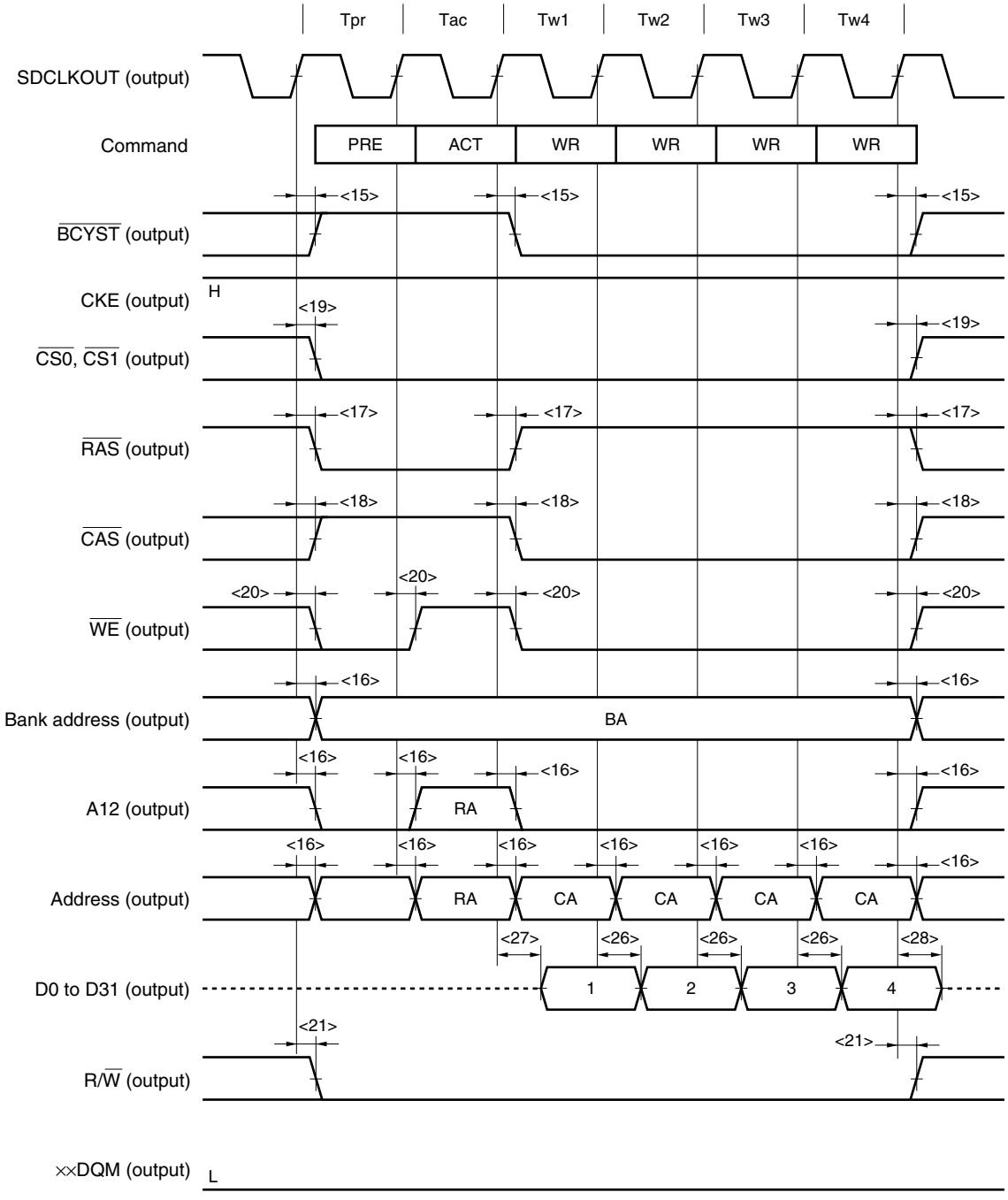
SDRAM single write cycle (on-page): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

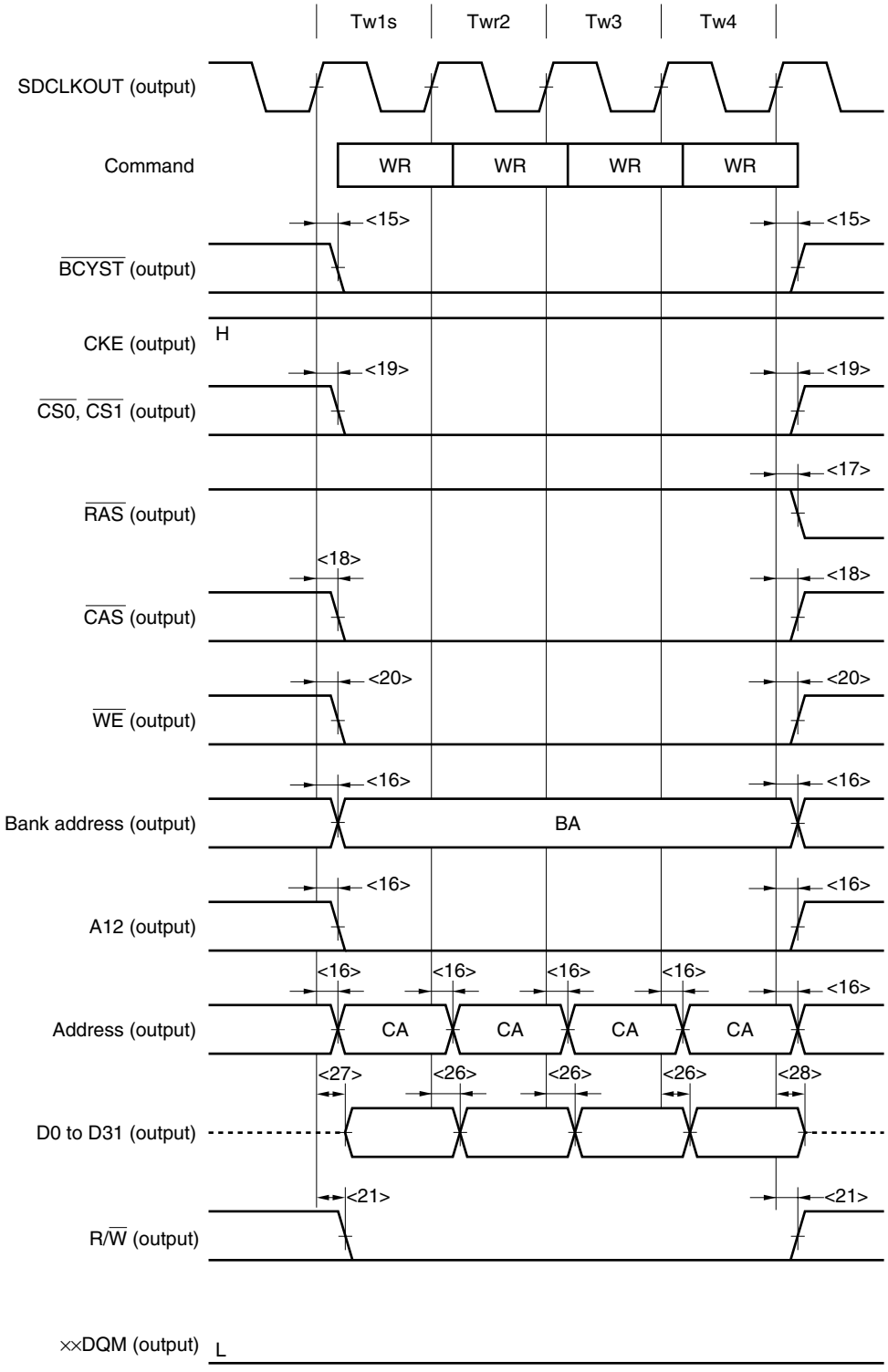
SDRAM burst write cycle (off-page) (TRP = 0, TRCD = 0): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

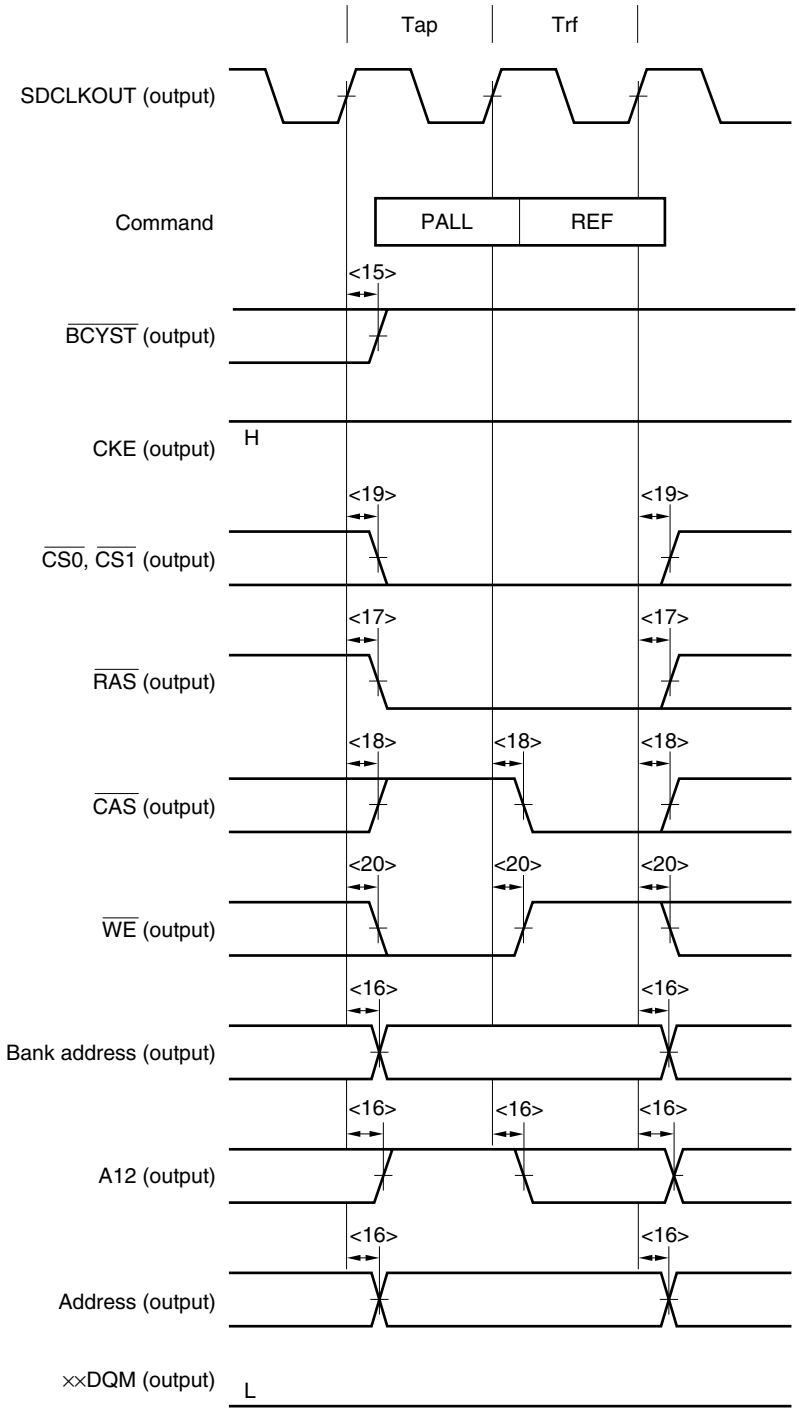
SDRAM burst write cycle (on-page): 32-bit data bus



Remarks 1. The broken lines indicate high impedance.

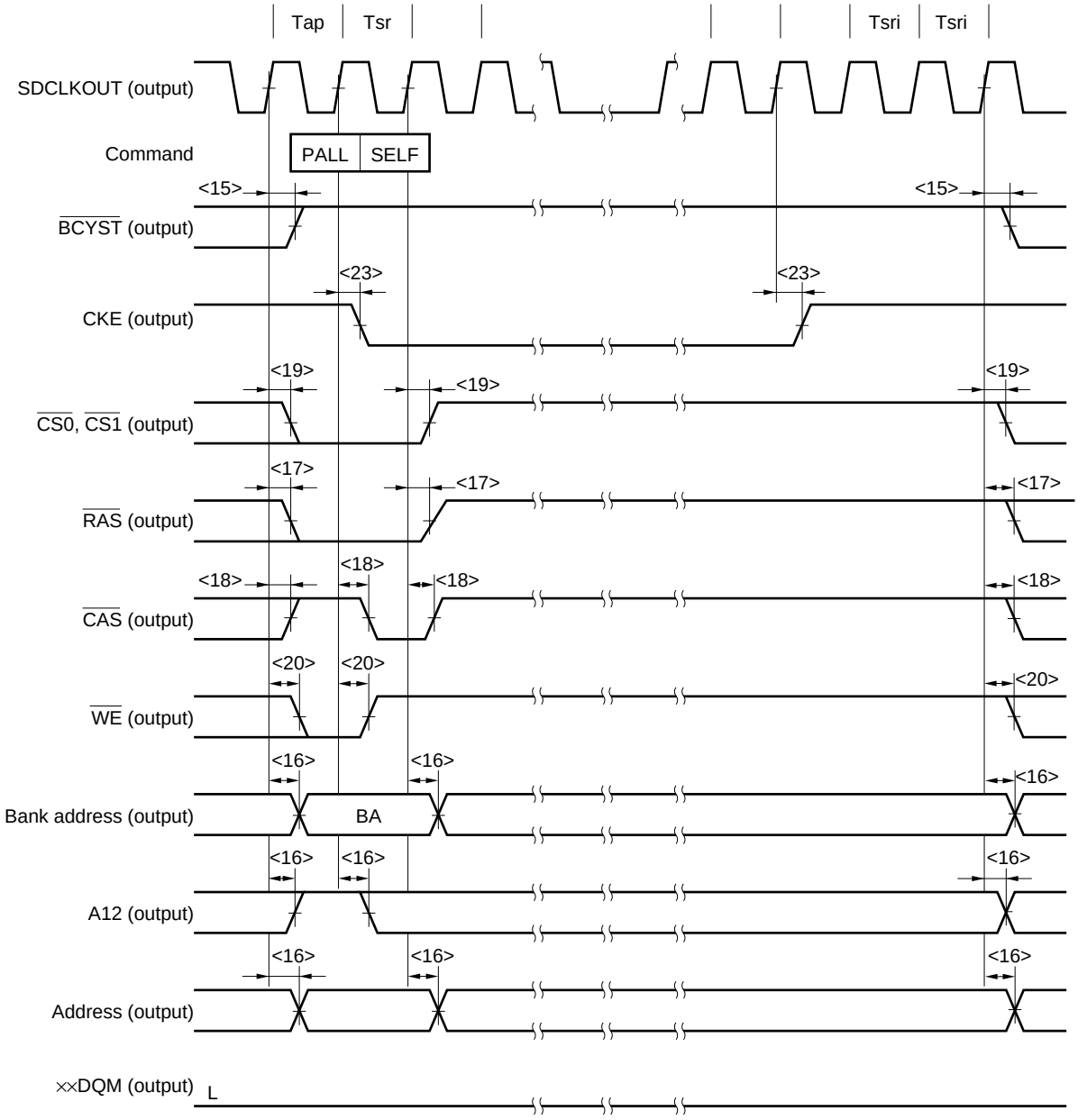
2. ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

Auto-refresh cycle (TRP = 0): 32-bit data bus



Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

Self-refresh cycle (TRP = 0): 32-bit data bus



Remark ××DQM: LLDQM, LUDQM, ULDQM, UUDQM

(5) Access timing of SRAM, Page ROM and I/O

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{BCYST}}$ delay time (from CLKOUT↑)	<15>	t_{DKBC}		2	12.5	ns
Address delay time (from CLKOUT↑)	<16>	t_{DKA}		2	12.5	ns
$\overline{\text{CSn}}$**Note** delay time (from CLKOUT↑)	<19>	t_{DKCS}		2	12.5	ns
R/$\overline{\text{W}}$ delay time (from CLKOUT↑)	<21>	t_{DKRW}		2	12.5	ns
Data output delay time (from active, from CLKOUT↑)	<26>	t_{DKDT}		2	12.5	ns
Data output delay time (from float, from CLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from CLKOUT↑)	<28>	t_{HZKDT}		3	20	ns
$\overline{\text{IORD}}$ output delay time (from CLKOUT↓)	<29>	t_{DKRD}		2	12.5	ns
$\overline{\text{MRD}}$ output delay time (from CLKOUT↓)	<30>	t_{DKMRD}		2	12.5	ns
$\overline{\text{IOWR}}$ output delay time (from CLKOUT↓)	<31>	t_{DKWR}		2	12.5	ns
$\overline{\text{MWR}}$ output delay time (from CLKOUT↓)	<32>	t_{DKMWR}		2	12.5	ns
××$\overline{\text{BEN}}$ delay time (from CLKOUT↓)	<33>	t_{DKBEN}		2	12.5	ns
Data input setup time (to CLKOUT↓)	<34>	t_{SDTK}		5		ns
Data input hold time (from CLKOUT↓)	<35>	t_{HKDT}		2		ns
$\overline{\text{READY}}$ setup time (to CLKOUT↑)	<36>	t_{SRYK}		7		ns
$\overline{\text{READY}}$ hold time (from CLKOUT↑)	<37>	t_{HKRY}		3		ns

Note $\overline{\text{CSn}}$ indicates $\overline{\text{CS1}}$ through $\overline{\text{CS7}}$. A different area is used depending on the n value.

n = 1 to 7: When SRAM (ROM) is selected

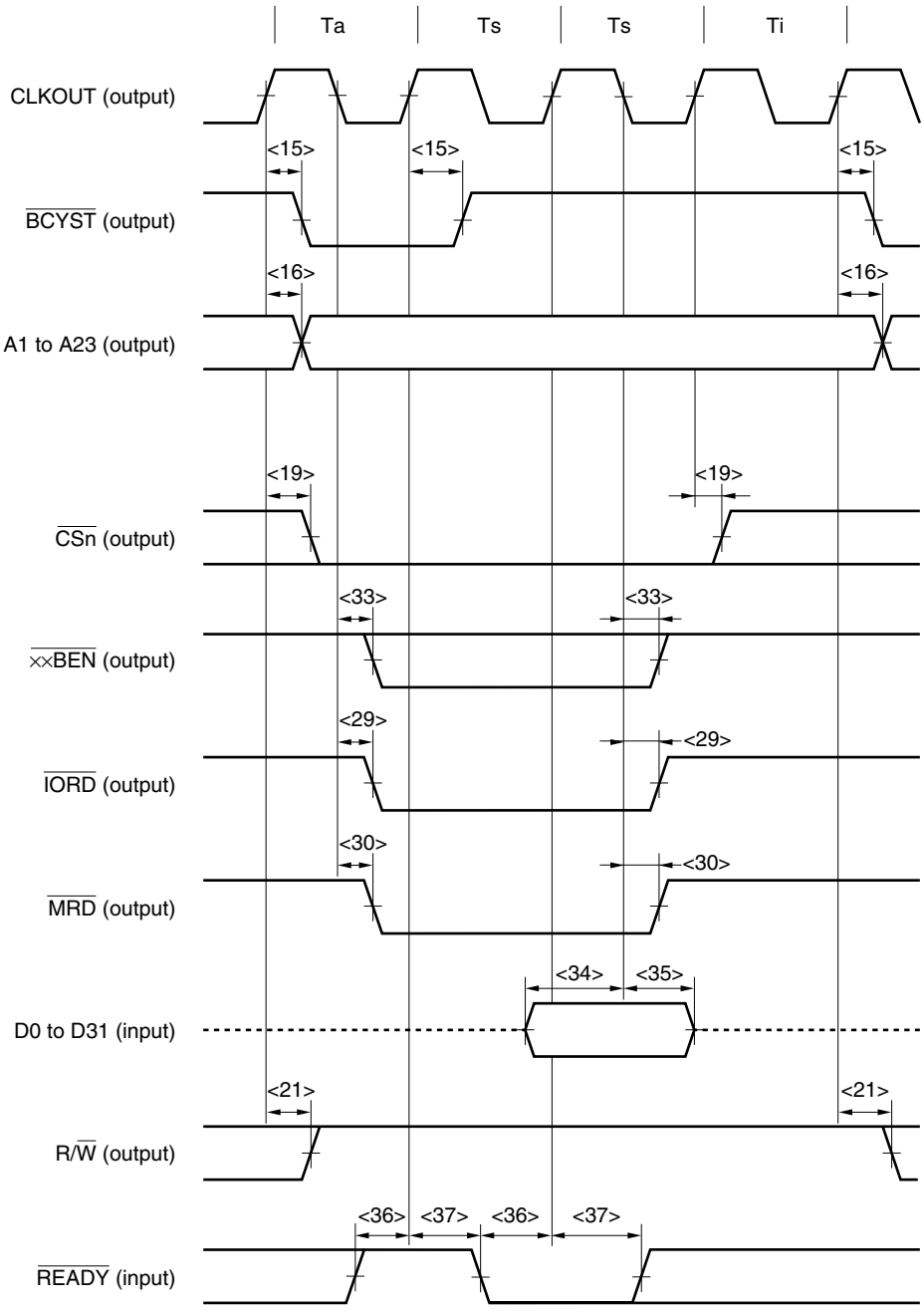
n = 7: When Page ROM is selected

n = 3 to 6: When I/O is selected

Remark ××$\overline{\text{BEN}}$: $\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$

SRAM (ROM), Page ROM single read cycle

I/O read timing



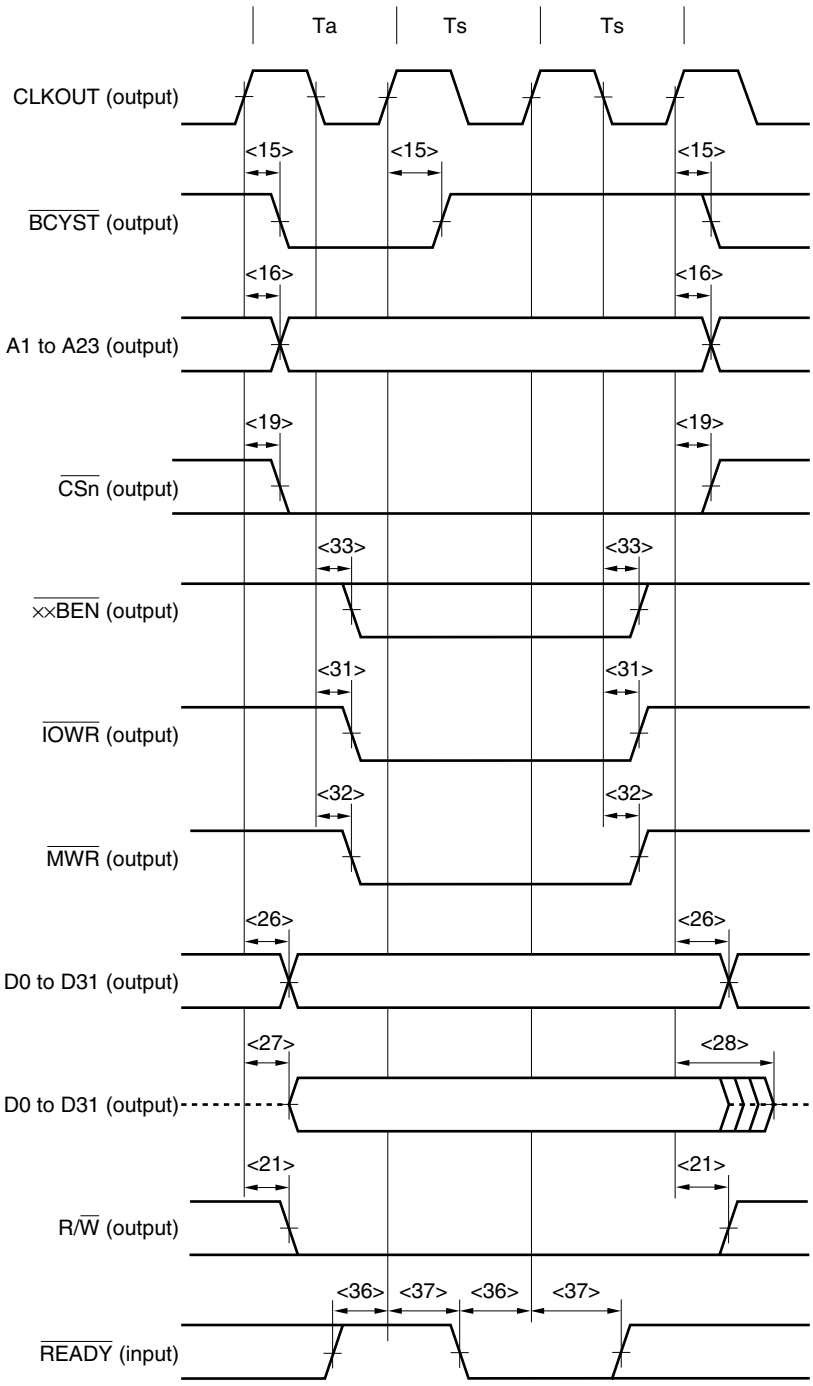
Remarks 1. The broken lines indicate high impedance.

2. n = 1 to 7

3. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

SRAM (ROM) single write cycle

I/O write timing

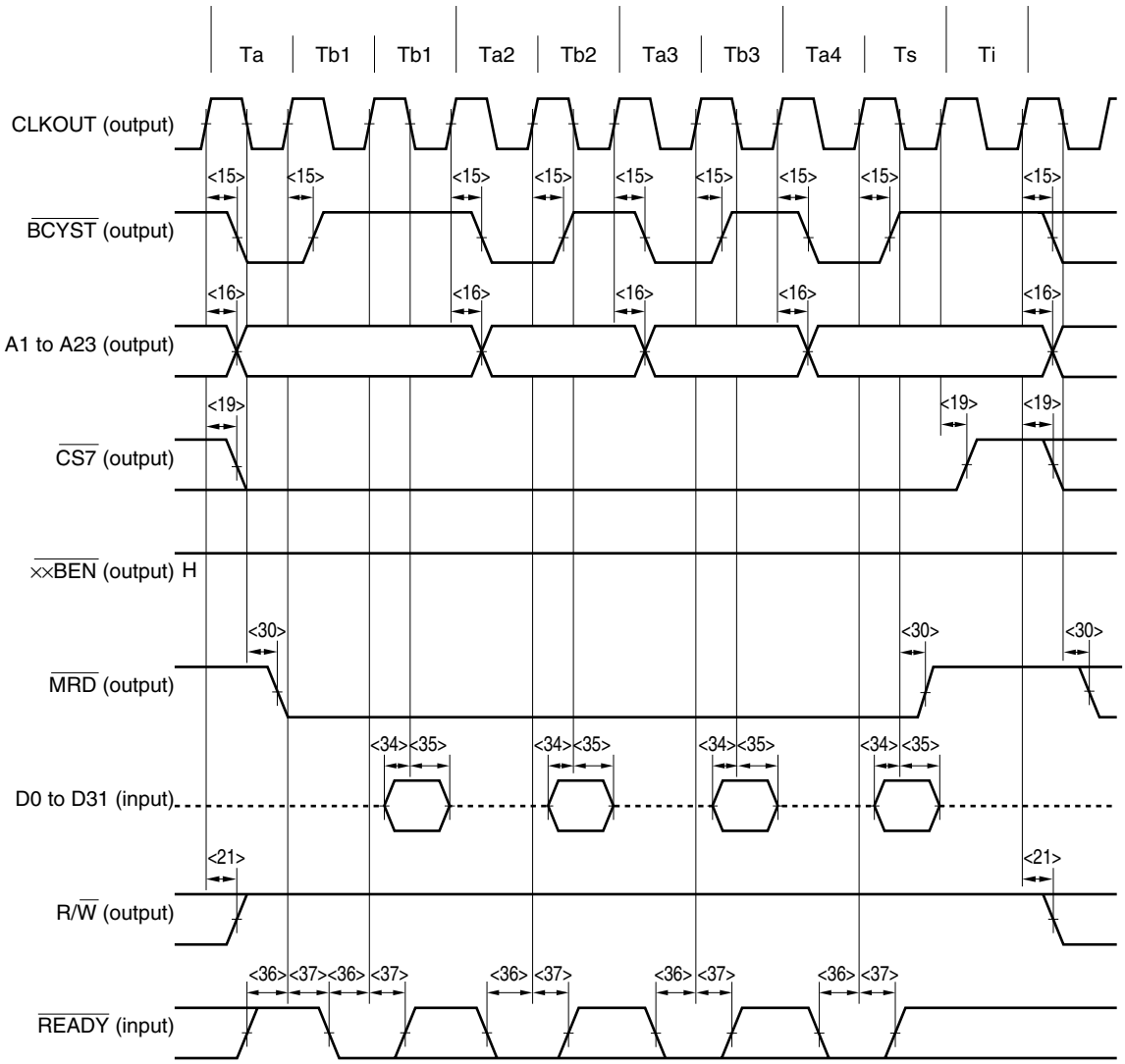


Remarks 1. The broken lines indicate high impedance.

2. n = 1 to 7

3. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

Page ROM burst read cycle (32-bit data bus)



Remarks 1. The broken lines indicate high impedance.

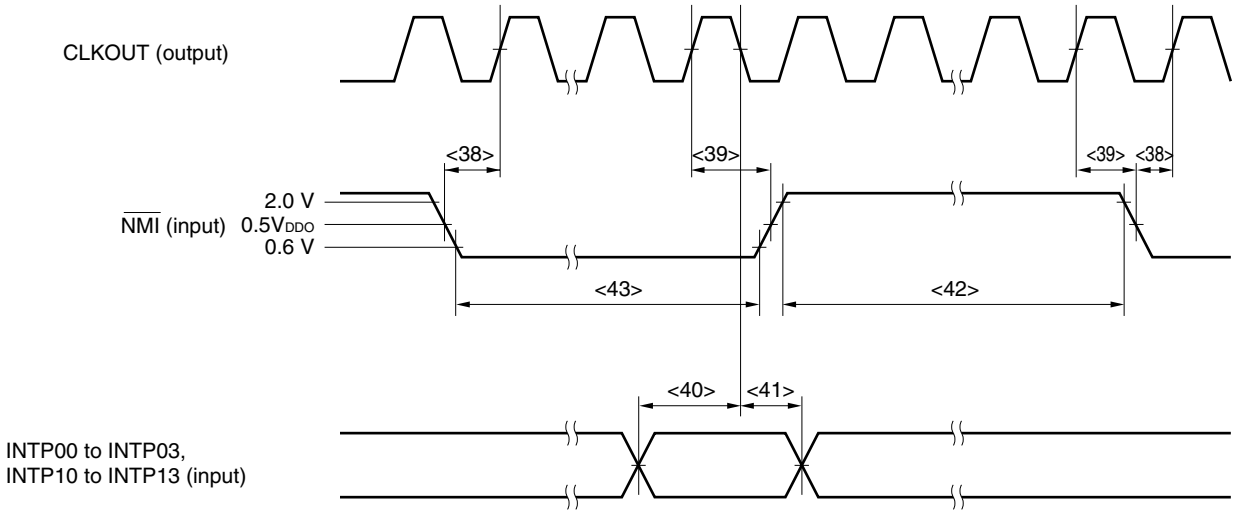
2. ××BEN: LLBEN, LUBEN, ULBEN, UUBEN

(6) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{NMI}$ setup time (to CLKOUT↑)	<38>	t_{SNK}		5		ns
$\overline{NMI}$ hold time (from CLKOUT↑)	<39>	t_{HKN}		7		ns
INTP×× setup time (to CLKOUT↓)	<40>	t_{SIK}		7		ns
INTP×× hold time (from CLKOUT↓)	<41>	t_{HKI}		3		ns
$\overline{NMI}$ high-level time	<42>	t_{NMH}		5T + 12		ns
$\overline{NMI}$ low-level time	<43>	t_{NML}		5T + 12		ns

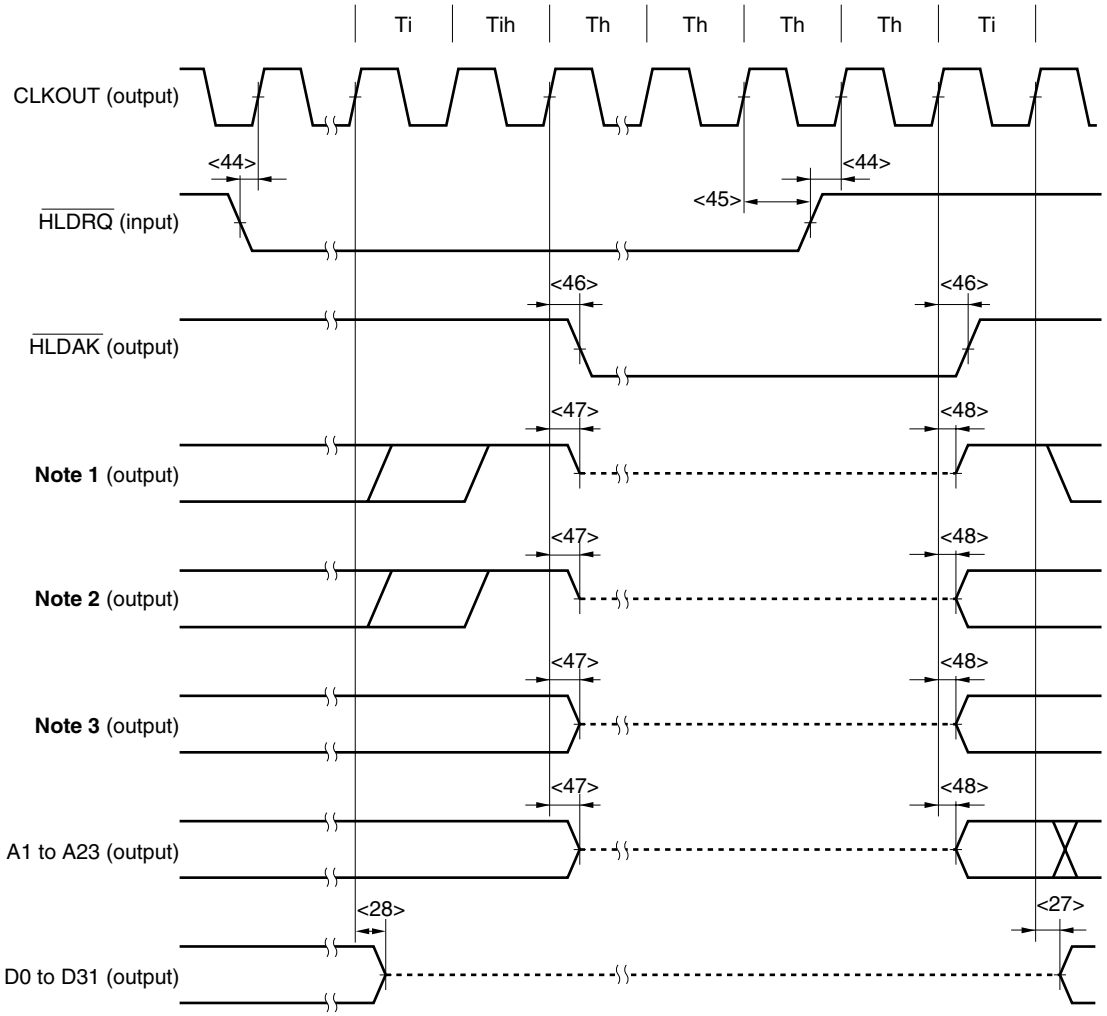
Remarks 1. T = T_{CYK} (external clock cycle)

2. Even if t_{SNK} and t_{HKN} are set to other than the above range, the NMI interrupt can be acknowledged, however, in this case the NMI acknowledgement timing may be delayed.



(7) Bus hold timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Data active delay time (from CLKOUT↑)	<27>	t_{LZKDT}		2	12.5	ns
Data float delay time (from CLKOUT↑)	<28>	t_{HZKDT}		3	20	ns
$\overline{\text{HLDRQ}}$ input setup time (to CLKOUT↑)	<44>	t_{SHQK}		7		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↑)	<45>	t_{HKHQ}		3		ns
$\overline{\text{HLDAK}}$ output delay time (from CLKOUT↑)	<46>	t_{DKHA}		2	12.5	ns
Address float delay time (from CLKOUT↑)	<47>	t_{HZKA}		3	20	ns
Address active delay time (from CLKOUT↑)	<48>	t_{LZKA}		2	12.5	ns



Notes 1. $\overline{\text{BCYST}}$, $\overline{\text{WE}}$, $\overline{\text{CS0}}$ to $\overline{\text{CS7}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, CKE

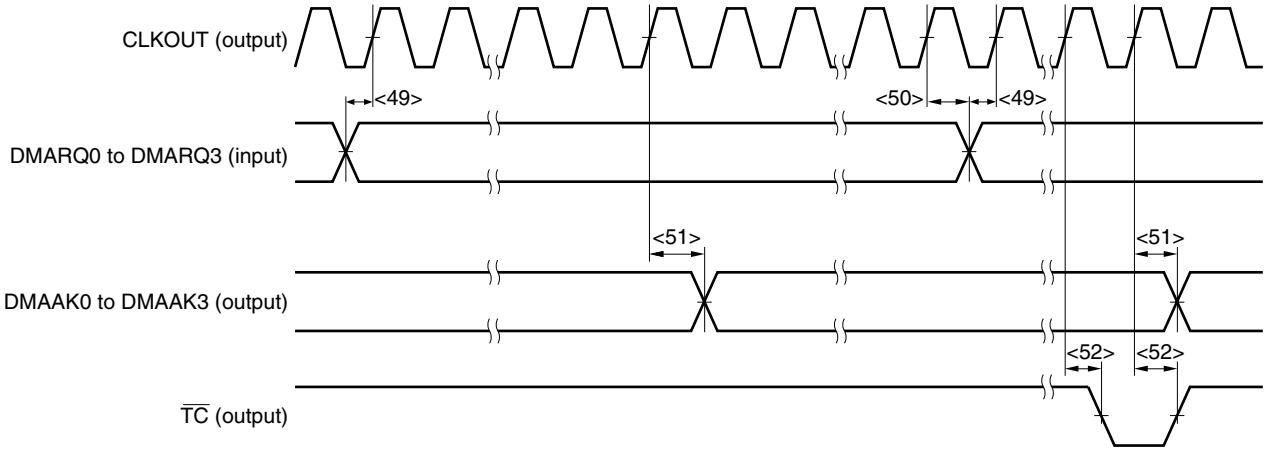
2. R/$\overline{\text{W}}$, $\overline{\text{LLBEN}}$, $\overline{\text{LUBEN}}$, $\overline{\text{ULBEN}}$, $\overline{\text{UUBEN}}$

3. LLDQM, LUDQM, ULDQM, UUDQM

Remark The broken lines indicate high impedance.

(8) DMA timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
DMARQ input setup time (to CLKOUT↑)	<49>	t_{SDQK}		7		ns
DMARQ hold time (from CLKOUT↑)	<50>	t_{HKDQ}		3		ns
DMAAK output delay time	<51>	t_{DKDAK}		2	12.5	ns
$\overline{TC}$ output delay time	<52>	t_{DKTC}		2	12.5	ns

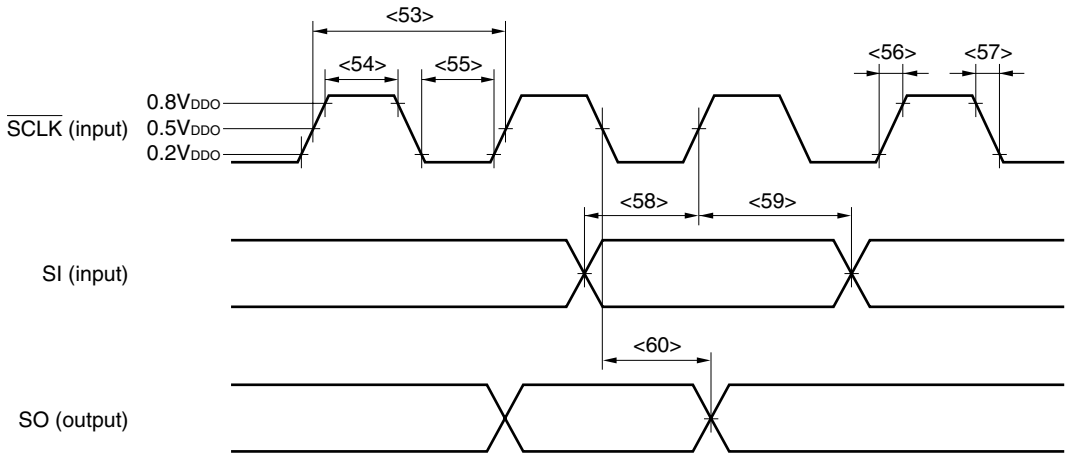


(9) CSI timing

(a) $\overline{\text{SCLK}}$ input mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{SCLK}}$ cycle	<53>	t_{CYSI}		4T		ns
$\overline{\text{SCLK}}$ high-level time	<54>	t_{SIH}		$t_{CYSI}/2 - 10$		ns
$\overline{\text{SCLK}}$ low-level time	<55>	t_{SIL}		$t_{CYSI}/2 - 10$		ns
$\overline{\text{SCLK}}$ rise time	<56>	t_{SIR}			10	ns
$\overline{\text{SCLK}}$ fall time	<57>	t_{SIF}			10	ns
SI input setup time (to $\overline{\text{SCLK}}\uparrow$)	<58>	t_{SDTS}		21		ns
SI input hold time (from $\overline{\text{SCLK}}\uparrow$)	<59>	t_{HSDT}		21		ns
SO output delay time (from $\overline{\text{SCLK}}\downarrow$)	<60>	t_{DSDT}		2	21	ns

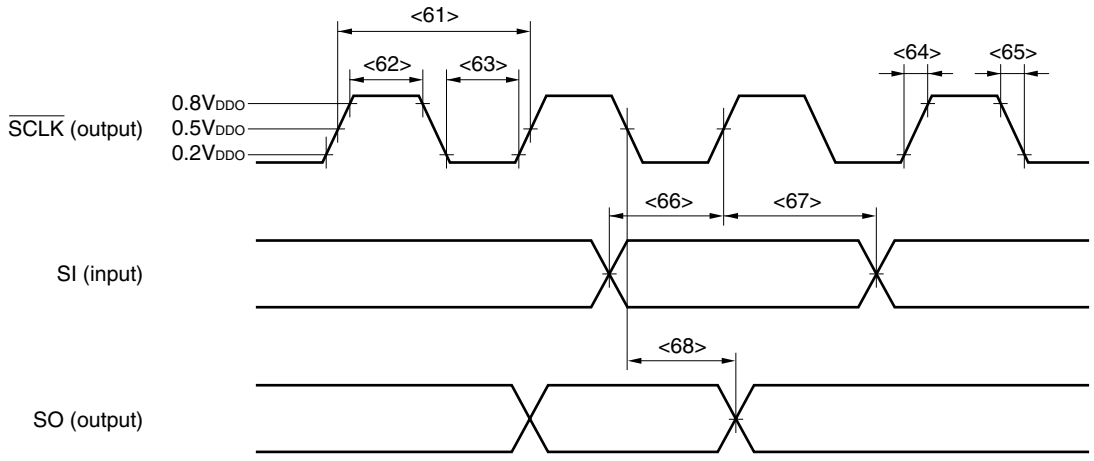
Remark T = T_{CYK} (external clock cycle)



(b) $\overline{\text{SCLK}}$ output mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{SCLK}}$ cycle	<61>	t_{CYSO}		4T		ns
$\overline{\text{SCLK}}$ high-level time	<62>	t_{SOH}		$t_{CYSO}/2 - 10$		ns
$\overline{\text{SCLK}}$ low-level time	<63>	t_{SOL}		$t_{CYSO}/2 - 10$		ns
$\overline{\text{SCLK}}$ rise time	<64>	t_{SOR}			10	ns
$\overline{\text{SCLK}}$ fall time	<65>	t_{SOF}			10	ns
SI input setup time (to $\overline{\text{SCLK}}\uparrow$)	<66>	t_{SDTS}		21		ns
SI input hold time (from $\overline{\text{SCLK}}\uparrow$)	<67>	t_{HSDT}		21		ns
SO output delay time (from $\overline{\text{SCLK}}\downarrow$)	<68>	t_{DSDT}		2	21	ns

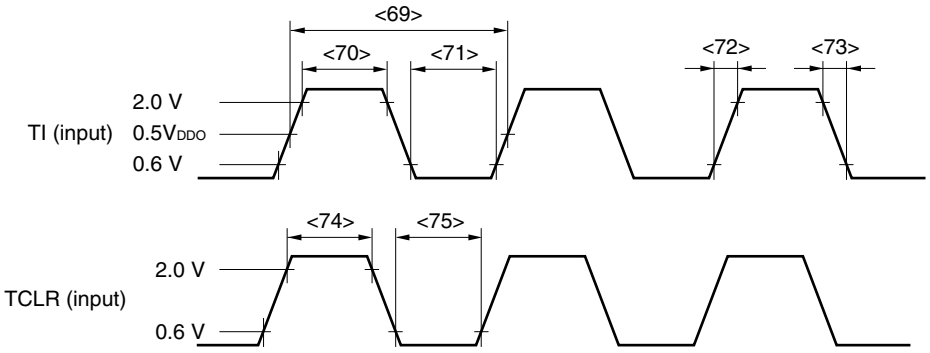
Remark T = T_{CYK} (external clock cycle)



(10) Timer timing

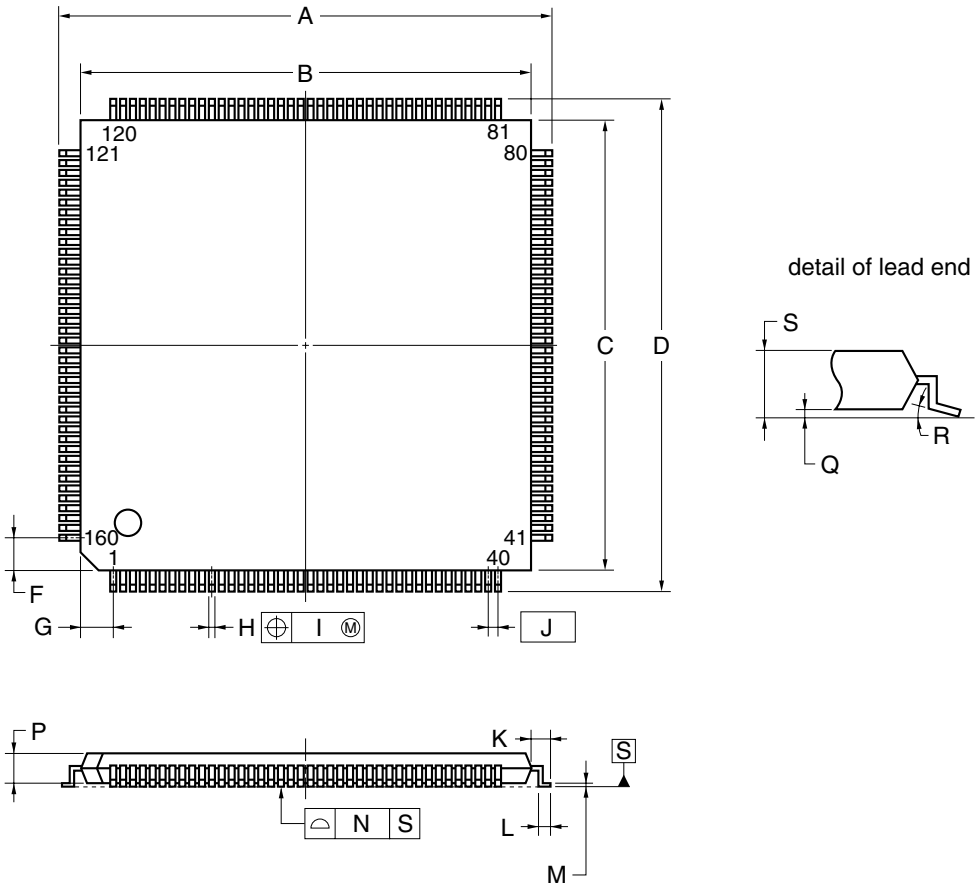
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI clock cycle	<69>	t_{CYT}		8T		ns
TI clock high-level time	<70>	t_{TIH}		4T + 10		ns
TI clock low-level time	<71>	t_{TIL}		4T + 10		ns
TI clock rise time	<72>	t_{TR}			10	ns
TI clock fall time	<73>	t_{TF}			10	ns
TCLR clock high-level time	<74>	t_{CLH}		4T + 10		ns
TCLR clock low-level time	<75>	t_{CLL}		4T + 10		ns

Remark T = T_{CYK} (external clock cycle)



4. PACKAGE DRAWING

160-PIN PLASTIC LQFP (FINE PITCH) (24x24)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	26.0±0.2
B	24.0±0.2
C	24.0±0.2
D	26.0±0.2
F	2.25
G	2.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.4±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S160GM-50-8ED-3

5. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions

μPD705102GM-143-8ED: 160-pin plastic LQFP (fine pitch) (24 × 24)
μPD705102GM-133-8ED: 160-pin plastic LQFP (fine pitch) (24 × 24)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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