PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD703128, μPD703129

V850E/CA2™ JUPITER
32-/16-BIT ROMLESS MICROCONTROLLER

DESCRIPTION

The V850E/CA2 Jupiter ROM-less microcontroller is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.
The V850E/CA2 Jupiter offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI) and measurement inputs (A/D converter), with dedicated CAN network support.
The device offers power-saving modes to manage the power consumption effectively under varying conditions.
Thus equipped, the V850E/CA2 Jupiter is ideally suited for automotive applications, like dashboard, gateway or body. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- 4 K iCache (2-way associative)
- Full-CAN Interface: 2 or 4 channels
- Serial Interfaces: 5 channels
  - 3-wire mode: 3 channels
  - UART mode: 2 channels
- Timers: 7 channels
  - 16-bit multi purpose timer/event counter: channels: 2 channels
  - 16-bit multi purpose timer: 1 channel
  - 16-bit OS timer: 2 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- 10-bit resolution A/D Converter: 12 channels
- External Bus Interface (16-bit data / 24-bit address)
- I/O lines: 78
- Power supply voltage range:
  - +4.5 V ≤ V_{DD5} ≤ +5.5 V
  - +3.0 V ≤ V_{DD3} ≤ +3.6 V
- Frequency range: up to 32 MHz
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Built-in clock oscillator circuit with internal Spread Spectrum PLL for CPU/ BCU clock operation
- Temperature range:
  - -40 °C to +85 °C (μPD703128(A), μPD703129(A))
  - -40 °C to +110 °C (μPD703129(A1))
- Package:
  - 144 LQFP, 0.5 mm pin-pitch (20 x 20 mm)

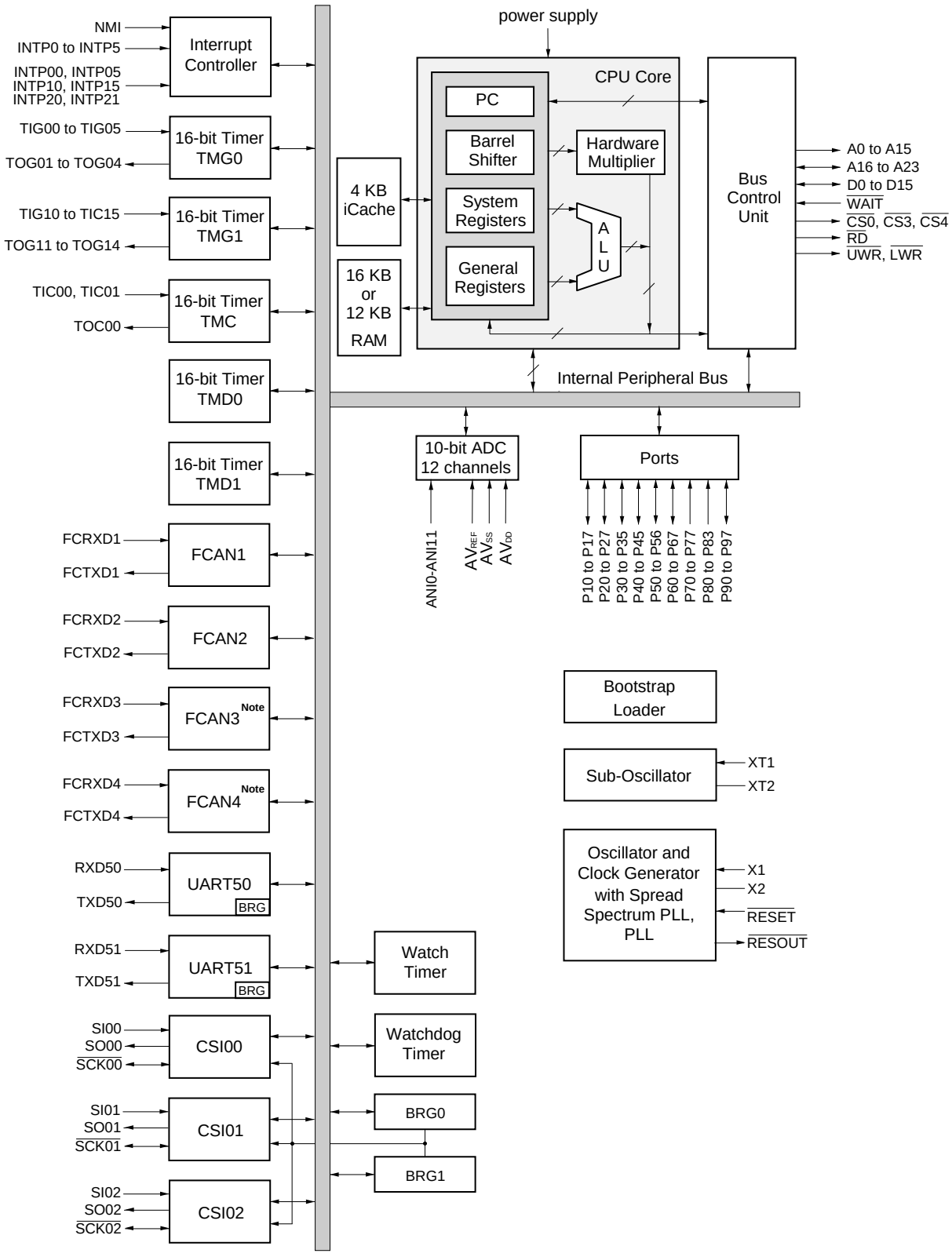
ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	FCAN Option	Operating Temperature (T_A)
V850E/CA2	μPD703129GJ(A)-xxx-UEN	LQFP144 20 x 20 mm	ROM-less	16 K	4 Channels	-40°C ~ +85°C
	μPD703129GJ(A1)-xxx-UEN		ROM-less	16 K	4 Channels	-40°C ~ +110°C
	μPD703128GJ(A)-xxx-UEN		ROM-less	12 K	2 Channels	-40°C ~ +85°C

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

Document No. U16307EE1V0DS00
Data Published: January 2003

INTERNAL BLOCK DIAGRAM



Note: FCRXD3, FCTXD3, FCRXD4 and FCTXD4 are available only in the derivatives μPD703129(A) and μPD703129(A1).

PIN IDENTIFICATION

A0 to A23	Address Bus	P80 to P83	Port 8
D0 to D15	Data Bus	P90 to P97	Port 9
ANI0 to ANI11	Analog Input	PAH0 to PAH7	Port AH
AV_{DD}	Analog Power Supply	PCM0	Port CM0
AV_{REF}	Analog Reference Voltage	PCS0, PCS3, PCS4	Port CS
AV_{SS}	Analog Ground	PCT0, PCT1, PCT4	Port CT
FCRXD1 to FCRXD4**Note**	CAN Receive Line Input	$\overline{\text{RESET}}$	Reset
FCTXD1 to FCTXD4**Note**	CAN Transmit Line Output	$\overline{\text{RESOUT}}$	Reset Out
CV_{DD}	Clock Generator Power Supply	RXD50 to RXD51	Receive Data Input
CV_{SS}	Clock Generator Ground	$\overline{\text{SCK00}}$ to $\overline{\text{SCK02}}$	Serial Clock
GND_{30} to GND_{36}	Ground for 3 V Power Supply	SI00 to SI02	Serial Input
GND_{50} to GND_{52}	Ground for 5 V Power Supply	SO00 to SO02	Serial Output
INTP0 to INTP5	External Interrupt Request	TIG00 to TIG05, TIG10 to TIG15, TIC00, TIC01	Timer Input
INTPn0, INTPn5, INTP2n	External Interrupt Request	TOG01 to TOG04, TOG11 to TOG14, TOC00	Timer Output
MODE0 to MODE2	Mode Inputs	TXD50 to TXD51	Transmit Data Output
NMI	Non-Maskable Interrupt Request	V_{DD30} to V_{DD36}	3 V Power Supply
P10 to P17	Port 1	V_{DD50} to V_{DD52}	5 V Power Supply
P20 to P27	Port 2	$\overline{\text{WAIT}}$	Wait
P30 to P35	Port 3	$\overline{\text{LWR}}$, $\overline{\text{UWR}}$	Write Enable
P40 to P45	Port 4	$\overline{\text{RD}}$	Read
P50 to P56	Port 5	$\overline{\text{CS0}}$, $\overline{\text{CS3}}$, $\overline{\text{CS4}}$	Chip Select
P60 to P67	Port 6	X1, X2	Crystal (Main-OSC)
P70 to P77	Port 7	XT1, XT2	Crystal (Sub-OSC)

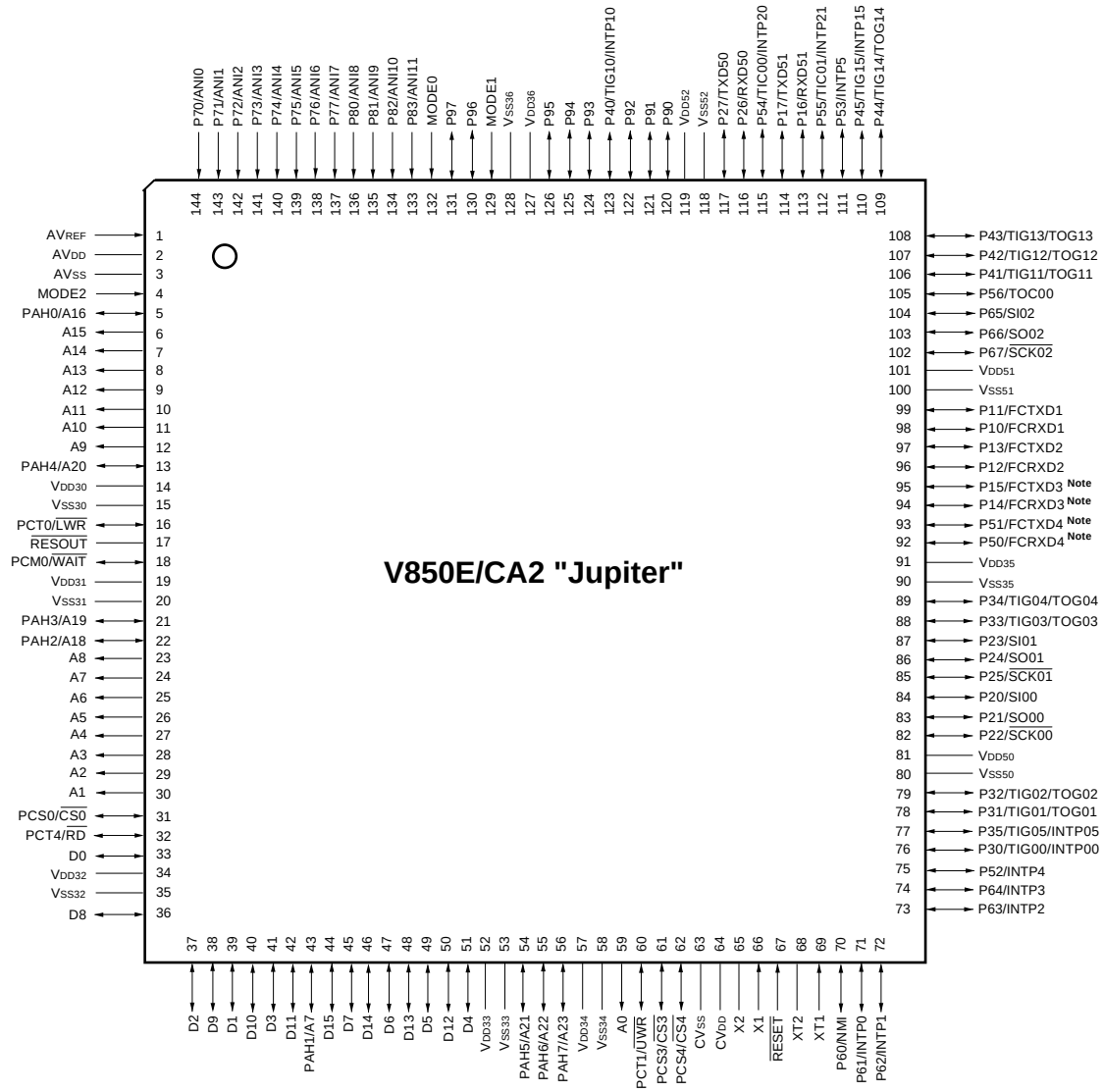
Note: FCRxD3, FCTxD3, FCRxD4 and FCTxD4 are available only in the derivative μPD703129 (A) and μPD703129 (A1).

Remark: n = 0, 1

PIN CONFIGURATION (Top View)

144-Pin Plastic LQFP (fine pitch) (20 mm × 20 mm)

- μPD703128(A)
- μPD703129(A)
- μPD703129(A1)



Note: FCRXD3, FCTXD3, FCRXD4 and FCTXD4 are available only in the derivatives μPD703129(A) and μPD703129(A1).

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1. Pin Functions

1.1 Port Pins

Table 1-1: Port Function (1/3)

Port	I/O	Function	Driver Type	Alternate
P10	I/O	Port 1: 8-bit input/output port	5-K	FCRXD1
P11				FCTXD1
P12				FCRXD2
P13				FCTXD2
P14				FCRXD3[Note]
P15				FCTXD3[Note]
P16				RXD51
P17				TXD51
P20	I/O	Port 2: 8-bit input/output port	5-K	SI00
P21				SO00
P22				$\overline{\text{SCK00}}$
P23				SI01
P24				SO01
P25				$\overline{\text{SCK01}}$
P26				RXD50
P27				TXD50
P30	I/O	Port 3: 6-bit input/output port	5-K	TIG00, INTP00
P31				TIG01, TOG01
P32				TIG02, TOG02
P33				TIG03, TOG03
P34				TIG04, TOG04
P35				TIG05, INTP05
P40	I/O	Port 4: 6-bit input/output port	5-K	TIG10, INTP10
P41				TIG11, TOG11
P42				TIG12, TOG12
P43				TIG13, TOG13
P44				TIG14, TOG14
P45				TIG15, INTP15
P50	I/O	Port 5: 7-bit input/output port	5-K	FCRXD4[Note]
P51				FCTXD4[Note]
P52				INTP4
P53				INTP5
P54				TIC00, INTP20
P55				TIC01, INTP21
P56				TOC0

Table 1-1: Port Function (2/3)

Port	I/O	Function	Driver Type	Alternate
P60	I/O	Port 6: 8-bit input/output port	5-K	$\overline{NMI}$
P61				INTP0
P62				INTP1
P63				INTP2
P64				INTP4
P65				SI02
P66				SO02
P67				$\overline{SCK02}$
P70	I	Port 78: 12-bit input port	9-C	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80				ANI8
P81				ANI9
P82				ANI10
P83				ANI11
P90	I/O	Port 9: 8-bit input/output port	5-K	-
P91				-
P92				-
P93				-
P94				-
P95				-
P96				-
P97				-
PAH0	I/O	Port AH: 8-bit input/output port	5	A16
PAH1				A17
PAH2				A18
PAH3				A19
PAH4				A20
PAH5				A21
PAH6				A22
PAH7				A23
PCS0	I/O	Port CS: 3-bit input/output port	5	$\overline{CS0}$
PCS3				$\overline{CS3}$
PCS4				$\overline{CS4}$

Table 1-1: Port Function (3/3)

Port	I/O	Function	Driver Type	Alternate
PCT0	I/O	Port CT: 2-bit input/ 3-bit output port	5	$\overline{WR0}$
PCT1				$\overline{WR1}$
PCT4	O			$\overline{RD}$
PCM0	I/O	Port CM: 1-bit input/output port	5	$\overline{WAIT}$

Note: FCRXD3, FCTXD3, FCRXD4 and FCTXD4 are available only in the derivatives μPD703129(A) and μPD703129(A1).

1.2 Non-port Pins

Table 1-2: Non-Port Functions (1/3)

Pin Name	I/O	Function	Termination if unused	Driver Type
V_{DD50} -V_{DD52}	–	Power supply 5.0 V	–	–
V_{SS50} - V_{SS52}		Ground for power supply 5.0 V		
V_{DD30} -V_{DD36} **Note 1**		Power supply 3.3 V		
V_{SS30} - V_{SS36}		Ground for power supply 3.3 V		
CV_{DD} **Note 2**		Power supply 3.3 V clock oscillator and PLL		
CV_{SS}		Ground for clock oscillator and PLL circuit		
X1	Input	Clock oscillator connection pins Caution: pins are 3.3 V	Refer to oscillator recommendations	16
X2	Output			
XT1	Input	Sub-Clock oscillator connection pins Caution: pins are 3.3 V		
XT2	Output			
MODE0 - MODE2	Input	Selects operating mode	–	2
$\overline{\text{RESET}}$	Input	System reset input	–	2
$\overline{\text{RESOUT}}$	Output	System reset output (incl. Watch dog timer reset)	–	3
AV_{DD}	–	Power supply for A/D converter	V_{DD5x}	–
AV_{SS}		Ground for A/D converter	V_{SS5x}	
AV_{REF}	Input	Reference voltage input for A/D converter	V_{DD5x}	
ANI0 - ANI11	Input	Analog input to A/D converter	V_{SS5x}	
$\overline{\text{NMI}}$	Input	Non-maskable interrupt	100 K to V_{DD5x}	5-K
SI00	Input	Serial receive data input to CSI00		
SO00	Output	Serial transmit data output from CSI00		
$\overline{\text{SCK00}}$	I/O	Serial clock I/O from/to CSI00		
SI01	Input	Serial receive data input to CSI01		
SO01	Output	Serial transmit data output from CSI01		
$\overline{\text{SCK01}}$	I/O	Serial clock I/O from/to CSI01		
SI02	Input	Serial receive data input to CSI02		
SO02	Output	Serial transmit data output from CSI02		
$\overline{\text{SCK02}}$	I/O	Serial clock I/O from/to CSI02		
RXD50	Input	Serial receive data input to UART50		
TXD50	Output	Serial transmit data output from UART50		
RXD51	Input	Serial receive data input to UART51		
TXD51	Output	Serial transmit data output from UART51		
FCRXD1	Input	Serial receive data input to FCAN1		
FCTXD1	Output	Serial transmit data output to FCAN1		
FCRXD2	Input	Serial receive data input to FCAN2		
FCTXD2	Output	Serial transmit data output FCAN2		

Table 1-2: Non-Port Functions (2/3)

Pin Name	I/O	Function	Termination if unused	Driver Type
FCRXD3[Note 3]	Input	Serial receive data input to FCAN3	100 K to V_{DD5x}	5-K
FCTXD3[Note 3]	Output	Serial transmit data output to FCAN3		
FCRXD4[Note 3]	Input	Serial receive data input to FCAN4		
FCTXD4[Note 3]	Output	Serial transmit data output to FCAN4		
INTP0 - INTP5	Input	External maskable interrupts 0-5		
INTP00	Input	External maskable interrupt 00		
INTP05	Input	External maskable interrupt 05		
INTP10	Input	External maskable interrupt 10		
INTP15	Input	External maskable interrupt 15		
INTP20	Input	External maskable interrupt 20		
INTP21	Input	External maskable interrupt 21		
TIG00	Input	Timer G0 capture input 0		
TIG01	Input	Timer G0 capture input 1		
TIG02	Input	Timer G0 capture input 2		
TIG03	Input	Timer G0 capture input 3		
TIG04	Input	Timer G0 capture input 4		
TIG05	Input	Timer G0 capture input 5		
TOG01	Output	Timer G0 compare output 1		
TOG02	Output	Timer G0 compare output 2		
TOG03	Output	Timer G0 compare output 3		
TOG04	Output	Timer G0 compare output 4		
TIG10	Input	Timer G1 capture input 0		
TIG11	Input	Timer G1 capture input 1		
TIG12	Input	Timer G1 capture input 2		
TIG13	Input	Timer G1 capture input 3		
TIG14	Input	Timer G1 capture input 4		
TIG15	Input	Timer G1 capture input 5		
TOG11	Output	Timer G1 compare output 1		
TOG12	Output	Timer G1 compare output 2		
TOG13	Output	Timer G1 compare output 3		
TOG14	Output	Timer G1 compare output 4		
TIC00	Input	Timer C1 capture input 0		
TIC01	Input	Timer C1 capture input 1		
TOC0	Output	Timer C1 compare output		

Table 1-2: Non-Port Functions (3/3)

Pin Name	I/O	Function	Termination if unused	Driver Type
D0 - D15	I/O	Data bus of external bus	100 K to V_{DD5x}	5
A0 - A7	Output	Address bus of external bus		4
A8 - A15	Output			
A16 - A23	I/O			5
$\overline{WR0}$	Output	Write strobe lower byte (bit 0 - 7)		
$\overline{WR1}$	Output	Write strobe upper byte (bit 8 - 15)		
$\overline{RD}$	Output	Read strobe for external bus		
$\overline{WAIT}$	Input	Wait control signal for external bus		
$\overline{CS0}$, $\overline{CS3}$, $\overline{CS4}$	Output	Chip select output for external bus		

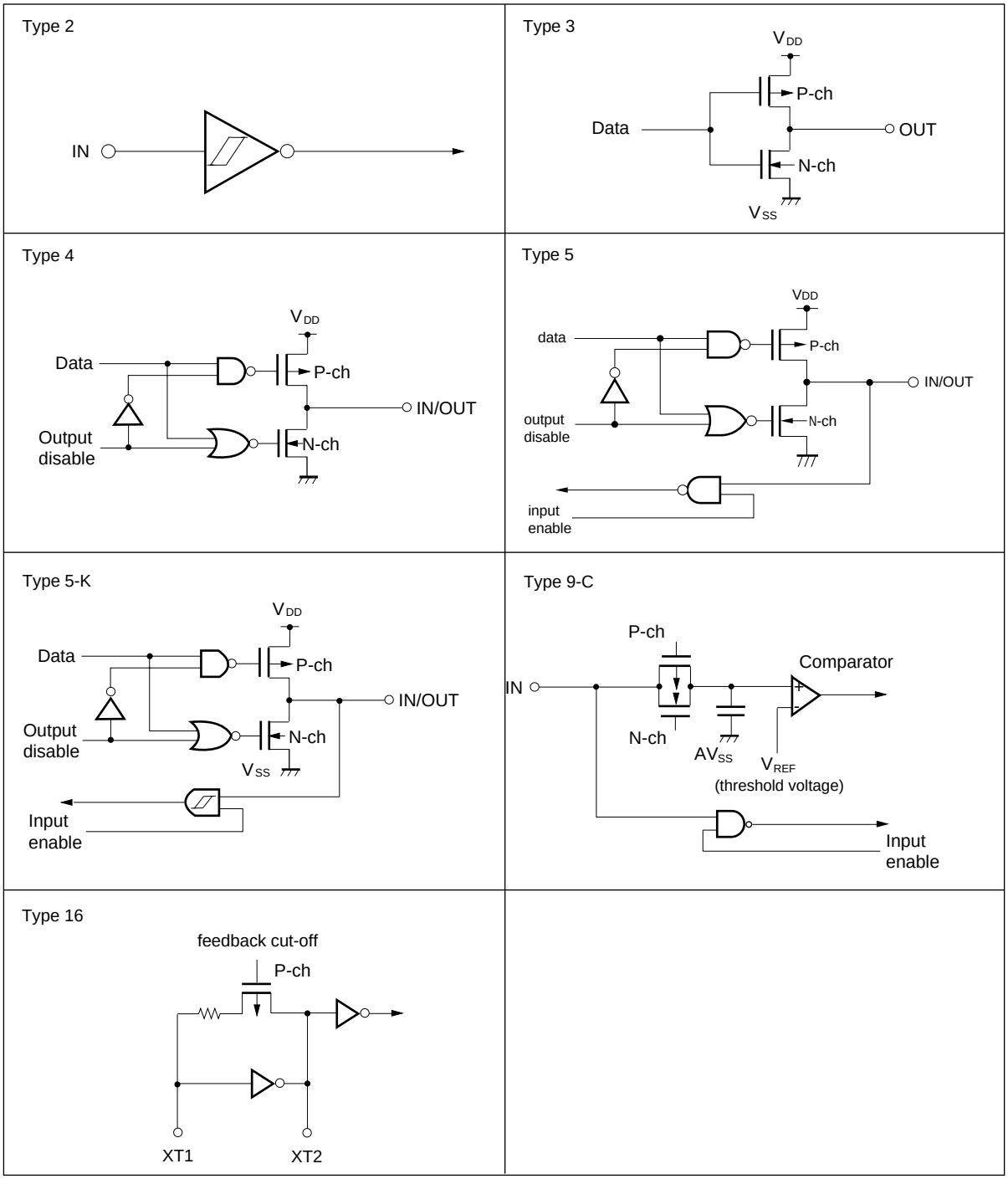
Notes: 1. All V_{DD3x} power supply pins must be tied together externally.
Resistance between V_{DD3x} pins must not exceed 0.1Ω DC /2.5 Ω at 20 MHz.

2. CV_{DD} and V_{DD3x} must be tied together externally.

3. FCRXD3, FCTXD3, FCRXD4 and FCTXD4 are available only in the derivatives μPD703129(A) and μPD703129(A1).

1.3 I/O Circuits

Figure 1-1: Input / Output Circuits



2. Electrical Specifications

2.1 Absolute Maximum Ratings

(T_A = 25°C, V_{SS3x} = 0V)

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD5x}		-0.5 ~ +6.0	V
		AV_{DD}	$AV_{DD} \leq V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
		V_{DD3x}		-0.5 ~ +4.6	V
		CV_{DD}		-0.5 ~ +4.6	V
		V_{SS5x}		-0.5 ~ +0.5	V
		AV_{SS}		-0.5 ~ +0.5	V
		CV_{SS}		-0.5 ~ +0.5	V
Input voltage	5 V pins	V_{I1} **Note 1**	$V_{I1} < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
		AV_{REF}	$AV_{REF} \leq AV_{DD}$ + 0.5 V	-0.5 ~ +6.0	V
	3.3 V pins	V_{I2} **Note 2**	$V_{I2} < V_{DD3x}$ + 0.5 V	-0.5 ~ +4.6	V
	P7, P8	V_{IA}	$V_{IA} < AV_{DD}$ + 0.5 V	-0.5 ~ +6.0	V
Output current low	1 pin	I_{OL0}		4.0	mA
	All pins	I_{OL1}		50	mA
Output current high	1 pin	I_{OH0}		-4.0	mA
	All pins	I_{OH1}		-50	mA
Output voltage	5 V pins **Note 3**	V_{O1}	$V_{O1} < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
Output voltage	3.3 V pins **Note 4**	V_{O2}	$V_{O2} < V_{DD3x}$ + 0.5 V	-0.5 ~ +4.6	V
Operating temperature		T_{OPR}	μPD703128(A), μPD703129(A)	-40 ~ +85	°C
			μPD703129(A1)	-40 ~ +110	°C
Storage temperature		T_{STGB}		-55 ~ +150	°C

Notes: 1. Referenced 5 V pins are P1, P2, P3, P4, P5, P6, P9, $\overline{\text{RESET}}$, MODE0, MODE1

2. Referenced 3.3 V pins are PAH, PD, PCS, PCM, PCT, MODE2

3. Referenced 5 V pins are P1, P2, P3, P4, P5, P6, P9

4. Referenced 3.3 V pins are PA, PD, PCS, PCM, PCT, $\overline{\text{RESOUT}}$

2.2 General Characteristics

2.2.1 Main Oscillator Characteristics

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = A_{VDD}$ = 4.0 V ~ 5.5 V, $CV_{DD} = V_{DD3x}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-2: Main Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			10	ms
Main oscillator frequency	f_{OSC}	OSC MODE	4		5	MHz

2.2.2 Sub Oscillator Characteristics

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = A_{VDD}$ = 4.0 V ~ 5.5 V, $CV_{DD} = V_{DD3x}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-3: Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{SOST}	OSC MODE			tbd.	ms
Sub oscillator frequency	f_{SOSC}	OSC MODE		32.768		KHz

2.2.3 Peripheral PLL Characteristics

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = A_{VDD}$ = 4.0 V ~ 5.5 V, $CV_{DD} = V_{DD3x}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-4: Peripheral PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL lock time	T_{PLL}	OSC MODE: T_A = -40 ~ +85°C			1	ms
		OSC MODE: T_A = -40 ~ +110°C			1	ms

2.2.4 Spread Spectrum PLL Characteristics

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = A_{VDD}$ = 4.0 V ~ 5.5 V, $CV_{DD} = V_{DD3x}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-5: Spread Spectrum PLL Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SSCG lock time	T_{SSCG}	T_A = -40 ~ +85°C			3	ms
		T_A = -40 ~ +110°C			3	ms
Frequency multiplication	M_{SSCG}	f_{OSC} = 4 MHz		32.0		-
		f_{OSC} = 5 MHz		25.5		-
Frequency modulation		Dithering enabled		0.65		%

2.2.5 I/O Capacitances

(T_A = 25°C, $V_{DD5x} = V_{SS5x} = V_{DD3x} = V_{SS3x} = CV_{DD} = CV_{SS} = A_{VDD} = A_{VSS}$ = 0 V)

Table 2-6: I/O Capacitances

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

2.3 Operating Conditions

2.3.1 Peripheral Clock Operating Frequency

(V_{DD5x} = AV_{DD} = 4.0 V ~ 5.5 V, CV_{DD} = V_{DD3x}, V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 2-7: Peripheral Clock Operating Frequency

Operation Mode	Operating Temperature (T_A)		Supply Voltage (V_{DD3x})	Inside Operation Clock Frequency
Main OSC Mode, PLL on**Note 1**	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	16 to 20 MHz
	μPD703129(A1)	-40°C ~ +110°C		
Main OSC Mode, PLL off**Note 2**	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	4 to 5 MHz
	μPD703129(A1)	-40°C ~ +110°C		

Notes: 1. The inside peripheral operation clock frequency is the crystal frequency multiplied with the multiplication factor x4.

2. The inside peripheral operation clock frequency is the crystal frequency.

2.3.2 CPU Clock Operating Frequency

(V_{DD5x} = AV_{DD} = 4.0 V ~ 5.5 V, CV_{DD} = V_{DD3x}, V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 2-8: CPU Clock Operating Frequency

Operation Mode	Operating Temperature (T_A)		Supply Voltage (V_{DD3x})	Inside Operation Clock Frequency
Main OSC Mode, SSCG on[Note 1]	μPD703128(A), μPD703129(A), μPD703129(A1)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	16 to 32 MHz
	μPD703129(A1)	-40°C ~ +110°C		16 to 20 MHz
Main OSC Mode, PLL on[Note 2]	μPD703128(A), μPD703129(A), μPD703129(A1)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	16 to 32 MHz
	μPD703129(A1)	-40°C ~ +110°C		16 to 20 MHz
Main OSC Mode, SSCG off, PLL off[Note 3]	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	4 to 5 MHz
	μPD703129(A1)	-40°C ~ +110°C		
Sub-OSC Mode	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	32 KHz
	μPD703129(A1)	-40°C ~ +110°C		

Notes: 1. The max. inside operation clock frequency is the crystal frequency multiplied with a multiplication factor configured in the SSCG Frequency Control Register 1 (SCFC1) and divided by a factor configured in the SSCG Frequency Modulation Control Register (SCFMC).

2. The inside operation clock frequency is the crystal frequency multiplied with the multiplication factor x4 or x8 according to the setting of the Processor Clock Control Register (PCC).

3. The inside operation clock frequency is the crystal frequency.

2.3.3 Watch Timer Clock Operating Frequency

(V_{DD5x} = AV_{DD} = 4.0 V ~ 5.5 V, CV_{DD} = V_{DD3x}, V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 2-9: Peripheral Clock Operating Frequency

Operation Mode	Operating Temperature (T_A)		Supply Voltage (V_{DD3x})	Inside Operation Clock Frequency
Main OSC Mode	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	$f_{Main-OSC}$/128, $f_{Main-OSC}$/512, $f_{Main-OSC}$/4096
	μPD703129(A1)	-40°C ~ +110°C		
Sub-OSC Mode	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	$f_{Sub-OSC}$/4, $f_{Sub-OSC}$/32
	μPD703129(A1)	-40°C ~ +110°C		

2.3.4 Watchdog Timer Clock Operating Frequency

(V_{DD5x} = AV_{DD} = 4.0 V ~ 5.5 V, CV_{DD} = V_{DD3x}, V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS} = 0 V)

Table 2-10: Peripheral Clock Operating Frequency

Operation Mode	Operating Temperature (T_A)		Supply Voltage (V_{DD3x})	Inside Operation Clock Frequency
Main OSC Mode	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	$f_{Main-OSC}$, $f_{Main-OSC}$/128
	μPD703129(A1)	-40°C ~ +110°C		
Sub-OSC Mode	μPD703128(A), μPD703129(A)	-40°C ~ +85°C	3.0 V ≤ V_{DD3x} ≤ 3.6 V	$f_{Sub-OSC}$
	μPD703129(A1)	-40°C ~ +110°C		

2.4 DC Characteristics

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-11: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	Port pins group 1**Not 1**	V_{IH1}	4.0 V ≤ V_{DD5x} = AV_{DD} ≤ 5.5 V	0.8 V_{DD5x}		V_{DD5x}	V
Input voltage low	Port pins group 1**Note1**	V_{IL1}	4.0 V ≤ V_{DD5x} = AV_{DD} ≤ 5.5 V	0		0.2 V_{DD5x}	V
Input voltage high	P9	V_{IH2}		0.8 V_{DD5x}		V_{DD5x}	V
Input voltage low	P9	V_{IL2}		0		0.4 V_{DD5x}	V
Input voltage high	Port pins group 2**Note2**	V_{IH3}		0.7 V_{DD3x}		V_{DD3x}	V
Input voltage low	Port pins group 2**Not 2**	V_{IL3}		0		0.3 V_{DD3x}	V
Input voltage high	MODE2	V_{IH4}		0.8 V_{DD3x}		V_{DD3x}	V
Input voltage low	MODE2	V_{IL4}		0		0.2 V_{DD3x}	V
Input voltage high	P7, P8	V_{IHA}	V_{DD5x} - 0.3 V ≤ AV_{DD} ≤ V_{DD5x}	0.7 V_{DD5x}		V_{DD5x}	V
Input voltage low	P7, P8	V_{ILA}	V_{DD5x} - 0.3 V ≤ AV_{DD} ≤ V_{DD5x}	0		0.3 V_{DD5x}	V
Output voltage high	Port pins group 3**Note3**	V_{OH1}	I_{OH5} = -3.0 mA	V_{DD5x} - 1.0 V			V
		V_{OH1A}	I_{OH5} = -0.5 mA, V_{DD5x} = AV_{DD} = 4.0 V	V_{DD5x} - 1.0 V			V
Output voltage low	Port pins group 3**Note3**	V_{OL1}	I_{OL5} = 3.0 mA			0.4	V
		V_{OL1A}	I_{OL5} = 0.5 mA, V_{DD5x} = AV_{DD} = 4.0 V			0.4	V
Output voltage high	Port pins group 4**Note4**	V_{OH2}	I_{OH3} = -2.5 mA	V_{DD3x} - 1.0 V			V
Output voltage low	Port pins group 4**Note4**	V_{OL2}	I_{OL3} = 2.5 mA			0.4	V
Input leakage current, high	Port pins group 1**Note1**, P9	I_{LIH1}	V_I = V_{DD5}			5	μA
Input leakage current, low	Port pins group 1**Note1**, P9	I_{LIL1}	V_I = 0 V			-5	μA

Table 2-11: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	P7, P8	I_{LIHA}	$AV_{IN} = AV_{DD}$			2	μA
Input leakage current, low	P7, P8	I_{LILA}	$AV_{IN} = 0$ V			-2	μA
Input leakage current, high	Port pins group 2**Note2**, MODE2	I_{LIH2}	$V_I = V_{DD3}$			5	μA
Input leakage current, low	Port pins group 2**Note2**, MODE2	I_{LIL2}	$V_I = 0$ V			-5	μA

Notes: 1. Port pins group 1: P1, P2, P3, P4, P5, P6, MODE0, MODE1, $\overline{\text{RESET}}$

2. Port pins group 2: PAH, PD, PCS, PCM, PCT, MODE2

3. Port pins group 3: P1, P2, P3, P4, P5, P6, P9

4. Port pins group 4: PA, PAH, PD, PCS, PCM, PCT, RESOUT

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
V_{DD5x} = AV_{DD} = 4.5 V ~ 5.5 V, V_{DD3x} = CV_{DD} = 3.0 V ~ 3.6 V, V_{SS5x} = V_{SS3x} = AV_{SS} = CV_{SS} = 0 V,
f_{OSC} = 4 MHz)

Table 2-11: DC Characteristics (1/2)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1SC1}	Operating (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		86	129	mA
	I_{DD1SC2}	Operating (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		48	72	mA
	I_{DD1P1}	Operating (PLL1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		78	117	mA
	I_{DD1P2}	Operating (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		55	83	mA
	I_{DD1O}	Operating (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		18	27	mA
	I_{DD2SC1}	HALT (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		65	98	mA
	I_{DD2SC2}	HALT (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		40	60	mA
	I_{DD2P1}	HALT (PLL1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		55	83	mA
	I_{DD2P2}	HALT (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		38	57	mA
	I_{DD2O}	HALT (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		10	15	mA

Table 2-11: DC Characteristics (2/2)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD3SC1}	IDLE (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		11	22	mA
	I_{DD3SC2}	IDLE (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		11	22	mA
	I_{DD3P1}	IDLE (PLL1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		1.8	3.6	mA
	I_{DD3P2}	IDLE (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		1.8	3.6	mA
	I_{DD3O}	IDLE (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		1.1	2.3	mA
	I_{DD4}	WATCH[Note 2]		700	1300	μA
	I_{DD5P}	STOP		50	300	μA

Notes: 1. All supply currents specified above are representing the total current consumption of the power supply pins V_{DD31}, V_{DD34}, V_{DD35} and V_{DD36}. ADC and I/O buffer are not included.

2. The Watch timer and the Watchdog timer are supplied with a clock of 32 KHz.

(T_A= -40 ~ +110°C: μPD703129 (A1),
V_{DD5x} = AV_{DD} = 4.5 V ~ 5.5 V, V_{DD3x} = CV_{DD} = 3.0 V ~ 3.6 V, V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS} = 0 V,
f_{OSC} = 4 MHz)

Table 2-11: DC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1SC2}	Operating (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		48	72	mA
	I_{DD1P2}	Operating (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		55	83	mA
	I_{DD1O}	Operating (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		18	27	mA
	I_{DD2SC2}	HALT (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		40	60	mA
	I_{DD2P2}	HALT (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		38	57	mA
	I_{DD2O}	HALT (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		10	15	mA
	I_{DD3SC2}	IDLE (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: on, PLL: on		tbd.	tbd.	mA
	I_{DD3P2}	IDLE (PLL2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 16 MHz SSCG: off, PLL: on		tbd.	tbd.	mA
	I_{DD3O}	IDLE (OSC): f_{CPU} = 4 MHz, $f_{Peripherals}$ = 4 MHz SSCG: off, PLL: off		1.2	2.4	mA
	I_{DD4}	WATCH[Note 2]		800	1600	μA
	I_{DD5P}	STOP		50	500	μA

Notes: 1. All supply currents specified above are representing the total current consumption of the power supply pins V_{DD31}, V_{DD34}, V_{DD35} and V_{DD36}. ADC and I/O buffer are not included.

2. The Watch timer and the Watchdog timer are supplied with a clock of 32 KHz.

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
V_{DD5x} = AV_{DD} = 4.5 V ~ 5.5 V, V_{DD3x} = CV_{DD} = 3.0 V ~ 3.6 V, V_{SS5x} = V_{SS3x} = AV_{SS} = CV_{SS} = 0 V,
f_{OSC} = 5 MHz)

Table 2-11: DC Characteristics (1/2)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1SC1}	Operating (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		108	162	mA
	I_{DD1SC2}	Operating (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		54	81	mA
	I_{DD1P2}	Operating (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		68	102	mA
	I_{DD1O}	Operating (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		21	32	mA
	I_{DD2SC1}	HALT (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		80	120	mA
	I_{DD2SC2}	HALT (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		44	66	mA
	I_{DD2P2}	HALT (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		42	63	mA
	I_{DD2O}	HALT (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		13	20	mA

Table 2-11: DC Characteristics (2/2)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD3SC1}	IDLE (SSCG1): f_{CPU} = 32 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		13	26	mA
	I_{DD3SC2}	IDLE (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		13	26	mA
	I_{DD3P2}	IDLE (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		2.5	5	mA
	I_{DD3O}	IDLE (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		1.4	2.8	mA
	I_{DD4}	WATCH[Note 2]		900	1800	μA
	I_{DD5P}	STOP		50	300	μA

Notes: 1. All supply currents specified above are representing the total current consumption of the power supply pins V_{DD31}, V_{DD34}, V_{DD35} and V_{DD36}. ADC and I/O buffer are not included.

2. The Watch timer and the Watchdog timer are supplied with a clock of 32 KHz.

(T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V,
f_{OSC} = 5 MHz)

Table 2-11: DC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1SC2}	Operating (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		54	81	mA
	I_{DD1P2}	Operating (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		68	102	mA
	I_{DD1O}	Operating (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		21	32	mA
	I_{DD2SC2}	HALT (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		40	60	mA
	I_{DD2P2}	HALT (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		45	68	mA
	I_{DD2O}	HALT (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		13	26	mA
	I_{DD3SC2}	IDLE (SSCG2): f_{CPU} = 16 MHz, $f_{Peripherals}$ = 20 MHz SSCG: on, PLL: on		13	26	mA
	I_{DD3P2}	IDLE (PLL2): f_{CPU} = 20 MHz, $f_{Peripherals}$ = 20 MHz SSCG: off, PLL: on		2.5	5	mA
	I_{DD3O}	IDLE (OSC): f_{CPU} = 5 MHz, $f_{Peripherals}$ = 5 MHz SSCG: off, PLL: off		1.4	3.0	mA
	I_{DD4}	WATCH[Note 2]		900	2000	μA
	I_{DD5P}	STOP		50	500	μA

Notes: 1. All supply currents specified above are representing the total current consumption of the power supply pins V_{DD31}, V_{DD34}, V_{DD35} and V_{DD36}. ADC and I/O buffer are not included.

2. The Watch timer and the Watchdog timer are supplied with a clock of 32 KHz.

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V,
f_{OSC} = 4 MHz ~ 5 MHz, Main-Osc: Off)

Table 2-11: DC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1S}	Operating[Note 2] (Sub-Osc.): f_{CPU} = 32 KHz, $f_{Peripherals}$ = 0 Hz SSCG: off, PLL: off		50	350	μA
	I_{DD4S}	Sub-WATCH[Note 3] (Sub-Osc.): SSCG: off, PLL: off		50	325	μA

(T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V,
f_{OSC} = 4 MHz ~ 5 MHz, Main-Osc: Off)

Table 2-11: DC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply Current[Note 1]	I_{DD1S}	Operating[Note 2] (Sub-Osc.): f_{CPU} = 32 KHz, $f_{Peripherals}$ = 0 Hz SSCG: off, PLL: off		60	550	μA
	I_{DD4S}	Sub-WATCH[Note 3] (Sub-Osc.): SSCG: off, PLL: off		60	550	μA

Notes: 1. All supply currents specified above are representing the total current consumption of the power supply pins V_{DD31}, V_{DD34}, V_{DD35} and V_{DD36}. ADC and I/O buffer are not included.

2. During the Sub-Oscillation mode the following operation limitations become valid :

- No iCache operation during the Sub-Osc. operating mode. Be sure to disable iCache operation before entering the Sub-Osc. operating mode
- No instruction fetcj from iRAM during operation in Sub-Osc. operating mode

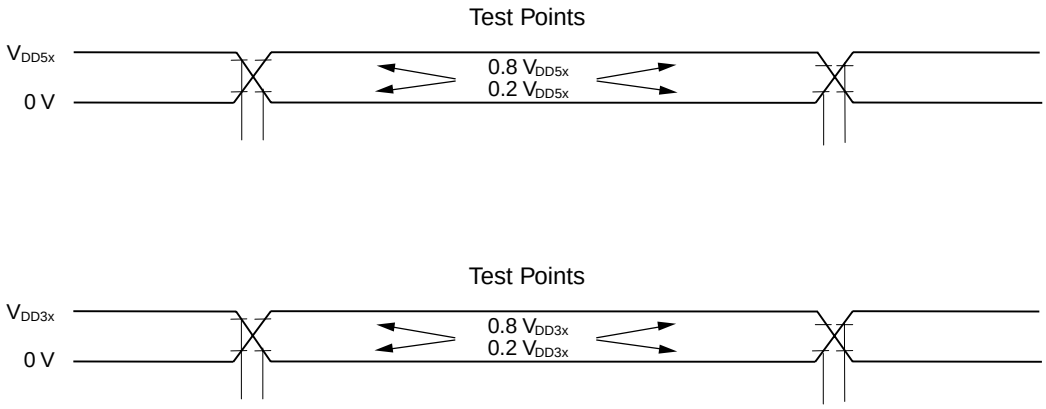
3. The Watch timer and the Watchdog timer are supplied with a clock of 32 KHz.

2.5 AC Characteristics

2.5.1 General

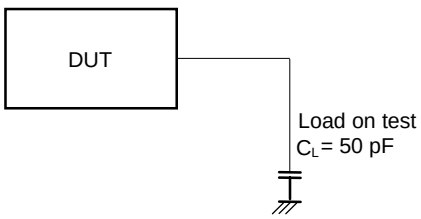
(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $V_{SS5x} = V_{SS3x} = AV_{SS} = CV_{SS}$ = 0 V,
Output pin load capacitance: C_L= 50 pF)

Figure 2-1: AC Test Input Waveform, AC Test Load Condition



2.5.2 AC Test Load Condition

Figure 2-2: AC Test Load Condition



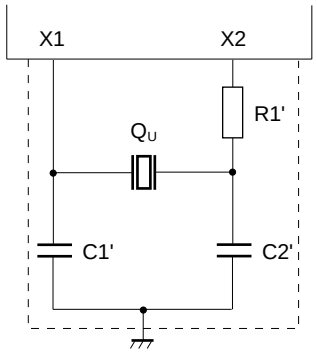
2.5.3 Recommended Main Oscillator Circuit

(1) Main system clock oscillator

(a) Ceramic resonator or crystal resonator connection

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1))

Figure 2-3: Main Oscillator Recommendations



Remark: Values of capacitors C1', C2' and R1' depend on used resonator and must be specified in cooperation with the manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Table 2-12: Main system clock crystal recommendation

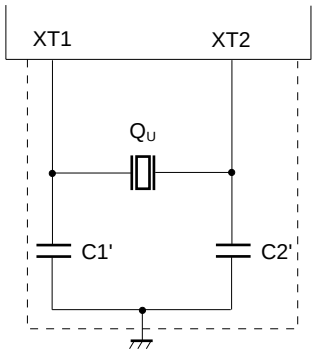
Manufacturer	Type/Series	Q_U [MHz]	R1' [Ω]	C1' [pF]	C2' [pF]
KINSEKI	CX-49F	4.000	1200	12	12
NDK	AT-51	4.000	0	12	12
ABRACON	HC49U P/N AB	4.000	0	15-22	15-22
ABRACON	HC49US P/N ABL	4.000	0	15-22	15-22

(2) Recommended Sub-system clock oscillator circuit

(a) Ceramic resonator or crystal resonator connection

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1))

Figure 2-4: Sub Oscillator Recommendations



Remark: Values of capacitors C1', C2' depend on used resonator and must be specified in cooperation with the manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the sub system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Table 2-13: Sub-system clock crystal recommendation

Manufacturer	Type/Series	Q_U [KHz]	C1' [pF]	C2' [pF]
		32.768	tbd.	tbd.

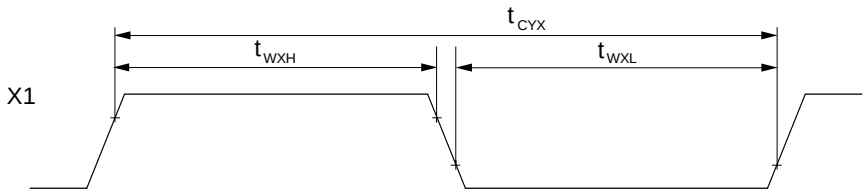
2.5.4 Clock timing

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
V_{DD5x} = 4.5 V ~ 5.5 V, V_{DD3x} = CV_{DD} = 3.0 V ~ 3.6 V, V_{SS5x} = V_{SS3x} = CV_{SS} = 0 V)

Table 2-14: Clock Timing

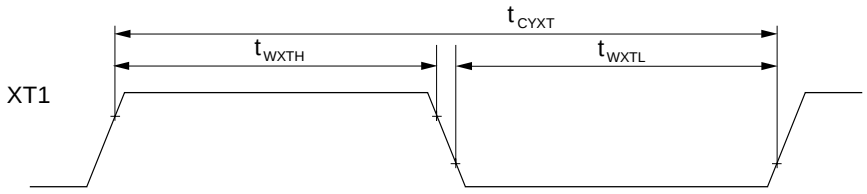
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
X1 input cycle	t_{CYX}	OSC Mode	200		250	ns
X1 input high-level width	t_{WXH}	OSC Mode	95			ns
X1 input low-level width	t_{WXL}	OSC Mode	95			ns
XT1 input cycle	t_{CYXT}	OSC Mode	30.5		30.6	μs
XT1 input high-level width	t_{WXTH}	OSC Mode	15			μs
XT1 input low-level width	t_{WXTL}	OSC Mode	15			μs

Figure 2-5: Clock Timing (1/2)



Caution: The voltage power on the main oscillator input pin X1 must not exceed 3.6 V

Figure 2-5: Clock Timing (2/2)



Caution: The voltage power on the sub-oscillator input pin XT1 must not exceed 3.6 V.

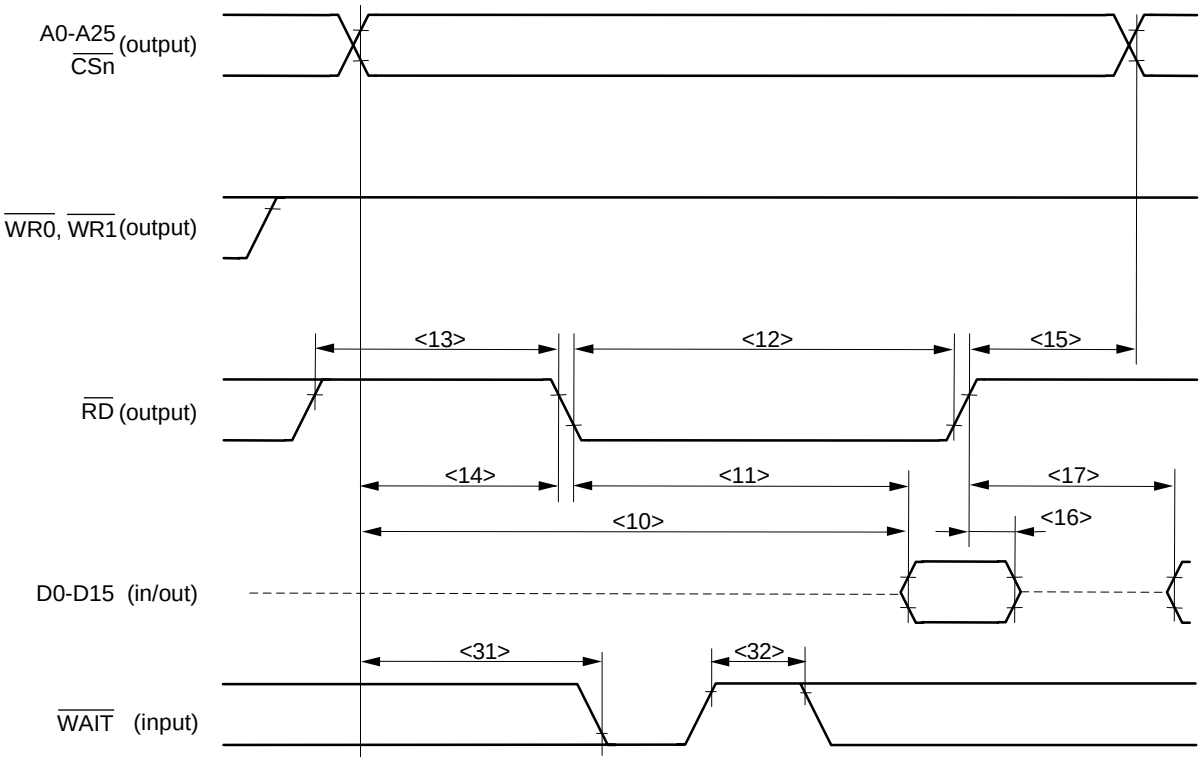
2.5.5 External Memory Access Read Timing in R1/S1 (Direct) Mode

Table 2-15: External Memory Access Read Timing in R1/S1 (Direct) Mode

Parameter		Symbol	MIN.	MAX.	Unit
Data input set up time (vs. address)	<10>	T_{SAIDD}		$(2 + w_{AS} + w_D + w)T - 23$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDIDD}		$(1.5 + w_D + w)T - 20$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDLD}	$(1.5 + w_D + w)T - 10$		ns
$\overline{RD}$ High level width	<13>	T_{WRDHD}	$(0.5 + w_{AS} + i)T - 10$		ns
Address, $\overline{CSn} \rightarrow \overline{RD}\downarrow$ delay time	<14>	T_{DARDD}	$(0.5 + w_{AS})T - 15$		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15>	T_{DRDAD}	iT - 8		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDIDD}	- 8		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17>	T_{DRDODD}	(0.5 + i)T - 6		ns
$\overline{WAIT}$ set up time (vs. address)	< 31 >	T_{SAWD}		$(1 + w_{AS})$ T- 30	ns
$\overline{WAIT}$ high level width	<32>	T_{WWHD}	T + 10		ns

Remarks:
1. T: $1/f_{CPU}$
2. i: Number of idle states specified by BCC register
3. w_{AS}: Number of waits specified by ASC register
4. w_D: Number of waits specified by DWC1, DWC2 register; $w_D \geq 1$
5. w: Number of waits due to $\overline{WAIT}$

Figure 2-6: External Memory Access Read Timing in R1/S1 (Direct) Mode



2.5.6 External Memory Access Write Timing in R1/S1 (Direct) Mode

Table 2-16: External Memory Access Write Timing in R1/S1 (Direct) Mode

Parameter		Symbol	MIN.	MAX.	Unit
Address, $\overline{CSn} \rightarrow \overline{WR0}$, $\overline{WR1}\downarrow$ delay time	<20>	T_{DAWRD}	$(0.5 + w_{AS})T - 12$		ns
Address set up (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<21>	T_{SAWRD}	$(1.5 + w_{AS} + w_D + w)T - 15$		ns
$\overline{WR0}$, $\overline{WR1}\uparrow \rightarrow$ address delay time	<22>	T_{DWRAD}	$(0.5 + i)T - 10$		ns
$\overline{WR0}$, $\overline{WR1}$ High level width	<23>	T_{WWRHD}	$(1 + i + w_{AS})T - 5$		ns
$\overline{WR0}$, $\overline{WR1}$ Low level width	<24>	T_{WWRLD}	$(1 + w + w_D)T - 10$		ns
Data output set up time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<25>	T_{SODWRD}	$(0.5 + w_{AS} + w_D + w)T - 18$		ns
Data output hold time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<26>	T_{HWRODD}	$(0.5 + i)T - 5$		ns
$\overline{WAIT}$ set up time (vs. address)	<31>	T_{SAWD}		$(1 + w_{AS})T - 30$	ns
$\overline{WAIT}$ high level width	<32>	TWWHD	T + 10		ns

Remarks: **1.** T: $1/f_{CPU}$

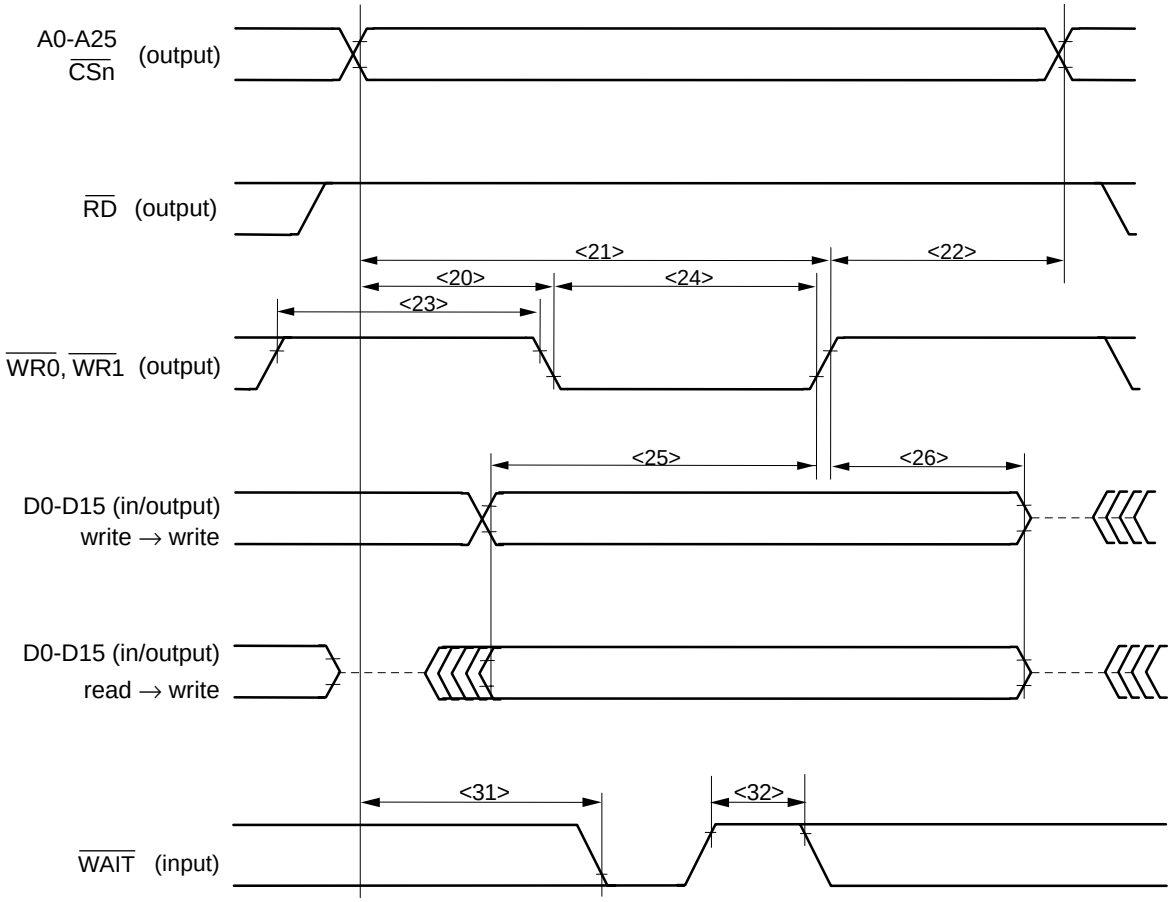
2. i: Number of idle states specified by BCC register

3. w_{AS}: Number of waits specified by ASC register

4. w_D: Number of waits specified by DWC1, DWC2 register; $w_D \geq 1$

5. w: Number of waits due to $\overline{WAIT}$

Figure 2-7: External Memory Access Write Timing in R1/S1 (Direct) Mode



2.5.7 External Memory Access Read Timing in R0/S0 (low EMI) Mode

Table 2-17: External Memory Access Read Timing in R0/S0 (low EMI) Mode

Parameter		Symbol	MIN.	MAX.	Unit
Data input set up time (vs. address)	<10>	T_{SAID}		$(2 + w_{AS} + w_D + w)T - 34$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}		$(1.5 + w_D + w)T - 22$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}	$(1.5 + w_D + w)T - 10$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}	$(0.5 + w_{AS} + i)T - 10$		ns
Address, $\overline{CSn} \rightarrow \overline{RD}\downarrow$ delay time	<14>	T_{DARD}	$(0.5 + w_{AS})T - 20$		ns
$\overline{RD}\uparrow \rightarrow$ address delay time	<15>	T_{DRDA}	$iT - 5$		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}	0		ns
$\overline{RD}\uparrow \rightarrow$ data output delay time	<17>	T_{DRDOD}	$(0.5 + i)T - 6$		ns
$\overline{WAIT}$ set up time (vs. address)	< 31 >	T_{SAW}		$(1 + w_{AS})$ T- 37	ns
$\overline{WAIT}$ high level width	<32>	T_{WWH}	T + 10		ns

Remarks: **1.** T: $1/f_{CPU}$

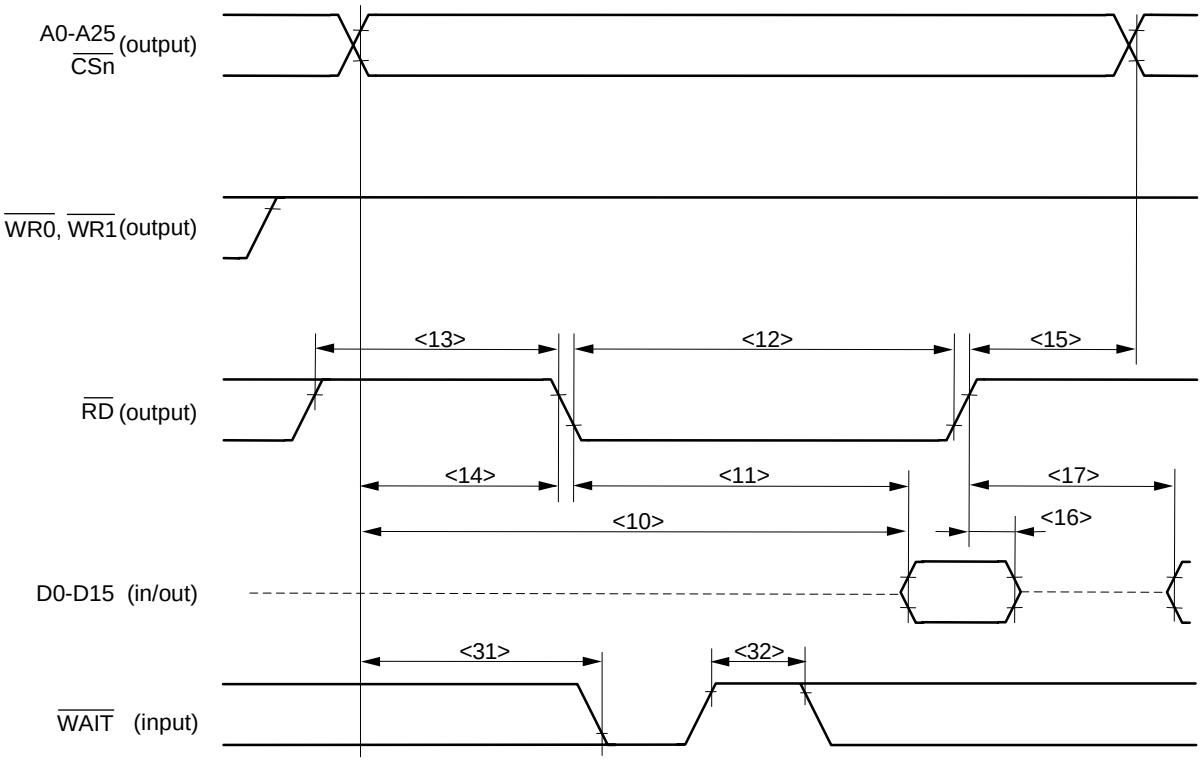
2. i: Number of idle states specified by BCC register

3. w_{AS}: Number of waits specified by ASC register

4. w_D: Number of waits specified by DWC1, DWC2 register; $w_D \geq 1$

5. w: Number of waits due to $\overline{WAIT}$

Figure 2-8: External Memory Access Read Timing in R0/S0 (low EMI) Mode



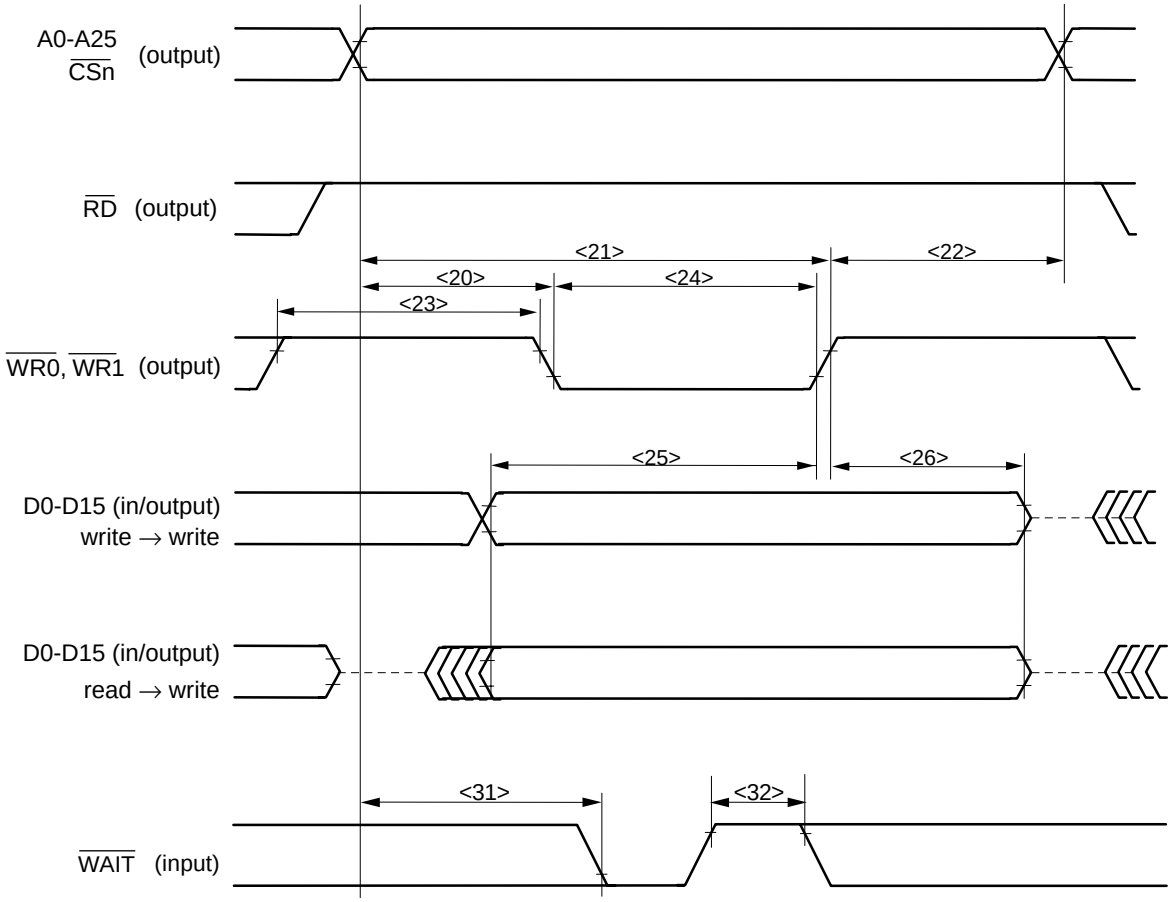
2.5.8 External Memory Access Write Timing in R0/S0 (low EMI) Mode

Table 2-18: External Memory Access Write Timing in R0/S0 (low EMI) Mode

Parameter		Symbol	MIN.	MAX.	Unit
Address, $\overline{CSn} \rightarrow \overline{WR0}$, $\overline{WR1}\downarrow$ delay time	<20>	T_{DAWR}	$(0.5 + w_{AS})T - 18$		ns
Address set up (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<21>	T_{SAWR}	$(1.5 + w_{AS} + w_D + w)T - 19$		ns
$\overline{WR0}$, $\overline{WR1}\uparrow \rightarrow$ address delay time	<22>	T_{DWRA}	$(0.5 + i)T - 5$		ns
$\overline{WR0}$, $\overline{WR1}$ High level width	<23>	T_{WWRH}	$(1 + i + w_{AS})T - 5$		ns
$\overline{WR0}$, $\overline{WR1}$ Low level width	<24>	T_{WWRL}	$(1 + w + w_D)T - 10$		ns
Data output set up time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<25>	T_{SODWR}	$(0.5 + w_{AS} + w_D + w)T - 18$		ns
Data output hold time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<26>	T_{HWROD}	$(0.5 + i)T - 5$		ns
$\overline{WAIT}$ set up time (vs. address)	<31>	T_{SAW}		$(1 + w_{AS})T - 37$	ns
$\overline{WAIT}$ high level width	<32>	TWWH	T + 10		ns

Remarks:
1. T: $1/f_{CPU}$
2. i: Number of idle states specified by BCC register
3. w_{AS}: Number of waits specified by ASC register
4. w_D: Number of waits specified by DWC1, DWC2 register; $w_D \geq 1$
5. w: Number of waits due to $\overline{WAIT}$

Figure 2-9: External Memory Access Write Timing in R0/S0 (low EMI) Mode



2.5.9 RESET (power up/down Sequence)

Table 2-19: Reset Timing

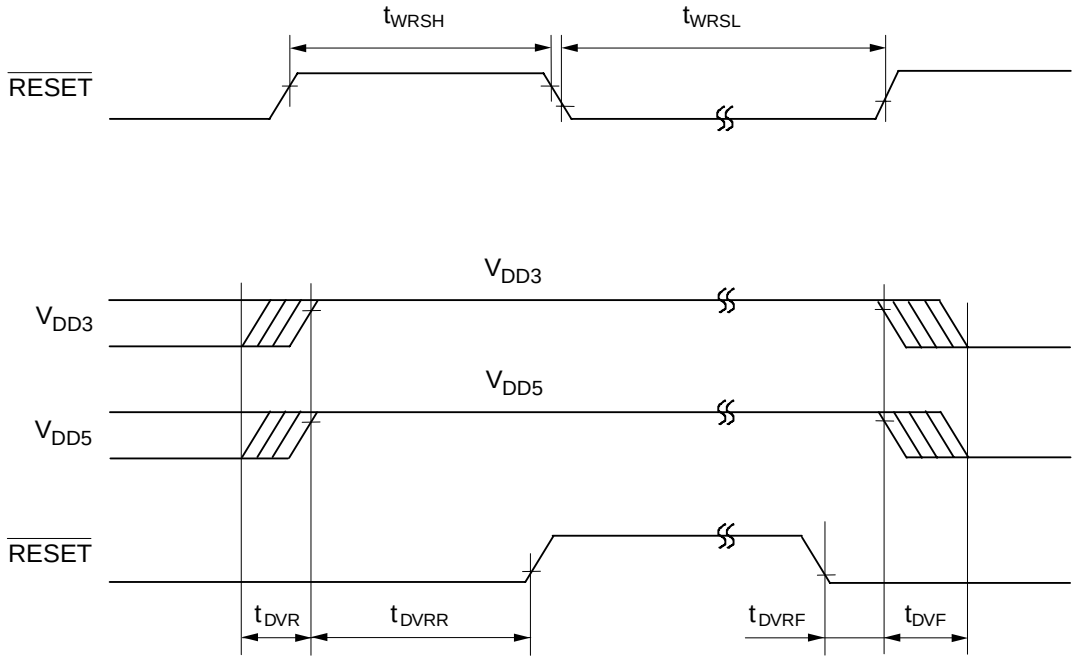
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL0}	STOP or Sub-WATCH Mode release	T_{OST} Note 1		ms
	t_{WRSL1}	except STOP or Sub-WATCH Mode release	500		ns
$V_{DD5x} \leftrightarrow V_{DD3x}$ power up delay	t_{DVR}		0		
$V_{DD5x} \leftrightarrow V_{DD3x}$ power down delay	t_{DVF}		0		
$\overline{\text{RESET}}$ hold time	t_{DVRR}		t_{WRSLn} Note 2		ms
$\overline{\text{RESET}}$ setup time	t_{DVRF}		0		ns

Notes: 1. T_{OST}: Oscillation stabilization time of main oscillator

2. n: 0, 1. Depending on operation condition

Remark: It must be guaranteed that a valid $\overline{\text{RESET}}$ signal (low active) is applied to the Reset pin at any time if the voltage power of V_{DD3x} becomes below 3.0 V

Figure 2-10: $\overline{\text{RESET}}$ Timing



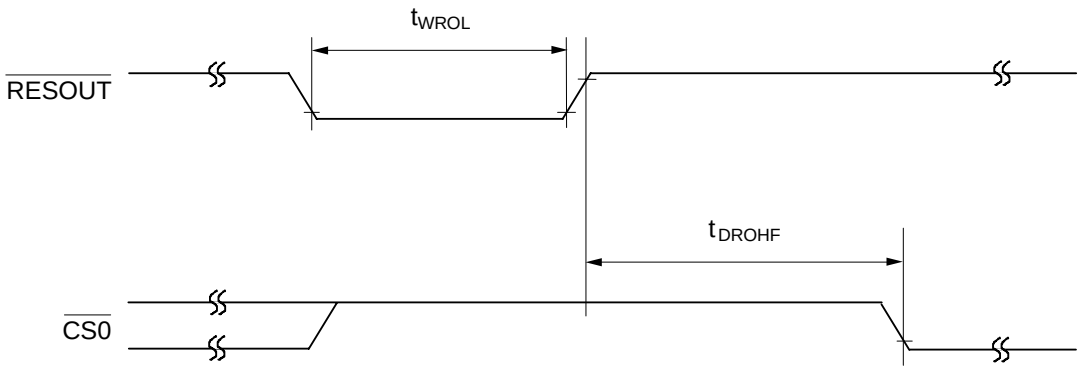
2.5.10 RESET Output

Table 2-20: Reset Output Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESOUT}}$ low-level width	t_{WROL}		4 T[Note]		ms
$\overline{\text{RESOUT}}\uparrow$ to first fetch ($\overline{\text{CS0}}\downarrow$)	t_{DROHF}		5 T[Note]		ms

Note: T: $1/f_{OSC}$, f_{OSC} = Main oscillator frequency

Figure 2-11: Reset Output Timing



2.5.11 Interrupt Timing

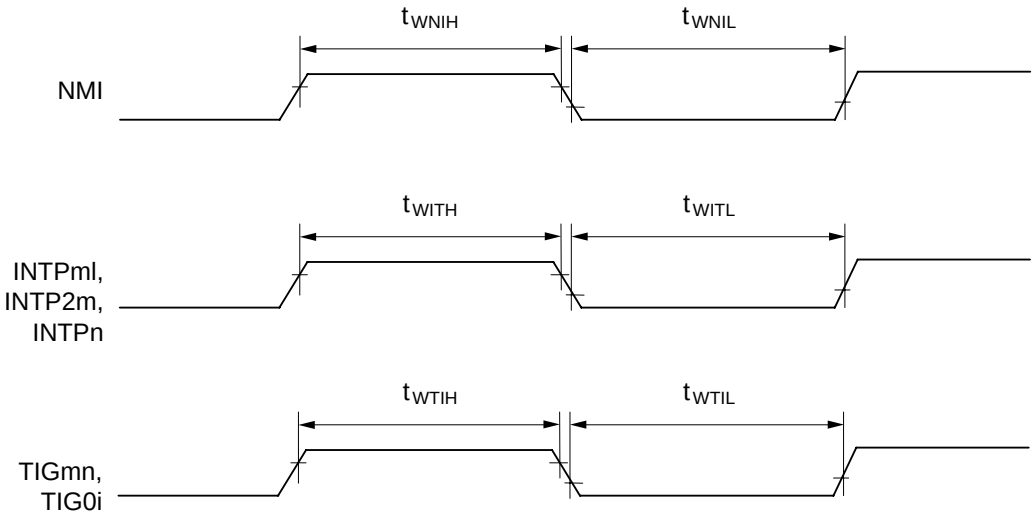
Table 2-21: Interrupt Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}		500		ns
NMI low-level width	t_{WNIL}		500		ns
INTP00, INTP05, INTP10, INTP15, INTP20, INTP21, INTPi**Note1** high-level width	t_{WITH}		500		ns
INTP00, INTP05, INTP10, INTP15, INTP20, INTP21, INTPi**Note 1** low-level width	t_{WITL}		500		ns
TIGmn, TIC0m**Note 2** high-level width	t_{WTIH}		500		ns
TIGmn, TIC0m**Note 2** low-level width	t_{WTIL}		500		ns

Notes: 1. i = 0 to 5

2. m = 0 to 1, n = 0 to 5

Figure 2-12: Interrupt Timing



Remarks: 1. n = 0 to 5

2. m = 0 to 1

3. i = 1 to 2

4. l = 0, 5

2.6 Peripheral Function Characteristics

2.6.1 Timer G/Timer C

Table 2-22: Timer G/Timer C Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
TIGmn high-level width[Note1]	t_{WTIGH}		100 + T_T[Note2]		ns
TIGmn low-level width[Note1]	t_{WTIGL}		100 + T_T[Note2]		ns
TIC0m high-level width[Note3]	t_{WTICH}		100 + T_T[Note2]		ns
TIC0m low-level width[Note3]	t_{WTICL}		100 + T_T[Note2]		ns

Notes: 1. m = 0 to 1, n = 0 to 5

2. T_T: Depends on selected clock source for the peripheral clock supply and the setup of the respective timer macro clock and timer channel setup

3. m = 0 to 1

Figure 2-13: Timer G Characteristics

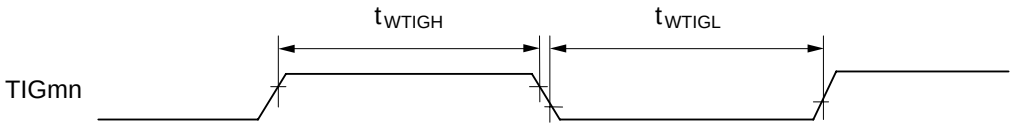
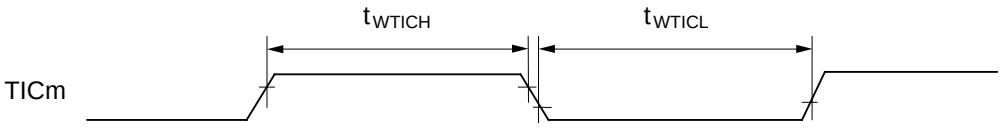


Figure 2-14: Timer C Characteristics



2.6.2 CSI

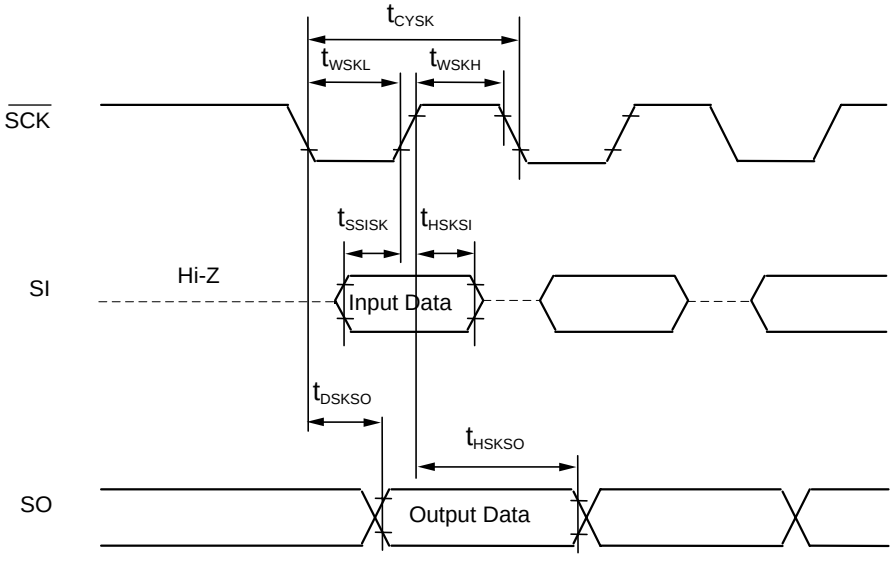
Table 2-23: CSI Master Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSKM}	Output	200		ns
$\overline{SCK}$ high level width	t_{WSKHM}	Output	0.5 t_{CYSK} - 15		ns
$\overline{SCK}$ low level width	t_{WSKLM}	Output	0.5 t_{CYSK} - 15		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISKM}		30		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSIM}		30		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSOM}			30	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSOM}		0.5 t_{CYSK} - 5		ns

Table 2-24: CSI Slave Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{CYSKS}	Input	200		ns
$\overline{SCK}$ high level width	t_{WSKHS}	Input	90		ns
$\overline{SCK}$ low level width	t_{WSKLS}	Input	90		ns
SI set up time (to $\overline{SCK}$ ↑)	t_{SSISKS}		15		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKSIS}		15		ns
SO output delay time (from $\overline{SCK}$ ↓)	t_{DSKSOS}			30	ns
SO output hold time (from $\overline{SCK}$ ↑)	t_{HSKSOS}		t_{WSKH}		ns

Figure 2-15: CSI Slave Mode Characteristics



2.6.3 UART

Table 2-25: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UART}	$f_{Peripheral} \geq 5$ MHz		312500	bps

2.6.4 FCAN

Table 2-26: FCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	$f_{Peripheral} \geq 16$ MHz		1	Mbps

2.6.5 A/D Converter

(T_A= -40 ~ +85°C: μPD703128 (A), μPD703129 (A),
T_A= -40 ~ +110°C: μPD703129 (A1),
$V_{DD5x} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{DD3x} = CV_{DD}$ = 3.0 V ~ 3.6 V, $AV_{REF} \leq AV_{DD}$
$V_{SS5x} = V_{SS3x} = CV_{SS} = AV_{SS}$ = 0 V)

Table 2-27: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall Error[Note1]	-	$AV_{REF} = AV_{DD}$			±3	LSB
		AV_{REF} = 3 V			±5	LSB
Conversion time[Note2]	T_{CONV}		5		12	μs
Sampling time[Note3]	T_{SAM}			T_{CONV}/6		μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog supply current	I_{AVDD}			3.0	6.0	mA.
Reference voltage	AV_{REF}		AV_{SS}		AV_{DD}	V
Reference voltage input current[Note4]	I_{AVREF}	$AV_{REF} = AV_{DD}$		1	2	mA
Reference voltage input leakage[Note5]	I_{LAVREF}	$AV_{REF} = AV_{DD}$			5	μA

Notes: 1. The quantization error is not included

2. The conversion time T_{CONV} depends on the setting of the ADM register

3. The sampling time T_{SAM} depends on the setting of the ADM register

4. The A/D converter reference voltage can be switched off internally by software

5. The leakage current specification becomes valid if the A/D converter's reference voltage is switched off

2.6.6 Serial "External Flash Memory" Programming Operation Characteristics

Table 2-28: Serial "External Flash Memory" Programming Characteristics

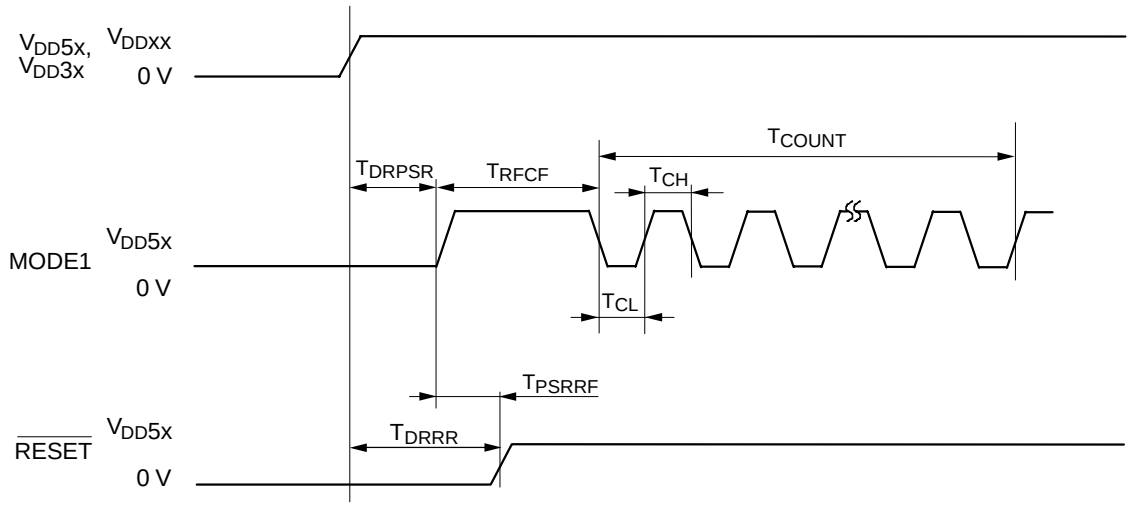
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
V_{DD5x} ↑ setup time to MODE1 ↑	T_{DRPSR}		100			ns
V_{DD5x} ↑ setup time to $\overline{RESET}$ ↑	T_{DRRR}		T_{OST} Note 1			ms
MODE1 ↑ setup time to $\overline{RESET}$ ↑	T_{PSRRF}		T_{OST} Note 1			ms
Count start setup time from $\overline{RESET}$ ↑	T_{RFCF}		5T Note 2 + 500			μs
Times of MODE1 counting	T_{COUNT}				10	ms
MODE1 count Hi/Low level width	T_{CH}, T_{CL}		1			μs
MODE1 pulse count for UART0	N_{PUART0}			0		-
MODE1 pulse count for CSI0	N_{PCSI0}			8		-

Notes: 1. T_{OST}: Oscillation stabilization time of main oscillator
For power up sequence of V_{DD5x}, V_{DD3x} please refer to Section 2.5.9.

2. T: $1/f_{OSC}$, f_{OSC} = Main oscillator frequency

Remark: The MODE1 input pin is a Schmitt-Trigger input buffer

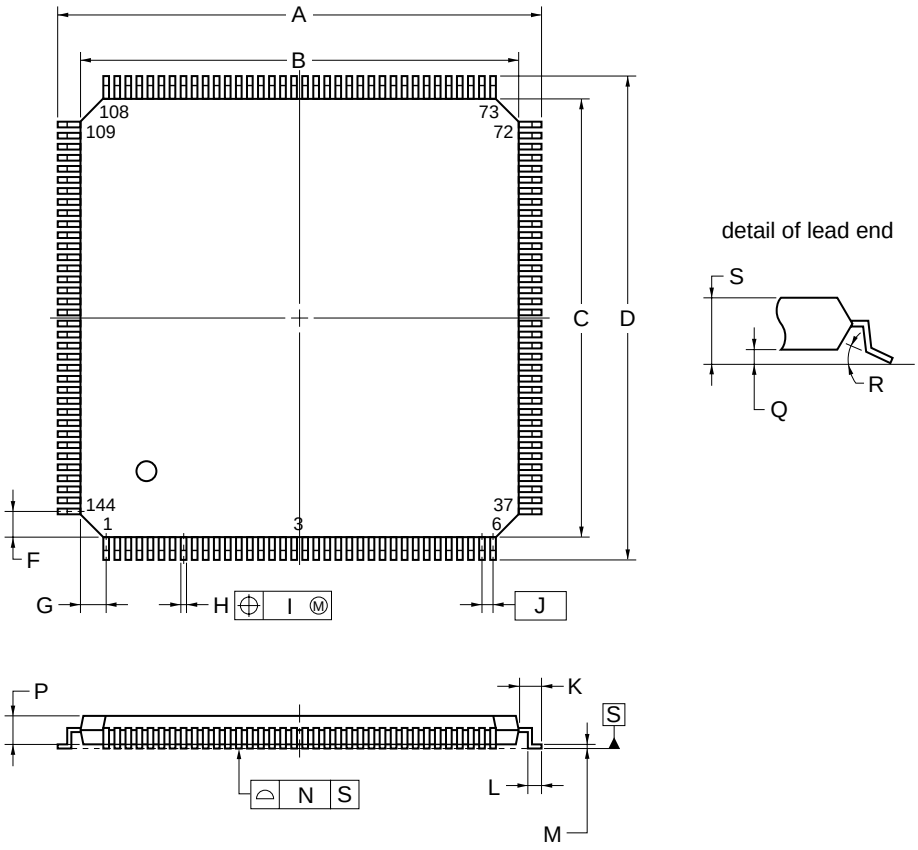
Figure 2-16: Serial "External Flash Memory" Programming Characteristics Timing



3. Package Drawing

Figure 3-1: Package Drawing

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:
Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Table 4-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 245 °C, Time: 30 seconds max. (210 °C min.), Number of times: 2 max., Number of days: 7 **Note**	IR45-207-2
VPS	Package peak temperature: 215 °C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 7**Note**	VP15-207-2
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per side of device)	-

Note: After that, prebaking is necessary at tbd °C for tbd hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 02.10

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- Device availability

  Ordering information

  Product release schedule

  Availability of related technical literature

  Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

  Network requirements

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