NEC

MOS INTEGRATED CIRCUIT

μPD703116, 703116(A), 703116(A1), 70F3116, 70F3116(A), 70F3116(A1)

V850E/IA1™
32-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

★ The μPD703116, 703116(A), 703116(A1), 70F3116, 70F3116(A), and 70F3116(A1) are products of the V850 Series™ of 32-bit single-chip microcontrollers for real-time control applications. These microcontrollers integrate a 32-bit CPU, ROM, RAM, an interrupt controller, timers such as a 3-phase sine wave PWM timer for motor, a serial interface, an FCAN controller, an A/D converter, a DMA controller, and other functions on a single chip.

The μPD70F3116, 70F3116(A), and 70F3116(A1) are products that substitute flash memory for the internal mask ROM of the μPD703116, 703116(A), and 703116(A1). This enables users to perform on-board program writing and erasure, making this product effective for evaluation during system development, small-lot production of multiple devices, and rapid production start.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/IA1 Hardware User's Manual: U14492E
V850E1 Architecture User's Manual: U14559E

FEATURES

- ○ Number of instructions: 83
- ○ Minimum instruction execution time: 20 ns (with a 50 MHz internal clock)
- ○ General-purpose registers: 32 bits × 32 registers
- ○ Instruction set suitable for control applications
- ★ ○ Internal memory
  - Mask ROM: 256 KB (μPD703116)
  - Flash memory: 256 KB (μPD70F3116)
  - RAM: 10 KB
- ○ Memory access control (supporting SRAM and ROM)
- ○ Real-time pulse unit suitable for control applications
  - 16-bit timers for 3-phase sine wave PWM inverter control: 2 ch
  - 16-bit up/down counter/timers for 2-phase encoder input: 2 ch
  - 16-bit general-purpose timer/counters: 2 ch
  - 16-bit general-purpose timer/event counter: 1 ch
  - 16-bit interval timer: 1 ch
- ○ Powerful serial interface (with dedicated on-chip baud rate generator)
  - Asynchronous serial interfaces: 3 ch
  - Clocked serial interfaces: 2 ch
- ○ Automotive LAN (FCAN controller): 1 ch
- ○ NBD (Non Break Debug) function
  - RAM monitor function
  - Event detection function
- ○ 10-bit resolution A/D converter: 8 inputs × 2 circuits
- ○ Sophisticated internal interrupt controller
- ○ DMA controller: 4 ch
- ○ I/O lines: Total 83
- ○ Clock generator
- ○ Power-saving functions
- ○ μPD70F3116, 70F3116(A), 70F3116(A1)
  - Can be replaced with mask ROM-incorporated μPD703116, 703116(A), or 703116(A1) for mass production

Unless otherwise specified, the μPD703116 or 70F3116 is used in this document as the representative product.

Document No. U15299EJ2V0DS00 (2nd edition)
Date Published June 2002 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

⋆ APPLICATIONS

- μPD703116, 70F3116: Consumer equipment (inverter air conditioners, etc.)
  Industrial equipment (motor control, general-purpose inverters, etc.)
- μPD703116(A), 703116(A1), 70F3116(A), 70F3116(A1): Automobile applications (electrical power steering, electric car control, etc.)

⋆ ORDERING INFORMATION

Part No.	Package	Quality Grade
μPD703116GJ-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD70F3116GJ-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD703116GJ(A)-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703116GJ(A1)-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD70F3116GJ(A)-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD70F3116GJ(A1)-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special

Remark xxx: ROM code suffix

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

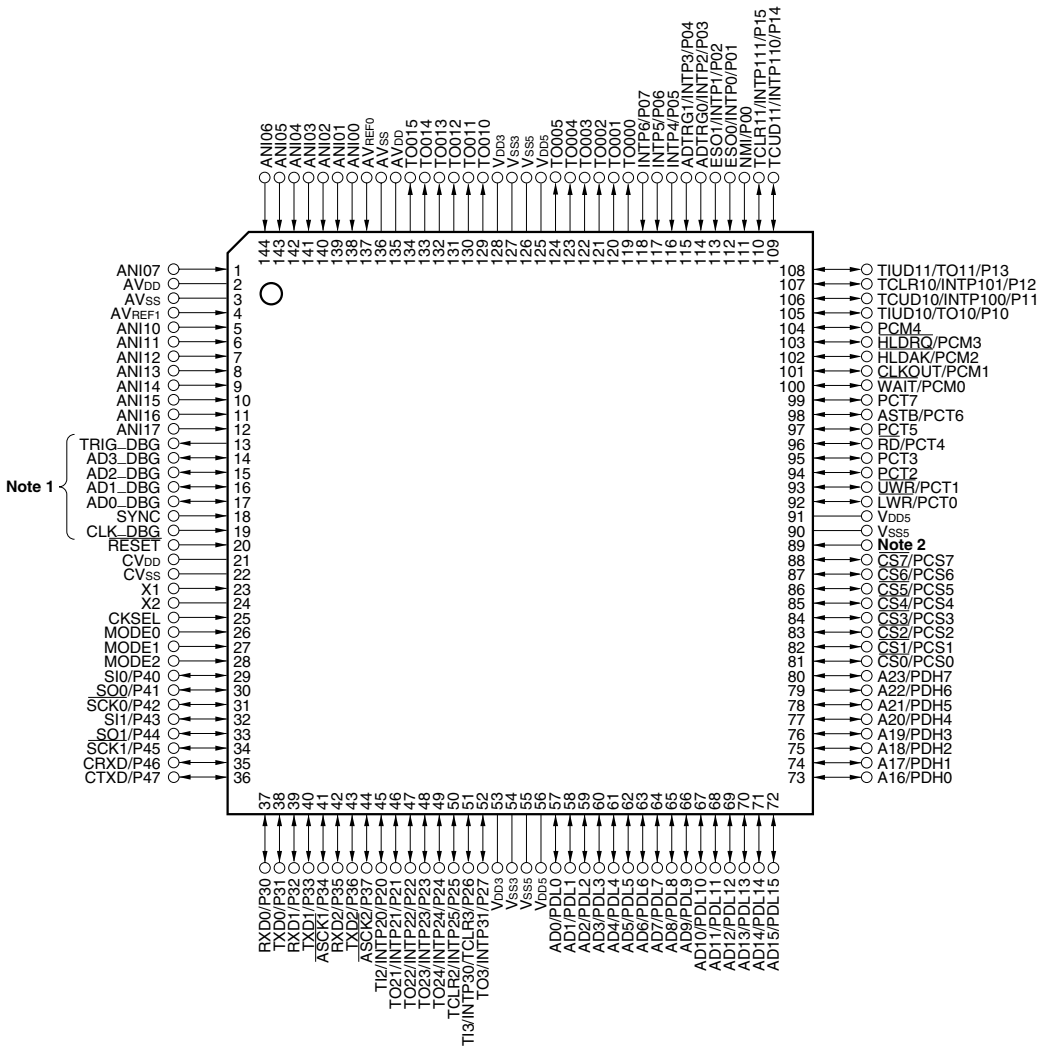
Differences between μPD703116, 703116(A), 703116(A1), 70F3116, 70F3116(A), and 70F3116(A1)

Part No. / Item	μPD703116	μPD703116(A)	μPD703116(A1)	μPD70F3116	μPD70F3116(A)	μPD70F3116(A1)
Quality grade	Standard grade	Special grade		Standard grade	Special grade	
Maximum operating frequency (MHz)	50		32	50		32
Operating ambient temperature (T_A)	−40 to +85°C		−40 to +110°C	−40 to +85°C		−40 to +110°C

PIN CONFIGURATION (TOP VIEW)

★ **• 144-pin plastic LQFP (fine pitch) (20 × 20)**

μPD703116GJ-×××-UEN, 703116GJ(A)-×××-UEN, 703116GJ(A1)-×××-UEN,
μPD70F3116GJ-UEN, 70F3116GJ(A)-UEN, 70F3116GJ(A1)-UEN



Notes 1. Incorporated in μPD70F3116 only.

★ μPD703116 is as follows.

TRIG_DBG: IC1, AD0_DBG to AD3_DBG: IC2, SYNC: IC3, CLK_DBG: IC4

★ **2.** μPD703116: IC5

μPD70F3116: V_{PP}

Cautions 1. When using the μPD70F3116 in normal mode, connect the V_{PP} pin to V_{SS5}.

★ **2. When using the μPD703116, the processing when the IC1 to IC5 pins are unused is as follows.**

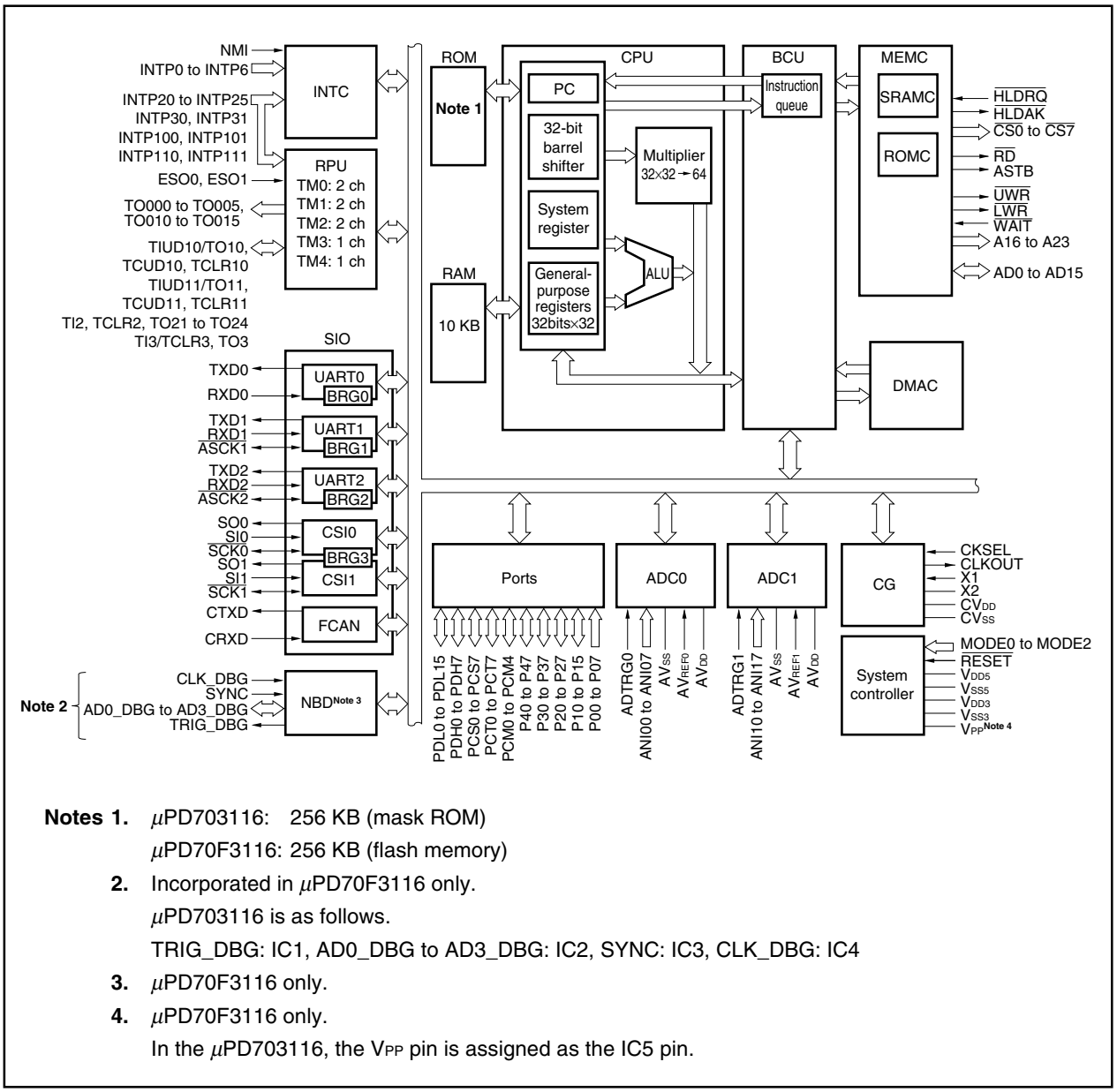
IC1 to IC4 pins: Leave open.

IC5 pin: Independently connect to V_{SS5} via a resistor.

PIN IDENTIFICATION

A16 to A23: Address bus
AD0 to AD15: Address/data bus
AD0_DBG to AD3_DBG: Debug address/data bus
ADTRG0, ADTRG1: A/D trigger input
ANI00 to ANI07, ANI10 to ANI17: Analog input
$\overline{\text{ASCK1}}$, $\overline{\text{ASCK2}}$: Asynchronous serial clock
ASTB: Address strobe
AV_{DD}: Analog power supply
AV_{REF0}, AV_{REF1}: Analog reference voltage
AV_{SS}: Analog ground
CKSEL: Clock generator operating mode select
CLK_DBG: Debug clock
CLKOUT: Clock output
CRXD: Receive data for controller area network
$\overline{\text{CS0}}$ to $\overline{\text{CS7}}$: Chip select
CTXD: Transmit data for controller area network
CV_{DD}: Clock generator power supply
CV_{SS}: Clock generator ground
ESO0, ESO1: Emergency shut off
$\overline{\text{HLDAK}}$: Hold acknowledge
$\overline{\text{HLDRQ}}$: Hold request
IC1 to IC5: Internally connected
INTP0 to INTP6, INTP100, INTP101, INTP110, INTP111, INTP20 to INTP25, INTP30, INTP31: Interrupt request from peripherals
$\overline{\text{LWR}}$: Lower write strobe
MODE0 to MODE2: Mode
NMI: Non-maskable interrupt request
P00 to P07: Port 0
P10 to P15: Port 1
P20 to P27: Port 2
P30 to P37: Port 3
P40 to P47: Port 4
PCM0 to PCM4: Port CM
PCS0 to PCS7: Port CS
PCT0 to PCT7: Port CT
PDH0 to PDH7: Port DH
PDL0 to PDL15: Port DL
$\overline{\text{RD}}$: Read strobe
$\overline{\text{RESET}}$: Reset
RXD0 to RXD2: Receive data
$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$: Serial clock
SI0, SI1: Serial input
SO0, SO1: Serial output
SYNC: Debug synchronization
TCLR10, TCLR11, TCLR2, TCLR3: Timer clear
TCUD10, TCUD11: Timer control pulse input
TI2, TI3: Timer input
TIUD10, TIUD11: Timer count pulse input
TO000 to TO005, TO010 to TO015, TO10, TO11, TO21 to TO24, TO3: Timer output
TRIG_DBG: Debug trigger
TXD0 to TXD2: Transmit data
$\overline{\text{UWR}}$: Upper write strobe
V_{DD3}, V_{DD5}: Power supply
V_{PP}: Programming power supply
V_{SS3}, V_{SS5}: Ground
$\overline{\text{WAIT}}$: Wait
X1, X2: Crystal

INTERNAL BLOCK DIAGRAM



★ **Notes 1.** μPD703116: 256 KB (mask ROM)
μPD70F3116: 256 KB (flash memory)

2. Incorporated in μPD70F3116 only.

★ μPD703116 is as follows.
TRIG_DBG: IC1, AD0_DBG to AD3_DBG: IC2, SYNC: IC3, CLK_DBG: IC4

3. μPD70F3116 only.

4. μPD70F3116 only.

★ In the μPD703116, the V_{PP} pin is assigned as the IC5 pin.

CONTENTS

1. DIFFERENCES BETWEEN PRODUCTS

Item	μPD703116	μPD703116(A)	μPD703116(A1)	μPD70F3116	μPD70F3116(A)	μPD70F3116(A1)
Internal ROM	Mask ROM			Flash memory		
	256 KB					
Internal RAM	10 KB					
NBD (Non Break Debug) function	Not provided (IC1 to IC4)			Provided (TRIG_DBG, AD0_DBG to AD3_DBG, SYNC, CLK_DBG)		
Flash memory programming pin	Not provided (IC5)			Provided (V_{PP})		
Flash memory programming mode	Not provided			Provided (MODE0 = H/L, MODE1 = H, MODE2 = L, V_{PP} = 7.8 V)		
Quality grade	Standard grade	Special grade		Standard grade	Special grade	
Electrical specifications	The maximum operating frequency, operating ambient temperature, and current consumption differ (refer to **3. ELECTRICAL SPECIFICATIONS**).					
Other	The noise immunity and noise radiation differ because the circuit scale and mask layout are different.					

Cautions 1. There are differences in noise immunity and noise radiation between the mask ROM version and flash memory version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

2. When switching from the flash memory version to the mask ROM version, write the same code to the free area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	Input	Port 0 8-bit input-only port	NMI
P01			ESO0/INTP0
P02			ESO1/INTP1
P03			ADTRG0/INTP2
P04			ADTRG1/INTP3
P05			INTP4
P06			INTP5
P07			INTP6
P10	I/O	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	TIUD10/TO10
P11			TCUD10/INTP100
P12			TCLR10/INTP101
P13			TIUD11/TO11
P14			TCUD11/INTP110
P15			TCLR11/INTP111
P20	I/O	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	TI2/INTP20
P21			TO21/INTP21
P22			TO22/INTP22
P23			TO23/INTP23
P24			TO24/INTP24
P25			TCLR2/INTP25
P26			TI3/TCLR3/INTP30
P27			TO3/INTP31
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	RXD0
P31			TXD0
P32			RXD1
P33			TXD1
P34			$\overline{\text{ASCK1}}$
P35			RXD2
P36			TXD2
P37			$\overline{\text{ASCK2}}$

(2/3)

Pin Name	I/O	Function	Alternate Function
P40	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	SI0
P41			SO0
P42			$\overline{SCK0}$
P43			SI1
P44			SO1
P45			$\overline{SCK1}$
P46			CRXD
P47			CTXD
PCM0	I/O	Port CM 5-bit I/O port Input/output can be specified in 1-bit units.	$\overline{WAIT}$
PCM1			CLKOUT
PCM2			$\overline{HLDAK}$
PCM3			$\overline{HLDRQ}$
PCM4			–
PCT0	I/O	Port CT 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{LWR}$
PCT1			$\overline{UWR}$
PCT2			–
PCT3			–
PCT4			$\overline{RD}$
PCT5			–
PCT6			ASTB
PCT7			–
PCS0	I/O	Port CS 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{CS0}$
PCS1			$\overline{CS1}$
PCS2			$\overline{CS2}$
PCS3			$\overline{CS3}$
PCS4			$\overline{CS4}$
PCS5			$\overline{CS5}$
PCS6			$\overline{CS6}$
PCS7			$\overline{CS7}$
PDH0	I/O	Port DH 8-bit I/O port Input/output can be specified in 1-bit units.	A16
PDH1			A17
PDH2			A18
PDH3			A19
PDH4			A20
PDH5			A21
PDH6			A22
PDH7			A23

(3/3)

Pin Name	I/O	Function	Alternate Function
PDL0	I/O	Port DL	AD0
PDL1		8-/16-bit I/O port	AD1
PDL2		Input/output can be specified in 1-bit units.	AD2
PDL3			AD3
PDL4			AD4
PDL5			AD5
PDL6			AD6
PDL7			AD7
PDL8			AD8
PDL9			AD9
PDL10			AD10
PDL11			AD11
PDL12			AD12
PDL13			AD13
PDL14			AD14
PDL15			AD15

2.2 Non-Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO000	Output	Timer 00 pulse signal output	–
TO001			–
TO002			–
TO003			–
TO004			–
TO005			–
TO010	Output	Timer 01 pulse signal output	–
TO011			–
TO012			–
TO013			–
TO014			–
TO015			–
TO10	Output	Timer 10 or 11 pulse signal output	P10/TIUD10
TO11			P13/TIUD11
TO21	Output	Timer 2 pulse signal output	P21/INTP21
TO22			P22/INTP22
TO23			P23/INTP23
TO24			P24/INTP24
TO3	Output	Timer 3 pulse signal output	P27/INTP31
ESO0	Input	Timer 00 or 01 output stop signal input	P01/INTP0
ESO1			P02/INTP1
TIUD10	Input	External count clock input to up/down counter (timer 10 or 11)	P10/TO10
TIUD11			P13/TO11
TCUD10	Input	Count operation switching signal to up/down counter (timer 10 or 11)	P11/INTP100
TCUD11			P14/INTP110
TCLR10	Input	Clear signal input to up/down counter (timer 10 or 11)	P12/INTP101
TCLR11			P15/INTP111
TI2	Input	Timer 2 or 3 external count clock input	P20/INTP20
TI3			P26/INTP30/TCLR3
TCLR2	Input	Timer 2 or 3 clear signal input	P25/INTP25
TCLR3			P26/INTP31/TI3
INTP0	Input	External maskable interrupt request input	P01/ESO0
INTP1			P02/ESO1
INTP2			P03/ADTRG0
INTP3			P04/ADTRG1
INTP4			P05
INTP5			P06
INTP6			P07

(2/3)

Pin Name	I/O	Function	Alternate Function
INTP100	Input	External maskable interrupt request input and timer 10 external capture trigger input	P11/TCUD10
INTP101			P12/TCLR10
INTP110	Input	External maskable interrupt request input and timer 11 external capture trigger input	P14/TCUD11
INTP111			P15/TCLR11
INTP20	Input	External maskable interrupt request input and timer 2 external capture trigger input	P20/TI2
INTP21			P21/TO21
INTP22			P22/TO22
INTP23			P23/TO23
INTP24			P24/TO24
INTP25			P25/TCLR2
INTP30	Input	External maskable interrupt request input and timer 3 external capture trigger input	P26/TI3/TCLR3
INTP31			P27/TO3
SO0	Output	Serial transmit data output (3-wire) of CSI0 and CSI1	P41
SO1			P44
SI0	Input	Serial receive data input (3-wire) of CSI0 and CSI1	P40
SI1			P43
$\overline{SCK0}$	I/O	Serial clock I/O (3-wire) of CSI0 and CSI1	P42
$\overline{SCK1}$			P45
TXD0	Output	Serial transmit data output of UART0 to UART2	P31
TXD1			P33
TXD2			P36
RXD0	Input	Serial receive data input of UART0 to UART2	P30
RXD1			P32
RXD2			P35
$\overline{ASCK1}$	I/O	Serial clock I/O of UART1 and UART2	P34
$\overline{ASCK2}$			P37
CTXD	Output	FCAN serial transmit data output	P47
CRXD	Input	FCAN serial receive data input	P46
ANI00 to ANI07	Input	Analog input to A/D converter	–
ANI10 to ANI17			–
ADTRG0	Input	External trigger input to A/D converter	P03/INTP2
ADTRG1			P04/INTP3
NMI	Input	Non-maskable interrupt request input	P00
MODE0	Input	Specifies V850E/IA1 operation mode	–
MODE1			–
MODE2			–
V_{PP} Note 1	–	Power application for flash memory write	–
★ IC1 to IC5 Note 2	–	Internal connection pins	–

Notes 1. μPD70F3116 only

2. μPD703116 only

(3/3)

Pin Name	I/O	Function	Alternate Function
$\overline{WAIT}$	Input	Control signal input to insert wait in bus cycle	PCM0
$\overline{HLDAK}$	Output	Bus hold acknowledge output	PCM2
$\overline{HLDRQ}$	Input	Bus hold request input	PCM3
$\overline{LWR}$	Output	External data lower byte write strobe signal output	PCT0
$\overline{UWR}$	Output	External data higher byte write strobe signal output	PCT1
$\overline{RD}$	Output	External data bus read strobe signal output	PCT4
ASTB	Output	External data bus address strobe signal output	PCT6
$\overline{CS0}$	Output	Chip select signal output	PCS0
$\overline{CS1}$			PCS1
$\overline{CS2}$			PCS2
$\overline{CS3}$			PCS3
$\overline{CS4}$			PCS4
$\overline{CS5}$			PCS5
$\overline{CS6}$			PCS6
$\overline{CS7}$			PCS7
AD0 to AD15	I/O	16-bit address/data bus for external memory	PDL0 to PDL15
A16 to A23	Output	Higher 8-bit address bus for external memory	PDH0 to PDH7
$\overline{RESET}$	Input	System reset input (3 V interface, 5 V tolerance)	–
X1	Input	Crystal resonator connection pin for system clock oscillation (3 V interface). Input to X1 pin when providing clocks from outside.	–
X2	–		–
CLKOUT	Output	System clock output	PCM1
CKSEL	Input	Input specifying clock generator operation mode	–
AV_{REF0}	Input	Reference voltage input for A/D converter 0	–
AV_{REF1}	Input	Reference voltage input for A/D converter 1	–
AV_{DD}	–	Positive power supply for A/D converter	–
AV_{SS}	–	Ground potential for A/D converter	–
CV_{DD}	–	Positive power supply for dedicated clock generator	–
CV_{SS}	–	Ground potential for dedicated clock generator	–
V_{DD5}	–	Positive power supply for peripheral interface	–
V_{SS5}	–	Ground potential for peripheral interface	–
V_{DD3}	–	3.3 V positive power supply pin for internal CPU	–
V_{SS3}	–	Ground pin for internal CPU	–
CLK_DBG[Note]	Input	Debugging interface clock input (3.3 V interface)	–
SYNC[Note]	Input	Debugging interface command synchronization input (3.3 V interface)	–
AD0_DBG[Note]	I/O	Command interface input for debugging (3.3 V interface)	–
AD1_DBG[Note]			–
AD2_DBG[Note]			–
AD3_DBG[Note]			–
TRIG_DBG[Note]	Output	Address match trigger signal output for debugging (3.3 V interface)	–

Note μPD70F3116 only

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

The I/O circuit configuration of each type is schematically shown in Figure 2-1.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V_{DD5}, V_{SS5}, CV_{DD}, CV_{SS}, or AV_{SS} via a resistor.

Table 2-1. Types of Pin I/O Circuits and Recommended Connection (1/2)

Pin	I/O Circuit Type	Recommended Connection
P00/NMI	2	Connect directly to V_{SS5}.
P01/ESO0/INTP0 P02/ESO1/INTP1		
P03/ADTRG0/INTP2 P04/ADTRG1/INTP3		
P05/INTP4 to P07/INTP6		
P10/TIUD10/TO10	5-AC	Input: Independently connect to V_{DD5} or V_{SS5} via a resistor. Output: Leave open.
P11/TCUD10/INTP100		
P12/TCLR10/INTP101		
P13/TIUD11/TO11		
P14/TCUD11/INTP110		
P15/TCLR11/INTP111		
P20/TI2/INTP20		
P21/TO21/INTP21 to P24/TO24/INTP24		
P25/TCLR2/INTP25		
P26/TI3/TCLR3/INTP30		
P27/TO3/INTP31		
P30/RXD0		
P31/TXD0	5	
P32/RXD1	5-AC	
P33/TXD1	5	
P34/$\overline{\text{ASCK1}}$	5-AC	
P35/RXD2		
P36/TXD2	5	
P37/$\overline{\text{ASCK2}}$	5-AC	
P40/SI0		
P41/SO0	5	
P42/$\overline{\text{SCK0}}$	5-AC	
P43/SI1		
P44/SO1	5	
P45/$\overline{\text{SCK1}}$	5-AC	
P46/CRXD		
P47/CTXD	5	

Table 2-1. Types of Pin I/O Circuits and Recommended Connection (2/2)

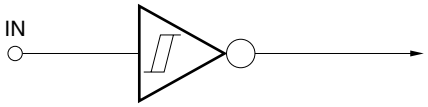
Pin	I/O Circuit Type	Recommended Connection
PCM0/$\overline{\text{WAIT}}$	5	Input: Independently connect to V_{DD5} or V_{SS5} via a resistor. Output: Leave open.
PCM1/CLKOUT		
PCM2/$\overline{\text{HLDAK}}$		
PCM3/$\overline{\text{HLDRQ}}$		
PCM4		
PCT0/$\overline{\text{LWR}}$		
PCT1/$\overline{\text{UWR}}$		
PCT2		
PCT3		
PCT4/$\overline{\text{RD}}$		
PCT5		
PCT6/ASTB		
PCT7		
PCS0/$\overline{\text{CS0}}$		
PCS1/$\overline{\text{CS1}}$		
PCS2/$\overline{\text{CS2}}$		
PCS3/$\overline{\text{CS3}}$		
PCS4/$\overline{\text{CS4}}$		
PCS5/$\overline{\text{CS5}}$		
PCS6/$\overline{\text{CS6}}$		
PCS7/$\overline{\text{CS7}}$		
PDH0/A16 to PDH7/A23		
PDL0/AD0 to PDL15/AD15		
AD0_DBG to AD3_DBG[Note 1]	5-AC	Independently connect to CV_{DD} or CV_{SS} via a resistor.
TRIG_DBG[Note 1]	3	Leave open (low-level output).
CLK_DBG[Note 1]	2	Independently connect to CV_{SS} via a resistor.
SYNC[Note 1]		Independently connect to CV_{DD} via a resistor.
★ IC1 to IC4[Note 2]	–	Leave open.
ANI00 to ANI07, ANI10 to ANI17	7	Connect to AV_{SS}.
TO000 to TO005, TO010 to TO015	4	Leave open.
MODE0 to MODE2	2	–
V_{PP}[Note 1]		Connect to V_{SS5}.
★ IC5[Note 2]		Independently connect to V_{SS5} via a resistor.
$\overline{\text{RESET}}$		–
CKSEL		–
X2	–	Leave open.
AV_{SS}	–	Connect to V_{SS5}.
AV_{REF0}, AV_{REF1}	–	Connect to V_{SS5}.
AV_{DD}	–	Connect to V_{DD5}.

Notes 1. μPD70F3116 only

2. μPD703116 only

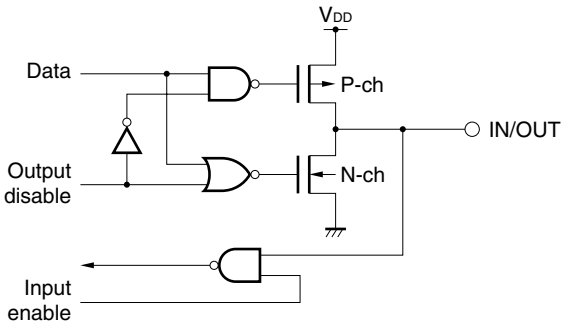
Figure 2-1. Pin I/O Circuits

Type 2

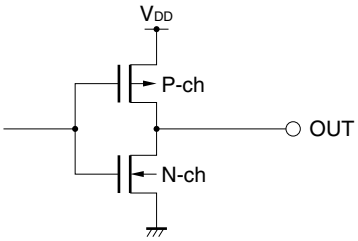


Schmitt-triggered input with hysteresis characteristics

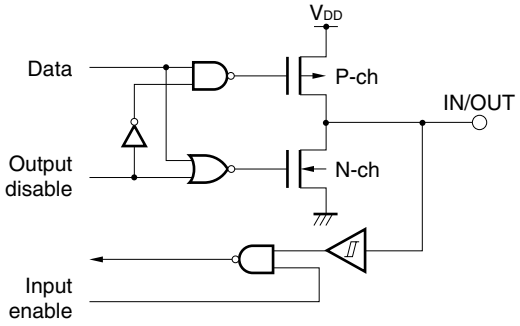
Type 5



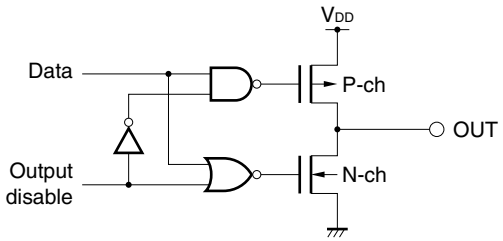
Type 3



Type 5-AC

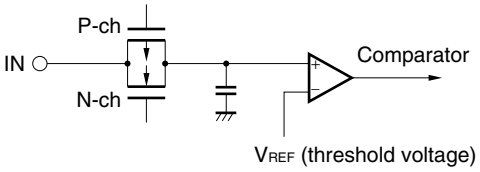


Type 4



Push-pull output with possible high-impedance output (P-ch, N-ch both off)

Type 7



3. ELECTRICAL SPECIFICATIONS

3.1 Normal Operation Mode

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD3}	V_{DD3} pin		−0.5 to +4.6	V
	V_{DD5}	V_{DD5} pin		−0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin		−0.5 to +4.6	V
	CV_{SS}	CV_{SS} pin		−0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		−0.5 to V_{DD5} + 0.5[Note 1]	V
	AV_{SS}	AV_{SS} pin		−0.5 to +0.5	V
Input voltage	V_{I1}	Other than X1 pin and pins for NBD[Note 2]		−0.5 to V_{DD5} + 0.5[Note 1]	V
	V_{I2}	V_{PP} pin, μPD70F3116[Note 3]		−0.5 to +8.5	V
	V_{I3}	Pins for NBD[Note 2]		−0.5 to V_{DD3} + 0.5[Note 1]	V
	V_{I4}	$\overline{\text{RESET}}$ pin (when V_{DD3} is supplied)		−0.5 to +6.0	V
Clock input voltage	V_K	X1 pin		−0.5 to V_{DD3} + 1.0[Note 1]	V
Analog input voltage	V_{IAN}	ANI00 to ANI07 pins, ANI10 to ANI17 pins	$AV_{DD} > V_{DD5}$	−0.5 to V_{DD5} + 0.5[Note 1]	V
			$V_{DD5} \geq AV_{DD}$	−0.5 to AV_{DD} + 0.5[Note 1]	V
Analog reference input voltage	AV_{REF}	AV_{REF0} pin, AV_{REF1} pin	$AV_{DD} > V_{DD5}$	−0.5 to V_{DD5} + 0.5[Note 1]	V
			$V_{DD5} \geq AV_{DD}$	−0.5 to AV_{DD} + 0.5[Note 1]	V
Output current, low	I_{OL}	Per pin for TO000 to TO005 and TO010 to TO015 pins		15	mA
		Per pin other than for TO000 to TO005 and TO010 to TO015 pins		4.0	mA
		Total for all pins		210	mA
Output current, high	I_{OH}	Per pin		−4.0	mA
		Total for all pins		−100	mA
Operating ambient temperature	T_A	μPD703116, 703116(A), μPD70F3116, 70F3116(A)		−40 to +85	°C
		μPD703116(A1), 70F3116(A1)		−40 to +110	°C
Storage temperature	T_{stg}			−65 to +150	°C

★ **Notes 1.** Be sure not to exceed the absolute maximum ratings (MAX. value) of each power supply voltage.

2. CLK_DBG, SYNC, AD0_DBG to AD3_DBG pins (μPD70F3116 only)

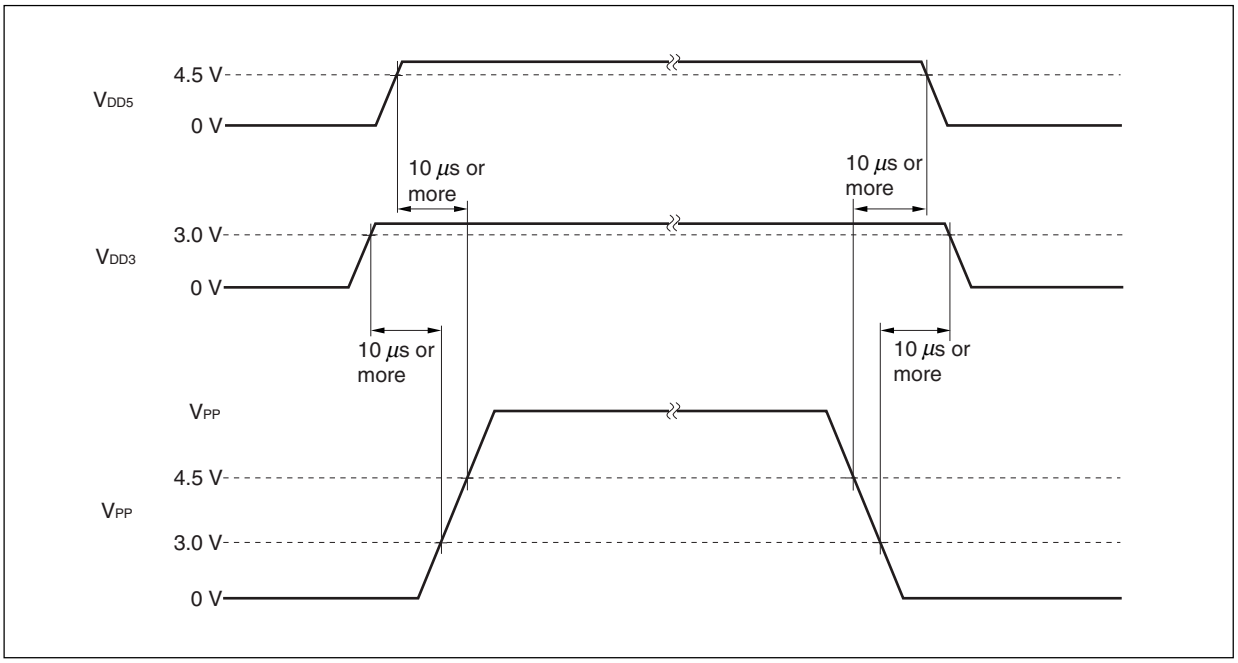
★ **3.** Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- When power supply voltage rises

  V_{PP} must exceed V_{DD3} and V_{DD5} 10 μs or more after V_{DD3} and V_{DD5} have reached the lower-limit value (V_{DD3}: 3.0 V, V_{DD5}: 4.5 V) of the operating voltage range.

- When power supply voltage drops

  V_{DD3} and V_{DD5} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (V_{DD3}: 3.0 V, V_{DD5}: 4.5 V) of the operating voltage range of V_{DD3} and V_{DD5}.



Cautions 1. Do not directly connect output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open drain pins or open collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD3} = V_{DD5} = V_{SS3} = V_{SS5} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF

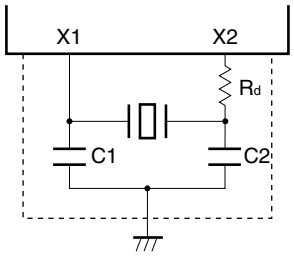
Operating Conditions

Operation Mode	Internal System Clock Frequency (f_{XX})		Operating Ambient Temperature (T_A)	Power Supply Voltage	
				V_{DD3}	V_{DD5}
Direct mode	μPD703116, 703116(A), 70F3116, 70F3116(A)	4 to 25 MHz	−40 to +85°C	3.3 V ±0.3 V	5.0 V ±0.5 V
	μPD703116(A1), 70F3116(A1)	4 to 16 MHz	−40 to +110°C	3.3 V ±0.3 V	5.0 V ±0.5 V
PLL mode	μPD703116, 703116(A), 70F3116, 70F3116(A)	4 to 50 MHz	−40 to +85°C	3.3 V ±0.3 V	5.0 V ±0.5 V
	μPD703116(A1), 70F3116(A1)	4 to 32 MHz	−40 to +110°C	3.3 V ±0.3 V	5.0 V ±0.5 V

Caution When interfacing to the external devices using the CLKOUT signal, make the internal system clock frequency (f_{XX}) 32 MHz or lower.

Clock Oscillator Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1))

(a) Ceramic resonator or crystal resonator connection



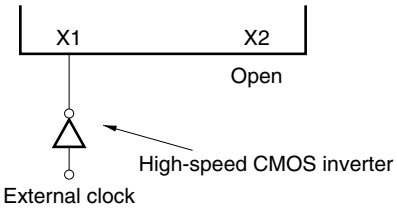
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	Oscillation frequency	f_X		4		6.4	MHz

Remarks 1. Connect the oscillator as close to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken lines.

3. For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

(b) External clock input



Cautions 1. Connect the high-speed CMOS inverter as closely to the X1 pin as possible.

2. Thoroughly evaluate the matching between the V850E/IA1 and the high-speed CMOS inverter.

★ **Recommended Oscillator Constant**

(a) Ceramic resonator

(i) Murata Mfg. Co., Ltd (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1))

Type	Product Name	Oscillation Frequency	Recommended Circuit Constant			Recommended Voltage Range	
		f_X (MHz)	C1 (pF)	C2 (pF)	R_d (Ω)	MIN. (V)	MAX. (V)
Surface mount	CSTCR4M00G55-R0	4.0	On-chip	On-chip	0	3.0	3.6
	CSTCR6M00G55-R0	6.0	On-chip	On-chip	0	3.0	3.6

Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.
If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.
The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850E/IA1 so that the internal operating conditions are within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1), V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins for bus control[Note 1]		2.2		V_{DD5}	V
	V_{IH2}	Pins for NBD[Note 2]		0.8V_{DD3}		V_{DD3}	V
	V_{IH3}	Port pins[Note 3]		0.7V_{DD5}		V_{DD5}	V
	V_{IH4}	Port pins other than **Notes 1, 2, 3**		0.8V_{DD5}		V_{DD5}	V
	V_{IH5}	X1 pin		0.8V_{DD3}		V_{DD3} +0.3	V
	V_{IH6}	$\overline{\text{RESET}}$ pin		0.8V_{DD3}		5.5	V
Input voltage, low	V_{IL1}	Pins for bus control[Note 1]		0		0.8	V
	V_{IL2}	Pins for NBD[Note 2]		0		0.2V_{DD3}	V
	V_{IL3}	Port pins[Note 3]		0		0.3V_{DD5}	V
	V_{IL4}	Port pins other than **Notes 1, 2, 3**		0		0.2V_{DD5}	V
	V_{IL5}	X1 pin		–0.5		0.15V_{DD3}	V
	V_{IL6}	$\overline{\text{RESET}}$ pin		0		0.2V_{DD3}	V
Output voltage, high	V_{OH1}	Pins other than **Note 4**	I_{OH} = –2.5 mA	V_{DD5} –1.0			V
	V_{OH2}	Pins for NBD[Note 4]	I_{OH} = –2.5 mA	V_{DD3} –1.0			V
Output voltage, low	V_{OL1}	PWM output[Note 5]	I_{OL} = 15 mA			2.0	V
			I_{OL} = 2.5 mA			0.4	V
	V_{OL2}	Pins other than **Notes 4, 5**	I_{OL} = 2.5 mA			0.4	V
	V_{OL3}	Pins for NBD[Note 4]	I_{OL} = 2.5 mA			0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD5}				10	μA
Input leakage current, low	I_{LIL}	V_I = 0 V				–10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD5}				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA
Analog pin input leakage current	I_{LIAN}	ANI00 to ANI07, ANI10 to ANI17 pins				±10	μA

Notes 1. AD0/PDL0 to AD15/PDL15, A16/PDH0 to A23/PDH7, $\overline{\text{LWR}}$/PCT0, $\overline{\text{UWR}}$/PCT1, PCT2, PCT3, $\overline{\text{RD}}$/PCT4, PCT5, ASTB/PCT6, PCT7, $\overline{\text{WAIT}}$/PCM0, CLKOUT/PCM1, $\overline{\text{HLDAK}}$/PCM2, $\overline{\text{HLDRQ}}$/PCM3, PCM4, $\overline{\text{CS0}}$/PCS0 to $\overline{\text{CS7}}$/PCS7 pins

2. CLK_DBG, SYNC, AD0_DBG to AD3_DBG pins (μPD70F3116 only)

3. P31/TXD0, P33/TXD1, P36/TXD2, P41/SO0, P44/SO1, P47/CTXD pins

4. AD0_DBG to AD3_DBG, TRIG_DBG pins (μPD70F3116 only)

5. TO000 to TO005, TO010 to TO015 pins

DC Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1), V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V) (2/2)

	Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
★	Power supply current[Note 1]	In normal mode	I_{DD1}	μPD703116	V_{DD3} + CV_{DD}	**Note 2**		1.9f_{XX} + 2.8	2.5f_{XX} + 5.0	mA
★					V_{DD5}	**Note 3**		0.8f_{XX} + 0.8	1.0f_{XX}	mA
★				μPD70F3116	V_{DD3} + CV_{DD}	**Note 2**		2.4f_{XX} + 12	3.6f_{XX} + 18	mA
					V_{DD5}	**Note 3**		30	50	mA
★		In HALT mode	I_{DD2}	μPD703116	V_{DD3} + CV_{DD}	**Note 2**		0.9f_{XX} + 6.8	1.8f_{XX} + 4.0	mA
★					V_{DD5}	**Note 3**		20	40	mA
				μPD70F3116	V_{DD3} + CV_{DD}	**Note 2**		1.2f_{XX}	2.3f_{XX}	mA
					V_{DD5}	**Note 3**		20	40	mA
		In IDLE mode	I_{DD3}	V_{DD3} + CV_{DD}				3.0	10	mA
★				V_{DD5}	**Note 3**			0.5	2.0	mA
★		In STOP mode	I_{DD4}	V_{DD3} + CV_{DD}	–40°C ≤ T_A ≤ +85°C			20	1200	μA
★					–40°C ≤ T_A ≤ +110°C			20	3500	μA
★				V_{DD5}	**Note 3**			10	120	μA

Notes 1. Value in the PLL mode

2. Determine the value by calculating f_{XX} from the operating conditions.

3. The current of the TO000 to TO005 and TO010 to TO015 pins is not included.

Remarks 1. f_{XX}: Internal system clock frequency (MHz)

2. An example of calculating the power supply current is shown below.

- Power supply current (TYP.) of the μPD70F3116 in normal mode when f_{XX} = 32 MHz

  V_{DD3} + CV_{DD}: I_{DD1} = 2.4f_{XX} + 12 = 2.4 × 32 + 12 = 88.8 mA

  V_{DD5}: I_{DD1} = 30 mA

Data Retention Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1))

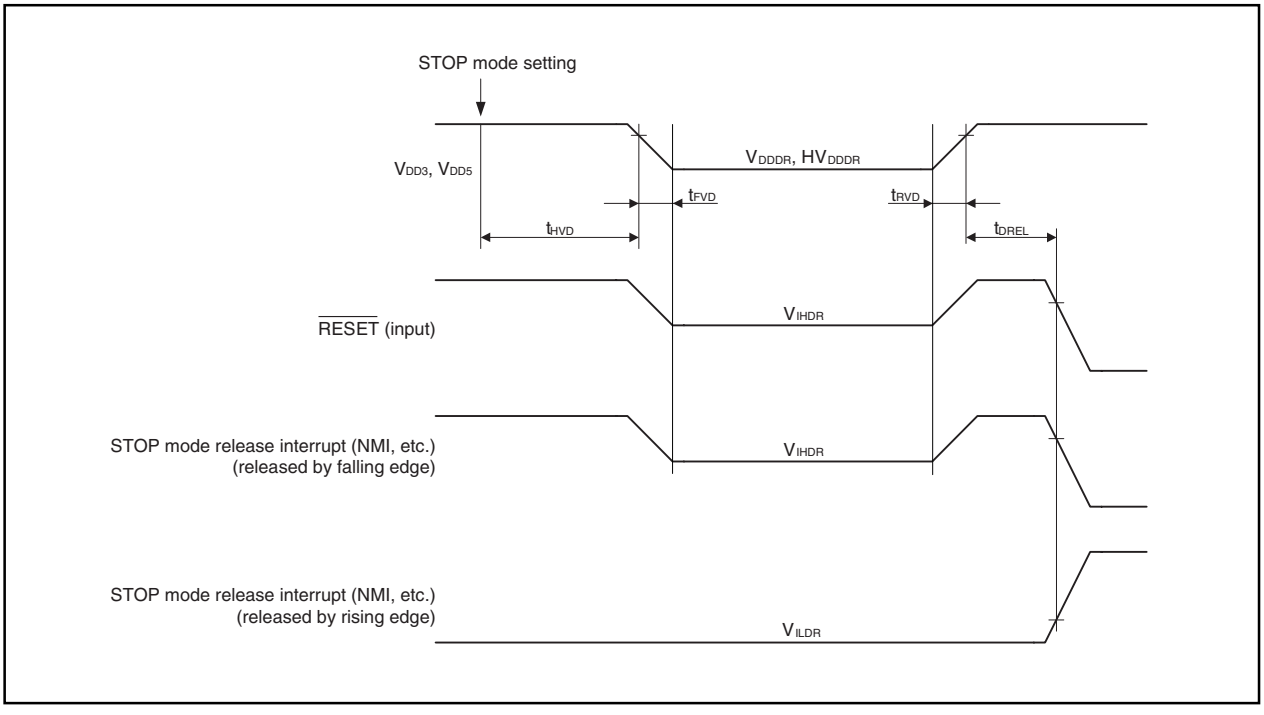
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Data retention voltage	V_{DDDR}	STOP mode, $V_{DD3} = V_{DDDR}$	1.5		3.6	V
		HV_{DDDR}	STOP mode, $V_{DD5} = HV_{DDDR}$	3.6		5.5	V
★	Data retention current	I_{DDDR}	$V_{DD3} = V_{DDDR}$, –40°C ≤ T_A ≤ +85°C		20	1200	μA
★			$V_{DD3} = V_{DDDR}$, –40°C ≤ T_A ≤ +110°C		20	3500	μA
★		HI_{DDDR}	$V_{DD5} = HV_{DDDR}$ **Note 1**		10	120	μA
	Power supply voltage rise time	t_{RVD}		200			μs
	Power supply voltage fall time	t_{FVD}		200			μs
	Power supply voltage retention time (from STOP mode setting)	t_{HVD}		0			ms
	STOP release signal input time	t_{DREL}		0			ns
	Data retention input voltage, high	V_{IHDR}	**Note 2**	0.8HV_{DDDR}		HV_{DDDR}	V
			Note 3	0.8V_{DDDR}		V_{DDDR}	V
	Data retention input voltage, low	V_{ILDR}	**Note 2**	0		0.2HV_{DDDR}	V
			Note 3	0		0.2V_{DDDR}	V

Notes 1. The current of the TO000 to TO005 and TO010 to TO015 pins is not included.

2. P00/NMI, P01/ESO0/INTP0, P02/ESO1/INTP1, P03/ADTRG0/INTP2, P04/ADTRG1/INTP3, P05/INTP4 to P07/INTP6, P10/TIUD10/TO10, P11/TCUD10/INTP100, P12/TCLR10/INTP101, P13/TIUD11/TO11, P14/TCUD11/INTP110, P15/TCLR11/INTP111, P20/TI2/INTP20, P21/TO21/INTP21 to P24/TO24/INTP24, P25/TCLR2/INTP25, P26/TI3/TCLR3/INTP30, P27/TO3/INTP31, P30/RXD0, P32/RXD1, P34/$\overline{\text{ASCK1}}$, P35/RXD2, P37/$\overline{\text{ASCK2}}$, P40/SI0, P42/$\overline{\text{SCK0}}$, P43/SI1, P45/$\overline{\text{SCK1}}$, P46/CRXD, MODE0 to MODE2, CKSEL, $\overline{\text{RESET}}$ pins

3. CLK_DBG, SYNC, AD0_DBG to AD3_DBG pins (μPD70F3116 only)

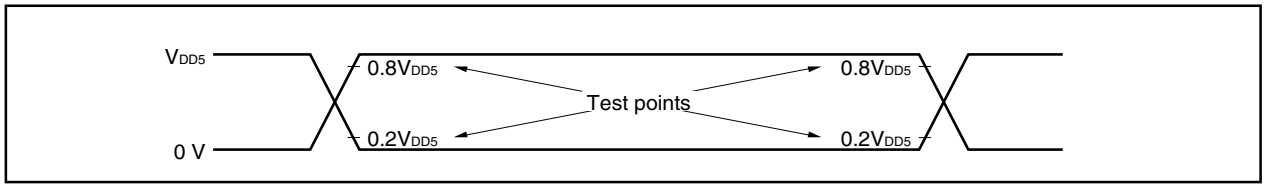
Remark The TYP. value is a reference value for when T_A = 25°C.



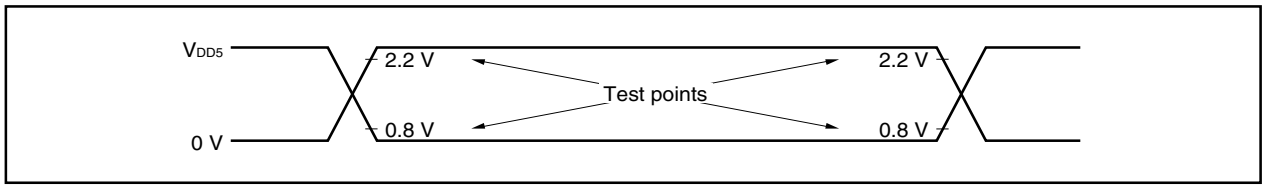
AC Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

AC test input test points

(a) Other than (b) to (d) below

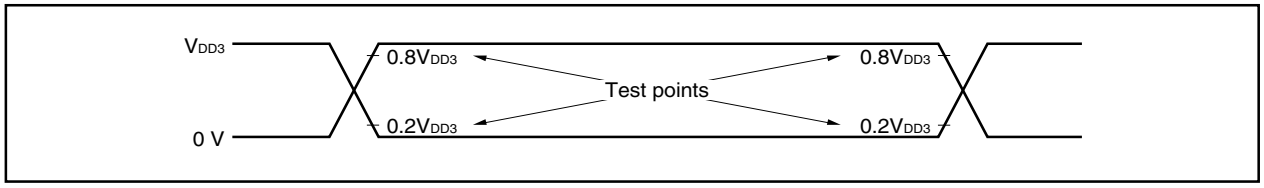


(b) AD0/PDL0 to AD15/PDL15, A16/PDH0 to A23/PDH7, $\overline{\text{LWR}}$/PCT0, $\overline{\text{UWR}}$/PCT1, PCT2, PCT3, RD/PCT4, PCT5, ASTB/PCT6, PCT7, $\overline{\text{WAIT}}$/PCM0, CLKOUT/PCM1, $\overline{\text{HLDAK}}$/PCM2, $\overline{\text{HLDRQ}}$/PCM3, PCM4, $\overline{\text{CS0}}$/PCS0 to CS7/PCS7 pins

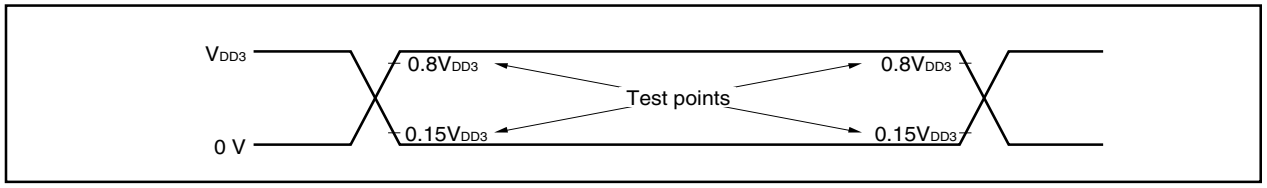


(c) CLK_DBG[Note], SYNC[Note], AD0_DBG to AD3_DBG[Note], $\overline{\text{RESET}}$ pins

Note μPD70F3116 only

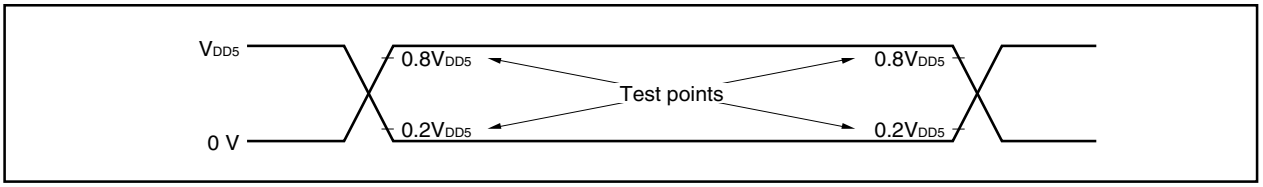


(d) X1 pin

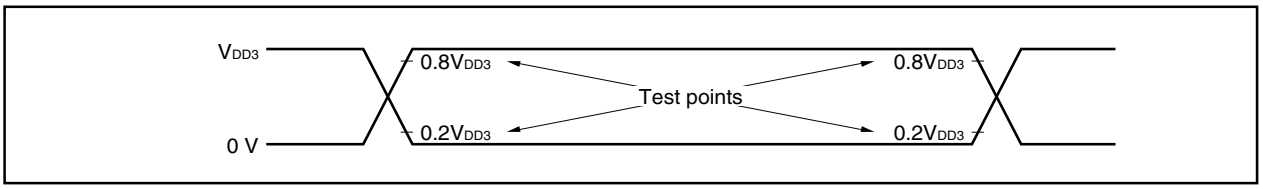


AC test output test points

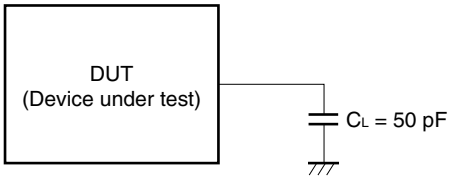
(a) Pins other than (b) below



(b) AD0_DBG to AD3_DBG, TRIG_DBG pins (μPD70F3116 only)



Load conditions



Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to 50 pF or lower.

(1) Clock timing (1/2)

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions		MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	**Note 1**	31.25	125	ns
			PLL mode		156	250	ns
			Direct mode	**Note 2**	20	125	ns
			PLL mode		156	250	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode		6		ns
			PLL mode		50		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode		6		ns
			PLL mode		50		ns
X1 input rise time	<4>	t_{XR}	Direct mode			4	ns
			PLL mode			10	ns
X1 input fall time	<5>	t_{XF}	Direct mode			4	ns
			PLL mode			10	ns
CPU operation frequency	–	f_{XX}	**Note 2**		4	50	MHz
			Note 1		4	32	MHz
			CLKOUT signal used[Note 3]		4	32	MHz
CLKOUT output cycle	<6>	t_{CYK}	**Note 2**		20	250	ns
			Note 1		31.25	250	ns
			CLKOUT signal used[Note 3]		31.25	250	ns
CLKOUT high-level width	<7>	t_{WKH}			0.5T – 9		ns
CLKOUT low-level width	<8>	t_{WKL}			0.5T – 11		ns
CLKOUT rise time	<9>	t_{KR}				11	ns
CLKOUT fall time	<10>	t_{KF}				9	ns
Delay time from X1↓ to CLKOUT	<11>	t_{DXK}	Direct mode			40	ns

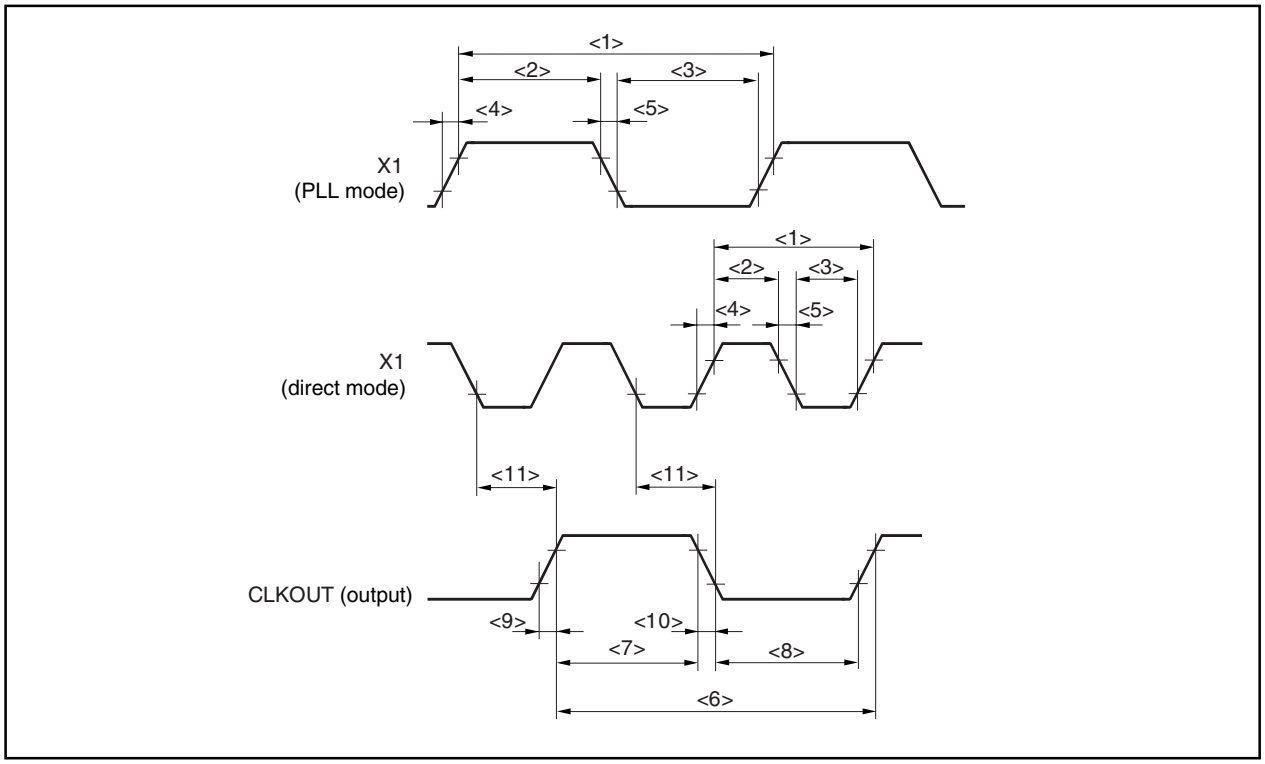
Notes 1. –40°C ≤ T_A ≤ +110°C

2. –40°C ≤ T_A ≤ +85°C

3. When interfacing to the external devices using the CLKOUT signal, make the internal system clock frequency (f_{XX}) 32 MHz or lower.

Remark T = t_{CYK}

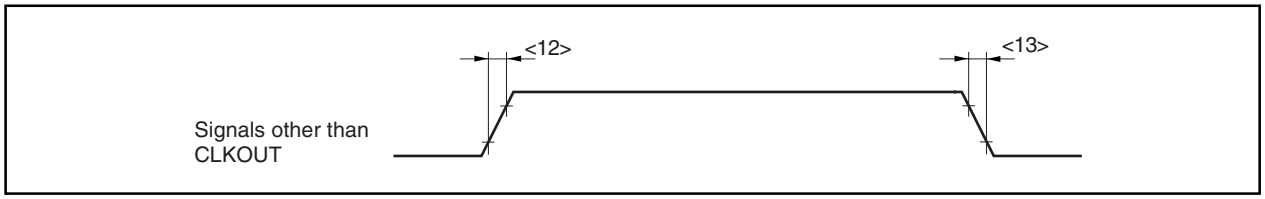
(1) Clock timing (2/2)



(2) Output waveform (except for CLKOUT)

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<12>	t_{OR}			15	ns
Output fall time	<13>	t_{OF}			15	ns



(3) Reset timing

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),

T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),

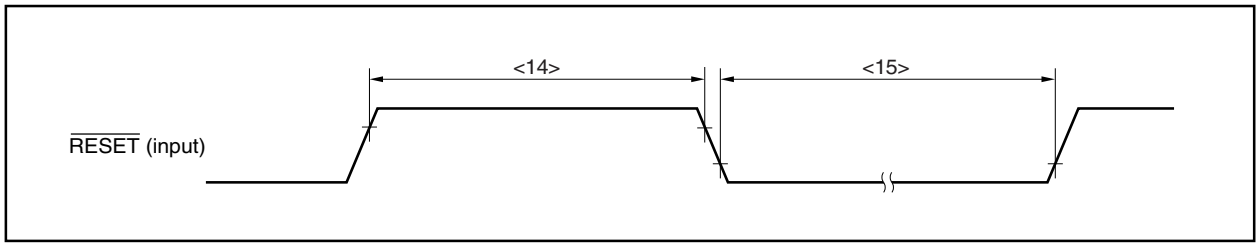
$V_{DD3} = CV_{DD}$ = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, $V_{SS3} = V_{SS5} = CV_{SS}$ = 0 V,

output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ pin high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ pin low-level width	<15>	t_{WRSL}	At power-on and at STOP mode release	500 + T_{OS}		ns
			Other than at power-on and at STOP mode release	500		ns

Caution Thoroughly evaluate the oscillation stabilization time.

Remark T_{OS}: Oscillation stabilization time



(4) Multiplex bus timing

(a) CLKOUT asynchronous (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1), $V_{DD3} = CV_{DD}$ = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, $V_{SS3} = V_{SS5} = CV_{SS}$ = 0 V, output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<16>	t_{SAST}		$(0.5 + w_{AS})T - 16$		ns
Address hold time (from ASTB↓)	<17>	t_{HSTA}		$(0.5 + w_{AH})T - 15$		ns
Address float delay time from $\overline{RD}$↓	<18>	t_{FRDA}			11	ns
Data input setup time from address	<19>	t_{SAID}			$(2 + w + w_{AS} + w_{AH})T - 40$	ns
Data input setup time from $\overline{RD}$ ↓	<20>	t_{SRDID}			$(1 + w)T - 40$	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$↓	<21>	$t_{DSTRDWR}$		$(0.5 + w_{AH})T - 15$		ns
Data input hold time (from $\overline{RD}$↑)	<22>	t_{HRDID}		0		ns
Address output time from $\overline{RD}$↑	<23>	t_{DRDA}		$(1 + i)T - 15$		ns
Delay time from $\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$ ↑ to ASTB↑	<24>	$t_{DRDWRST}$		$0.5T - 15$		ns
Delay time from $\overline{RD}$↑ to ASTB↓	<25>	t_{DRDST}		$(1.5 + i + w_{AS})T - 15$		ns
$\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$ low-level width	<26>	t_{WRDWRL}		$(1 + w)T - 22$		ns
ASTB high-level width	<27>	t_{WSTH}		$(1 + w_{AS})T - 15$		ns
Data output time from $\overline{LWR}$, $\overline{UWR}$↓	<28>	t_{DWROD}			10	ns
Data output setup time (to $\overline{LWR}$, $\overline{UWR}$↑)	<29>	t_{SODWR}		$(1 + w)T - 25$		ns
Data output hold time (from $\overline{LWR}$, $\overline{UWR}$↑)	<30>	t_{HWROD}		$T - 20$		ns
$\overline{WAIT}$ setup time (to address)	<31>	t_{SAWT1}	$w \geq 1$		$(1.5 + w_{AS} + w_{AH})T - 40$	ns
	<32>	t_{SAWT2}			$(1.5 + w + w_{AS} + w_{AH})T - 40$	ns
$\overline{WAIT}$ hold time (from address)	<33>	t_{HAWT1}	$w \geq 1$	$(0.5 + w + w_{AS} + w_{AH})T$		ns
	<34>	t_{HAWT2}		$(1.5 + w + w_{AS} + w_{AH})T$		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<35>	t_{SSTWT1}	$w \geq 1$		$(1 + w_{AH})T - 32$	ns
	<36>	t_{SSTWT2}			$(1 + w + w_{AH})T - 32$	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<37>	t_{HSTWT1}	$w \geq 1$	$(w + w_{AH})T$		ns
	<38>	t_{HSTWT2}		$(1 + w + w_{AH})T$		ns
$\overline{HLDRQ}$ high-level width	<39>	t_{WHQH}		$T + 10$		ns
$\overline{HLDAK}$ low-level width	<40>	t_{WHAL}		$T - 15$		ns
Delay time from address float to $\overline{HLDAK}$↓	<41>	t_{DFHA}		–12		ns
Delay time from $\overline{HLDAK}$↑ to bus output↑	<42>	t_{DHAC}		–7		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<43>	t_{DHQHA1}		2T		ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<44>	t_{DHQHA2}		0.5T	1.5T + 30	ns

Remarks 1. $T = t_{CYK}$

2. w: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle states inserted after the read cycle (0 or 1)

4. w_{AS}: Number of address setup wait states (0 or 1)

5. w_{AH}: Number of address hold wait states (0 or 1)

6. Observe at least either of the data input hold time t_{HKID} or t_{HRDID}.

(b) CLKOUT synchronous (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1), $V_{DD3} = CV_{DD} = 3.0$ to 3.6 V, $V_{DD5} = 5$ V ±0.5 V, $V_{SS3} = V_{SS5} = CV_{SS} = 0$ V, output pin load capacitance: C_L = 50 pF)

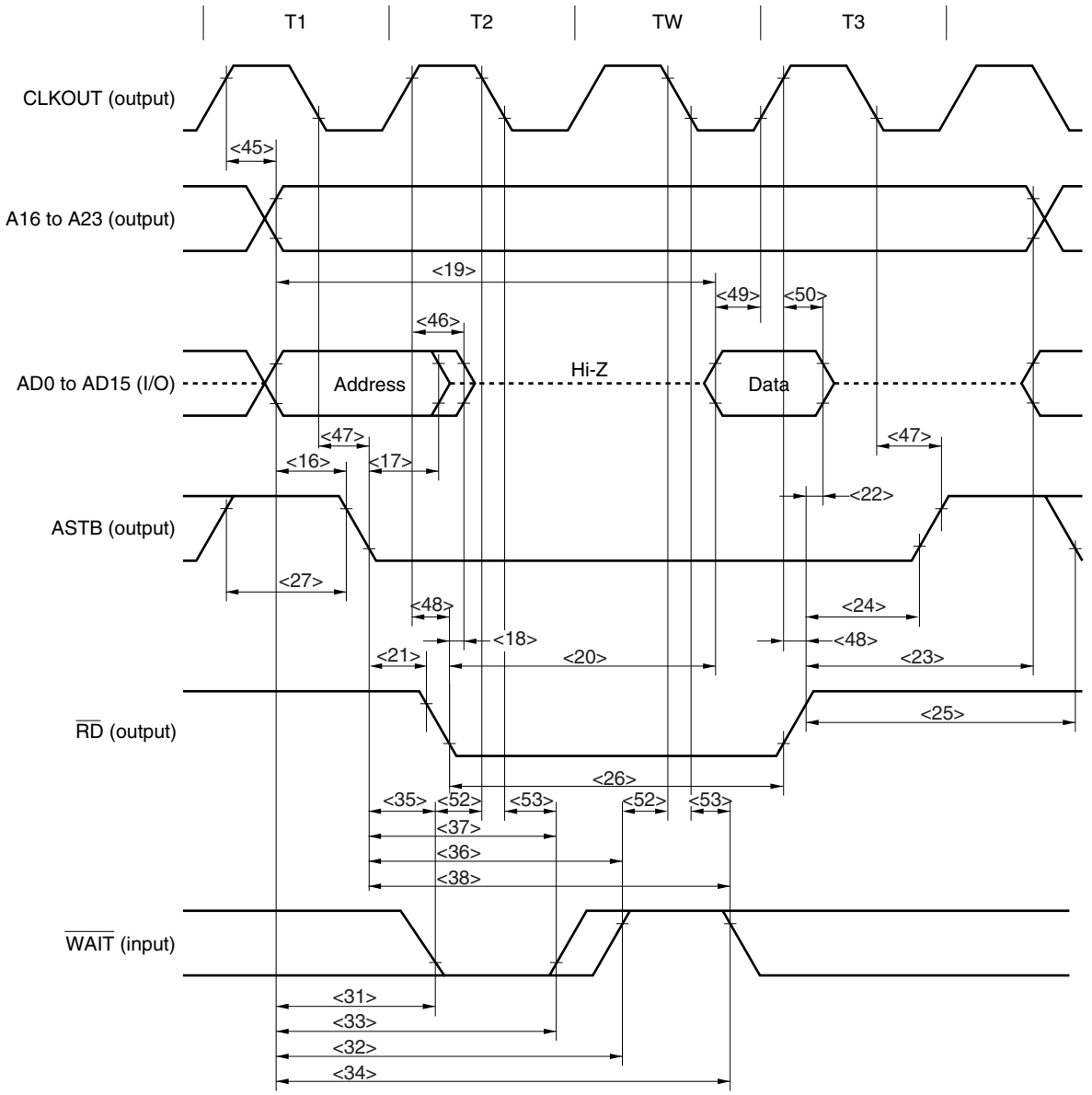
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<45>	t_{DKA}		–7	19	ns
Delay time from CLKOUT↑ to address float	<46>	t_{FKA}		–12	15	ns
Delay time from CLKOUT↓ to ASTB	<47>	t_{DKST}		–3 + w_{AH}T	19 + w_{AH}T	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$	<48>	t_{DKRDWR}		–5	19	ns
Data input setup time (to CLKOUT↑)	<49>	t_{SIDK}		21		ns
Data input hold time (from CLKOUT↑)	<50>	t_{HKID}		5		ns
Delay time from CLKOUT↑ to data output	<51>	t_{DKOD}			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<52>	t_{SWTK}		21		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<53>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<54>	t_{SHQK}		21		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<55>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<56>	t_{DKHA}			19	ns
Delay time from CLKOUT↑ to address float	<57>	t_{DKF}			19	ns

Remarks 1. T = t_{CYK}

2. w_{AH}: Number of address hold wait states (0 or 1)

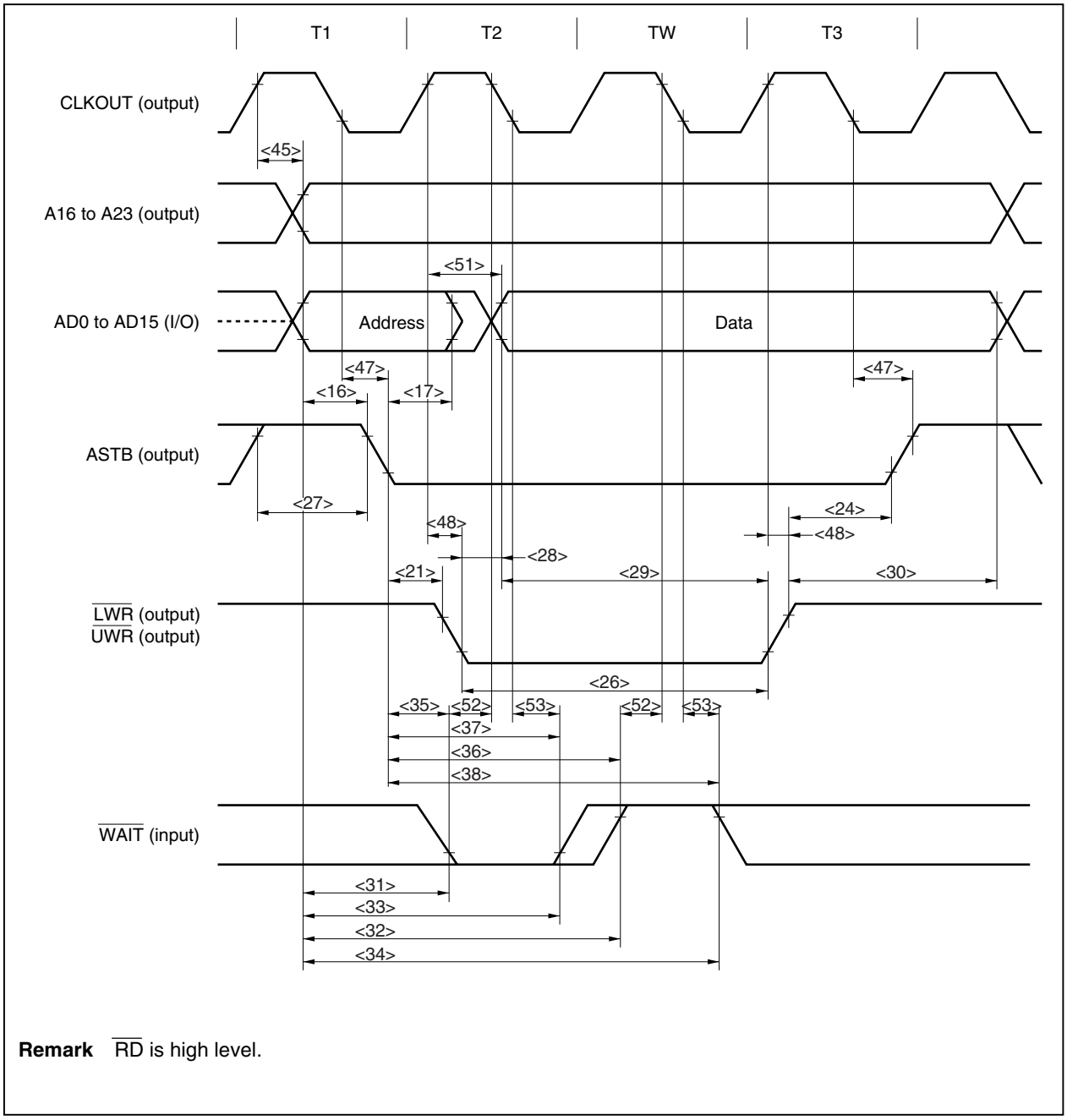
3. Observe at least either of the data input hold time t_{HKID} or t_{HRDID}.

(c) Read cycle (CLKOUT synchronous/asynchronous, 1 wait)



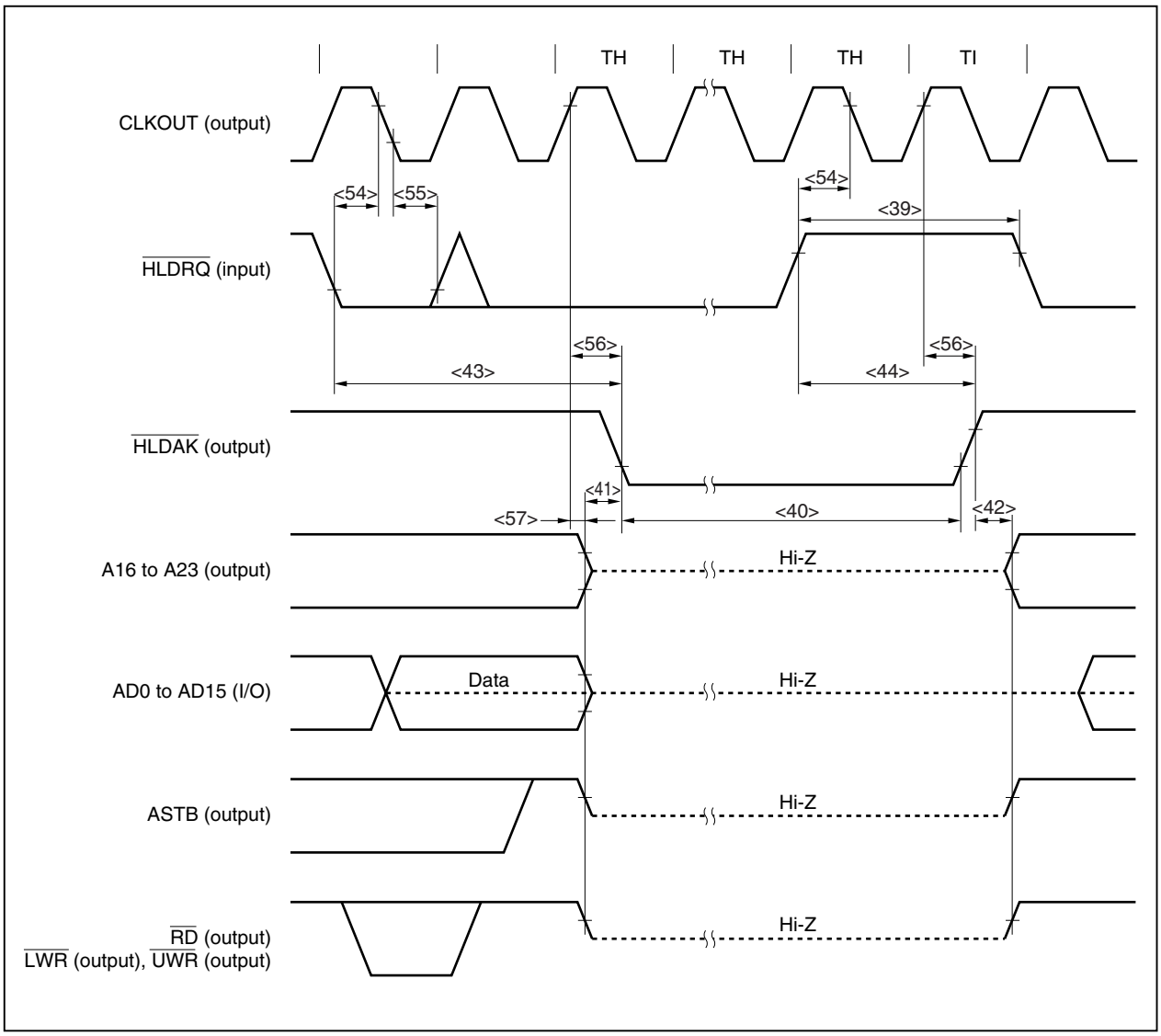
Remark $\overline{\text{LWR}}$ and $\overline{\text{UWR}}$ are high level.

(d) Write cycle (CLKOUT synchronous/asynchronous, 1 wait)



Remark $\overline{RD}$ is high level.

(e) Bus hold


TH
TH
TH
TI
CLKOUT (output)
<54>
<55>
<54>
<39>
HLDRQ (input)
<56>
<56>
<43>
<44>
HLDAK (output)
<41>
<57>
<40>
<42>
A16 to A23 (output)
Hi-Z
AD0 to AD15 (I/O)
Data
Hi-Z
ASTB (output)
Hi-Z
RD (output)
LWR (output), UWR (output)
Hi-Z

(5) Interrupt timing

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),

T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),

$V_{DD3} = CV_{DD}$ = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, $V_{SS3} = V_{SS5} = CV_{SS}$ = 0 V,

output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<58>	t_{WNIH}		500		ns
NMI low-level width	<59>	t_{WNIL}		500		ns
INTPn high-level width	<60>	t_{WITH}	n = 0 to 6	500		ns
			n = 100, 101, 110, 111, 30, 31	5T + 10		ns
			n = 20 to 25 (when analog filter specified)	500		ns
			n = 20 to 25 (when digital filter specified)	5T + 10		ns
INTPn low-level width	<61>	t_{WITL}	n = 0 to 6	500		ns
			n = 100, 101, 110, 111, 30, 31	5T + 10		ns
			n = 20 to 25 (when analog filter specified)	500		ns
			n = 20 to 25 (when digital filter specified)	5T + 10		ns

Remark T: Digital filter sampling clock

T can be selected by setting the following registers.

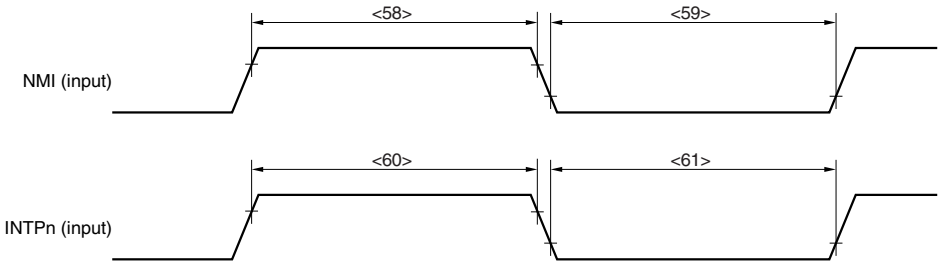
- INTP100, INTP101:

  Can be selected from f_{XXTM10}, $f_{XXTM10}/2$, $f_{XXTM10}/4$, and $f_{XXTM10}/8$ by setting the NRC101 and NRC100 bits of the timer 10 noise elimination time select register (NRC10) (f_{XXTM10}: clock selected with the timer 1/timer 2 clock select register (PRM02)).
- INTP110, INTP111:

  Can be selected from f_{XXTM11}, $f_{XXTM11}/2$, $f_{XXTM11}/4$, and $f_{XXTM11}/8$ by setting the NRC111 and NRC110 bits of the timer 11 noise elimination time select register (NRC11) (f_{XXTM11}: clock selected with the PRM02 register).
- INTP30:

  Can be selected from $f_{XXTM3}/2$, $f_{XXTM3}/4$, $f_{XXTM3}/8$, and $f_{XXTM3}/16$ by setting the NRC31 and NRC30 bits of the timer 3 noise elimination time select register (NRC3) (f_{XXTM3}: clock selected with the timer 3 clock select register (PRM03)).
- INTP31:

  Can be selected from $f_{XXTM3}/32$, $f_{XXTM3}/64$, $f_{XXTM3}/128$, and $f_{XXTM3}/256$ by setting the NRC33 and NRC32 bits of the timer 3 noise elimination time select register (NRC3) (f_{XXTM3}: clock selected with the PRM03 register).



Remark n = 0 to 6, 100, 101, 110, 111, 20 to 25, 30, 31

(6) Timer input timing

(T_A = −40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),

T_A = −40 to +110°C: μPD703116(A1), μPD70F3116(A1),

$V_{DD3} = CV_{DD} = 3.0$ to 3.6 V, $V_{DD5} = 5$ V ±0.5 V, $V_{SS3} = V_{SS5} = CV_{SS} = 0$ V,

output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIUDn, TCUDn high-/low-level width	<62>	t_{WUDH}, t_{WUDL}	n = 10, 11	5T + 10		ns
TIUDn, TCUDn input time difference	<63>	t_{PHUD}	n = 10, 11	2T + 10		ns
TCLRn high-/low-level width	<64>	t_{WTCH}, t_{WTCL}	n = 10, 11, 2 (other than for through input), 3	5T + 10		ns
			n = 2 (for through input[Note])	2T + 10		ns
TIn high-/low-level width	<65>	t_{WTIH}, t_{WTIL}	n = 2 (other than for through input), 3	5T + 10		ns
			n = 2 (for through input[Note])	2T + 10		ns

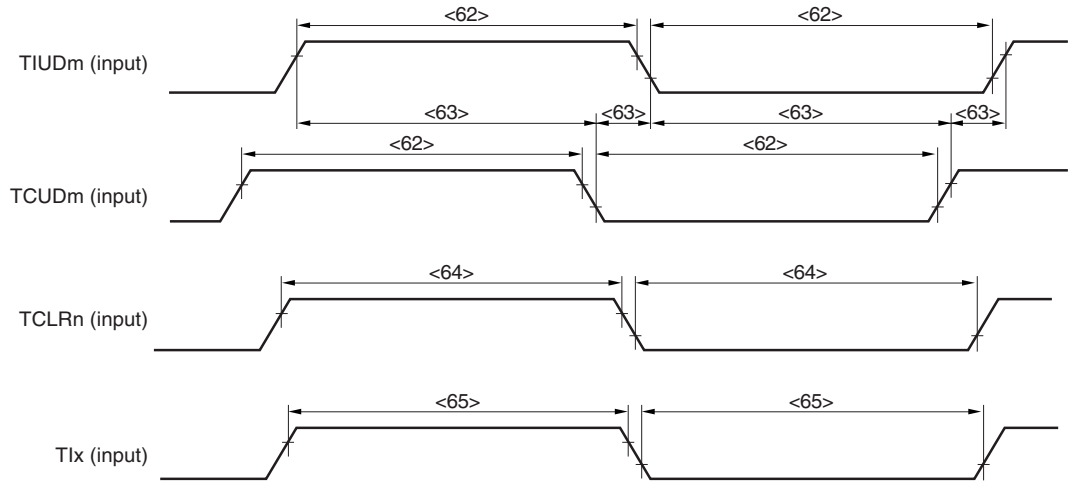
Note When setting the timer 2 count clock/control edge select register 0 (CSE0)'s CESE1 bit to 1 and CESE0 bit to 0.

Remarks 1. T: Digital filter sampling clock

T can be selected by setting the following registers.

- When using TIUDn, TCUDn, and TCLRn (n = 10, 11), the following cycles can be selected by setting the NRCn1 and NRCn0 bits of timer n noise elimination time select register (NRCn).
  - When $f_{XX}/2$ is selected for the timer n basic clock: $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$
  - When $f_{XX}/4$ is selected for the timer n basic clock: $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$
- When using TCLR2 and TI2, the following cycles can be selected by setting the PRM2 bit of the timer 1/timer 2 clock select register (PRM02).
  - When $f_{XX}/2$ is selected for the timer 2 basic clock: $f_{XX}/2$
  - When $f_{XX}/4$ is selected for the timer 2 basic clock: $f_{XX}/4$
- When using TCLR3 and TI3, the following cycles can be selected by setting the NRC31 and NRC30 bits of timer 3 noise elimination time select register (NRC3).
  - When f_{XX} is selected for the timer 3 basic clock: $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$
  - When $f_{XX}/2$ is selected for the timer 3 basic clock: $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$

2. f_{XX}: Internal system clock frequency



Remark m = 10, 11 n = 10, 11, 2, 3 x = 2, 3

(7) Timer operating frequency

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Timer 00, 01 operating frequency	T_0	–40°C ≤ T_A ≤ +85°C		40	MHz
		–40°C ≤ T_A ≤ +110°C		32	MHz
Timer 10, 11 operating frequency	T_1			16	MHz
Timer 20, 21 operating frequency	T_2			16	MHz
Timer 3 operating frequency	T_3			32	MHz

(8) CSI timing (1/2)

(a) Master mode

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<66>	t_{CYSK1}	Output	200		ns
$\overline{SCKn}$ high-level width	<67>	t_{WSK1H}	Output	$0.5t_{CYSK1}$ – 25		ns
$\overline{SCKn}$ low-level width	<68>	t_{WSK1L}	Output	$0.5t_{CYSK1}$ – 25		ns
SIn setup time (to $\overline{SCKn}$↑)	<69>	t_{SSISK}		35		ns
SIn hold time (from $\overline{SCKn}$↑)	<70>	t_{HSKSI}		30		ns
SOn output delay time (from $\overline{SCKn}$↓)	<71>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{SCKn}$↑)	<72>	t_{HSKSO}		$0.5t_{CYSK1}$ – 20		ns

Remark n = 0, 1

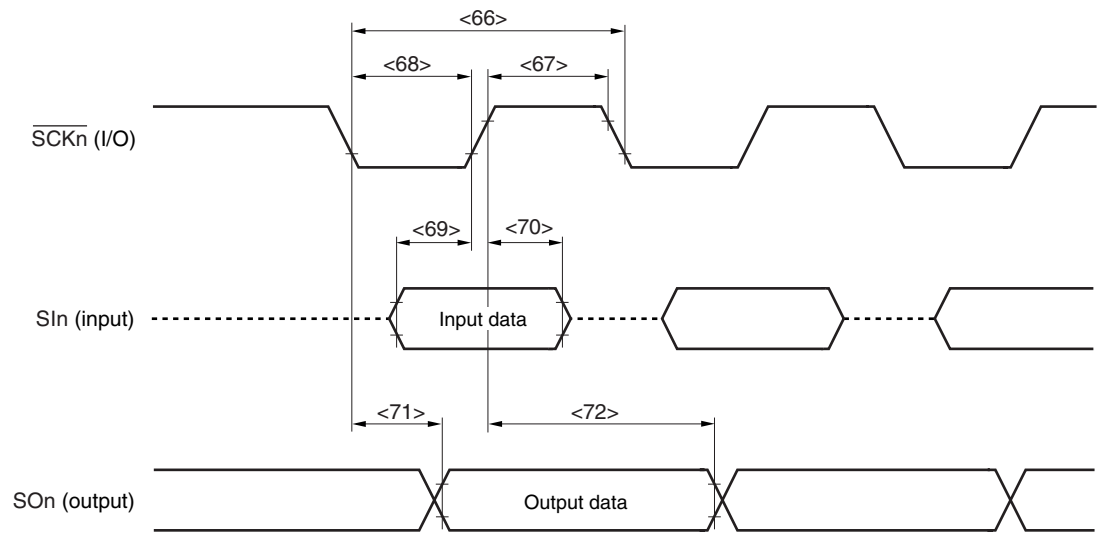
(b) Slave mode

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<66>	t_{CYSK1}	Input	200		ns
$\overline{SCKn}$ high-level width	<67>	t_{WSK1H}	Input	90		ns
$\overline{SCKn}$ low-level width	<68>	t_{WSK1L}	Input	90		ns
SIn setup time (to $\overline{SCKn}$↑)	<69>	t_{SSISK}		50		ns
SIn hold time (from $\overline{SCKn}$↑)	<70>	t_{HSKSI}		50		ns
SOn output delay time (from $\overline{SCKn}$↓)	<71>	t_{DSKSO}			55	ns
SOn output hold time (from $\overline{SCKn}$↑)	<72>	t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0, 1

(8) CSI timing (2/2)



Remarks 1. The broken lines indicate high impedance.

2. n = 0, 1

(9) UART0 timing

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),

T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),

V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,

output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UART0 baud rate generator input frequency	f_{BRG}			25	MHz

Remark f_{BRG} (UART0 baud rate generator input frequency) can be selected from f_{XX}, f_{XX}/2, f_{XX}/4, f_{XX}/8, f_{XX}/16, f_{XX}/32, f_{XX}/64, f_{XX}/128, f_{XX}/256, f_{XX}/512, f_{XX}/1024, and f_{XX}/2048 by setting the TPS3 to TPS0 bits of clock select register 0 (CKSR0) (f_{XX}: Internal system clock frequency).

(10) UART1, UART2 timing (1/2)

(a) Clocked master mode

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{ASCKn}}$ cycle	<73>	t_{CYSK0}	Output	1000		ns
$\overline{\text{ASCKn}}$ high-level width	<74>	t_{WSK0H}	Output	k T – 20		ns
$\overline{\text{ASCKn}}$ low-level width	<75>	t_{WSK0L}	Output	k T – 20		ns
RXDn setup time (to $\overline{\text{ASCKn}}$↑)	<76>	t_{SRXSK}		1.5 T + 35		ns
RXDn hold time (from $\overline{\text{ASCKn}}$↑)	<77>	t_{HSKRX}		0		ns
TXDn output delay time (from $\overline{\text{ASCKn}}$↓)	<78>	t_{DSKTX}			T + 10	ns
TXDn output hold time (from $\overline{\text{ASCKn}}$↑)	<79>	t_{HSKTX}		(k + 1)T – 20		ns

Remarks **1.** T = $2t_{CYK}$

2. k: Setting value of prescaler compare register n (PRSCMn) of UARTn

3. n = 1, 2

(b) Clocked slave mode

(T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A),
T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1),
V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V,
output pin load capacitance: C_L = 50 pF)

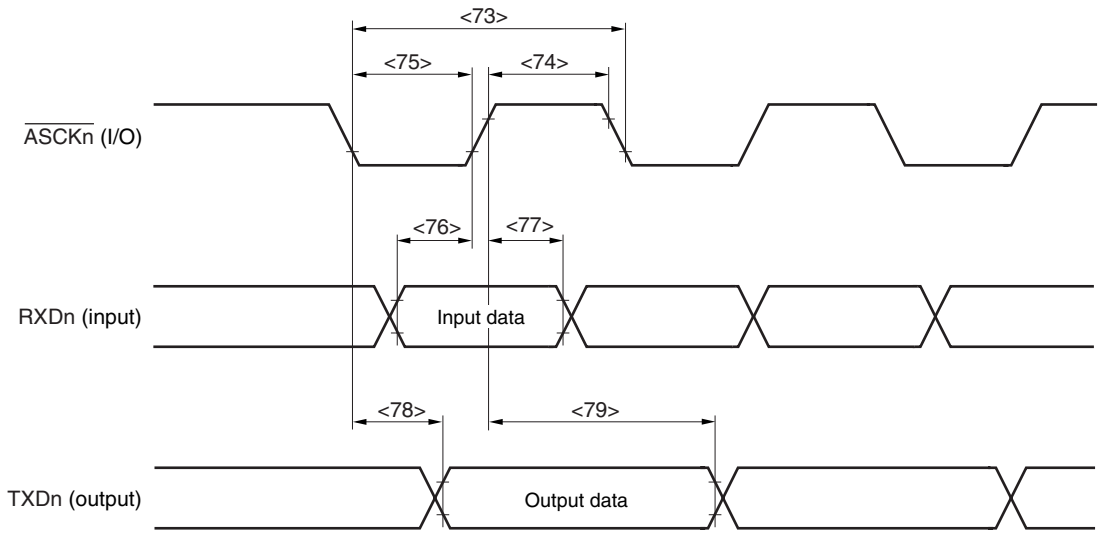
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{ASCKn}}$ cycle	<73>	t_{CYSK0}	Input	1000		ns
$\overline{\text{ASCKn}}$ high-level width	<74>	t_{WSK0H}	Input	4 T + 80		ns
$\overline{\text{ASCKn}}$ low-level width	<75>	t_{WSK0L}	Input	4 T + 80		ns
RXDn setup time (to $\overline{\text{ASCKn}}$↑)	<76>	t_{SRXSK}		T + 10		ns
RXDn hold time (from $\overline{\text{ASCKn}}$↑)	<77>	t_{HSKRX}		T + 10		ns
TXDn output delay time (from $\overline{\text{ASCKn}}$↓)	<78>	t_{DSKTX}			2.5 T + 45	ns
TXDn output hold time (from $\overline{\text{ASCKn}}$↑)	<79>	t_{HSKTX}		k T + 1.5 T		ns

Remarks **1.** T = $2t_{CYK}$

2. k: Setting value of PRSCMn register of UARTn

3. n = 1, 2

(10) UART1, UART2 timing (2/2)

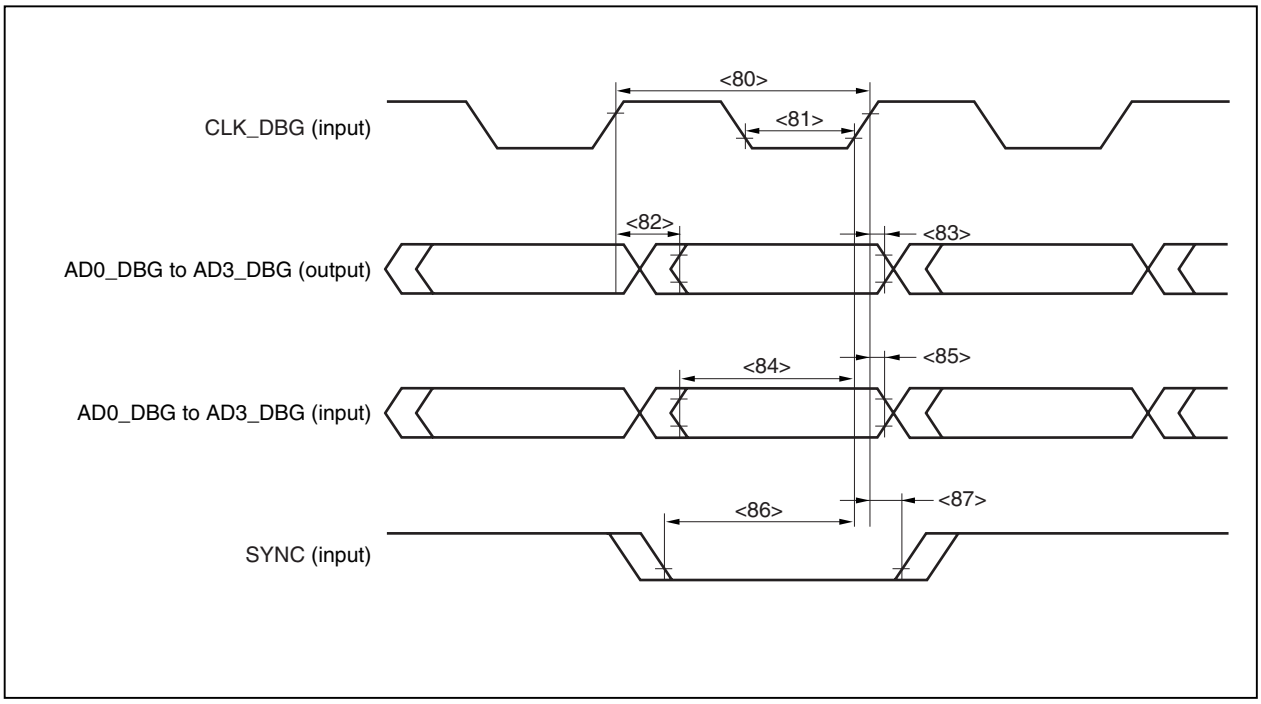


Remark n = 1, 2

(11) NBD timing (μPD70F3116 only)

(T_A = 0 to +40°C, V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V, output pin load capacitance: C_L = 100 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NBD cycle	<80>	t_{NDCYC}		80		ns
NBD cycle low-level width	<81>	t_{NDL}		35		ns
NBD data output delay time	<82>	t_{NDD}		5	t_{NDCYC} –20	ns
NBD data output hold time	<83>	t_{NDHD}		2		ns
NBD data input setup time	<84>	t_{NDS}		20		ns
NBD data input hold time	<85>	t_{NDH}		5		ns
SYNC input setup time	<86>	t_{NDSYS}		20		ns
SYNC input hold time	<87>	t_{NDSYH}		5		ns



A/D Converter Characteristics (T_A = –40 to +85°C: μPD703116, 703116(A), 70F3116, 70F3116(A), T_A = –40 to +110°C: μPD703116(A1), 70F3116(A1), $V_{DD3} = CV_{DD}$ = 3.0 to 3.6 V, $AV_{DD} = V_{DD5}$ = 5 V ±0.5 V, $AV_{SS} = V_{SS3} = V_{SS5} = CV_{SS}$ = 0 V, output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error[Note 1]	–				±5	LSB
Quantization error	–				±1/2	LSB
Conversion time	t_{CONV}		5		10	μs
Sampling time	t_{SAMP}		833			ns
Zero-scale error[Note 1]	–				±3	LSB
Full-scale error[Note 1]	–				±3	LSB
Differential linearity error[Note 1]	–				±3	LSB
Integral linearity error[Note 1]	–				±5	LSB
Analog input voltage	V_{IAN}		–0.3		AV_{REFn} + 0.3	V
Analog reference voltage	AV_{REF}	$AV_{REFn} = AV_{DD}$	4.5		5.5	V
AV_{REFn} input current[Note 2]	AI_{REF}			1	2	mA
AV_{DD} power supply current[Note 2]	AI_{DD}			3	6	mA

Notes 1. The quantization error (±0.5 LSB) is not included.

2. The V850E/IA1 incorporates two A/D converters. This is the rated value for one converter.

Remarks 1. LSB: Least Significant Bit

2. n = 0, 1

3.2 Flash Memory Programming Mode (μPD70F3116 only)

Basic Characteristics (T_A = 0 to 70°C (during rewrite),

T_A = –40 to +85°C (except during rewrite): μPD70F3116, 70F3116(A),

T_A = –40 to +110°C (except during rewrite): μPD70F3116(A1),

V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		4		50	MHz
V_{PP} supply voltage	V_{PP1}	During flash memory programming	7.5	7.8	8.1	V
	V_{PPL}	V_{PP} low-level detection	$0.8V_{DD3}$	V_{DD3}	$1.2V_{DD3}$	V
	V_{PPM}	V_{PP}, V_{DD3} level detection	$0.65V_{DD3}$		V_{DD3} + 0.3	V
	V_{PPH}	V_{PP} high-voltage level detection	7.5	7.8	8.1	V
V_{DD3} supply current	I_{DD1}	V_{PP} = V_{PP1}			4.5fx	mA
V_{PP} supply current	I_{PP}	V_{PP} = 7.8 V			100	mA
Step erase time	t_{ER}	**Note 1**	0.398	0.4	0.402	s
Overall erase time per area	t_{ERA}	When the step erase time = 0.4 s, **Note 2**			40	s/area
Write-back time	t_{WB}	**Note 3**	0.99	1	1.01	ms
Number of write-backs per write-back command	C_{WB}	When the write-back time = 1 ms, **Note 4**			300	Count/write-back command
Number of erase/write-backs	C_{ERWB}				16	Count
Step writing time	t_{WT}	**Note 5**	18	20	22	μs
Overall writing time per word	t_{WTW}	When the step writing time = 20 μs (1 word = 4 bytes), **Note 6**	20		200	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite, **Note 7**	100			Count/area

Notes 1. The recommended setting value of the step erase time is 0.4 s.

2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.

3. The recommended setting value of the write-back time is 1 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step writing time is 20 μs.

6. 20 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

7. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

Shipped product ——→ P → E → P → E → P: 3 rewrites

Shipped product → E → P → E → P → E → P: 3 rewrites

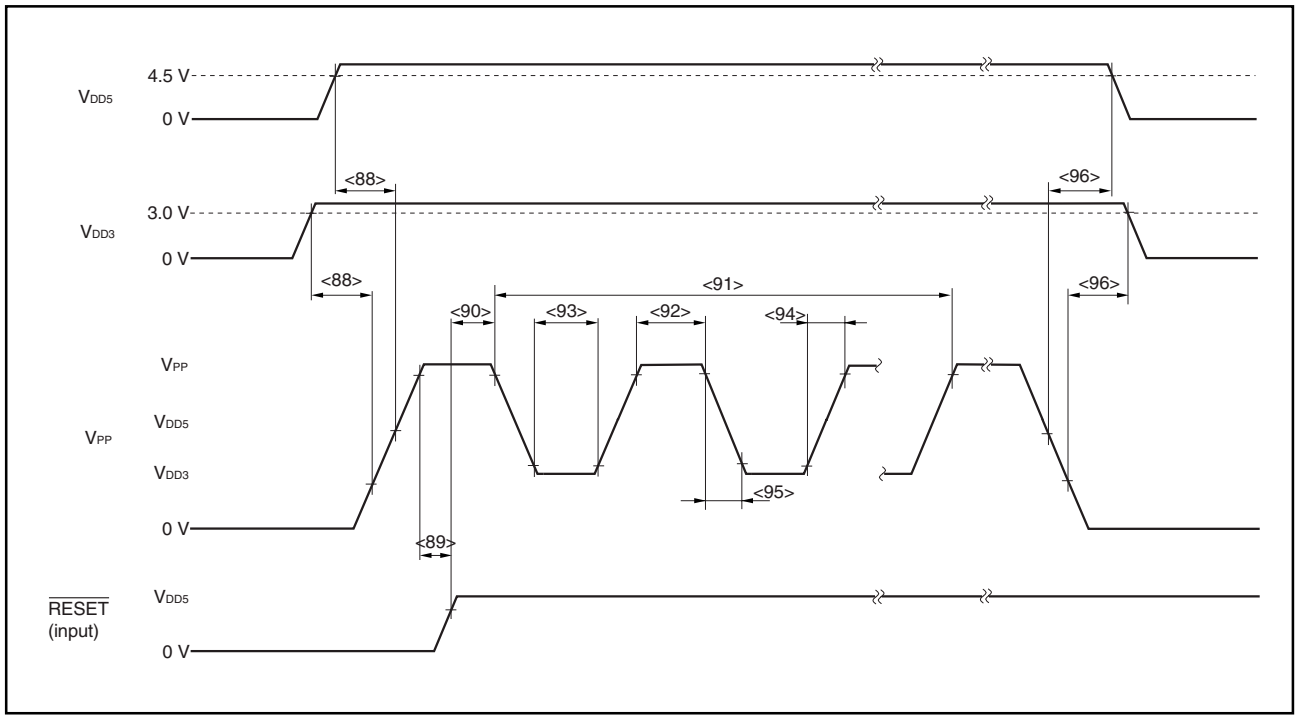
Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.

2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH

Serial Write Operation Characteristics (T_A = 0 to 70°C, V_{DD3} = CV_{DD} = 3.0 to 3.6 V, V_{DD5} = 5 V ±0.5 V, V_{SS3} = V_{SS5} = CV_{SS} = 0 V)

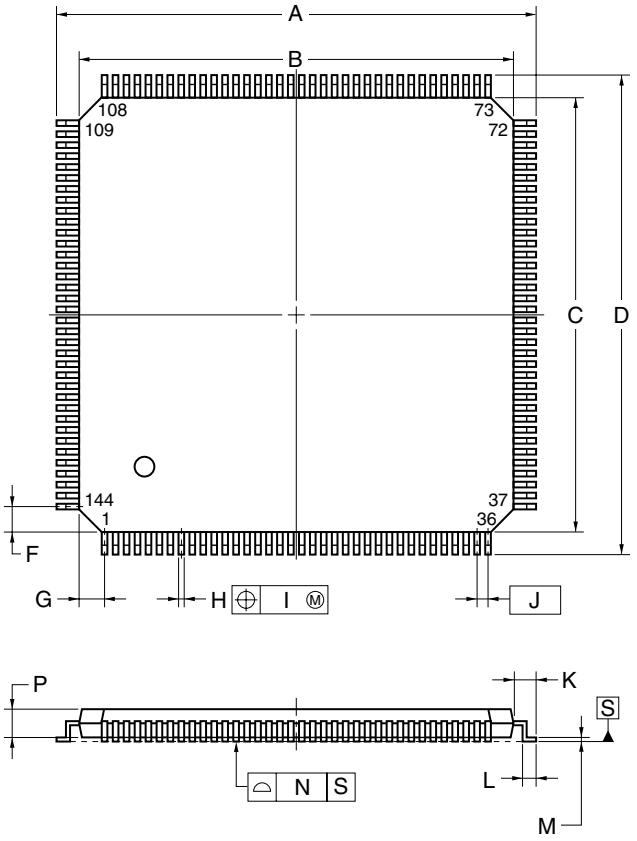
Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
V_{DD3}, V_{DD5}↑ to V_{PP}↑ set time	<88>	t_{DRPSR}		10			μs
V_{PP}↑ to $\overline{RESET}$↑ set time	<89>	t_{PSRRF}		1			μs
$\overline{RESET}$↑ to V_{PP} count start time	<90>	t_{RFOF}	V_{PP} = 7.8 V	10T + 1500			ns
Count execution time	<91>	t_{COUNT}				15	ms
V_{PP} counter high-level width	<92>	t_{CH}		1			μs
V_{PP} counter low-level width	<93>	t_{CL}		1			μs
V_{PP} counter rise time	<94>	t_R				1	μs
V_{PP} counter fall time	<95>	t_F				1	μs
V_{PP}↓ to V_{DD3}, V_{DD5}↓ reset time	<96>	t_{PFDR}		10			μs

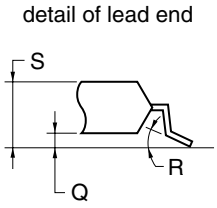
Remark T = t_{CYK}



4. PACKAGE DRAWING

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)





NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

5. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions

μPD703116GJ-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD703116GJ(A)-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD703116GJ(A1)-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD70F3116GJ-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD70F3116GJ(A)-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD70F3116GJ(A1)-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR30-103-2
★ VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

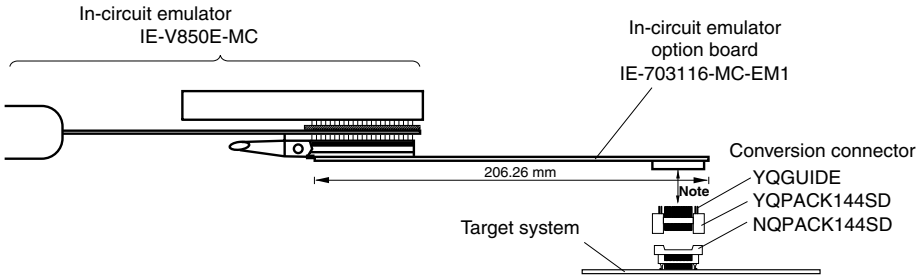
Caution Do not use different soldering methods together.

⋆ APPENDIX NOTES ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system based on this configuration.

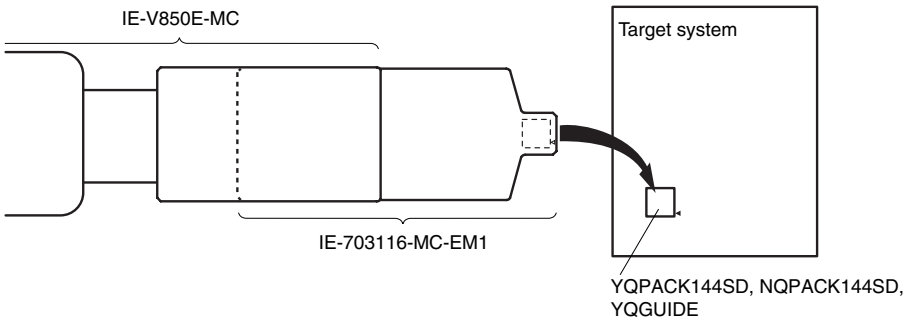
Appendix-1. 144-pin Plastic LQFP (Fine Pitch) (20 × 20)

Side view

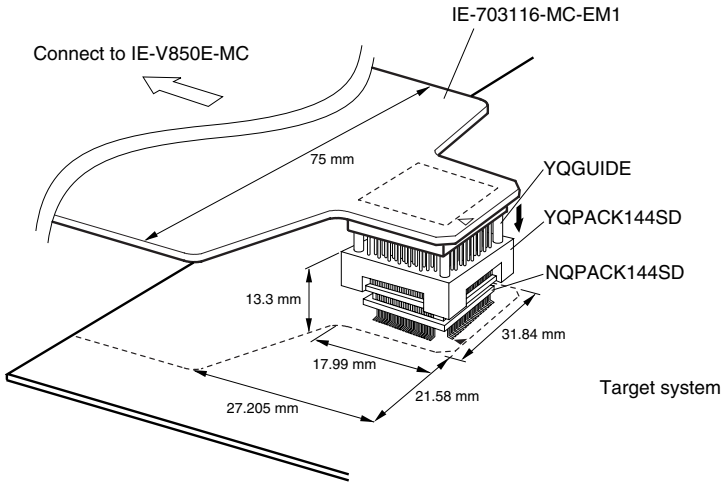


Note YQSOCKET144SDN (sold separately) can be inserted here to adjust the height (height: 3.2 mm).

Top view



Connection condition diagram



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference document: Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

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