

# MOS INTEGRATED CIRCUIT

# $\mu$ PD703106, 703107

## V850E/MA1™

### 32-/16-BIT SINGLE-CHIP MICROCONTROLLER

#### DESCRIPTION

The  $\mu$ PD703106 and 703107 are products of the V850 Family™ of 32-bit single-chip microcontroller for real-time control applications. These microcontrollers integrate a 32-bit CPU, ROM, RAM, an interrupt controller, a real-time pulse unit, a serial interface, an A/D converter, a DMA controller, and other functions on a single chip.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MA1 User's Manual Hardware: U14359E  
V850E1 User's Manual Architecture: U14559E

#### FEATURES

- Number of instructions: 83
- Minimum instruction execution time: 20 ns (with a 50 MHz internal clock)
- General-purpose registers: 32 bits  $\times$  32 registers
- Instruction set suitable for control applications
- Internal memory
  - ROM: 128 KB ( $\mu$ PD703106)
  - 256 KB ( $\mu$ PD703107)
  - RAM: 10 KB ( $\mu$ PD703106, 703107)
- Memory access control (supporting EDO DRAM, SDRAM, and page ROM)
- Sophisticated internal interrupt controller
- Real-time pulse unit suitable for control applications
- Powerful serial interface (with dedicated internal baud rate generator)
- Clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power-saving functions

#### APPLICATIONS

- Office machines (such as ink jet printers, facsimiles, and PPCs)
- Multimedia systems (such as digital still cameras, DVD players, and video printers)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

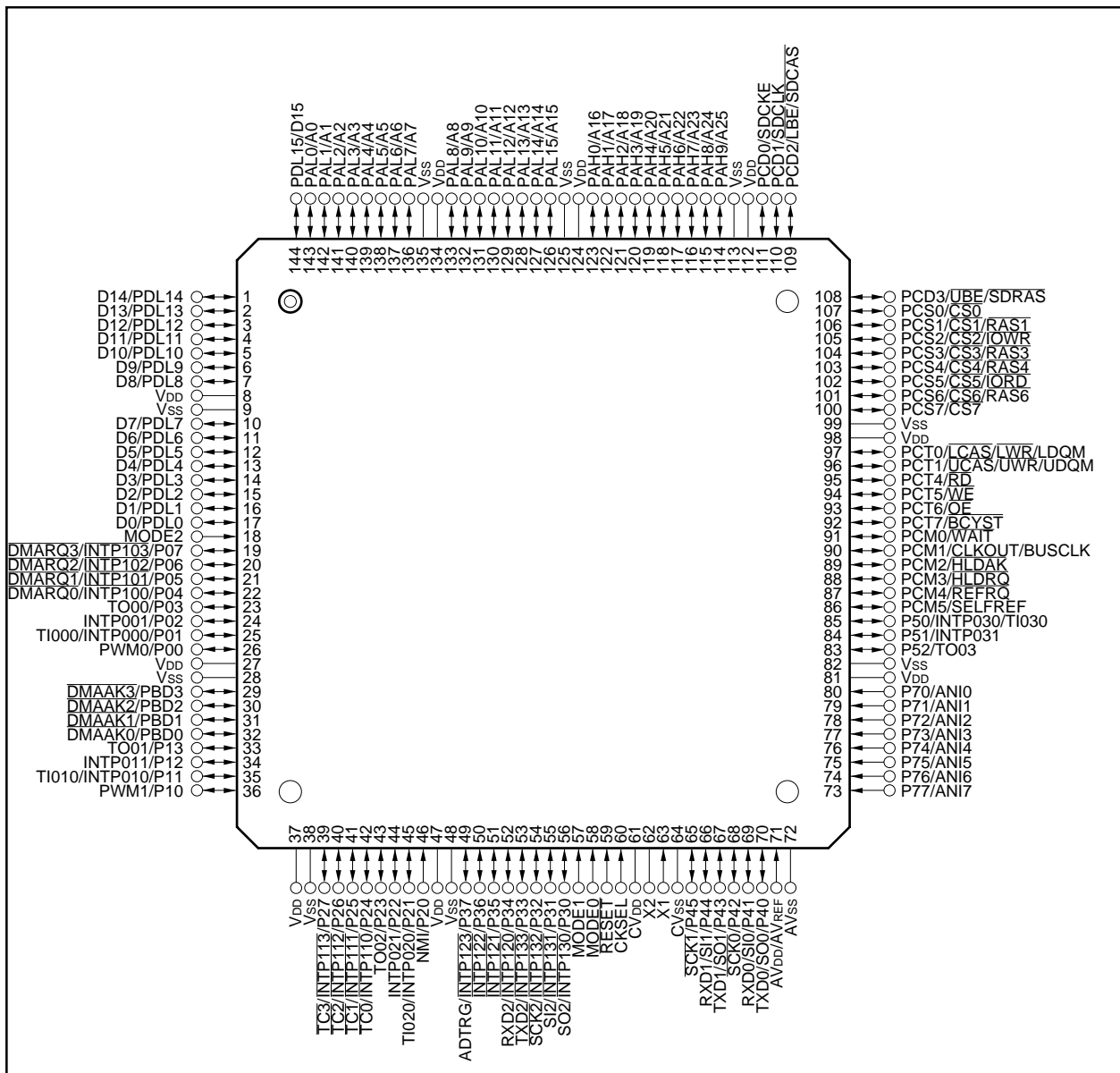
Part Number	Package	Internal ROM
μPD703106GJ-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	128 KB (mask ROM)
μPD703107GJ-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	256 KB (mask ROM)

Remark xxx indicates ROM code suffix.

PIN CONFIGURATION (TOP VIEW)

144-pin plastic LQFP (fine pitch) (20 × 20)

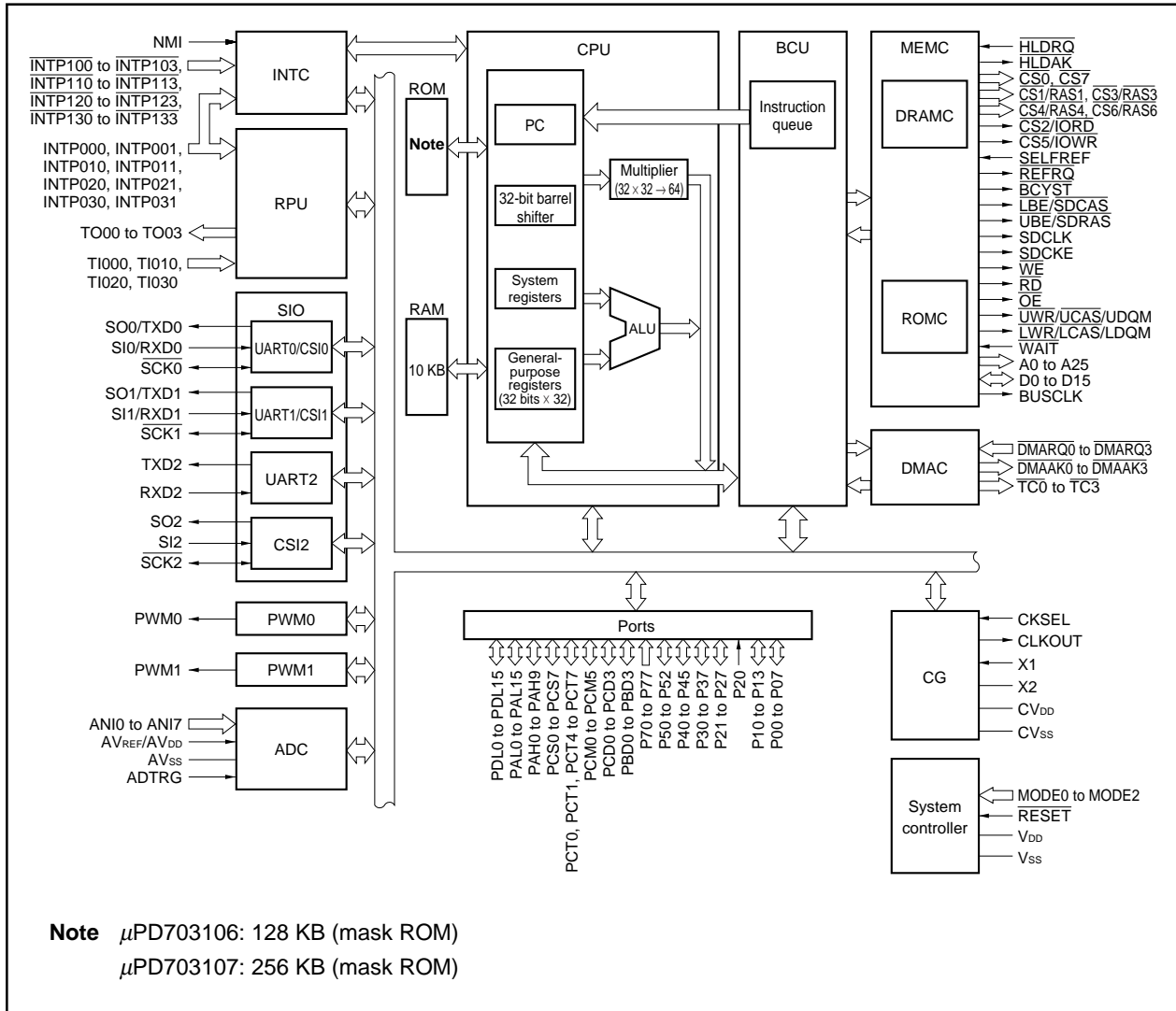
- μPD703106GJ-xxx-UEN
- μPD703107GJ-xxx-UEN



**PIN IDENTIFICATION**

A0 to A25:	Address Bus	P50 to P52:	Port 5
ADTRG:	AD Trigger Input	P70 to P77:	Port 7
ANI0 to ANI7:	Analog Input	PAH0 to PAH9:	Port AH
AV <sub>DD</sub> :	Analog Power Supply	PAL0 to PAL15:	Port AL
AV <sub>REF</sub> :	Analog Reference Voltage	PBD0 to PBD3:	Port BD
AV <sub>SS</sub> :	Analog Ground	PCD0 to PCD3:	Port CD
BCYST:	Bus Cycle Start Timing	PCM0 to PCM5:	Port CM
BUSCLK:	Bus Clock Output	PCS0 to PCS7:	Port CS
CKSEL:	Clock Generator Operating Mode Select	PCT0, PCT1, :	Port CT
CLKOUT:	Clock Output	PCT4 to PCT7	
CS0 to CS7:	Chip Select	PDL0 to PDL15:	Port DL
CV <sub>DD</sub> :	Clock Generator Power Supply	PWM0, PWM1:	Pulse Width Modulation
CV <sub>SS</sub> :	Clock Generator Ground	RAS1, RAS3,	
D0 to D15:	Data Bus	RAS4, RAS6:	Row Address Strobe
DMAAK0 to DMAAK3:	DMA Acknowledge	RD:	Read
DMARQ0 to DMARQ3:	DMA Request	REFRQ:	Refresh Request
HLDAK:	Hold Acknowledge	RESET:	Reset
HLDREQ:	Hold Request	RXD0 to RXD2:	Receive Data
INTP000, INTP001, INTP010, INTP011, INTP020, INTP021, INTP030, INTP031, INTP100 to INTP103, INTP110 to INTP113, INTP120 to INTP123, INTP130 to INTP133	Interrupt Request from Peripherals	SCK0 to SCK2:	Serial Clock
IORD:	I/O Read Strobe	SDCAS:	SDRAM Column Address Strobe
IOWR:	I/O Write Strobe	SDCKE:	SDRAM Clock Enable
LBE:	Lower Byte Enable	SDCLK:	SDRAM Clock Output
LCAS:	Lower Column Address Strobe	SDRAS:	SDRAM Row Address Strobe
LDQM:	Lower DQ Mask Enable	SELFREF:	Self-refresh Request
LWR:	Lower Write Strobe	SI0 to SI2:	Serial Input
MODE0 to MODE2:	Mode	SO0 to SO2:	Serial Output
NMI:	Non-Maskable Interrupt Request	TC0 to TC3:	Terminal Count Signal
OE:	Output Enable	TI000, TI010, TI020, TI030:	Timer Input
P00 to P07:	Port 0	TO00 to TO03:	Timer Output
P10 to P13:	Port 1	TXD0 to TXD2:	Transmit Data
P20 to P27:	Port 2	UBE:	Upper Byte Enable
P30 to P37:	Port 3	UCAS:	Upper Column Address Strobe
P40 to P45:	Port 4	UDQM:	Upper DQ Mask Enable
		UWR:	Upper Write Strobe
		V <sub>DD</sub> :	Power Supply for Internal Unit
		V <sub>SS</sub> :	Ground
		WAIT:	Wait
		WE:	Write Enable
		X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



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1. DIFFERENCES AMONG PRODUCTS

1.1 Differences Between μPD70F3107 and μPD703106, 703107

Item \ Product	μPD70F3107	μPD703106	μPD703107
Internal ROM	Flash memory (256 KB)	Mask ROM (128 KB)	Mask ROM (256 KB)
Internal RAM	10 KB		
Flash memory programming pin	Provided (V <sub>PP</sub> )	None	
Flash memory programming mode	Provided (MODE0 = H/L, MODE1 = H, MODE2/V <sub>PP</sub> = 7.8 V)	None	
Electrical specifications	Current consumption etc. differs (see individual data sheets).		
Others	Circuit scale and mask layout differ, thus noise immunity, noise radiation, etc. differ.		

- Cautions**
1. There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.
  2. When switching from the flash memory version to the mask ROM version, write the same code to the free area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units.	PWM0
P01			TI000/INTP000
P02			INTP001
P03			TO00
P04			DMARQ0/INTP100
P05			DMARQ1/INTP101
P06			DMARQ2/INTP102
P07			DMARQ3/INTP103
P10	I/O	Port 1 4-bit I/O port Input/output mode can be specified in 1-bit units.	PWM1
P11			INTP010/TI010
P12			INTP011
P13			TO01
P20	Input	Port 2 P20 is an input-only port. If a valid edge is input, it operates as an NMI input. Also, the status of the NMI input is shown by bit 0 of the P2 register. P21 to P27 are 7-bit I/O port. Input/output mode can be specified in 1-bit units.	NMI
P21	I/O		INTP020/TI020
P22			INTP021
P23			TO02
P24			TC0/INTP110
P25			TC1/INTP111
P26			TC2/INTP112
P27			TC3/INTP113
P30	I/O	Port 3 8-bit I/O port Input/output mode can be specified in 1-bit units.	SO2/INTP130
P31			SI2/INTP131
P32			SCK2/INTP132
P33			TXD2/INTP133
P34			RXD2/INTP120
P35			INTP121
P36			INTP122
P37			ADTRG/INTP123
P40	I/O	Port 4 6-bit I/O port Input/output mode can be specified in 1-bit units.	TXD0/SO0
P41			RXD0/SI0
P42			SCK0
P43			TXD1/SO1
P44			RXD1/SI1
P45			SCK1
P50	I/O	Port 5 3-bit I/O port Input/output mode can be specified in 1-bit units.	INTP030/TI030
P51			INTP031
P52			TO03

(2/2)

Pin Name	I/O	Function	Alternate Function
P70 to P77	Input	Port 7 8-bit input-only port	ANI0 to ANI7
PBD0 to PBD3	I/O	Port BD 4-bit I/O port Input/output mode can be specified in 1-bit units.	DMAAK0 to DMAAK3
PCM0	I/O	Port CM 6-bit I/O port Input/output mode can be specified in 1-bit units.	WAIT
PCM1			CLKOUT/BUSCLK
PCM2			HLDKAK
PCM3			HLDKAK
PCM4			REFRQ
PCM5			SELFREF
PCT0	I/O	Port CT 6-bit I/O port Input/output mode can be specified in 1-bit units.	LCAS/LWR/LDQM
PCT1			UCAS/UWR/UDQM
PCT4			RD
PCT5			WE
PCT6			OE
PCT7			BCYST
PCS0	I/O	Port CS 8-bit I/O port Input/output mode can be specified in 1-bit units.	CS0
PCS1			CS1/RAS1
PCS2			CS2/IOWR
PCS3			CS3/RAS3
PCS4			CS4/RAS4
PCS5			CS5/IORD
PCS6			CS6/RAS6
PCS7			CS7
PCD0	I/O	Port CD 4-bit I/O port Input/output mode can be specified in 1-bit units.	SDCKE
PCD1			SDCLK
PCD2			LBE/SDCAS
PCD3			UBE/SDRAS
PAH0 to PAH9	I/O	Port AH 8-/10-bit I/O port Input/output mode can be specified in 1-bit units.	A16 to A25
PAL0 to PAL15	I/O	Port AL 8-/16-bit I/O port Input/output mode can be specified in 1-bit units.	A0 to A15
PDL0 to PDL15	I/O	Port DL 8-/16-bit I/O port Input/output mode can be specified in 1-bit units.	D0 to D15



2.2 Non-Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO00	Output	Pulse signal output of timer C0 to C3	P03
TO01			P13
TO02			P23
TO03			P52
TI000	Input	External count input of timer C0 to C3	P01/INTP000
TI010			P11/INTP010
TI020			P21/INTP020
TI030			P50/INTP030
INTP000	Input	External maskable interrupt request input, or timer C0 external capture trigger input	P01/TI000
INTP001			P02
INTP010	Input	External maskable interrupt request input, or timer C1 external capture trigger input	P11/TI010
INTP011			P12
INTP020	Input	External maskable interrupt request input, or timer C2 external capture trigger input	P21/TI020
INTP021			P22
INTP030	Input	External maskable interrupt request input, or timer C3 external capture trigger input	P50/TI030
INTP031			P51
$\overline{\text{INTP100}}$	Input	External maskable interrupt request input	P04/ $\overline{\text{DMARQ0}}$
$\overline{\text{INTP101}}$			P05/ $\overline{\text{DMARQ1}}$
$\overline{\text{INTP102}}$			P06/ $\overline{\text{DMARQ2}}$
$\overline{\text{INTP103}}$			P07/ $\overline{\text{DMARQ3}}$
$\overline{\text{INTP110}}$			P24/ $\overline{\text{TC0}}$
$\overline{\text{INTP111}}$			P25/ $\overline{\text{TC1}}$
$\overline{\text{INTP112}}$			P26/ $\overline{\text{TC2}}$
$\overline{\text{INTP113}}$			P27/ $\overline{\text{TC3}}$
$\overline{\text{INTP120}}$			P34/RXD2
$\overline{\text{INTP121}}$			P35
$\overline{\text{INTP122}}$			P36
$\overline{\text{INTP123}}$			P37/ADTRG
$\overline{\text{INTP130}}$			P30/SO2
$\overline{\text{INTP131}}$			P31/SI2
$\overline{\text{INTP132}}$			P32/ $\overline{\text{SCK2}}$
$\overline{\text{INTP133}}$			P33/TXD2
SO0	Output	CSI0 to SCI2 serial transmission data output (3-wire)	P40/TXD0
SO1			P43/TXD1
SO2			P30/INTP130
SI0	Input	CSI0 to CSI2 serial reception data input (3-wire)	P41/RXD0
SI1			P44/RXD1
SI2			P31/INTP131

(2/3)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{SCK0}}$	I/O	CSI0 to CSI2 serial clock I/O (3-wire)	P42
$\overline{\text{SCK1}}$			P45
$\overline{\text{SCK2}}$			P32/ $\overline{\text{INTP132}}$
TXD0	Output	UART0 to UART2 serial transmission data output	P40/SO0
TXD1			P43/SO1
TXD2			P33/ $\overline{\text{INTP133}}$
RXD0	Input	UART0 to UART2 serial reception data input	P41/SI0
RXD1			P44/SI1
RXD2			P34/ $\overline{\text{INTP120}}$
PWM0	Output	PWM pulse signal output	P00
PWM1			P10
ANI0 to ANI7	Input	Analog inputs to the A/D converter	P70 to P77
ADTRG	Input	A/D converter external trigger input	P37/ $\overline{\text{INTP123}}$
$\overline{\text{DMARQ0}}$	Input	DMA request signal input	P04/ $\overline{\text{INTP100}}$
$\overline{\text{DMARQ1}}$			P05/ $\overline{\text{INTP101}}$
$\overline{\text{DMARQ2}}$			P06/ $\overline{\text{INTP102}}$
$\overline{\text{DMARQ3}}$			P07/ $\overline{\text{INTP103}}$
$\overline{\text{DMAAK0}}$	Output	DMA acknowledge signal output	PBD0
$\overline{\text{DMAAK1}}$			PBD1
$\overline{\text{DMAAK2}}$			PBD2
$\overline{\text{DMAAK3}}$			PBD3
$\overline{\text{TC0}}$	Output	DMA transfer termination (terminal count) signal output	P24/ $\overline{\text{INTP110}}$
$\overline{\text{TC1}}$			P25/ $\overline{\text{INTP111}}$
$\overline{\text{TC2}}$			P26/ $\overline{\text{INTP112}}$
$\overline{\text{TC3}}$			P27/ $\overline{\text{INTP113}}$
NMI	Input	Non-maskable interrupt request signal input	P20
MODE0	Input	V850E/MA1 operating mode specification	–
MODE1			–
MODE2			–
$\overline{\text{WAIT}}$	Input	Control signal input that inserts a wait in the bus cycle	PCM0
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	PCM2
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	PCM3
$\overline{\text{REFRQ}}$	Output	Refresh request signal output for DRAM	PCM4
SELFREF	Input	Self refresh request input for DRAM	PCM5
$\overline{\text{LCAS}}$	Output	Column address strobe signal output for DRAM lower data	PCT0/ $\overline{\text{LWR}}/\overline{\text{LDQM}}$
$\overline{\text{UCAS}}$	Output	Column address strobe signal output for DRAM higher data	PCT1/ $\overline{\text{UWR}}/\overline{\text{UDQM}}$
$\overline{\text{LWR}}$	Output	External data lower byte write enable signal output	PCT0/ $\overline{\text{LCAS}}/\overline{\text{LDQM}}$
$\overline{\text{UWR}}$	Output	External data higher byte write enable signal output	PCT1/ $\overline{\text{UCAS}}/\overline{\text{UDQM}}$

Pin Name	I/O	Function	Alternate Function
LDQM	Output	Output disable/write mask signal output for SDRAM lower data	PCT0/LCAS/LWR
UDQM	Output	Output disable/write mask signal output for SDRAM higher data	PCT1/UCAS/UWR
RD	Output	External data bus read strobe signal output	PCT4
WE	Output	Write enable signal output for DRAM	PCT5
OE	Output	Output enable signal output for DRAM	PCT6
BCYST	Output	Strobe signal output that shows the start of the bus cycle	PCT7
CS0	Output	Chip select signal output	PCS0
CS1			PCS1/RAS1
CS2			PCS2/IOWR
CS3			PCS3/RAS3
CS4			PCS4/RAS4
CS5			PCS5/IORD
CS6			PCS6/RAS6
CS7			PCS7
RAS1	Output	Row address strobe signal output for DRAM	PCS1/CS1
RAS3			PCS3/CS3
RAS4			PCS4/CS4
RAS6			PCS6/CS6
IOWR	Output	DMA write strobe signal output	PCS2/CS2
IORD	Output	DMA read strobe signal output	PCS5/CS5
SDCKE	Output	SDRAM clock enable signal output	PCD0
SDCLK	Output	SDRAM clock signal output	PCD1
SDCAS	Output	Column address strobe signal output for SDRAM	PCD2/LBE
SDRAS	Output	Row address strobe signal output for SDRAM	PCD3/UBE
LBE	Output	External data bus lower byte enable signal output	PCD2/SDCAS
UBE	Output	External data bus higher byte enable signal output	PCD3/SDRAS
D0 to D15	I/O	16-bit data bus for external memory	PDL0 to PDL15
A0 to A15	Output	26-bit address bus for external memory	PAL0 to PAL15
A16 to A25			PAH0 to PAH9
RESET	Input	System reset input	-
X1	Input	Connects the crystal resonator for system clock oscillation. In the case of an external source supplying the clock, it is input to X1 pin.	-
X2	-		-
CLKOUT	Output	System clock output	PCM1/BUSCLK
BUSCLK	Output	Bus clock output	PCM1/CLKOUT
CKSEL	Input	Input which specifies the clock generator's operating mode	-
AVREF	Input	Reference voltage applied to A/D converter	AVDD
AVDD	-	Positive power supply for A/D converter	AVREF
AVSS	-	Ground potential for A/D converter	-
CVDD	-	Positive power supply for the dedicated clock generator	-
CVSS	-	Ground potential for the dedicated clock generator	-
VDD	-	Positive power supply	-
VSS	-	Ground potential	-

**2.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

The input/output circuit configuration of each type is schematically shown in Figure 2-1.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V<sub>DD</sub> or V<sub>SS</sub> via a resistor.

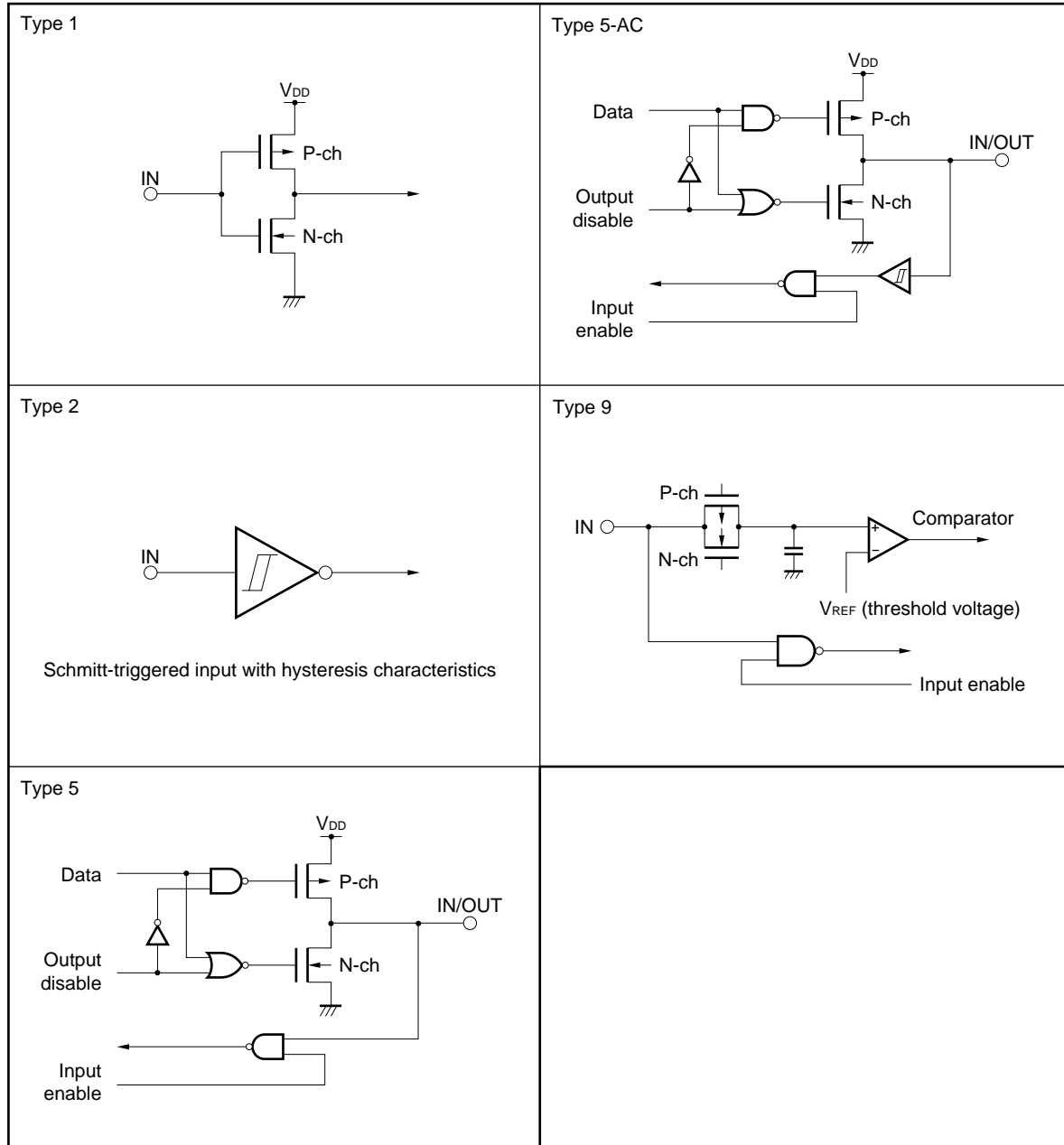
**Table 2-1. Types of Pin I/O Circuits and Recommended Connection (1/2)**

Pin Name	I/O Circuit Type	Recommended Connection
P00/PWM0	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P01/INTP000/TI000	5-AC	
P02/INTP001		
P03/TO00	5	
P04/ $\overline{\text{DMARQ0}}$ /INTP100 to P07/ $\overline{\text{DMARQ3}}$ /INTP103	5-AC	
P10/PWM1	5	
P11/INTP010/TI010	5-AC	
P12/INTP011		
P13/TO01	5	
P20/NMI	2	
P21/INTP020/TI020	5-AC	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P22/INTP021		
P23/TO02	5	
P24/ $\overline{\text{TC0}}$ /INTP110 to P27/ $\overline{\text{TC3}}$ /INTP113	5-AC	
P30/ $\overline{\text{SO2}}$ /INTP130		
P31/ $\overline{\text{SI2}}$ /INTP131		
P32/ $\overline{\text{SCK2}}$ /INTP132		
P33/ $\overline{\text{TXD2}}$ /INTP133		
P34/ $\overline{\text{RXD2}}$ /INTP120		
P35/INTP121		
P36/INTP122		
P37/ $\overline{\text{ADTRG}}$ /INTP123		
P40/TXD0/SO0		5
P41/RXD0/SI0	5-AC	
P42/ $\overline{\text{SCK0}}$		
P43/TXD1/SO1	5	
P44/RXD1/SI1	5-AC	
P45/ $\overline{\text{SCK1}}$		
P50/INTP030/TI030	5	
P51/INTP031		
P52/TO03	5	
P70/ANI0 to P77/ANI7	9	Connect directly to V <sub>SS</sub> .
PBD0/ $\overline{\text{DMAAK0}}$ to PBD3/ $\overline{\text{DMAAK3}}$	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open

Table 2-1. Types of Pin I/O Circuits and Recommended Connection (2/2)

Pin Name	I/O Circuit Type	Recommended Connection
PCM0/ $\overline{\text{WAIT}}$	5	Input: Independently connect to $V_{DD}$ via a resistor
PCM1/ $\overline{\text{CLKOUT}}$ / $\overline{\text{BUSCLK}}$	5	Input: Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor
PCM2/ $\overline{\text{HLD\AA K}}$		Output: Leave open
PCM3/ $\overline{\text{HLDRQ}}$	5	Input: Independently connect to $V_{DD}$ via a resistor
PCM4/ $\overline{\text{REFRQ}}$	5	Input: Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor Output: Leave open
PCM5/ $\overline{\text{SELFREF}}$	5	Input: Independently connect to $V_{SS}$ via a resistor
PCT0/ $\overline{\text{LCAS}}$ / $\overline{\text{LWR}}$ / $\overline{\text{LDQM}}$	5	Input: Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor Output: Leave open
PCT1/ $\overline{\text{UCAS}}$ / $\overline{\text{UWR}}$ / $\overline{\text{UDQM}}$		
PCT4/ $\overline{\text{RD}}$		
PCT5/ $\overline{\text{WE}}$		
PCT6/ $\overline{\text{OE}}$		
PCT7/ $\overline{\text{BCYST}}$		
PCS0/ $\overline{\text{CS0}}$		
PCS1/ $\overline{\text{CS1}}$ / $\overline{\text{RAS1}}$		
PCS2/ $\overline{\text{CS2}}$ / $\overline{\text{IOWR}}$		
PCS3/ $\overline{\text{CS3}}$ / $\overline{\text{RAS3}}$		
PCS4/ $\overline{\text{CS4}}$ / $\overline{\text{RAS4}}$		
PCS5/ $\overline{\text{CS5}}$ / $\overline{\text{IORD}}$		
PCS6/ $\overline{\text{CS6}}$ / $\overline{\text{RAS6}}$		
PCS7/ $\overline{\text{CS7}}$		
PCD0/ $\overline{\text{SDCKE}}$		
PCD1/ $\overline{\text{SDCLK}}$		
PCD2/ $\overline{\text{LBE}}$ / $\overline{\text{SDCAS}}$		
PCD3/ $\overline{\text{UBE}}$ / $\overline{\text{SDRAS}}$		
PAH0/A16 to PAH9/A25		
PAL0/A0 to PAL15/A15		
PDL0/D0 to PDL15/D15		
MODE0 to MODE2	2	–
$\overline{\text{RESET}}$	2	Connect to $V_{SS}$ .
CKSEL	1	Connect to $V_{DD}$ .
$\text{AV}_{SS}$	–	Connect to $V_{SS}$ .
$\text{AV}_{DD}$ / $\text{AV}_{REF}$	–	Connect to $V_{DD}$ .

Figure 2-1. Pin I/O Circuits



### 3. ELECTRICAL SPECIFICATIONS

#### Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V <sub>DD</sub>	V <sub>DD</sub> pin	-0.5 to +4.6	V
	CV <sub>DD</sub>	CV <sub>DD</sub> pin	-0.5 to +4.6	V
	CV <sub>SS</sub>	CV <sub>SS</sub> pin	-0.5 to +0.5	V
	AV <sub>DD</sub>	AV <sub>DD</sub> pin	-0.5 to +4.6	V
	AV <sub>SS</sub>	AV <sub>SS</sub> pin	-0.5 to +0.5	V
Input voltage	V <sub>I</sub>	Except X1 pin	-0.5 to +6.0	V
Clock input voltage	V <sub>K</sub>	X1, V <sub>DD</sub> = 3.3 V ±0.3 V	-0.5 to V <sub>DD</sub> + 1.0	V
Output current, low	I <sub>OL</sub>	Per pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I <sub>OH</sub>	Per pin	-4.0	mA
		Total of all pins	-100	mA
Output voltage	V <sub>O</sub>	V <sub>DD</sub> = 3.3 V ±0.3 V	-0.5 to V <sub>DD</sub> + 0.5	V
Analog input voltage	V <sub>WASN</sub>	ANI0 to ANI7, V <sub>DD</sub> = 3.3 V ±0.3 V	-0.3 to AV <sub>DD</sub> + 0.3	V
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-60 to +150	°C

- Cautions**
1. Do not directly connect output (or input/output) pins of this IC product with each other, and also avoid direct connections to V<sub>DD</sub>, V<sub>CC</sub>, or GND. However, the open drain pins or the open collector pins can be directly connected with each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to a high-impedance state.
  2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

#### Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f <sub>c</sub> = 1 MHz			15	pF
I/O capacitance	C <sub>IO</sub>	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C <sub>O</sub>				15	pF

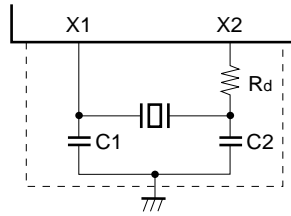
**Operating Conditions**

Operation Mode	Internal Operation Clock Frequency ( $\phi$ )	Operating Ambient Temperature ( $T_A$ )	Power Supply Voltage ( $V_{DD}$ )
Direct mode	4 to 25 MHz	-40 to +85°C	$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$
PLL mode	4 to 50 MHz	-40 to +85°C	$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$

**Recommended Oscillator**

**(a) Ceramic resonator**

**(i) Murata Mfg. Co., Ltd. ( $T_A = -40$  to  $+85^\circ\text{C}$ )**

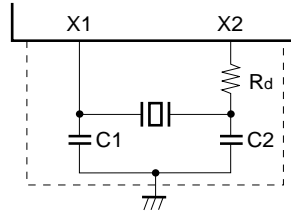


Type	Product	Oscillation Frequency $f_{xx}$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms)
			C1 (pF)	C2 (pF)	$R_d$ (kΩ)	MIN. (V)	MAX. (V)	
Surface mount	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.09
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.09
Lead	CSA4.00MG	4.0	30	30	0	3.0	3.6	0.05
	CST4.00MGW	4.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0400MG06	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	CSA5.00MG	5.0	30	30	0	3.0	3.6	0.05
	CST5.00MGW	5.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0500MG06	5.0	On-chip	On-chip	0	3.0	3.6	0.11

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the μPD703106, 703107 and the resonator.



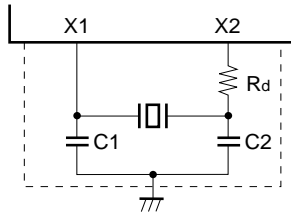
(ii) TDK (T<sub>A</sub> = -40 to +85°C)



Type	Product	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
Surface mount	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.3

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the μPD703106, 703107 and the resonator.

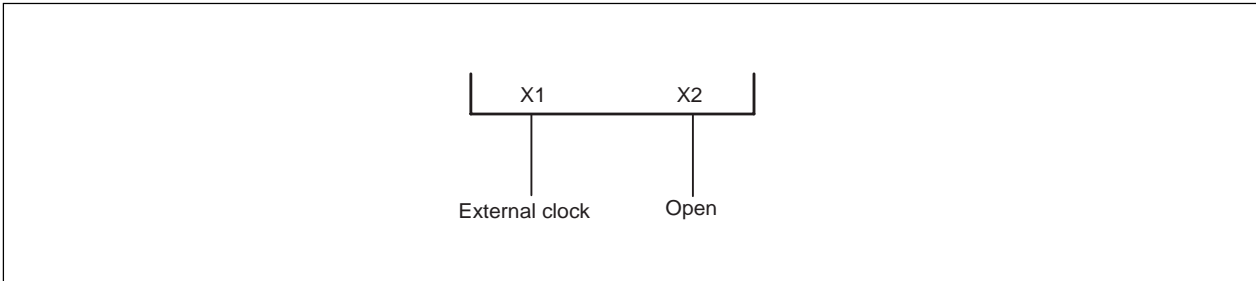
(iii) Kyocera Corporation (T<sub>A</sub> = -20 to +80°C)



Type	Product	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
Surface mount	PBRC4.00AR-A	4.0	33	33	0	3.0	3.6	0.11
	PBRC4.00BR-A	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	PBRC5.00AR-A	5.0	33	33	0	3.0	3.6	0.08
	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.08
Lead	KBR-4.0MSB	4.0	33	33	0	3.0	3.6	0.11
	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	KBR-5.0MSB	5.0	33	33	0	3.0	3.6	0.08
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.08

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the μPD703106, 703107 and the resonator.

(b) External clock input ( $T_A = -40$  to  $+85^\circ\text{C}$ )



**DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.3 V ±0.3 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH</sub>	Except for <b>Note 1</b>	2.0		5.5	V	
		<b>Note 1</b>	0.75V <sub>DD</sub>		5.5	V	
Input voltage, low	V <sub>IL</sub>	Except for <b>Note 1</b>	-0.5		0.8	V	
		<b>Note 1</b>	-0.5		0.2V <sub>DD</sub>	V	
Clock input voltage, high	V <sub>XH</sub>	X1 pin	Direct mode		V <sub>DD</sub> + 0.3	V	
			PLL mode	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Clock input voltage, low	V <sub>XL</sub>	X1 pin	Direct mode		0.15V <sub>DD</sub>	V	
			PLL mode	-0.5		0.15V <sub>DD</sub>	V
Schmitt-triggered input threshold voltage	V <sub>T</sub> <sup>+</sup>	<b>Note 1</b> , rising edge		2.0		V	
	V <sub>T</sub> <sup>-</sup>	<b>Note 1</b> , falling edge		1.0		V	
Schmitt-triggered input hysteresis width	V <sub>T</sub> <sup>+</sup> - V <sub>T</sub> <sup>-</sup>	<b>Note 1</b>	0.3			V	
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA	0.8V <sub>DD</sub>			V	
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.4			V	
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 2.5 mA			0.45	V	
Input leakage current, high	I <sub>LIH</sub>	V <sub>I</sub> = V <sub>DD</sub> , except for <b>Note 2</b>			10	μA	
Input leakage current, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V, except for <b>Note 2</b>			-10	μA	
Output leakage current, high	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub>			10	μA	
Output leakage current, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V			-10	μA	
Analog pin input leakage current	I <sub>LWASN</sub>	<b>Note 2</b>			±10	μA	
Power supply current	During normal operation	I <sub>DD1</sub>	Direct mode		2.6 × f <sub>x</sub> + 30	3.9 × f <sub>x</sub> + 45	mA
			PLL mode		2.6 × f <sub>x</sub> + 30	3.9 × f <sub>x</sub> + 45	mA
	In HALT mode	I <sub>DD2</sub>	Direct mode		1.6 × f <sub>x</sub> + 20	2.4 × f <sub>x</sub> + 30	mA
			PLL mode		1.6 × f <sub>x</sub> + 20	2.4 × f <sub>x</sub> + 30	mA
	In IDLE mode	I <sub>DD3</sub>	Direct mode		10	30	mA
			PLL mode		10	30	mA
	In STOP mode	I <sub>DD4</sub>	-40°C ≤ T <sub>A</sub> ≤ +40°C		10	60	μA
			40°C < T <sub>A</sub> ≤ 85°C			250	μA

**Notes 1.** P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

**2.** P70/ANI0 to P77/ANI7

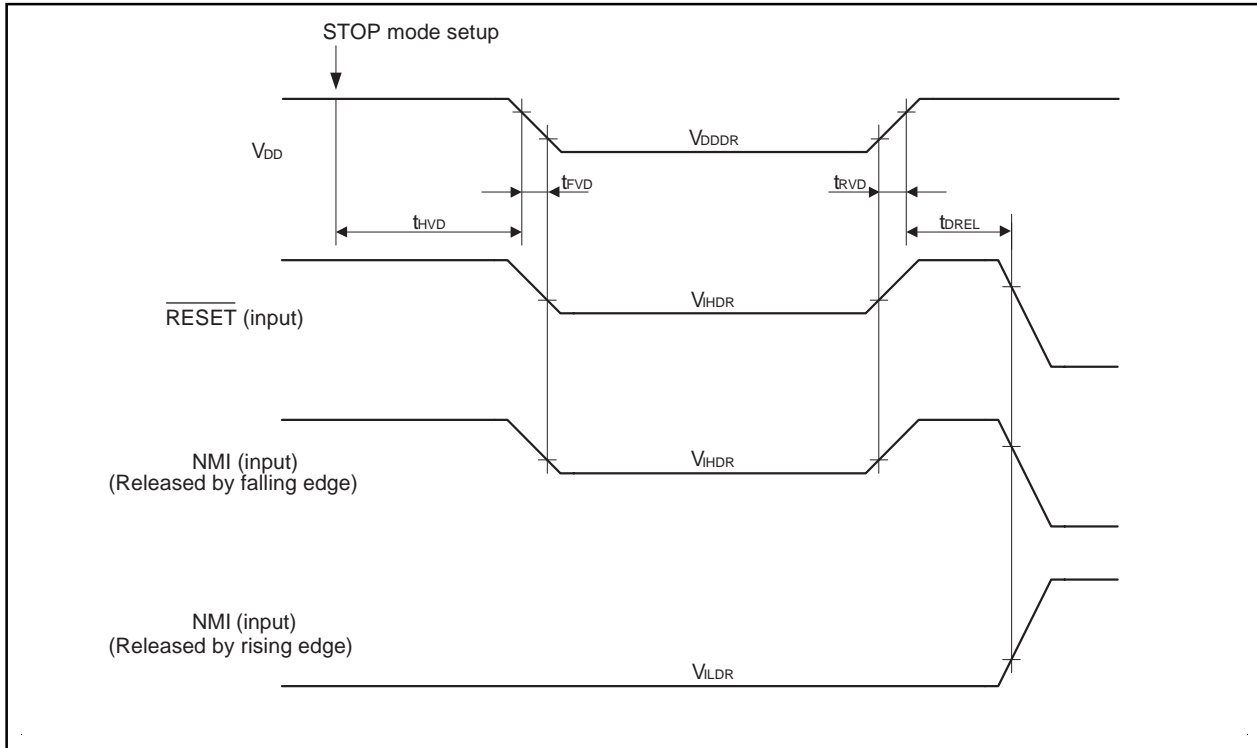
**Remark** The TYP. value is a reference value for when T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3 V. The current does not include the current flowing through pull-up resistors.

**Data Hold Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold voltage	V <sub>DDDR</sub>	STOP mode and V <sub>DD</sub> = V <sub>DDDR</sub>	1.5		3.6	V
Data hold current	I <sub>DDDR</sub>	V <sub>DD</sub> = V <sub>DDDR</sub> -40°C ≤ T <sub>A</sub> ≤ +40°C		10	60	μA
		40°C < T <sub>A</sub> ≤ 85°C			250	μA
Power supply voltage rise time	t <sub>rVD</sub>		200			μs
Power supply voltage fall time	t <sub>fVD</sub>		200			μs
Power supply voltage hold time (from STOP mode setting)	t <sub>hVD</sub>		0			ms
STOP release signal input time	t <sub>dREL</sub>		0			ns
Data hold high-level input voltage	V <sub>IHDR</sub>	<b>Note</b>	0.8V <sub>DDDR</sub>		V <sub>DDDR</sub>	V
Data hold low-level input voltage	V <sub>ILDR</sub>	<b>Note</b>	-0.5		0.2V <sub>DDDR</sub>	V

**Note** P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

**Remark** The TYP. value is a reference value for when T<sub>A</sub> = 25°C.

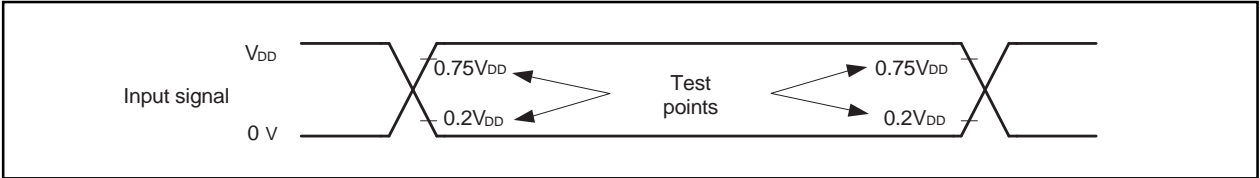


**AC Characteristics**

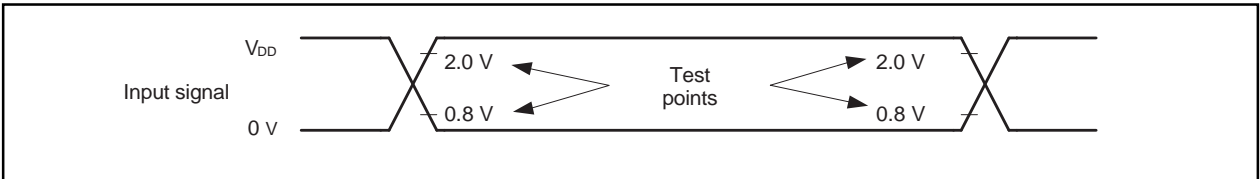
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , output pin load capacitance:  $C_L = 50\text{ pF}$ )

**AC test input waveform**

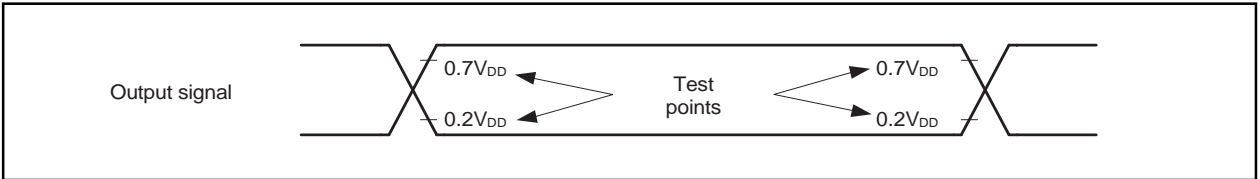
- (a) P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031



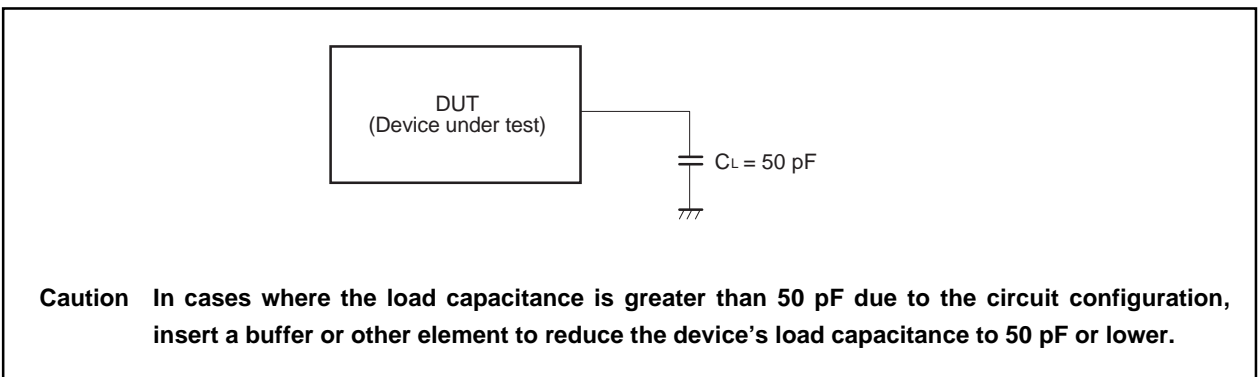
- (b) Other than (a) above



**AC test output test points**



**Load condition**



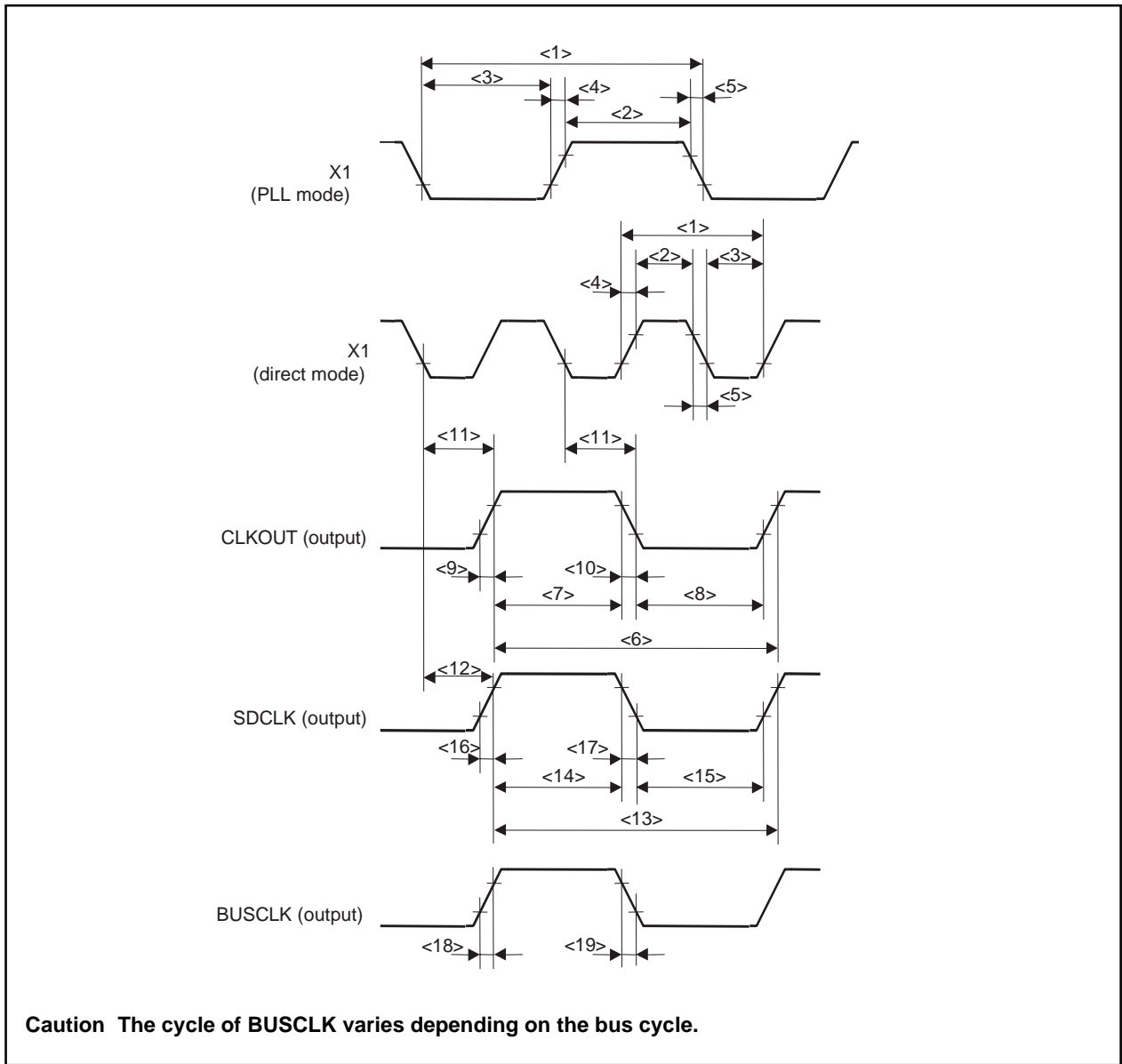
(1) Clock timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	<1>	t <sub>CYX</sub>	Direct mode	20	125	ns
			PLL mode	200	250	ns
X1 input high-level width	<2>	t <sub>WXH</sub>	Direct mode	5		ns
			PLL mode	50		ns
X1 input low-level width	<3>	t <sub>WXL</sub>	Direct mode	5		ns
			PLL mode	50		ns
X1 input rise time	<4>	t <sub>XR</sub>	Direct mode		4	ns
			PLL mode		10	ns
X1 input fall time	<5>	t <sub>XF</sub>	Direct mode		4	ns
			PLL mode		10	ns
CPU operation frequency	–	φ		4	50	MHz
CLKOUT output cycle	<6>	t <sub>CYK1</sub>		20	250	ns
CLKOUT high-level width	<7>	t <sub>WKH1</sub>		0.5T – 5		ns
CLKOUT low-level width	<8>	t <sub>WKL1</sub>		0.5T – 6		ns
CLKOUT rise time	<9>	t <sub>KR1</sub>			5	ns
CLKOUT fall time	<10>	t <sub>KF1</sub>			4	ns
Delay time from X1↓ to CLKOUT	<11>	t <sub>DKX</sub>			40	ns
Delay time from X1↓ to SDCLK	<12>	t <sub>DSX</sub>			40	ns
SDCLK output cycle	<13>	t <sub>CYK2</sub>		20	250	ns
SDCLK high-level width	<14>	t <sub>WKH2</sub>		0.5T – 5		ns
SDCLK low-level width	<15>	t <sub>WKL2</sub>		0.5T – 6		ns
SDCLK rise time	<16>	t <sub>KR2</sub>			5	ns
SDCLK fall time	<17>	t <sub>KF2</sub>			4	ns
BUSCLK rise time	<18>	t <sub>KR3</sub>			5	ns
BUSCLK fall time	<19>	t <sub>KF3</sub>			4	ns

Remarks 1. T = t<sub>CYK</sub>

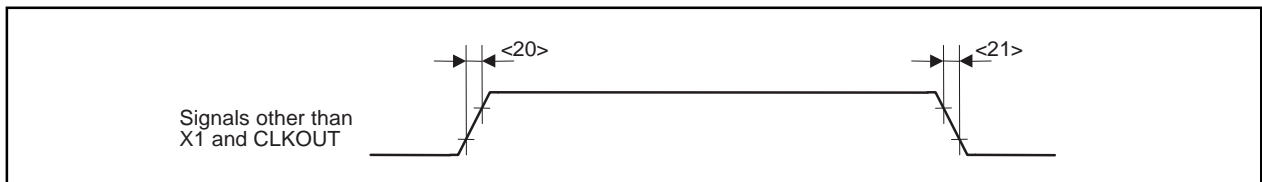
2. The phase difference between CLKOUT and SDCLK, and between CLKOUT and BUSCLK cannot be defined.

(1) Clock timing (2/2)



(2) Output waveform (except for X1 and CLKOUT)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	<20>	tor		5	ns
Output fall time	<21>	tof		4	ns

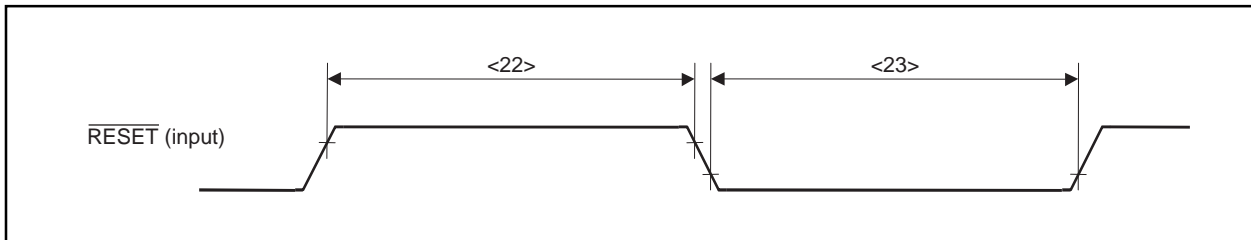


(3) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ pin high-level width	<22>	tWRSH		500		ns
$\overline{\text{RESET}}$ pin low-level width	<23>	tWRSL	At power-on and at STOP mode release	500 + T <sub>os</sub>		ns
			Except at power-on and at STOP mode release	500		ns

**Caution** Thoroughly evaluate the oscillation stabilization time.

**Remark** T<sub>os</sub>: Oscillation stabilization time





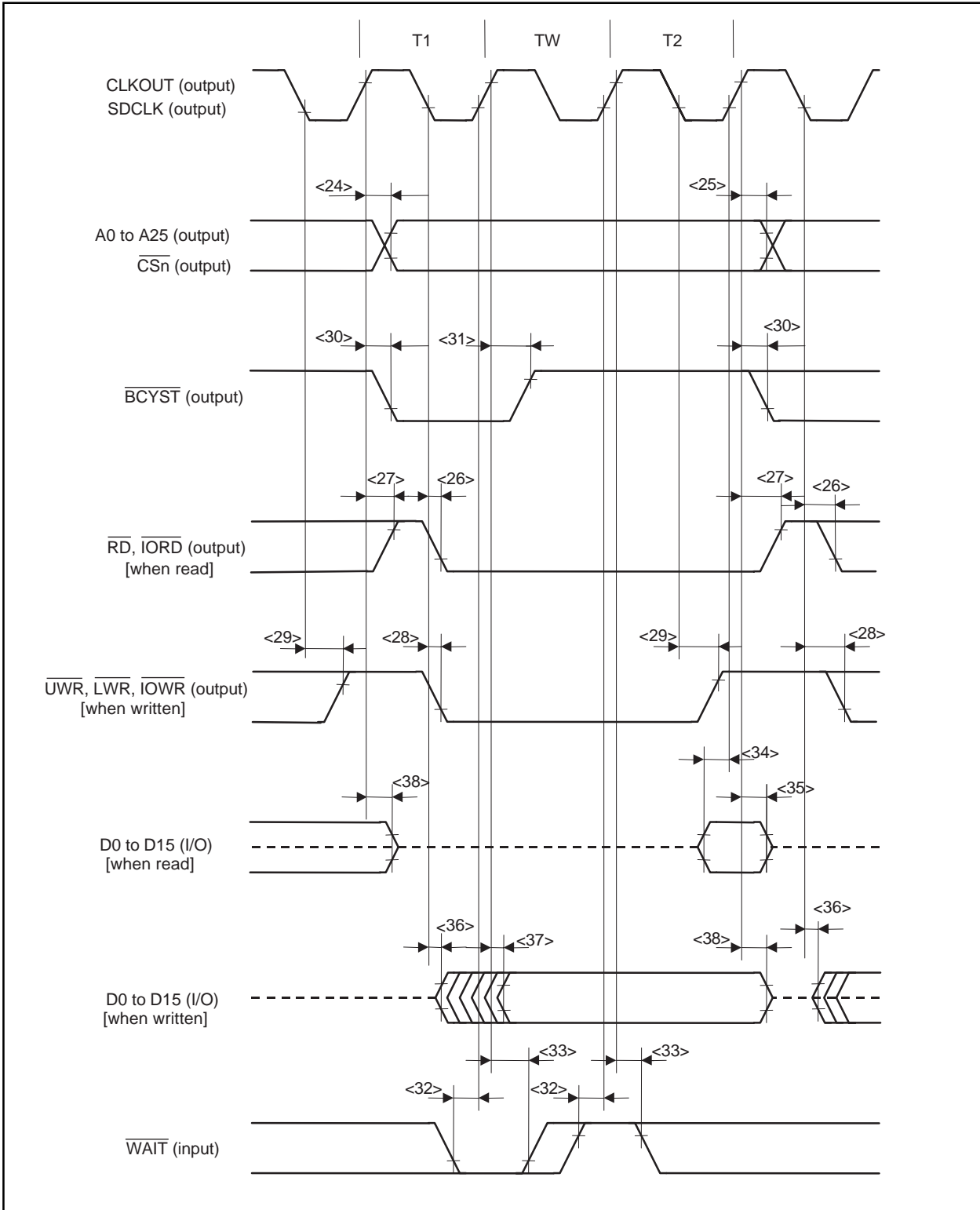
(4) SRAM, external ROM, and external I/O access timing

(a) Access timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address, $\overline{CS}_n$ output delay time (from CLKOUT↑)	<24> tDKA		2	13	ns
Address, $\overline{CS}_n$ output delay time (from SDCLK↑)			0	13	ns
Address, $\overline{CS}_n$ output hold time (from CLKOUT↑)	<25> tHKA		2	13	ns
Address, $\overline{CS}_n$ output hold time (from SDCLK↑)			0	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from CLKOUT↓)	<26> tDKRDL		2	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from SDCLK↓)			0	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from CLKOUT↑)	<27> tHKRDH		2	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from SDCLK↑)			0	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from CLKOUT↓)	<28> tDKWRL		2	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from SDCLK↓)			0	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from CLKOUT↓)	<29> tHKWRH		2	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from SDCLK↓)			0	13	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT↑)	<30> tDKBSL		2	13	ns
$\overline{BCYST}$ ↓ delay time (from SDCLK↑)			0	13	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT↑)	<31> tHKBSH		2	13	ns
$\overline{BCYST}$ ↑ delay time (from SDCLK↑)			0	13	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32> tSWK		8		ns
$\overline{WAIT}$ setup time (to SDCLK↑)			10		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33> tHKW		2		ns
$\overline{WAIT}$ hold time (from SDCLK↑)			2		ns
Data input setup time (to CLKOUT↑)	<34> tSKID		8		ns
Data input setup time (to SDCLK↑)			10		ns
Data input hold time (from CLKOUT↑)	<35> tHKID		2		ns
Data input hold time (from SDCLK↑)			2		ns
Data output delay time (from CLKOUT↓)	<36> tDKOD1		2	13	ns
Data output delay time (from SDCLK↓)			0	13	ns
Data output delay time (from CLKOUT↑)	<37> tDKOD2		2	13	ns
Data output delay time (from SDCLK↑)			0	13	ns
Data float delay time (from CLKOUT↑)	<38> tHKOD		2	13	ns
Data float delay time (from SDCLK↑)			0	13	ns

- Remarks**
1. Maintain at least one of the data input hold times, tHRDID or tHKID.
  2. n = 0 to 7

(a) Access timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits based on the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3. n = 0 to 7

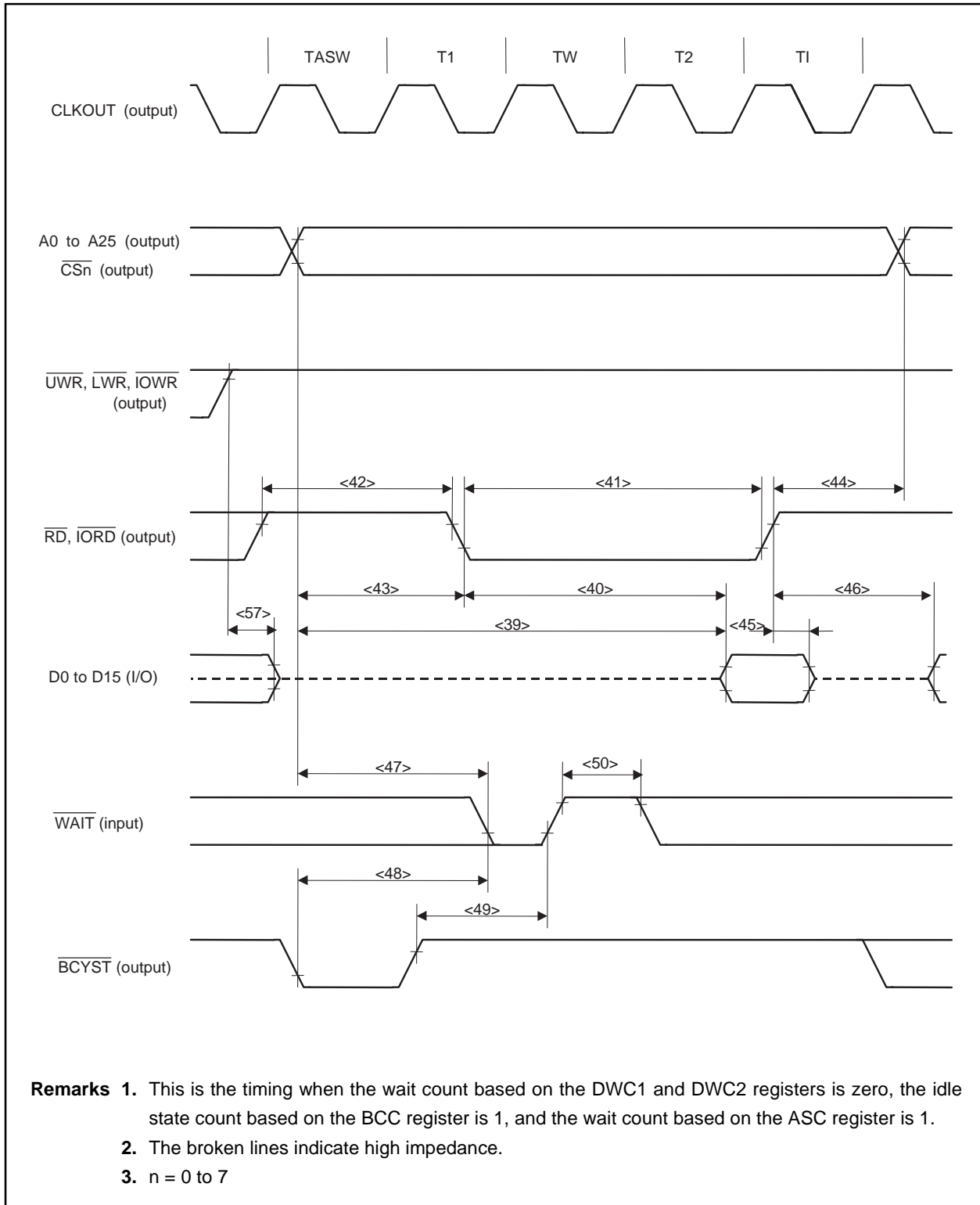
(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to address)	<39>	t <sub>SAID</sub>		$(2 + w + w_D + w_{AS})T - 21$	ns
Data input setup time (to $\overline{RD}$ )	<40>	t <sub>SRDID</sub>		$(1.5 + w + w_D)T - 21$	ns
$\overline{RD}$ , $\overline{IORD}$ low-level width	<41>	t <sub>WRDL</sub>	$(1.5 + w + w_D)T - 10$		ns
$\overline{RD}$ , $\overline{IORD}$ high-level width	<42>	t <sub>WRDH</sub>	$(0.5 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{CS}_n$ , to $\overline{RD}$ , $\overline{IORD}$ ↓	<43>	t <sub>DARD</sub>	$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{RD}$ , $\overline{IORD}$ ↑ to address	<44>	t <sub>DRDA</sub>	iT		ns
Data input hold time (from $\overline{RD}$ , $\overline{IORD}$ ↑)	<45>	t <sub>HRDID</sub>	0		ns
Delay time from $\overline{RD}$ , $\overline{IORD}$ ↑ to data output	<46>	t <sub>DRDOD</sub>	$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<47>	t <sub>SAW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<48>	t <sub>SBSW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<49>	t <sub>HBSW</sub>	<b>Note</b>	T - 10	ns
$\overline{WAIT}$ high-level width	<50>	t <sub>WWH</sub>		T - 10	ns
Data output hold time (from $\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑)	<57>	t <sub>HWRDOD</sub>		$(0.5 + i)T - 8$	ns

**Note** For the first  $\overline{WAIT}$  sampling when the wait count based on the DWC1 and DWC2 registers is zero.

- Remarks**
1. T = t<sub>cyk</sub>
  2. w: Wait count based on  $\overline{WAIT}$
  3. w<sub>D</sub>: Wait count based on the DWC1 and DWC2 registers
  4. Maintain at least one of the data input hold times t<sub>HRDID</sub> or t<sub>HKID</sub>
  5. n = 0 to 7
  6. i: Idle state count
  7. w<sub>AS</sub>: Address setup wait count based on the ASC register

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



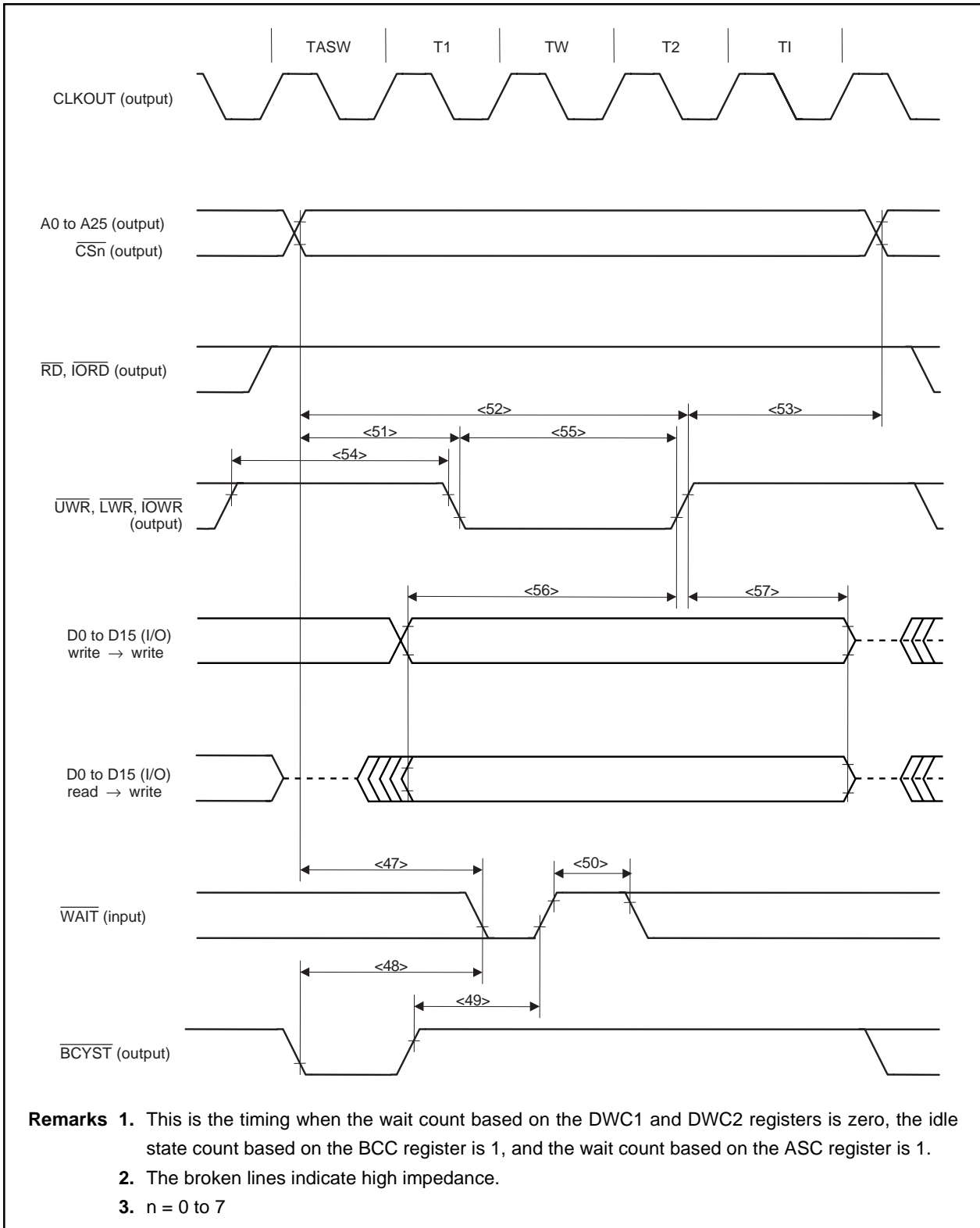
(c) Write timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{SBSW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.5 + w_{\text{AS}})T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.5 + w + w_{\text{D}} + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(0.5 + i)T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(0.5 + i + w_{\text{AS}})T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ low-level width	<55> $t_{\text{WURL}}$		$(1 + w + w_{\text{D}})T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<56> $t_{\text{SODW}}$ R		$(0.5 + w_{\text{AS}} + w + w_{\text{D}})T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<57> $t_{\text{HWRO}}$ D		$(0.5 + i)T - 8$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the wait count based on the DWC1 and DWC2 registers is zero.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_{\text{D}}$ : Wait count based on the DWC1 and DWC2 registers
  4.  $n = 0$  to 7
  5.  $i$ : Idle state count
  6.  $w_{\text{AS}}$ : Address setup wait count based on the ASC register

(c) Write timing (SRAM, external ROM, external I/O) (2/2)



(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> $t_{\text{SWK}}$		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> $t_{\text{HKW}}$		0		ns
$\overline{\text{RD}}$ low-level width	<41> $t_{\text{WRDL}}$		$(1.5 + w + w_D)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<42> $t_{\text{WRDH}}$		$(0.5 + w_{\text{AS}} + i)T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{RD}}\downarrow$	<43> $t_{\text{DARD}}$		$(0.5 + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{RD}}\uparrow$ to address	<44> $t_{\text{DRDA}}$		$iT$		ns
Delay time from $\overline{\text{RD}}\uparrow$ to data output	<46> $t_{\text{DRDOD}}$		$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{BSW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address to $\overline{\text{IOWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.5 + w_{\text{AS}})T - 10$		ns
Address setup time (to $\overline{\text{IOWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.5 + w + w_D + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(1.5 + i)T - 10$		ns
$\overline{\text{IOWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(0.5 + i + w_{\text{AS}})T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<55> $t_{\text{WRRL}}$		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{RD}}\uparrow$	<58> $t_{\text{DIWRRD}}$		$1.5T - 10$		ns
Delay time from $\overline{\text{DMAAKm}}\downarrow$ to $\overline{\text{IOWR}}\downarrow$	<59> $t_{\text{DDAWR}}$		$(0.5 + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{DMAAKm}}\uparrow$	<60> $t_{\text{DWRDA}}$		$(1.5 + i)T - 10$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the number of waits based on the DWC1 and DWC2 registers is zero.

**Remarks 1.**  $T = t_{\text{CYK}}$

**2.**  $w$ : Wait count based on  $\overline{\text{WAIT}}$

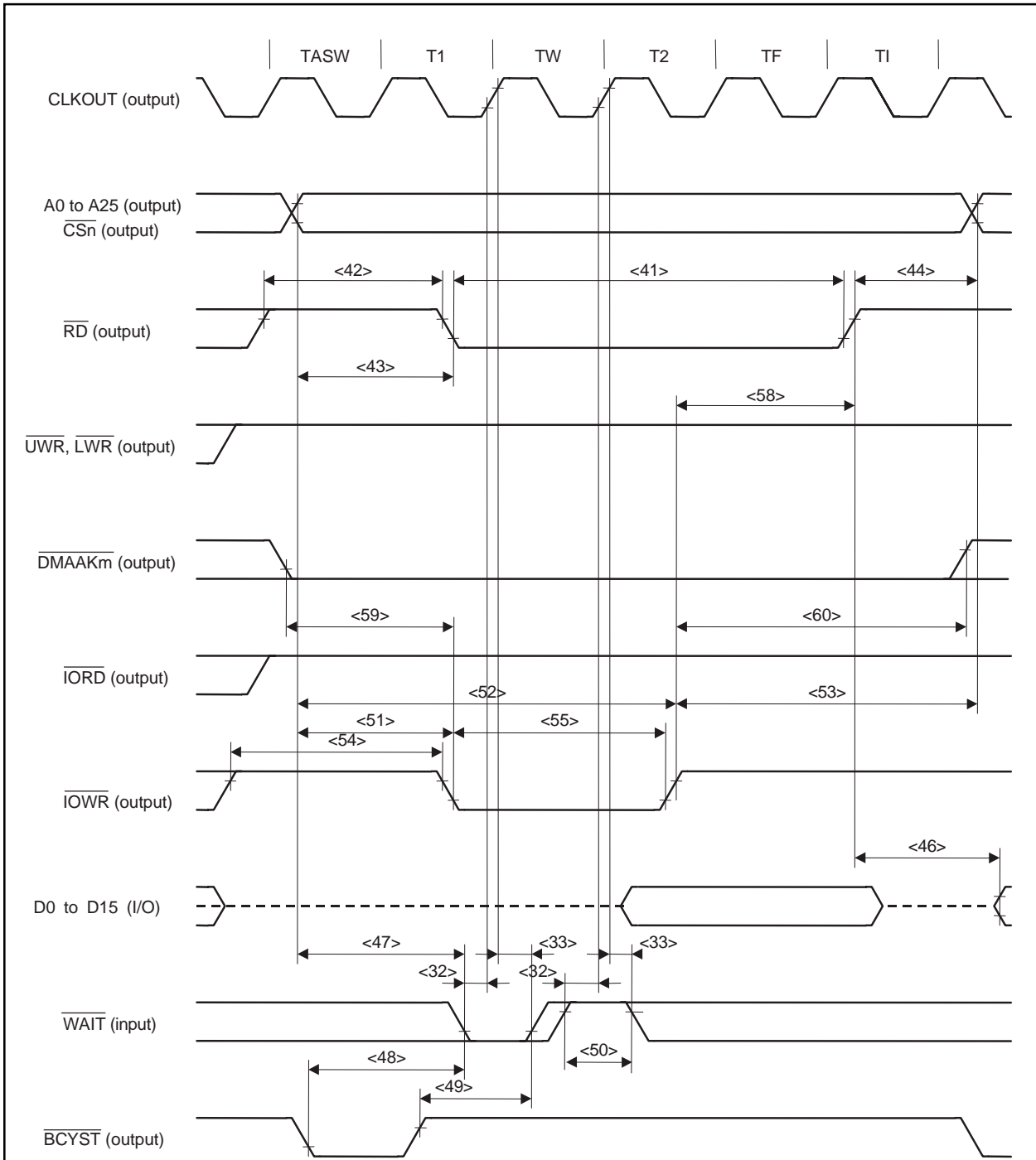
**3.**  $w_D$ : Wait count based on the DWC1 and DWC2 registers

**4.**  $n = 0$  to 7,  $m = 0$  to 3

**5.**  $i$ : Idle state count

**6.**  $w_{\text{AS}}$ : Address setup wait count based on the ASC register

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



- Remarks**
1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.
  2. The broken lines indicate high impedance.
  3.  $n = 0$  to 7,  $m = 0$  to 3



(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> $t_{\text{SWK}}$		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> $t_{\text{HKW}}$		0		ns
$\overline{\text{IORD}}$ low-level width	<41> $t_{\text{WRDL}}$		$(2 + w + w_D)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<42> $t_{\text{WRDH}}$		$(1 + i + w_{AS})T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{IORD}}\downarrow$	<43> $t_{\text{DARD}}$		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to address	<44> $t_{\text{DRDA}}$		$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to data output	<46> $t_{\text{DRDOD}}$		$(1 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{SBSW}}$	<b>Note</b>		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address to $\overline{\text{UWR}}, \overline{\text{LWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(0.5 + i)T - 10$		ns
$\overline{\text{UWR}}, \overline{\text{LWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{\text{UWR}}, \overline{\text{LWR}}$ low-level width	<55> $t_{\text{WWRL}}$		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ to $\overline{\text{IORD}}\uparrow$	<61> $t_{\text{WRIRD}}$		$T - 10$		ns
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{IORD}}\downarrow$	<62> $t_{\text{DDARD}}$		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to $\overline{\text{DMAAK}}_m\uparrow$	<63> $t_{\text{DRDDA}}$		$(0.5 + i)T - 10$		ns

**Note** For first  $\overline{\text{WAIT}}$  sampling when wait count based on the DWC1 and DWC2 registers is zero.

**Remarks** 1.  $T = t_{\text{CYK}}$

2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$

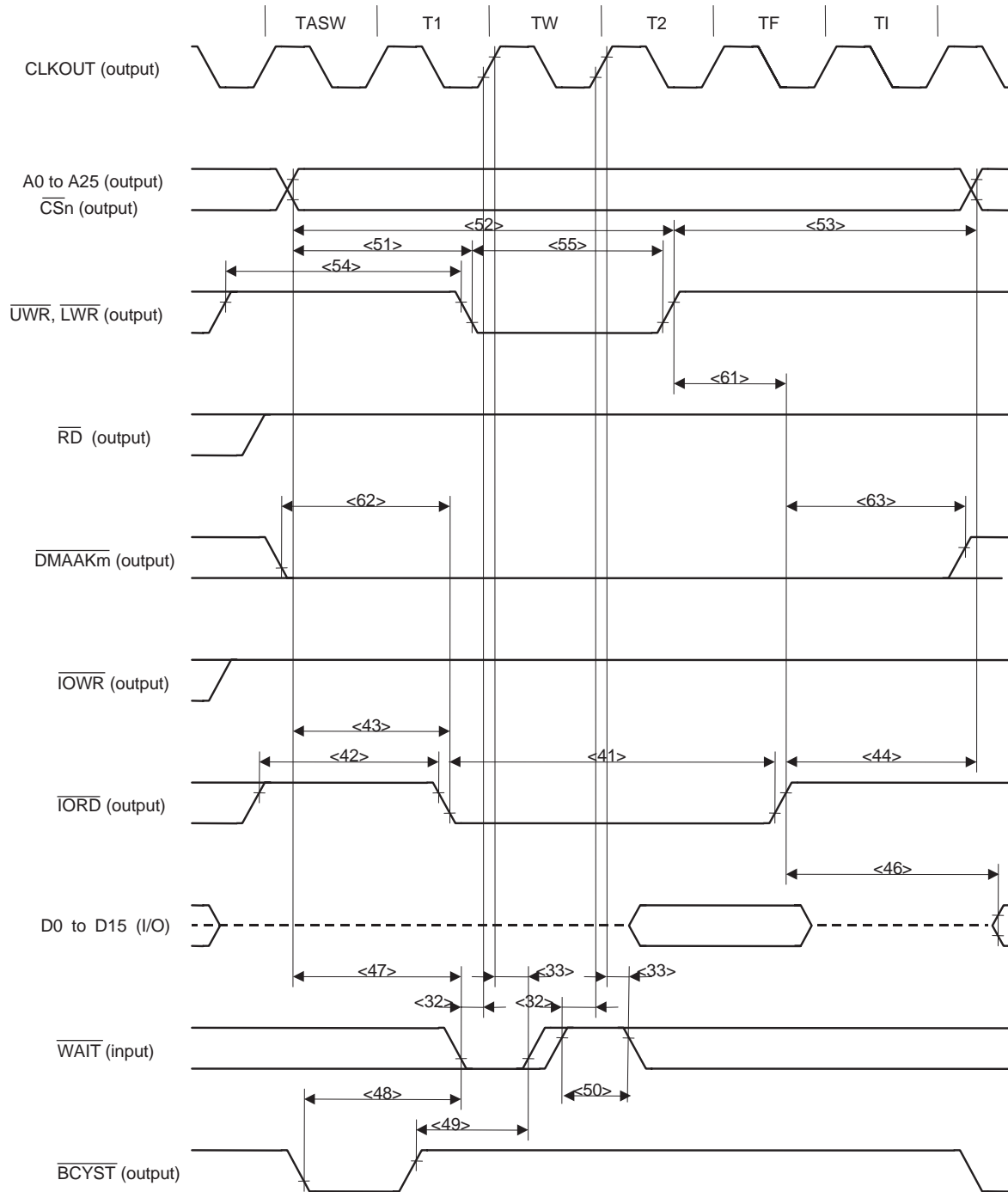
3.  $w_D$ : Wait count based on the DWC1 and DWC2 registers

4.  $n = 0$  to 7,  $m = 0$  to 3

5.  $i$ : Count of idle states inserted when a write cycle follows a read cycle

6.  $w_{AS}$ : Address setup wait count based on the ASC register

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



- Remarks**
1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.
  2. The broken lines indicate high impedance.
  3.  $n = 0$  to 7,  $m = 0$  to 3

(5) Page ROM access timing

(a) 8-bit bus width (halfword/word access), 16-bit bus width (word access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> t <sub>SWK</sub>		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> t <sub>HKW</sub>		0		ns
Data input setup time (to CLKOUT↑)	<34> t <sub>SKID</sub>		8		ns
Data input hold time (from CLKOUT↑)	<35> t <sub>HKID</sub>		0		ns
Off-page data input setup time (to address)	<39> t <sub>SAID</sub>			$(2 + w + w_D + w_{AS})T - 21$	ns
Off-page data input setup time (to $\overline{\text{RD}}$ )	<40> t <sub>SRDID</sub>			$(1.5 + w + w_D)T - 21$	ns
Data input hold time (from $\overline{\text{RD}}$ ↑)	<45> t <sub>HRDID</sub>		0		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<46> t <sub>DRDOD</sub>		$(0.5 + i)T - 10$		ns
On-page data input setup time (to address)	<64> t <sub>SOAID</sub>			$(2 + w + w_{PR} + w_{AS})T - 21$	ns

Remarks 1. T = t<sub>CYK</sub>

2. w: Wait count based on  $\overline{\text{WAIT}}$

3. w<sub>D</sub>: Wait count based on the DWC1 and DWC2 registers

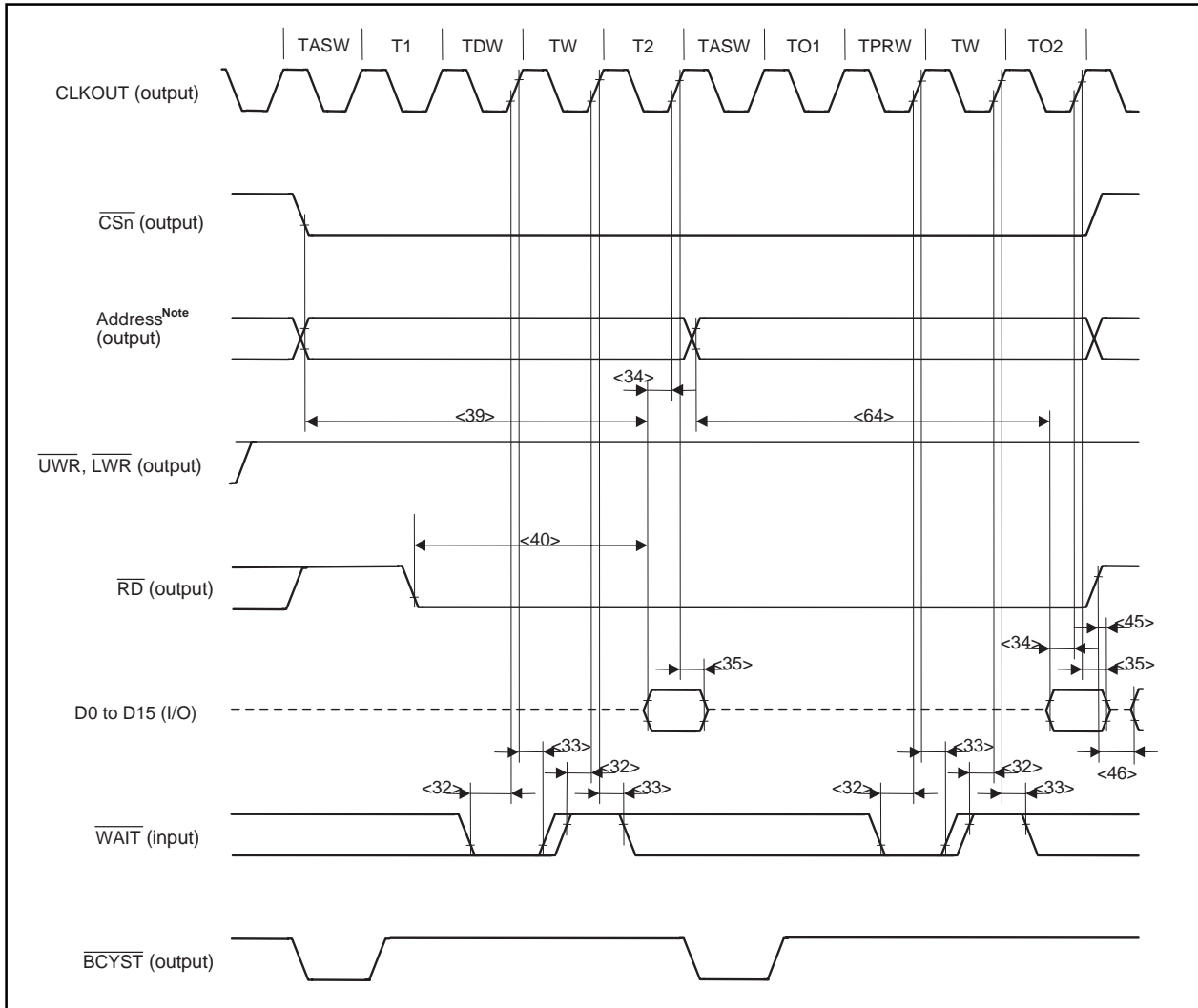
4. w<sub>PR</sub>: Wait count based on the PRC register

5. i: Count of idle states inserted when a write cycle follows a read cycle

6. w<sub>AS</sub>: Address setup wait count based on the ASC register

7. Maintain at least one of the data input hold times t<sub>HKID</sub> or t<sub>HRDID</sub>

(a) 8-bit bus width (halfword/word access), 16-bit bus width (word access) (2/2)



**Note** On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

- Remarks**
- This is the timing for the following case.  
 Wait count based on the DWC1 and DWC2 registers (TDW): 1  
 Wait count based on the PRC register (TPRW): 1  
 Wait count based on the ASC register (TASW): 1
  - The broken lines indicate high impedance.
  - n = 0 to 7

**(b) 8-bit bus width (byte access), 16-bit bus width (byte/halfword access) (1/2)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> t <sub>SWK</sub>		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> t <sub>HKW</sub>		0		ns
Data input setup time (to CLKOUT↑)	<34> t <sub>SKID</sub>		8		ns
Data input hold time (from CLKOUT↑)	<35> t <sub>HKID</sub>		0		ns
Off-page data input setup time (to address)	<39> t <sub>SAID</sub>			$(2 + w + w_d + w_{AS})T - 21$	ns
Off-page data input setup time (to $\overline{\text{RD}}$ )	<40> t <sub>SRDID</sub>			$(1.5 + w + w_d)T - 21$	ns
Off-page $\overline{\text{RD}}$ low-level width	<171> t <sub>WRDL</sub>		$(1.5 + w + w_d)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<172> t <sub>WRDH</sub>		$(0.5 + w_{AS})T - 10$		ns
Data input hold time (from $\overline{\text{RD}}$ ↑)	<45> t <sub>HRDID</sub>		0		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<46> t <sub>DRDOD</sub>		$(0.5 + i)T - 10$		ns
On-page $\overline{\text{RD}}$ low-level width	<173> t <sub>WORDL</sub>		$(1.5 + w + w_{PR})T - 10$		ns
On-page data input setup time (to address)	<64> t <sub>SOAID</sub>			$(2 + w + w_{PR} + w_{AS})T - 21$	ns
On-page data input setup time (to $\overline{\text{RD}}$ )	<174> t <sub>SORDID</sub>			$(1.5 + w + w_{PR})T - 21$	ns

**Remarks 1.** T = t<sub>CYK</sub>

**2.** w: Wait count based on  $\overline{\text{WAIT}}$

**3.** w<sub>d</sub>: Wait count based on the DWC1 and DWC2 registers

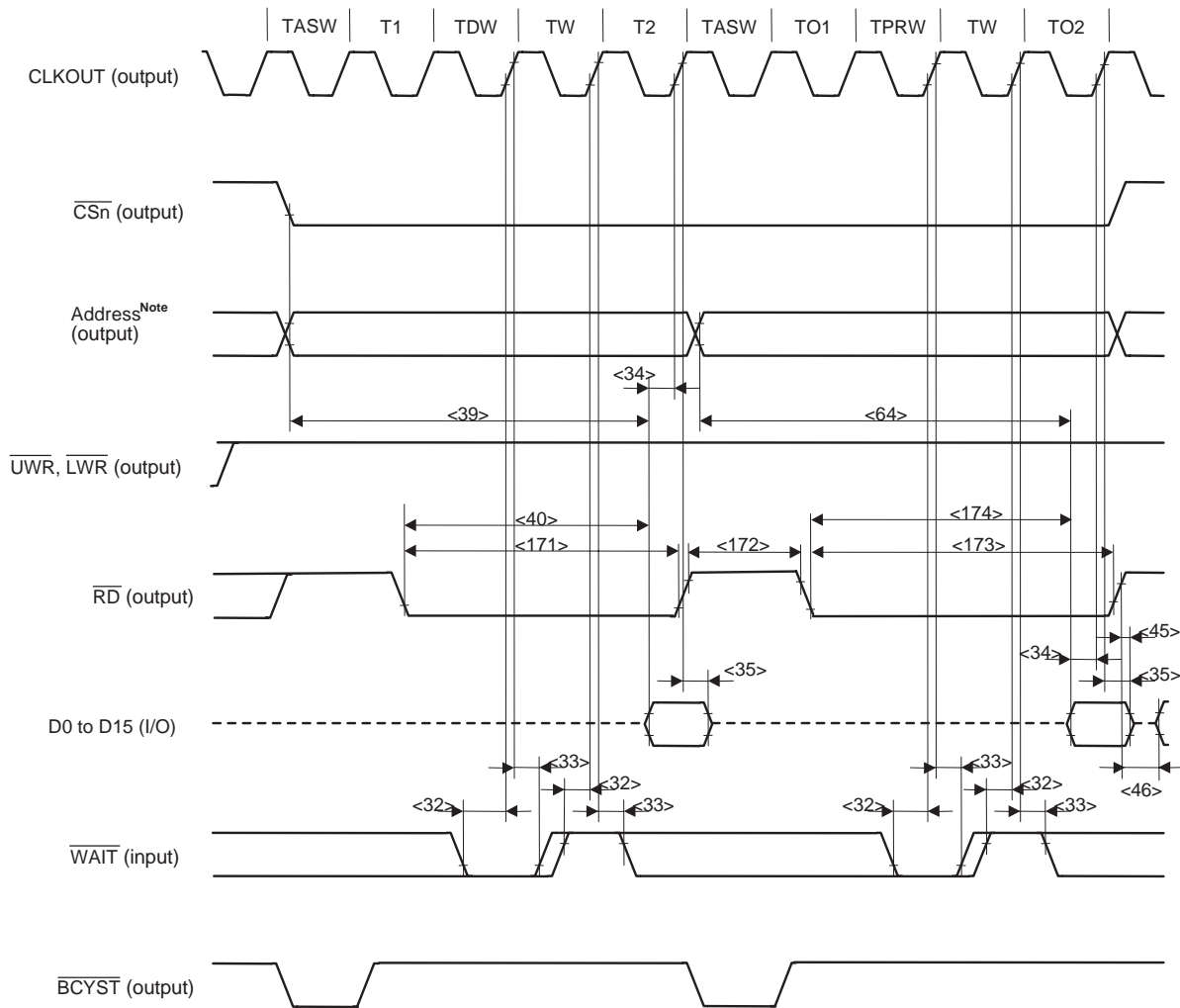
**4.** w<sub>PR</sub>: Wait count based on the PRC register

**5.** i: Count of idle states inserted when a write cycle follows a read cycle

**6.** w<sub>AS</sub>: Address setup wait count based on the ASC register

**7.** Maintain at least one of the data input hold times t<sub>HKID</sub> or t<sub>HRDID</sub>

(b) 8-bit bus width (byte access), 16-bit bus width (byte/halfword access) (2/2)



**Note** On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

- Remarks**
- This is the timing for the following case.  
 Wait count based on the DWC1 and DWC2 registers (TDW): 1  
 Wait count based on the PRC register (TPRW): 1  
 Wait count based on the ASC register (TASW): 1
  - The broken lines indicate high impedance.
  - n = 0 to 7

(6) DRAM access timing

(a) Read timing (EDO DRAM) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
Data input setup time (to CLKOUT↓)	<34>	t <sub>SKID</sub>	8		ns	
Data input hold time (from CLKOUT↓)	<35>	t <sub>HKID</sub>	0		ns	
Delay time from $\overline{OE}\uparrow$ to data output	<46>	t <sub>DRDOD</sub>	$(1 + i)T - 10$		ns	
Read/write cycle time	<65>	t <sub>HPC</sub>	$(1 + W_{DA} + W_{CP})T - 10$		ns	
Row address setup time	<66>	t <sub>ASR</sub>	$0.5T - 10$		ns	
Row address hold time	<67>	t <sub>RAH</sub>	$(0.5 + W_{RH})T - 10$		ns	
Column address setup time	<68>	t <sub>ASC</sub>	$0.5T - 10$		ns	
Column address hold time	<69>	t <sub>CAH</sub>	$(0.5 + W_{DA})T - 10$		ns	
$\overline{RAS}$ precharge time	<70>	t <sub>RP</sub>	W <sub>RP</sub> = 0	$T - 10$	ns	
			W <sub>RP</sub> ≥ 1	$W_{RP}T - 10$	ns	
Column address read time (from $\overline{RAS}\uparrow$ )	<71>	t <sub>RAL</sub>	$(1.5 + W_{CP} + W_{DA})T - 10$		ns	
$\overline{CAS}$ hold time	<72>	t <sub>CSH</sub>	$(1.5 + W_{RH} + W_{DA})T - 10$		ns	
Delay time from $\overline{RAS}$ to column address	<73>	t <sub>RAD</sub>	$(0.5 + W_{RH})T - 10$		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	<74>	t <sub>RCD</sub>	$(1 + W_{RH})T - 10$		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	<75>	t <sub>CRP</sub>	W <sub>RP</sub> = 0	$1.5T - 10$	ns	
			W <sub>RP</sub> ≥ 1	$(0.5 + W_{RP})T - 10$	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	<76>	t <sub>RHCP</sub>	$(1.5 + W_{CP} + W_{DA})T - 10$		ns	
$\overline{WE}$ setup time (to $\overline{CAS}\downarrow$ )	<77>	t <sub>RCS</sub>	W <sub>RP</sub> = 0	$(3 + W_{RH})T - 10$	ns	
			W <sub>RP</sub> ≥ 1	$(2 + W_{RP} + W_{RH})T - 10$	ns	
$\overline{WE}$ hold time (from $\overline{RAS}\uparrow$ )	<78>	t <sub>RRH</sub>	$(1 + i)T - 10$		ns	
$\overline{WE}$ hold time (from $\overline{CAS}\uparrow$ )	<79>	t <sub>RCH</sub>	$(1.5 + i)T - 10$		ns	
RAS pulse width	Off-page	<80>	t <sub>RASP</sub>	$(2 + W_{RH} + W_{DA})T - 10$	ns	
$\overline{CAS}$ pulse width		<81>	t <sub>HCAS</sub>	$(0.5 + W_{DA})T - 10$	ns	
$\overline{CAS}$ precharge time		<82>	t <sub>CP</sub>	$(0.5 + W_{CP})T - 10$	ns	
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<83>	t <sub>CH1</sub>	W <sub>RP</sub> = 0	$(2.5 + W_{RH} + W_{DA})T - 10$	ns
				W <sub>RP</sub> ≥ 1	$(1.5 + W_{RP} + W_{RH} + W_{DA})T - 10$	ns
	On-page	<84>	t <sub>CH2</sub>	$(0.5 + W_{CP} + W_{DA})T - 10$	ns	
Access time to $\overline{CAS}$ precharge		<85>	t <sub>ACP</sub>		$(1.5 + W_{CP} + W_{DA})T - 21$	ns
Data input hold time (from $\overline{CAS}\downarrow$ )		<86>	t <sub>DHC</sub>	0	ns	
$\overline{CAS}$ access time		<87>	t <sub>CAC</sub>		$(1 + W_{DA})T - 21$	ns
Access time from column address		<88>	t <sub>AA</sub>		$(1.5 + W_{DA})T - 21$	ns

(a) Read timing (EDO DRAM) (2/3)

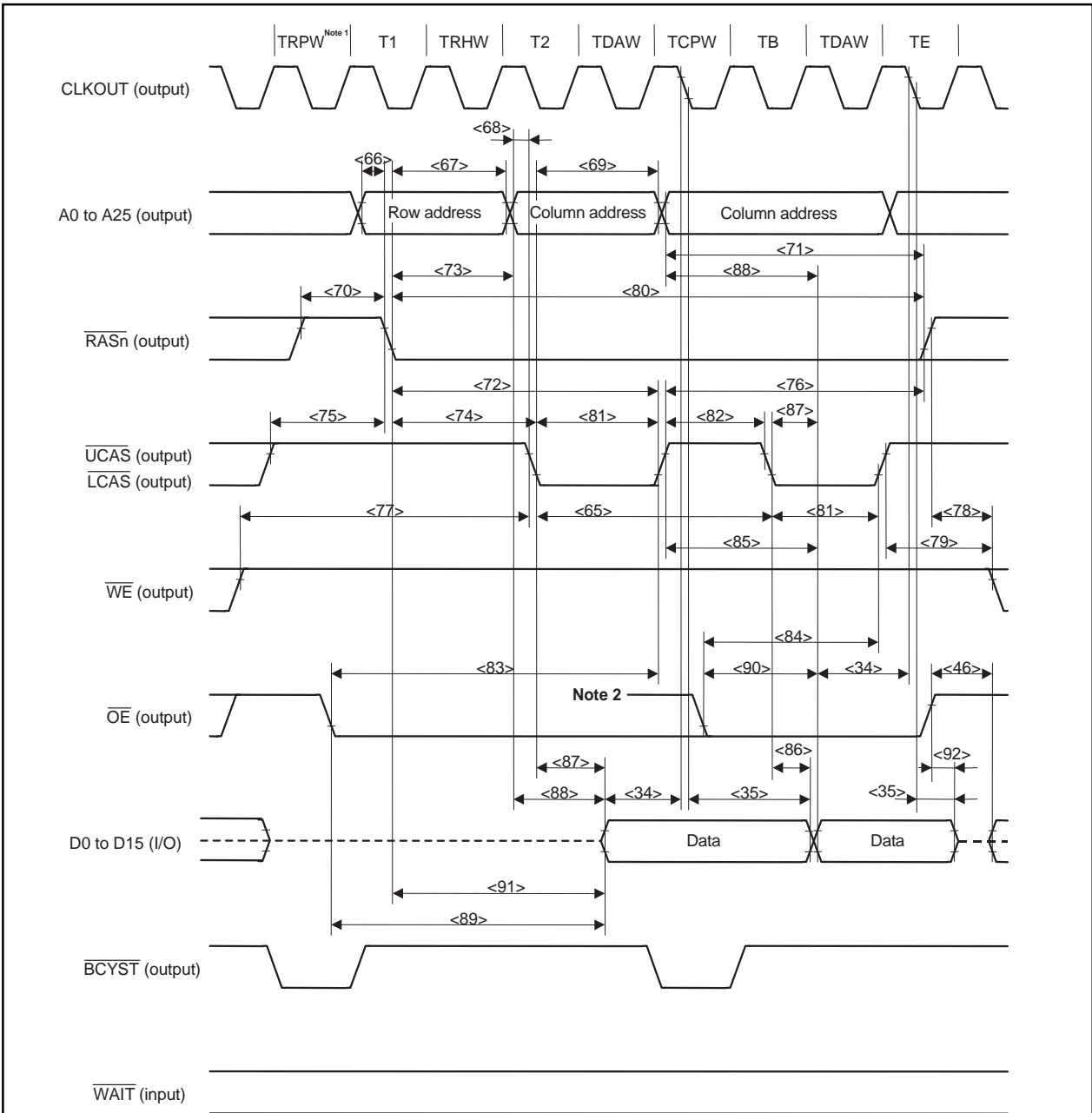
Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Output enable access time	Off-page	<89>	t <sub>OE1</sub>	WRP = 0		$(3 + WRP + WRH + WDA)T - 21$	ns
				WRP ≥ 1		$(2 + WRP + WRH + WDA)T - 21$	ns
	Off-page	<90>	t <sub>OE2</sub>			$(1 + WCP + WDA)T - 21$	ns
RAS access time		<91>	t <sub>RAC</sub>			$(2 + WRH + WDA)T - 21$	ns
Output buffer turn-off delay time (from $\overline{OE}$ )		<92>	t <sub>OEZ</sub>		0		ns

- Cautions**
1. At least one clock is inserted in  $WRP$  by default regardless of the setting of the  $RPC1n$  and  $RPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, \text{ or } 6$ )
  2. The  $\overline{WAIT}$  signal cannot be controlled using the  $\overline{BCYST}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{CYK}$
  2.  $WDA$ : Wait count based on the  $DAC1n$  and  $DAC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  3.  $WCP$ : Wait count based on the  $CPC1n$  and  $CPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  4.  $WRP$ : Wait count based on the  $RPC1n$  and  $RPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  5.  $WRH$ : Wait count based on the  $RHC1n$  and  $RHC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  6. i: Idle state counts



(a) Read timing (EDO DRAM) (3/3)



- Notes**
1. At least one clock is always inserted in TRPW cycle.
  2. During on-page access from other cycles while RAS is low level.

**Remarks 1.** This is the timing for the following case.

- Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
- Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
- Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
- Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.
3. n = 1, 3, 4, 6

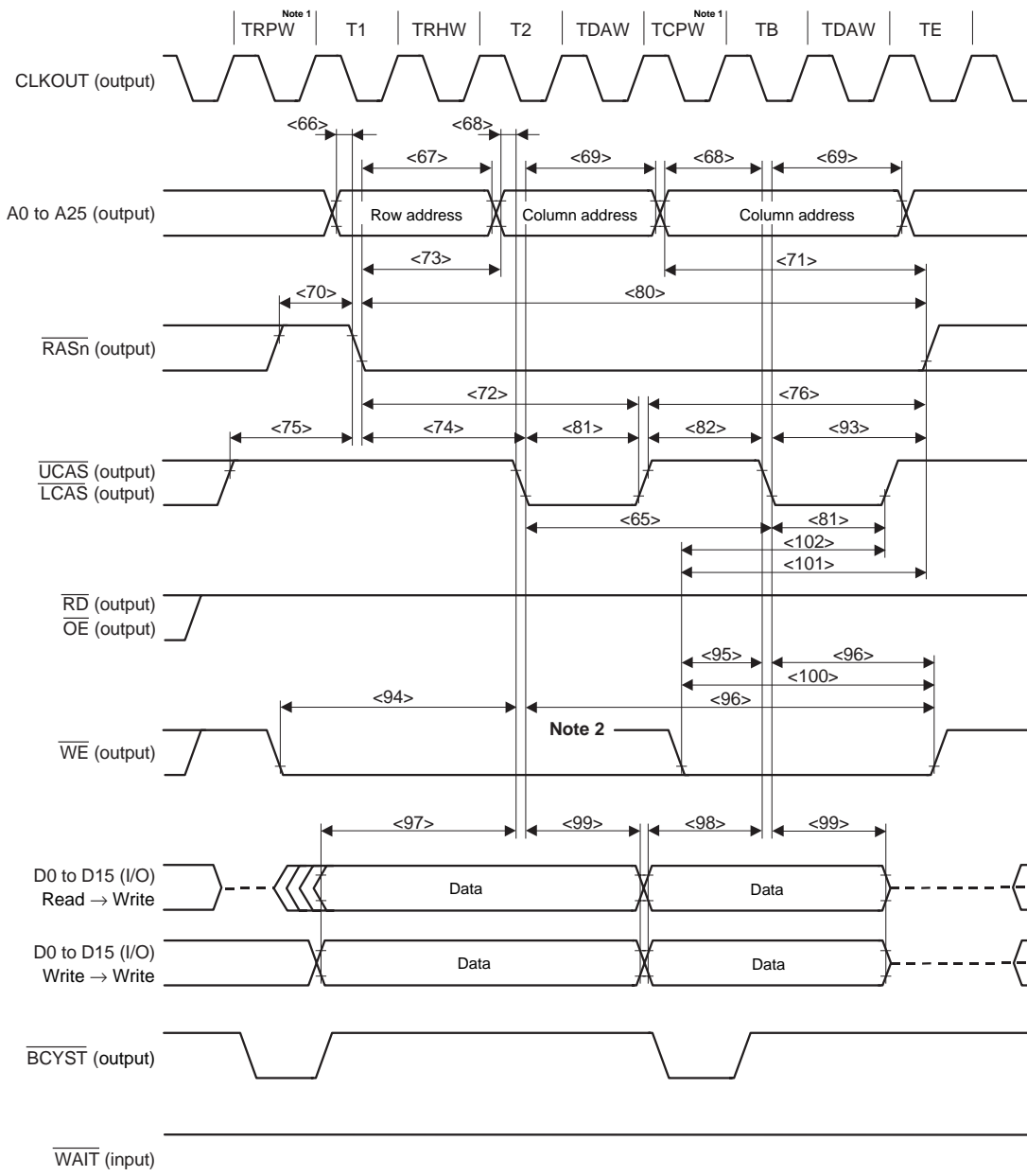
(b) Write timing (EDO DRAM) (1/2)

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Read/write cycle time		t <sub>HPC</sub>	WCP = 0	(2 + WDA)T - 10		ns
			WCP ≥ 1	(1 + WDA + WCP)T - 10		ns
Row address setup time		t <sub>ASR</sub>		0.5T - 10		ns
Row address hold time		t <sub>RAH</sub>		(0.5 + WRH)T - 10		ns
Column address setup time		t <sub>ASC</sub>		0.5T - 10		ns
Column address hold time		t <sub>CAH</sub>		(0.5 + WDA)T - 10		ns
RAS precharge time		t <sub>RP</sub>	WRP = 0	T - 10		ns
			WRP ≥ 1	WRPT - 10		ns
Column address read time (from RAS↓)		t <sub>RAL</sub>	WCP = 0	(2.5 + WDA)T - 10		ns
			WCP ≥ 1	(1.5 + WCP + WDA)T - 10		ns
CAS hold time		t <sub>CSH</sub>		(1.5 + WRH + WDA)T - 10		ns
Delay time from RAS to column address		t <sub>RAD</sub>		(0.5 + WRH)T - 10		ns
RAS to CAS delay time		t <sub>RCD</sub>		(1 + WRH)T - 10		ns
CAS to RAS precharge time		t <sub>CRP</sub>	WRP = 0	1.5T - 10		ns
			WRP ≥ 1	(0.5 + WRP)T - 10		ns
RAS hold time from CAS precharge		t <sub>RHCP</sub>	WCP = 0	(2.5 + WDA)T - 10		ns
			WCP ≥ 1	(1.5 + WCP + WDA)T - 10		ns
RAS pulse width	Off-page	<80>	t <sub>RASP</sub>	(2 + WRH + WDA)T - 10		ns
CAS pulse width		<81>	t <sub>HCAS</sub>	(0.5 + WDA)T - 10		ns
CAS precharge time		t <sub>CP</sub>	WCP = 0	1.5T - 10		ns
			WCP ≥ 1	(0.5 + WCP)T - 10		ns
RAS hold time		<93>	t <sub>RSH</sub>	(1 + WDA)T - 10		ns
WE setup time (to CAS↓)	Off-page	<94>	t <sub>WCS1</sub>	WRP = 0	(2 + WRH)T - 10	ns
				WRP ≥ 1	(1 + WRP + WRH)T - 10	ns
	On-page	<95>	t <sub>WCS2</sub>	WCP = 0	T - 10	ns
				WCP ≥ 1	WCP T - 10	ns
WE hold time (from CAS↓)		<96>	t <sub>WCH</sub>	(1 + WDA)T - 10		ns
Data setup time (to CAS↓)	Off-page	<97>	t <sub>DS1</sub>	(1.5 + WRH)T - 10		ns
	On-page	<98>	t <sub>DS2</sub>	WCP = 0	1.5T - 10	ns
WCP ≥ 1				(0.5 + WCP)T - 10	ns	
Data hold time (from CAS↓)		<99>	t <sub>DH</sub>	(0.5 + WDA)T - 10		ns
WE pulse width	On-page	<100>	t <sub>WP</sub>	WCP = 0	(2 + WDA)T - 10	ns
				WCP ≥ 1	(1 + WDA + WCP)T - 10	ns
WE read time (from RAS↑)	On-page	<101>	t <sub>RWL</sub>	WCP = 0	(2 + WDA)T - 10	ns
				WCP ≥ 1	(1 + WDA + WCP)T - 10	ns
WE read time (from CAS↑)	On-page	<102>	t <sub>CWL</sub>	WCP = 0	(1.5 + WDA)T - 10	ns
				WCP ≥ 1	(0.5 + WDA + WCP)T - 10	ns

- Cautions**
1. At least one clock is inserted in  $w_{RP}$  by default regardless of the setting of the  $RPC1n$  and  $RPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, 6$ ).
  2. At least one clock is inserted in  $w_{CP}$  by default regardless of the setting of the  $CPC1n$  and  $CPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, 6$ ).
  3. The  $\overline{WAIT}$  signal cannot be controlled using the  $\overline{BCYST}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{CYK}$
  2.  $w_{DA}$ : Wait count based on the  $DAC1n$  and  $DAC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  3.  $w_{CP}$ : Wait count based on the  $CPC1n$  and  $CPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  4.  $w_{RP}$ : Wait count based on the  $RPC1n$  and  $RPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  5.  $w_{RH}$ : Wait count based on the  $RHC1n$  and  $RHC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )

(b) Write timing (EDO DRAM) (2/2)



- Notes**
1. At least one clock is always inserted in TRPW and TCPW cycles.
  2. During on-page access from other cycles while RAS is low level.

- Remarks**
1. This is the timing for the following case.
    - Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
    - Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
    - Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
    - Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1
  2. The broken lines indicate high impedance.
  3. n = 1, 3, 4, 6

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
$\overline{\text{WAIT}}$ setup time (to $\text{CLKOUT}\uparrow$ )	<32>	t <sub>SWK</sub>	8		ns	
$\overline{\text{WAIT}}$ hold time (from $\text{CLKOUT}\uparrow$ )	<33>	t <sub>HKW</sub>	0		ns	
Delay time from $\overline{\text{OE}}\uparrow$ to data output	<46>	t <sub>DRDOD</sub>	$(1 + i)T - 10$		ns	
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<53>	t <sub>DWRA</sub>	$1.5T - 10$		ns	
$\overline{\text{IOWR}}$ low-level width	<55>	t <sub>WWRL</sub>	WRP = 0	$(3 + \text{WRH} + \text{WDA} + w)T - 10$	ns	
			WRP ≥ 1	$(2 + \text{WRP} + \text{WDA} + \text{WRH} + w)T - 10$	ns	
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{OE}}\uparrow$	<58>	t <sub>DWRRD</sub>	$T - 10$		ns	
Row address setup time	<66>	t <sub>ASR</sub>	$0.5T - 10$		ns	
Row address hold time	<67>	t <sub>RAH</sub>	$(0.5 + \text{WRH})T - 10$		ns	
Column address setup time	<68>	t <sub>ASC</sub>	$0.5T - 10$		ns	
Column address hold time	<69>	t <sub>CAH</sub>	$(2.5 + \text{WDA} + w)T - 10$		ns	
RAS precharge time	<70>	t <sub>RP</sub>	WRP = 0	$T - 10$	ns	
			WRP ≥ 1	$\text{WRP}T - 10$	ns	
Column address read time (to $\overline{\text{RAS}}$ )	<71>	t <sub>RAL</sub>	$(3.5 + \text{WCP} + \text{WDA} + w)T - 10$		ns	
$\overline{\text{CAS}}$ hold time	<72>	t <sub>CSH</sub>	$(3 + \text{WRH} + \text{WDA} + w)T - 10$		ns	
RAS to column address delay time	<73>	t <sub>RAD</sub>	$(0.5 + \text{WRH})T - 10$		ns	
RAS to $\overline{\text{CAS}}$ delay time	<74>	t <sub>RCD</sub>	$(1 + \text{WRH})T - 10$		ns	
$\overline{\text{CAS}}$ to RAS precharge time	<75>	t <sub>CRP</sub>	WRP = 0	$2T - 10$	ns	
			WRP ≥ 1	$(1 + \text{WRP})T - 10$	ns	
RAS hold time from $\overline{\text{CAS}}$ precharge	<76>	t <sub>RHCP</sub>	$(4 + \text{WCP} + \text{WDA} + w)T - 10$		ns	
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}\downarrow$ )	<77>	t <sub>RCS</sub>	WRP = 0	$(3 + \text{WRH})T - 10$	ns	
			WRP ≥ 1	$(2 + \text{WRP} + \text{WRH})T - 10$	ns	
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}\uparrow$ )	<78>	t <sub>RRH</sub>	0		ns	
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}\uparrow$ )	<79>	t <sub>RCH</sub>	$T - 10$		ns	
RAS pulse width	Off-page	<80>	t <sub>RASP</sub>	$(4 + \text{WRH} + \text{WDA} + w)T - 10$	ns	
$\overline{\text{CAS}}$ precharge time		<82>	t <sub>CP</sub>	$(1 + \text{WCP})T - 10$	ns	
$\overline{\text{OE}} \rightarrow \overline{\text{CAS}}$ hold time	Off-page	<83>	t <sub>OCH1</sub>	WRP = 0	$(4 + \text{WRH} + \text{WDA} + w)T - 10$	ns
				WRP ≥ 1	$(3 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$	ns
	On-page	<84>	t <sub>OCH2</sub>	$(2 + \text{WCP} + \text{WDA} + w)T - 10$	ns	
Output buffer turn-off delay time (from $\overline{\text{OE}}\uparrow$ )	<92>	t <sub>OEZ</sub>	0		ns	
RAS hold time	<93>	t <sub>RSH</sub>	$(3 + \text{WDA} + w)T - 10$		ns	
Read/write cycle time	<103>	t <sub>RC</sub>	WRP = 0	$(5.5 + \text{WRH} + \text{WDA} + w)T - 10$	ns	
			WRP ≥ 1	$(4.5 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$	ns	
$\overline{\text{CAS}}$ pulse width	<104>	t <sub>CAS</sub>	$(2 + \text{WDA} + w)T - 10$		ns	
$\overline{\text{CAS}}$ precharge time	<105>	t <sub>CPN</sub>	WRP = 0	$(3 + \text{WRH})T - 10$	ns	
			WRP ≥ 1	$(2 + \text{WRP} + \text{WRH})T - 10$	ns	
High-speed page mode cycle time	<106>	t <sub>PC</sub>	$(3 + \text{WCP} + \text{WDA} + w)T - 10$		ns	

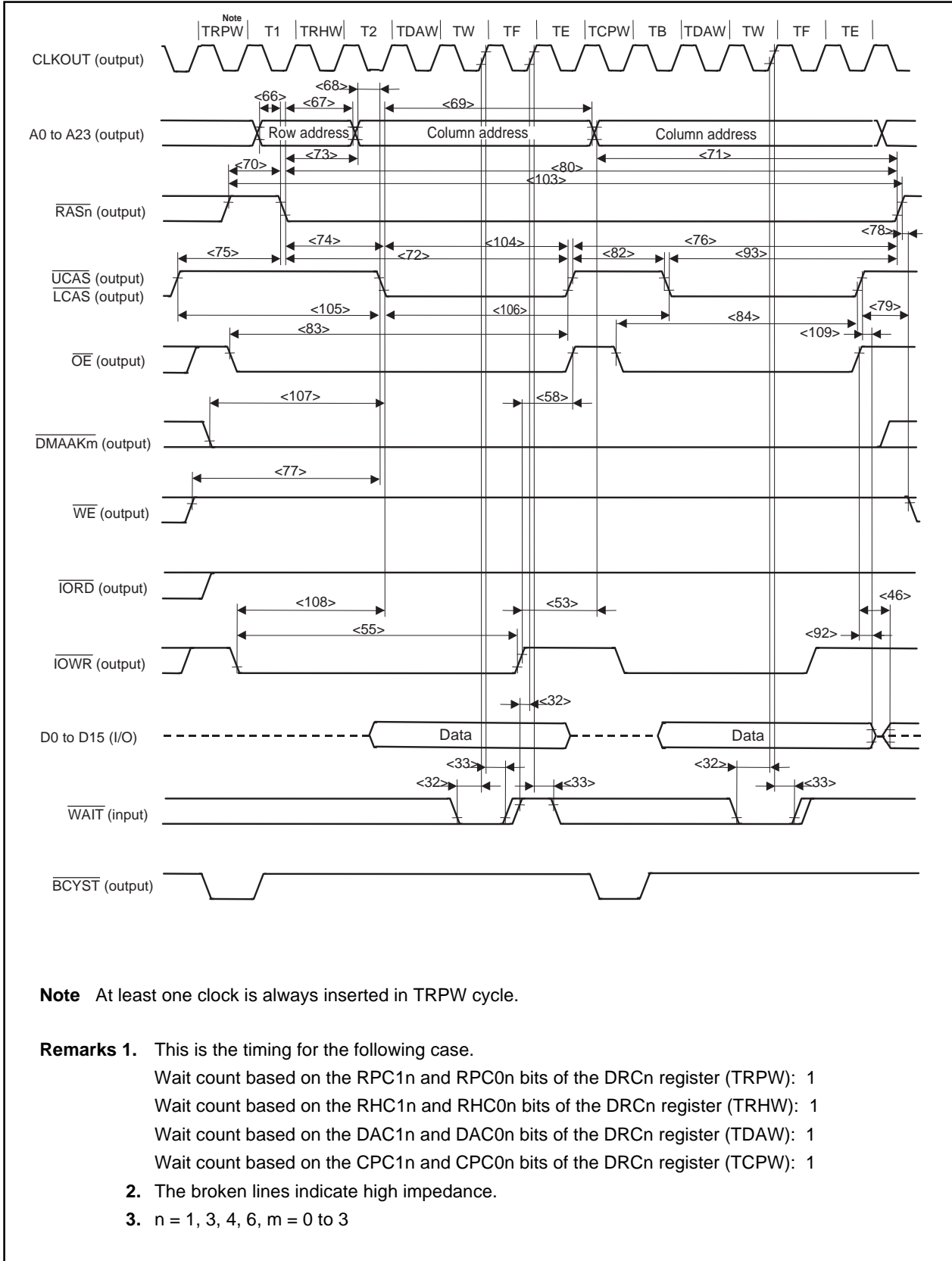
(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from $\overline{\text{DMAAK}}_m \downarrow$ to $\overline{\text{CAS}} \downarrow$	<107>	$t_{\text{DDACS}}$	$WRP = 0$	$(2.5 + WRH)T - 10$	ns
			$WRP \geq 1$	$(1.5 + WRP + WRH)T - 10$	ns
Delay time from $\overline{\text{IOWR}} \downarrow$ to $\overline{\text{CAS}} \downarrow$	<108>	$t_{\text{DRDCS}}$	$WRP = 0$	$(2 + WRH)T - 10$	ns
			$WRP \geq 1$	$(1 + WRP + WRH)T - 10$	ns
Output buffer turn-off delay time (from $\overline{\text{CAS}} \uparrow$ )	<109>	$t_{\text{OFF}}$	0		ns

- Cautions**
1. At least one clock is inserted in  $w_{RP}$  by default regardless of the setting of the  $RPC1n$  and  $RPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, 6$ ).
  2. The  $\overline{\text{WAIT}}$  signal cannot be controlled using the  $\overline{\text{BCYST}}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_{DA}$ : Wait count based on the  $DAC1n$  and  $DAC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  4.  $w_{CP}$ : Wait count based on the  $CPC1n$  and  $CPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  5.  $w_{RP}$ : Wait count based on the  $RPC1n$  and  $RPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  6.  $w_{RH}$ : Wait count based on the  $RHC1n$  and  $RHC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  7.  $i$ : Idle state count
  8.  $m = 0$  to 3

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (3/3)



**Note** At least one clock is always inserted in TRPW cycle.

**Remarks 1.** This is the timing for the following case.

- Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
- Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
- Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
- Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

**2.** The broken lines indicate high impedance.

**3.** n = 1, 3, 4, 6, m = 0 to 3

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (1/3)

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)		<32>	t <sub>SWK</sub>	8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)		<33>	t <sub>HKW</sub>	0		ns
$\overline{\text{IORD}}$ low-level width		<41>	t <sub>WRDL</sub>	$(2 + \text{WRH} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{IORD}}$ high-level width		<42>	t <sub>WRDH</sub>	$\text{T} - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to address		<44>	t <sub>DRDA</sub>	$(0.5 + i)\text{T} - 10$		ns
Row address setup time		<66>	t <sub>ASR</sub>	$0.5\text{T} - 10$		ns
Row address hold time		<67>	t <sub>RAH</sub>	$(0.5 + \text{WRH})\text{T} - 10$		ns
Column address setup time		<68>	t <sub>ASC</sub>	$0.5\text{T} - 10$		ns
Column address hold time		<69>	t <sub>CAH</sub>	$(1.5 + \text{WDA})\text{T} - 10$		ns
RAS precharge time		<70>	t <sub>RP</sub>	WRP = 0	$\text{T} - 10$	ns
				WRP ≥ 1	$\text{WRP}\text{T} - 10$	ns
Column address read time (from $\overline{\text{RAS}}$ )		<71>	t <sub>RAL</sub>	$(2.5 + \text{WCP} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ hold time		<72>	t <sub>CSH</sub>	$(2 + \text{WRH} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{RAS}}$ to column address delay time		<73>	t <sub>RAD</sub>	$(0.5 + \text{WRH})\text{T} - 10$		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time		<74>	t <sub>RCd</sub>	$(1 + \text{WRH} + \text{w})\text{T} - 10$		ns
CAS to $\overline{\text{RAS}}$ precharge time		<75>	t <sub>CRP</sub>	WRP = 0	$2\text{T} - 10$	ns
				WRP ≥ 1	$(1 + \text{WRP})\text{T} - 10$	ns
RAS hold time from $\overline{\text{CAS}}$ precharge		<76>	t <sub>RHCP</sub>	$(4 + \text{WCP} + \text{WDA} + \text{w})\text{T} - 10$		ns
RAS pulse width	Off-page	<80>	t <sub>RASP</sub>	$(3 + \text{WRH} + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{CAS}}$ precharge time		<82>	t <sub>CP</sub>	$(1 + \text{WCP} + \text{w})\text{T} - 10$		ns
RAS hold time		<93>	t <sub>RSH</sub>	$(2 + \text{WDA})\text{T} - 10$		ns
Read/write cycle time		<103>	t <sub>RC</sub>	WRP = 0	$(4.5 + \text{WRH} + \text{WDA} + \text{w})\text{T} - 10$	ns
				WRP ≥ 1	$(3.5 + \text{WRP} + \text{WRH} + \text{WDA} + \text{w})\text{T} - 10$	ns
$\overline{\text{CAS}}$ pulse width		<104>	t <sub>CAS</sub>	$(1 + \text{WDA})\text{T} - 10$		ns
CAS precharge time		<105>	t <sub>CPN</sub>	WRP = 0	$(3 + \text{WRH} + \text{w})\text{T} - 10$	ns
				WRP ≥ 1	$(2 + \text{WRP} + \text{WRH} + \text{w})\text{T} - 10$	ns
High-speed page mode cycle time		<106>	t <sub>PC</sub>	$(2 + \text{WCP} + \text{WDA} + \text{w})\text{T} - 10$		ns
Delay time from $\overline{\text{DMAAKm}}\downarrow$ to $\overline{\text{CAS}}\downarrow$		<107>	t <sub>DDACS</sub>	WRP = 0	$(2.5 + \text{WRH} + \text{w})\text{T} - 10$	ns
				WRP ≥ 1	$(1.5 + \text{WRP} + \text{WRH} + \text{w})\text{T} - 10$	ns
Delay time from $\overline{\text{IORD}}\downarrow$ to $\overline{\text{CAS}}\downarrow$		<108>	t <sub>DRDCS</sub>	WRP = 0	$(2 + \text{WRH} + \text{w})\text{T} - 10$	ns
				WRP ≥ 1	$(1 + \text{WRP} + \text{WRH} + \text{w})\text{T} - 10$	ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}}\uparrow$ )		<110>	t <sub>RWL</sub>	$(3 + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{CAS}}\uparrow$ )		<111>	t <sub>CWL</sub>	$(2 + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{WE}}$ pulse width		<112>	t <sub>WP</sub>	$(2 + \text{WDA} + \text{w})\text{T} - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}\downarrow$ )	Off-page	<113>	t <sub>WCS1</sub>	$(2 + \text{WRH} + \text{w})\text{T} - 10$		ns
	On-page	<114>	t <sub>WCS2</sub>	$\text{T} - 10$		ns



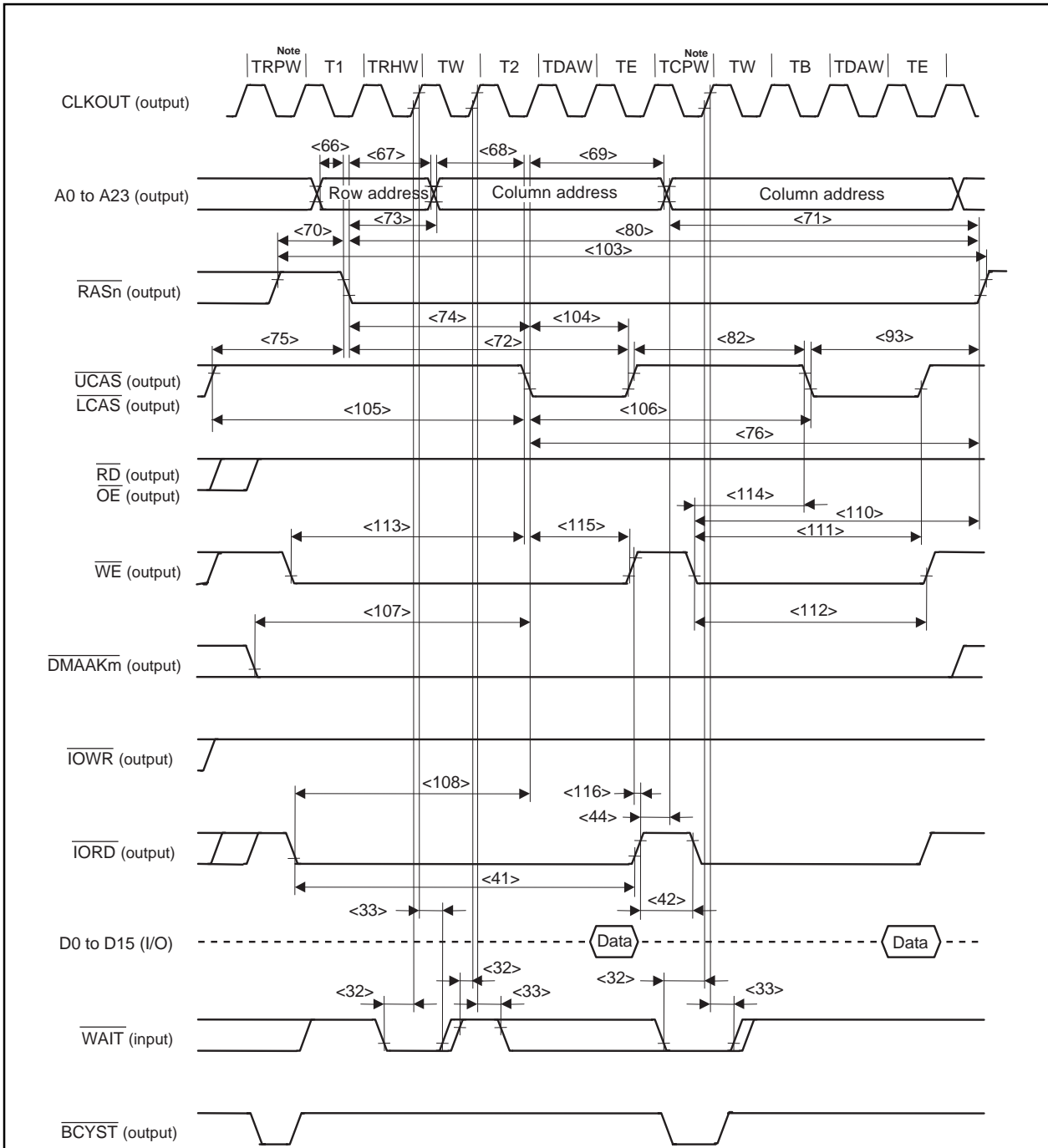
(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{WE}$ hold time (from $\overline{CAS}\downarrow$ )	<115> $t_{WCH}$		$(1 + w_{DA})T - 10$		ns
Delay time from $\overline{WE}\uparrow$ to $\overline{IORD}\uparrow$	<116> $t_{DWERD}$		0		ns

- Cautions**
1. At least one clock is inserted in  $w_{RP}$  by default regardless of the setting of the  $RPC1n$  and  $RPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, 6$ ).
  2. At least one clock is inserted in  $w_{CP}$  by default regardless of the setting of the  $CPC1n$  and  $CPC0n$  bits in the  $DRCn$  register ( $n = 1, 3, 4, 6$ ).
  3. The  $\overline{WAIT}$  signal cannot be controlled using the  $\overline{BCYST}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{CYK}$
  2.  $w$ : Wait counts based on  $\overline{WAIT}$
  3.  $w_{DA}$ : Wait count based on the  $DAC1n$  and  $DAC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  4.  $w_{CP}$ : Wait count based on the  $CPC1n$  and  $CPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  5.  $w_{RP}$ : Wait count based on the  $RPC1n$  and  $RPC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  6.  $w_{RH}$ : Wait count based on the  $RHC1n$  and  $RHC0n$  bits of the  $DRCn$  register ( $n = 1, 3, 4, 6$ )
  7.  $i$ : Idle state count
  8.  $m = 0$  to 3

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (3/3)



**Note** At least one clock is always inserted in TRPW and TCPW cycles.

- Remarks 1.** This is the timing for the following case.
- Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
  - Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
  - Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
  - Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1
- 2.** The broken lines indicate high impedance.
- 3.** n = 1, 3, 4, 6, m = 0 to 3

(e) CBR refresh timing

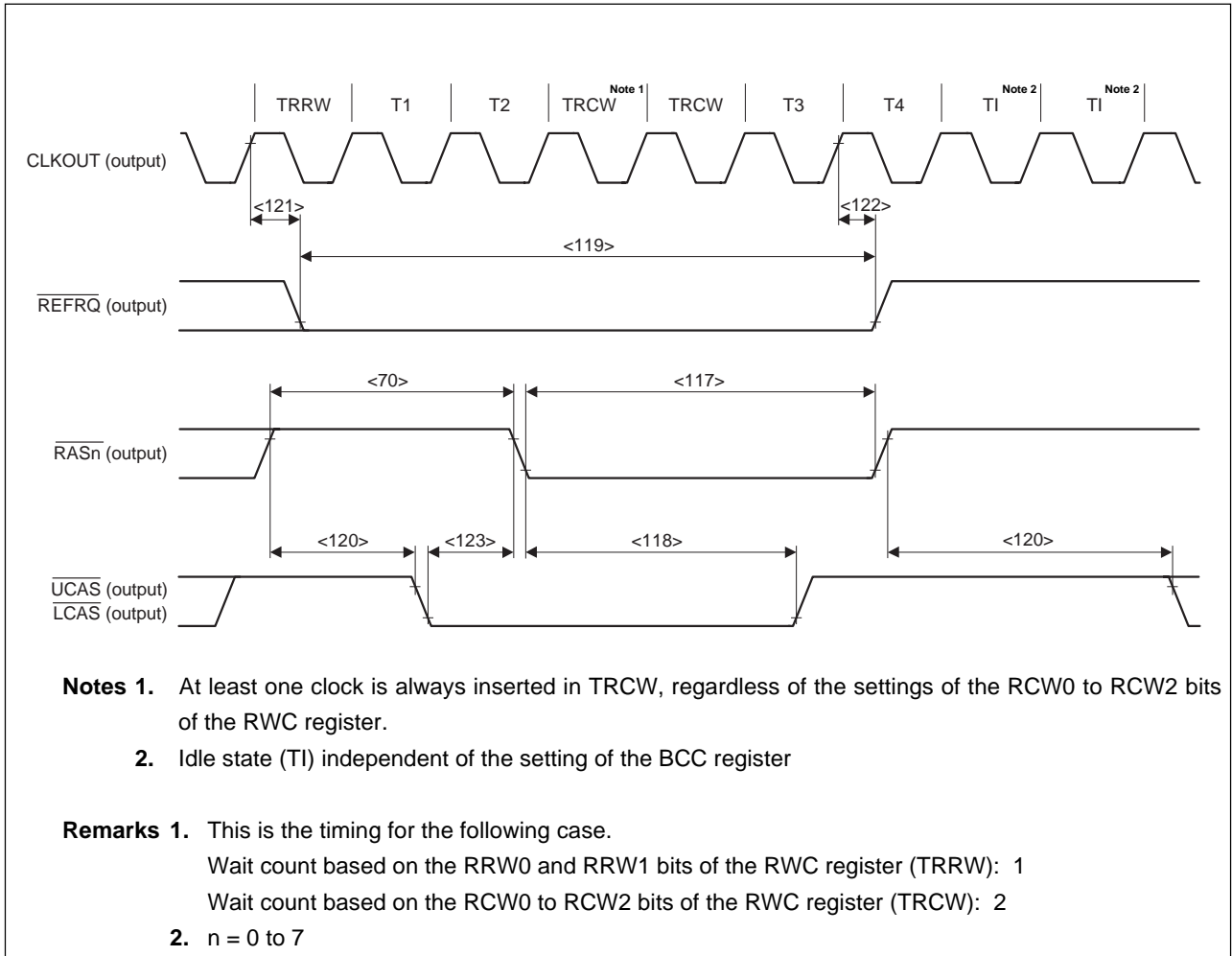
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RAS precharge time	<70>	$t_{RP}$	$(1.5 + W_{RRW})T - 10$		ns
RAS pulse width	<117>	$t_{RAS}$	$(1.5 + W_{RCW}^{Note})T - 10$		ns
CAS hold time	<118>	$t_{CHR}$	$(0.5 + W_{RCW}^{Note})T - 10$		ns
REFRQ pulse width	<119>	$t_{WRFL}$	$(3 + W_{RRW} + W_{RCW}^{Note})T - 10$		ns
RAS precharge CAS hold time	<120>	$t_{RPC}$	$(2.5 + W_{RRW})T - 10$		ns
REFRQ active delay time (from CLKOUT↑)	<121>	$t_{DKRF}$	2	13	ns
REFRQ inactive delay time (from CLKOUT↑)	<122>	$t_{HKRF}$	2	13	ns
CAS setup time	<123>	$t_{CSR}$	$T - 10$		ns

**Note** At least one clock is always inserted in  $W_{RCW}$  by default, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

**Remarks 1.**  $T = t_{CYK}$

**2.**  $W_{RRW}$ : Wait count based on the RRW0 and RRW1 bits of the RWC register

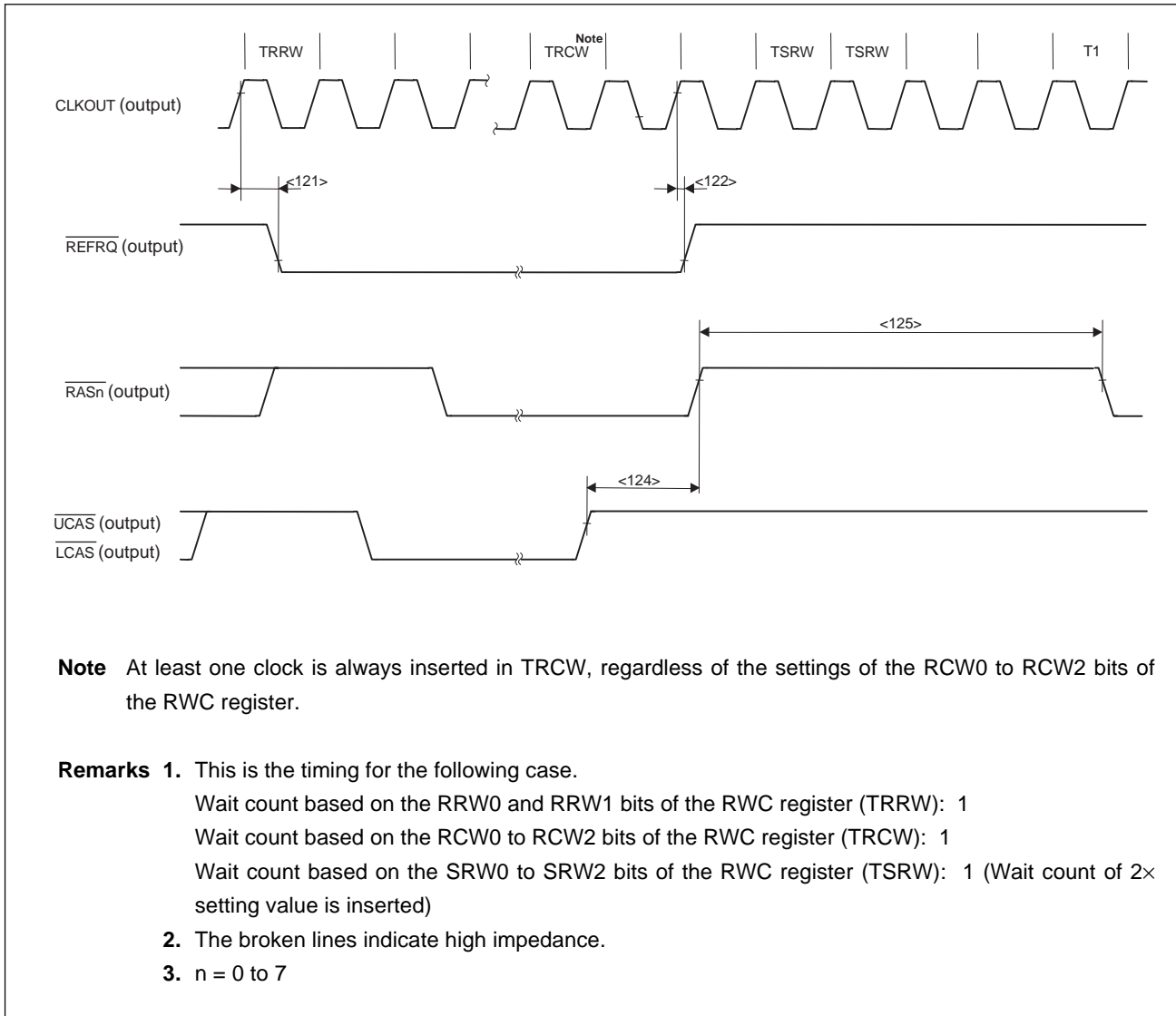
**3.**  $W_{RCW}$ : Wait count based on the RCW0 to RCW2 bits of the RWC register



(f) CBR self-refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
REFRQ active delay time (from CLKOUT↑)	<121>	t <sub>DKRF</sub>	2	13	ns
REFRQ inactive delay time (from CLKOUT↑)	<122>	t <sub>HKRF</sub>	2	13	ns
CAS hold time	<124>	t <sub>CHS</sub>	-(WRCWT - 10)		ns
RAS precharge time	<125>	t <sub>RPS</sub>	WRP = 0	(3 + 2W <sub>SRW</sub> )T - 10	ns
			WRP ≥ 1	(2 + 2W <sub>SRW</sub> + W <sub>RPW</sub> )T - 10	ns

- Remarks**
1. T = t<sub>cyk</sub>
  2. W<sub>SRW</sub>: Wait count based on the SRW0 to SRW2 bits of the RWC register
  3. WRCW: Wait count based on the RCW0 to RCW2 bits of the RWC register
  4. WRPW: Wait count based on the RRW0 and RRW1 bits of the RWC register



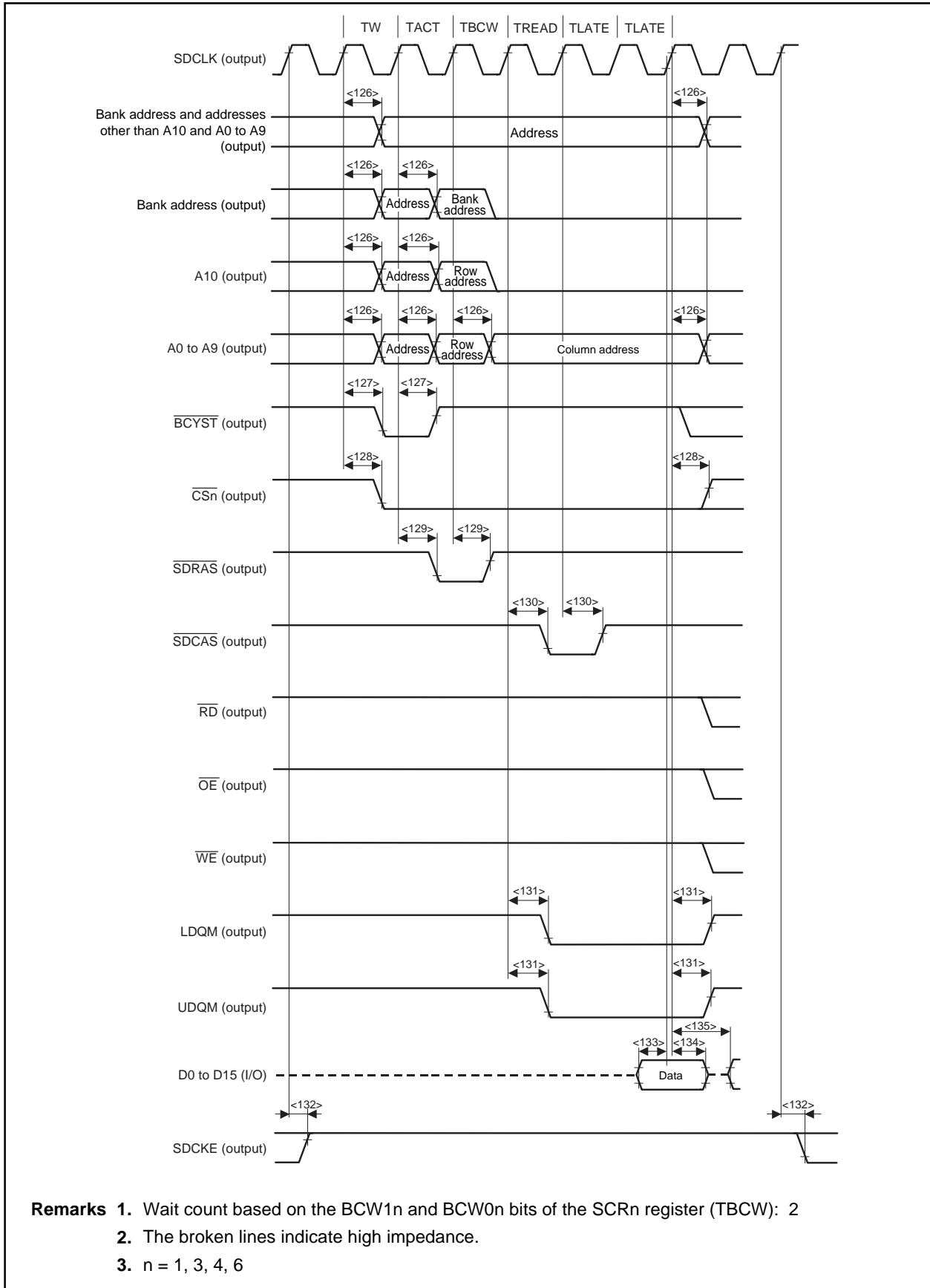
(7) SDRAM access timing

(a) Read timing (SDRAM access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126> t <sub>DKA</sub>		2	13	ns
BCYST delay time (from SDCLK↑)	<127> t <sub>DKBC</sub>		2	13	ns
C <sub>S</sub> n delay time (from SDCLK↑)	<128> t <sub>DKCS</sub>		2	13	ns
SDRAS delay time (from SDCLK↑)	<129> t <sub>DKRAS</sub>		2	13	ns
SDCAS delay time (from SDCLK↑)	<130> t <sub>DKCAS</sub>		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131> t <sub>DKDQM</sub>		2	13	ns
SDCKE delay time (from SDCLK↑)	<132> t <sub>DKCKE</sub>		2	13	ns
Data input setup time (at SDRAM read, to SDCLK↑)	<133> t <sub>SDRMK</sub>		8		ns
Data input hold time (at SDRAM read, from SDCLK↑)	<134> t <sub>HKDRM</sub>		0		ns
Delay time from SDCLK↑ to data output	<135> t <sub>DSDOD</sub>			(1 + i)T - 5	ns

- Remarks**
1. T = t<sub>cyk2</sub>
  2. i = Idle state count
  3. n = 1, 3, 4, 6

(a) Read timing (SDRAM access) (2/2)



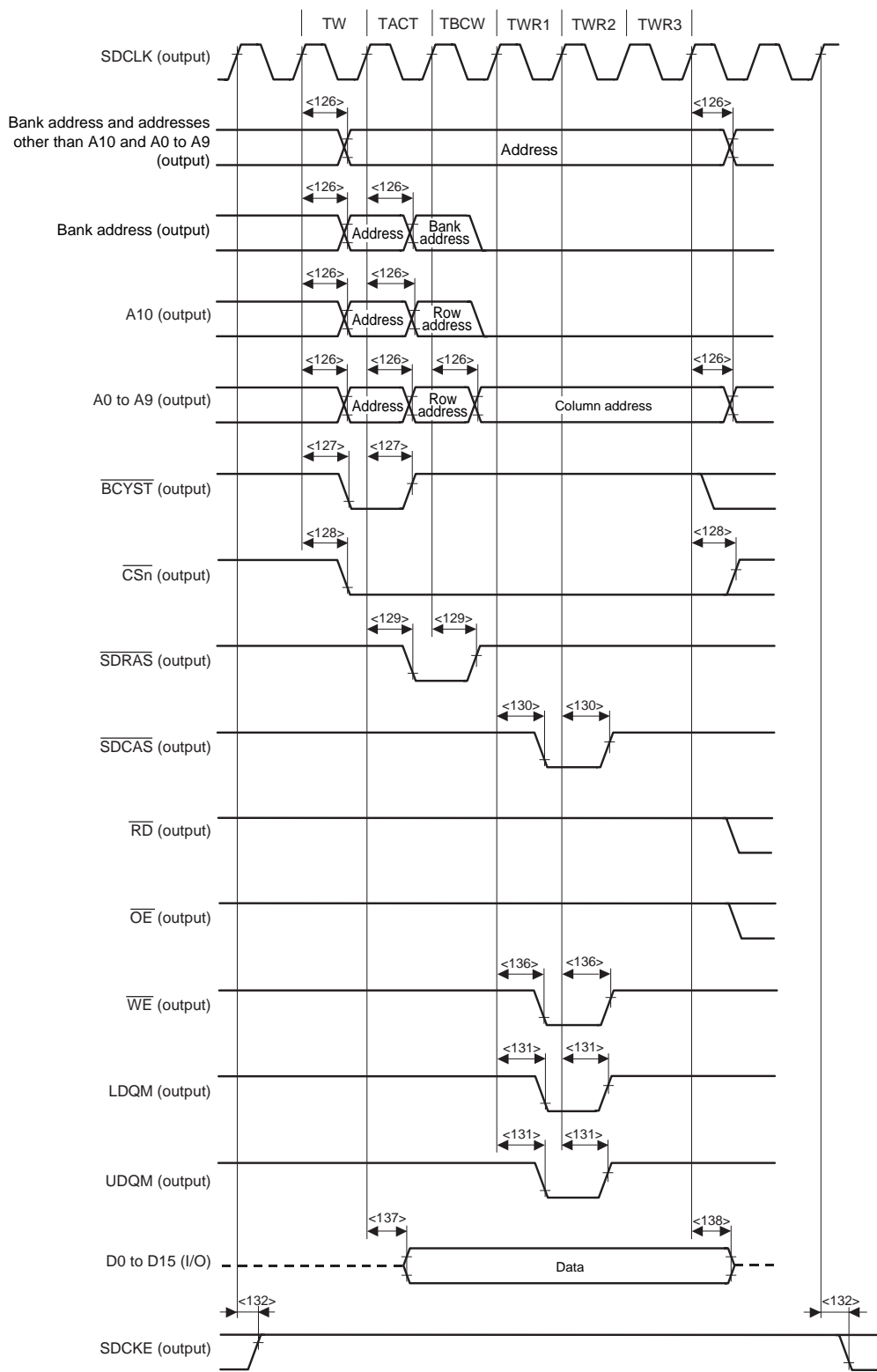
- Remarks**
1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2
  2. The broken lines indicate high impedance.
  3. n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126> t <sub>DKA</sub>		2	13	ns
BCYST delay time (from SDCLK↑)	<127> t <sub>DKBC</sub>		2	13	ns
CSn delay time (from SDCLK↑)	<128> t <sub>DKCS</sub>		2	13	ns
SDRAS delay time (from SDCLK↑)	<129> t <sub>DKRAS</sub>		2	13	ns
SDCAS delay time (from SDCLK↑)	<130> t <sub>DKCAS</sub>		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131> t <sub>DKDQM</sub>		2	13	ns
SDCKE delay time (from SDCLK↑)	<132> t <sub>DKCKE</sub>		2	13	ns
WE delay time (from SDCLK↑)	<136> t <sub>DKWE</sub>		2	13	ns
Data output delay time (from SDCLK↑)	<137> t <sub>DKDT</sub>		2	13	ns
Data float delay time (from SDCLK↑)	<138> t <sub>HZKDT</sub>		2	13	ns

**Remark** n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (2/2)



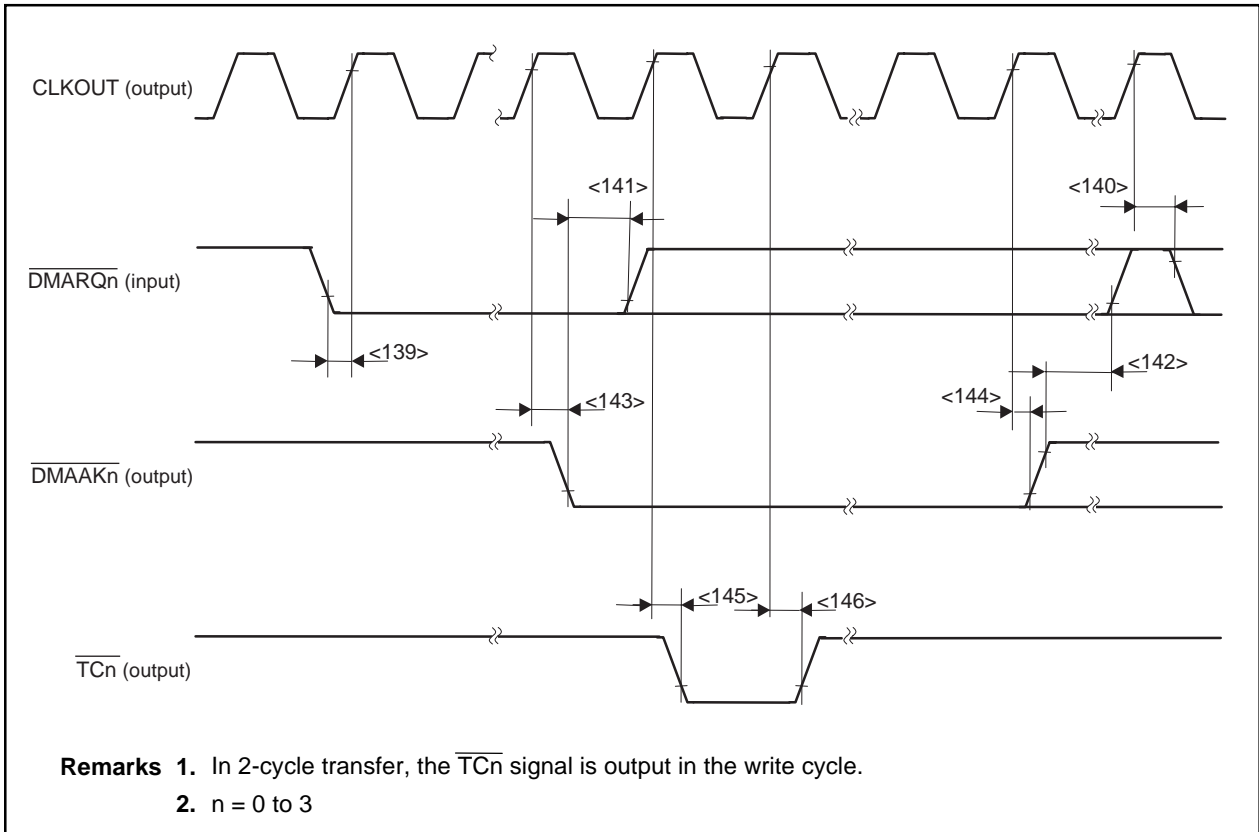
- Remarks**
1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2
  2. The broken lines indicate high impedance.
  3. n = 1, 3, 4, 6



(8) DMAC timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
DMARQn setup time (to CLKOUT↑)	<139> $t_{SDRK}$		8		ns
DMARQn hold time	<140> $t_{HKDR1}$	After inactive (from CLKOUT↑)	3		ns
	<141> $t_{HKDR2}$		Until DMAAKn↓		ns
Second DMA request disable timing in single transfer	<142> $t_{AKDR}$			3T	ns
DMAAKn output delay time (from CLKOUT↑)	<143> $t_{DKDA}$		2	13	ns
DMAAKn output hold time (from CLKOUT↑)	<144> $t_{HKDA}$		2	13	ns
TCn output delay time (from CLKOUT↑)	<145> $t_{HKTC}$		2	13	ns
TCn output hold time (from CLKOUT↑)	<146> $t_{HKTC}$		2	13	ns

- Remarks 1.** T = t<sub>cyk</sub>  
**2.** n = 0 to 3

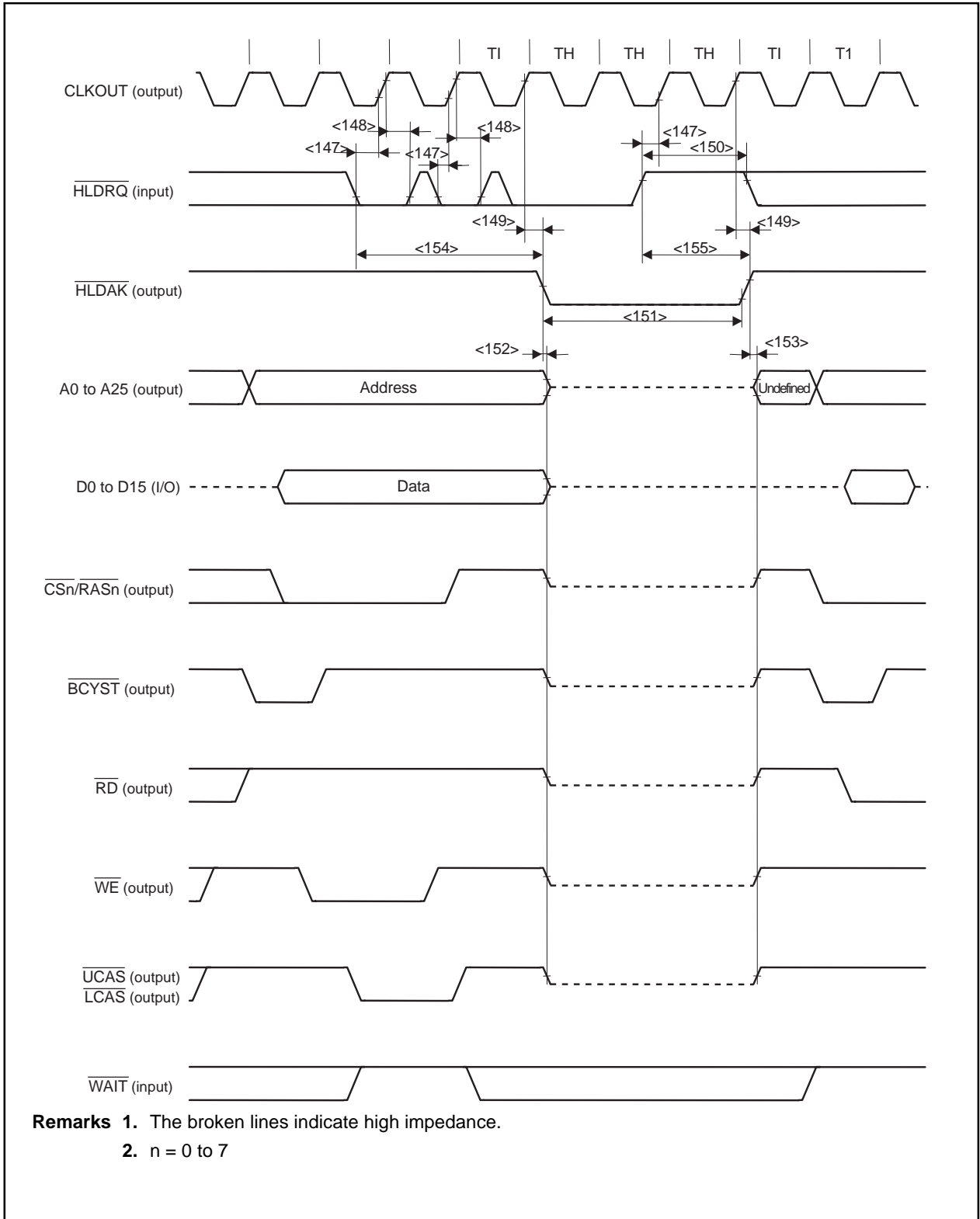


(9) Bus hold timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
H $\overline{\text{LDRQ}}$ setup time (to CLKOUT $\uparrow$ )	<147> t $\overline{\text{SHRK}}$		8		ns
H $\overline{\text{LDRQ}}$ hold time (from CLKOUT $\uparrow$ )	<148> t $\overline{\text{HKHR}}$		3		ns
Delay time from CLKOUT $\uparrow$ to H $\overline{\text{LDAK}}$	<149> t $\overline{\text{DKHA}}$		2	13	ns
H $\overline{\text{LDRQ}}$ high-level width	<150> t $\overline{\text{WHQH}}$		T + 3		ns
H $\overline{\text{LDAK}}$ low-level width	<151> t $\overline{\text{WHAL}}$		T - 11		ns
Delay time from H $\overline{\text{LDAK}}\downarrow$ to bus float	<152> t $\overline{\text{DKCF}}$		0		ns
Delay time from H $\overline{\text{LDAK}}\uparrow$ to bus output	<153> t $\overline{\text{DHAC}}$		2	13	ns
Delay time from H $\overline{\text{LDRQ}}\downarrow$ to H $\overline{\text{LDAK}}\downarrow$	<154> t $\overline{\text{DHQA1}}$		2T		ns
Delay time from H $\overline{\text{LDRQ}}\uparrow$ to H $\overline{\text{LDAK}}\uparrow$	<155> t $\overline{\text{DHQA2}}$		T	2T + 10	ns

**Remark** T = t<sub>cyk</sub>

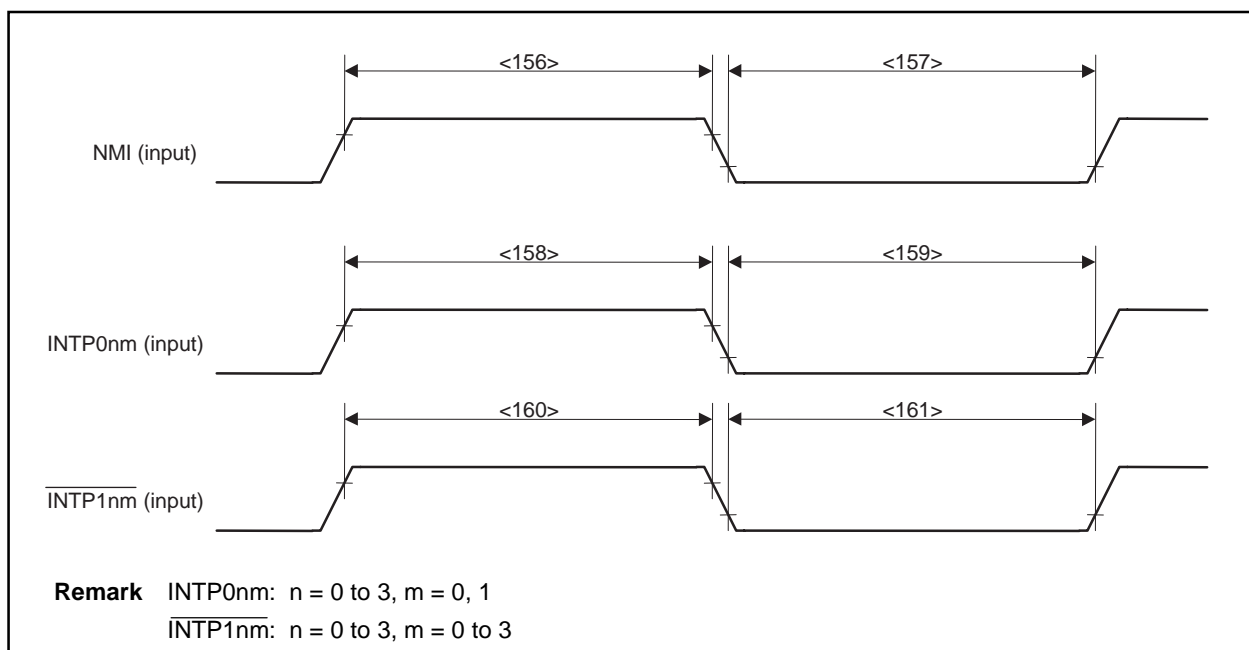
(9) Bus hold timing (2/2)



(10) Interrupt timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high-level width	<156> $t_{WNIH}$		500		ns
NMI low-level width	<157> $t_{WNIL}$		500		ns
INTP0nm high-level width	<158> $t_{WIT0H}$		$3T + 500$		ns
INTP0nm low-level width	<159> $t_{WIT0L}$		$3T + 500$		ns
INTP1nm high-level width	<160> $t_{WIT1H}$		500		ns
INTP1nm low-level width	<161> $t_{WIT1L}$		500		ns

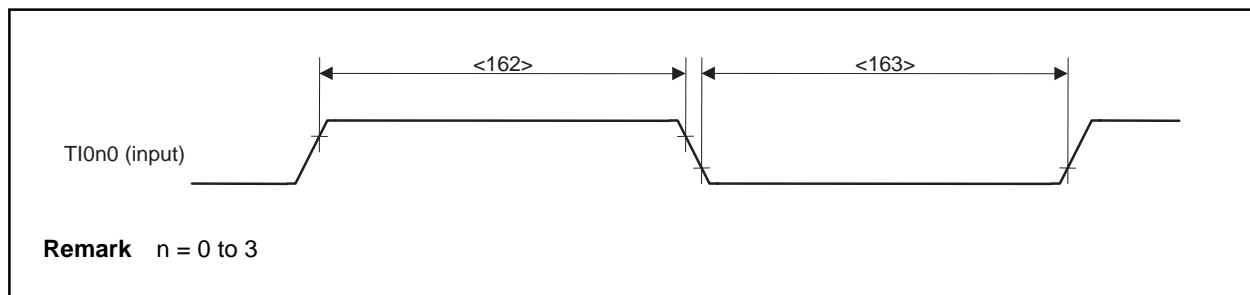
- Remarks** 1. INTP0nm: n = 0 to 3, m = 0, 1  
 INTP1nm: n = 0 to 3, m = 0 to 3  
 2. T = t<sub>cyk</sub>



(11) RPU timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Tl0n0 high-level width	<162> $t_{WTIH}$		$3T + 500$		ns
Tl0n0 low-level width	<163> $t_{WTIL}$		$3T + 500$		ns

- Remarks** 1. n = 0 to 3  
 2. T = t<sub>cyk</sub>



(12) CSI0 to CSI2 timing

(a) Master mode

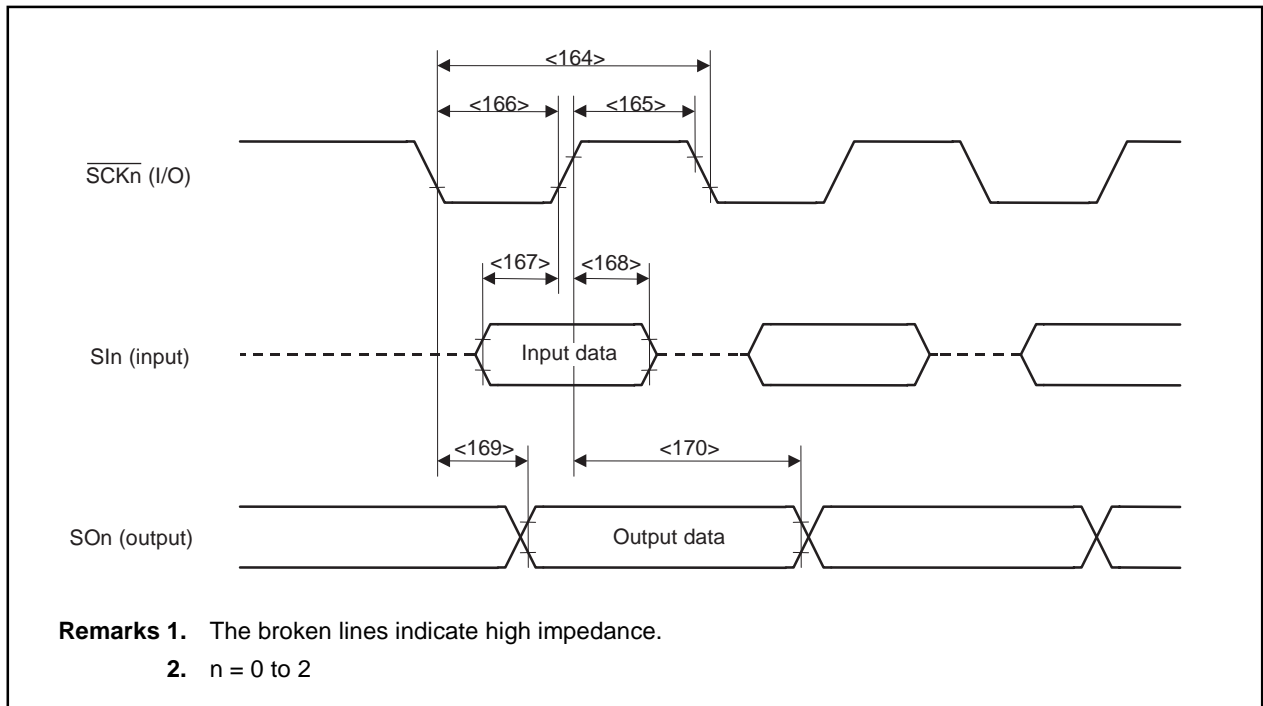
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164> $t_{CYSK1}$	Output	320		ns
$\overline{SCKn}$ high-level width	<165> $t_{WSK1H}$	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<166> $t_{WSK1L}$	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<167> $t_{SSISK}$		30		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<168> $t_{HSKSI}$		30		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<169> $t_{DSKSO}$			30	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<170> $t_{HSKSO}$		$0.5t_{CYSK1} - 5$		ns

Remark n = 0 to 2

(b) Slave mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164> $t_{CYSK1}$	Input	200		ns
$\overline{SCKn}$ high-level width	<165> $t_{WSK1H}$	Input	90		ns
$\overline{SCKn}$ low-level width	<166> $t_{WSK1L}$	Input	90		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<167> $t_{SSISK}$		50		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<168> $t_{HSKSI}$		50		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<169> $t_{DSKSO}$			50	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<170> $t_{HSKSO}$		$t_{WSK1H}$		ns

Remark n = 0 to 2



**A/D Converter Characteristics**

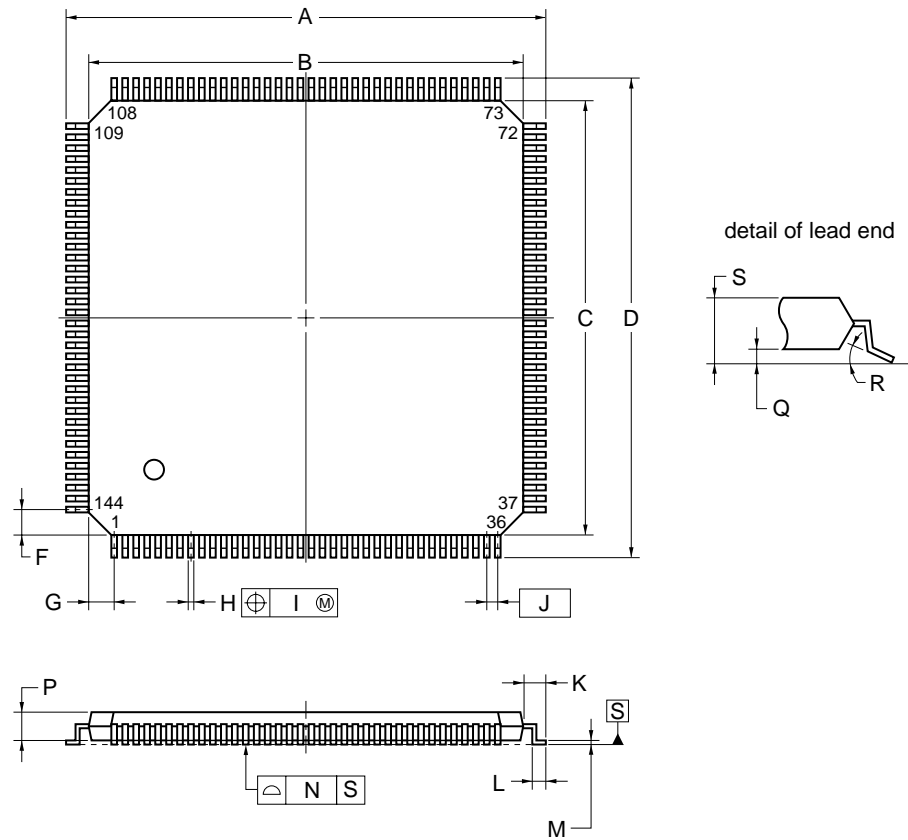
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 3.0$  to  $3.6$  V,  $V_{SS} = AV_{SS} = 0$  V, output pin load capacitance:  $C_L = 50$  pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Total error	–				±5	LSB
Quantization error	–				±1/2	LSB
Conversion time	t <sub>CONV</sub>		5		10	μs
Sampling time	t <sub>SAMP</sub>		Conversion clock <sup>Note</sup> /6			ns
Zero scale error	–				±5	LSB
Scale error	–				±5	LSB
Linearity error	–				±4	LSB
Analog input voltage	V <sub>WASN</sub>		–0.3		AV <sub>REF</sub> + 0.3	V
AV <sub>REF</sub> input voltage	AV <sub>REF</sub>	AV <sub>REF</sub> = AV <sub>DD</sub>	3.0		3.6	V
AV <sub>DD</sub> power supply current	AI <sub>DD</sub>				10	mA

**Note** Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.08
P	1.4
Q	0.10±0.05
R	3° <sup>+4°</sup> <sub>-3°</sub>
S	1.5±0.1

S144GJ-50-UEN

**5. RECOMMENDED SOLDERING CONDITIONS**

Undetermined



[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Related document:  $\mu$ PD70F3107 Data Sheet (U14618E)

Reference document: Electrical Characteristics for Microcomputer (IEI-601)<sup>Note</sup>

**Note** This document number is that of the Japanese version.

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