NEC

MOS INTEGRATED CIRCUIT

μPD703100-33, 703100-40, 703101-33, 703102-33

V850E/MS1™
32-/16-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD703101-33 and μPD703102-33 are members of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU core, ROM, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The μPD703100-33 and μPD703100-40 are ROMless versions of the μPD703101-33 and μPD703102-33 products.

The μPD703100A-33, μPD703100A-40, μPD703101A-33, and μPD703102A-33 are also available as products having a 3.3 V power supply for external pins.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MS1 User's Manual Hardware: U12688E
V850E/MS1 User's Manual Architecture: U12197E

FEATURES

- Number of instructions: 81
- Minimum instruction execution time 25 ns (@ 40 MHz operation) ·····μPD703100-40
  30 ns (@ 33 MHz operation) ·····μPD703100-33, 703101-33, 703102-33
- General-purpose registers 32 bits × 32
- Instruction set optimized for control applications
- Internal memory ROM: None (μPD703100-33, 703100-40),
  96 KB (μPD703101-33),
  128 KB (μPD703102-33)
  RAM: 4 KB
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power saving functions

APPLICATIONS

- Office automation equipment: printers, facsimile machines, PPCs, etc.
- Multimedia equipment: digital still cameras, video printers, etc.
- Consumer equipment: single-lens reflex cameras, etc.
- Industrial equipment: motor controllers, NC machine tools, etc.

Document No. U13995EJ2V0DS00 (2nd edition)
Date Published November 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ ORDERING INFORMATION

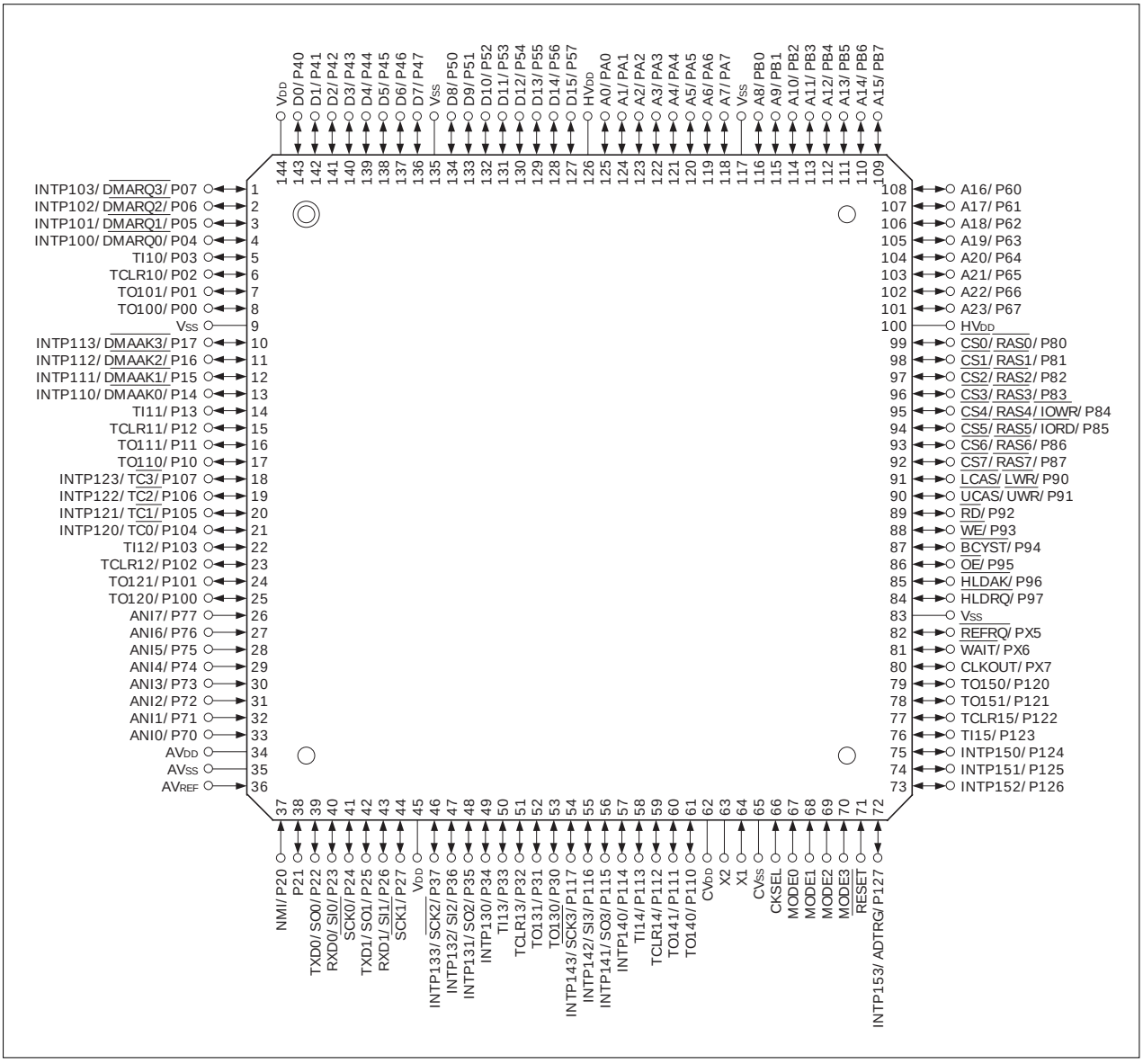
Part Number	Package	Maximum Operating Frequency	Internal ROM
μPD703100GJ-33-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	None
μPD703100GJ-40-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	40 MHz	None
μPD703101GJ-33-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	96 KB
μPD703102GJ-33-xxx-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	128 KB

Remark xxx indicates ROM code suffix.

PIN CONFIGURATION (TOP VIEW)

144-pin plastic LQFP (fine pitch) (20 × 20)

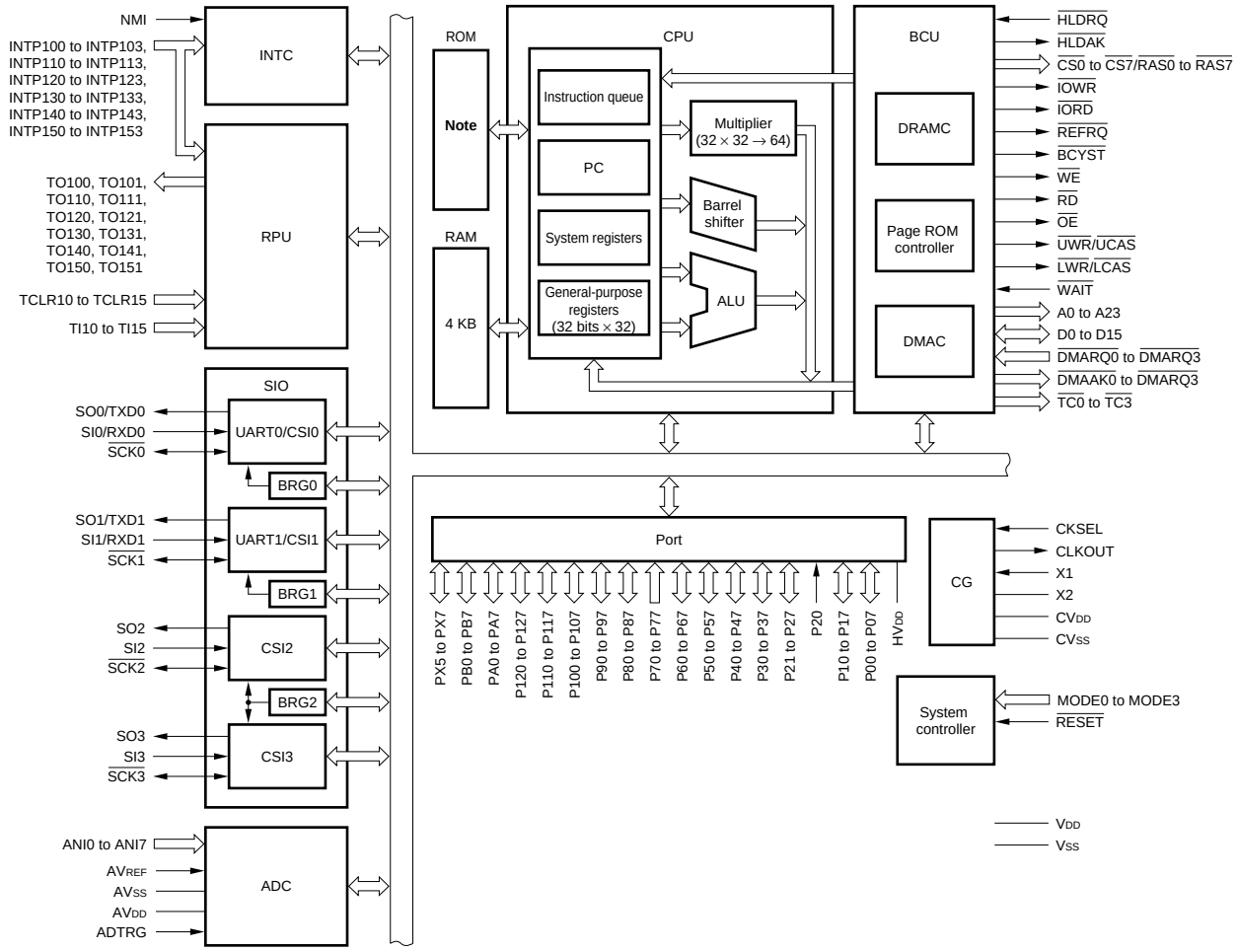
- μPD703100GJ-33-UEN
- μPD703100GJ-40-UEN
- μPD703101GJ-33-xxx-UEN
- μPD703102GJ-33-xxx-UEN



PIN NAMES

A0 to A23:	Address Bus	P50 to P57:	Port 5
ADTRG:	AD Trigger Input	P60 to P67:	Port 6
ANI0 to ANI7:	Analog Input	P70 to P77:	Port 7
AV_{DD}:	Analog Power Supply	P80 to P87:	Port 8
AV_{REF}:	Analog Reference Voltage	P90 to P97:	Port 9
AV_{SS}:	Analog Ground	P100 to P107:	Port 10
$\overline{BCYST}$:	Bus Cycle Start Timing	P110 to P117:	Port 11
CKSEL:	Clock Generator Operating Mode Select	P120 to P127:	Port 12
CLKOUT:	Clock Output	PA0 to PA7:	Port A
$\overline{CS0}$ to $\overline{CS7}$:	Chip Select	PB0 to PB7:	Port B
CV_{DD}:	Clock Generator Power Supply	PX5 to PX7:	Port X
CV_{SS}:	Clock Generator Ground	$\overline{RAS0}$ to $\overline{RAS7}$:	Row Address Strobe
D0 to D15:	Data Bus	$\overline{RD}$:	Read
$\overline{DMAAK0}$ to $\overline{DMAAK3}$:	DMA Acknowledge	$\overline{REFRQ}$:	Refresh Request
$\overline{DMARQ0}$ to $\overline{DMARQ3}$:	DMA Request	$\overline{RESET}$:	Reset
$\overline{HLDAK}$:	Hold Acknowledge	RXD0, RXD1:	Receive Data
$\overline{HLDRQ}$:	Hold Request	$\overline{SCK0}$ to $\overline{SCK3}$:	Serial Clock
HV_{DD}:	Power Supply for External Pins	SI0 to SI3:	Serial Input
INTP100 to INTP103, :	Interrupt Request from Peripherals	SO0 to SO3:	Serial Output
INTP110 to INTP113,		$\overline{TC0}$ to $\overline{TC3}$:	Terminal Count Signal
INTP120 to INTP123,		TCLR10 to TCLR15:	Timer Clear
INTP130 to INTP133,		TI10 to TI15:	Timer Input
INTP140 to INTP143,		TO100, TO101, :	Timer Output
INTP150 to INTP153		TO110, TO111,	
$\overline{IORD}$:	I/O Read Strobe	TO120, TO121,	
$\overline{IOWR}$:	I/O Write Strobe	TO130, TO131,	
$\overline{LCAS}$:	Lower Column Address Strobe	TO140, TO141,	
$\overline{LWR}$:	Lower Write Strobe	TO150, TO151	
MODE0 to MODE3:	Mode	TXD0, TXD1:	Transmit Data
NMI:	Non-Maskable Interrupt Request	$\overline{UCAS}$:	Upper Column Address Strobe
$\overline{OE}$:	Output Enable	$\overline{UWR}$:	Upper Write Strobe
P00 to P07:	Port 0	V_{DD}:	Power Supply for Internal Unit
P10 to P17:	Port 1	V_{SS}:	Ground
P20 to P27:	Port 2	$\overline{WAIT}$:	Wait
P30 to P37:	Port 3	$\overline{WE}$:	Write Enable
P40 to P47:	Port 4	X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



Note μPD703100-33, 703100-40: None
μPD703101-33: 96 KB (mask ROM)
μPD703102-33: 128 KB (mask ROM)

CONTENTS

1. DIFFERENCES AMONG PRODUCTS

Item \ Product Name	μPD703100				μPD703101		μPD703102		μPD70F3102	
	-33	-40	A-33	A-40	-33	A-33	-33	A-33	-33	A-33
Internal ROM	None				96 KB (mask ROM)		128 KB (mask ROM)		128 KB (flash memory)	
Maximum operating frequency	33 MHz	40 MHz	33 MHz	40 MHz	33 MHz					
HV_{DD}	4.5 to 5.5 V		3.0 to 3.6 V		4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V
Operation mode										
Single-chip mode 0, 1	None				Provided					
Flash memory programming mode	None								Provided	
Flash memory programming pin	None								Provided (V_{PP})	
Electrical specifications	Power consumptions differ (refer to the data sheet of each product).									
Package	144LQFP		144LQFP 157FBGA		144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA
Others	Noise tolerance and noise radiation will differ due to the differences in circuit scale and mask layout.									

Remark 144LQFP: 144-pin plastic LQFP (fine pitch) (20 × 20)
157FBGA: 157-pin plastic FBGA (14 × 14)

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units	TO100
P01			TO101
P02			TCLR10
P03			TI10
P04			INTP100/$\overline{\text{DMARQ0}}$
P05			INTP101/$\overline{\text{DMARQ1}}$
P06			INTP102/$\overline{\text{DMARQ2}}$
P07			INTP103/$\overline{\text{DMARQ3}}$
P10	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units	TO110
P11			TO111
P12			TCLR11
P13			TI11
P14			INTP110/$\overline{\text{DMAAK0}}$
P15			INTP111/$\overline{\text{DMAAK1}}$
P16			INTP112/$\overline{\text{DMAAK2}}$
P17			INTP113/$\overline{\text{DMAAK3}}$
P20	Input	Port 2 P20 is an input only port. When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P21 to P27 are 7-bit I/O port. Input/output can be specified in 1-bit units	NMI
P21	I/O		–
P22			TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO2
P36			INTP132/SI2
P37			INTP133/$\overline{\text{SCK2}}$
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units	D0 to D7

(2/3)

Pin Name	I/O	Function	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units	A16 to A23
P70 to P77	Input	Port 7 8-bit input only port	ANI0 to ANI7
P80	I/O	Port 8 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{CS0}$/$\overline{RAS0}$
P81			$\overline{CS1}$/$\overline{RAS1}$
P82			$\overline{CS2}$/$\overline{RAS2}$
P83			$\overline{CS3}$/$\overline{RAS3}$
P84			$\overline{CS4}$/$\overline{RAS4}$/$\overline{IOWR}$
P85			$\overline{CS5}$/$\overline{RAS5}$/$\overline{IORD}$
P86			$\overline{CS6}$/$\overline{RAS6}$
P87			$\overline{CS7}$/$\overline{RAS7}$
P90	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{LCAS}$/$\overline{LWR}$
P91			$\overline{UCAS}$/$\overline{UWR}$
P92			$\overline{RD}$
P93			$\overline{WE}$
P94			$\overline{BCYST}$
P95			$\overline{OE}$
P96			$\overline{HLDAK}$
P97			$\overline{HLDRQ}$
P100	I/O	Port 10 8-bit I/O port Input/output can be specified in 1-bit units	TO120
P101			TO121
P102			TCLR12
P103			TI12
P104			INTP120/$\overline{TC0}$
P105			INTP121/$\overline{TC1}$
P106			INTP122/$\overline{TC2}$
P107			INTP123/$\overline{TC3}$
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141/SO3
P116			INTP142/SI3
P117			INTP143/$\overline{SCK3}$

(3/3)

Pin Name	I/O	Function	Alternate Function
P120	I/O	Port 12 8-bit I/O port Input/output can be specified in 1-bit units	TO150
P121			TO151
P122			TCLR15
P123			TI15
P124			INTP150
P125			INTP151
P126			INTP152
P127			INTP153/ADTRG
PA0	I/O	Port A 8-bit I/O port Input/output can be specified in 1-bit units	A0
PA1			A1
PA2			A2
PA3			A3
PA4			A4
PA5			A5
PA6			A6
PA7			A7
PB0	I/O	Port B 8-bit I/O port Input/output can be specified in 1-bit units	A8
PB1			A9
PB2			A10
PB3			A11
PB4			A12
PB5			A13
PB6			A14
PB7			A15
PX5	I/O	Port X 3-bit I/O port Input/output can be specified in 1-bit units	$\overline{\text{REFRQ}}$
PX6			$\overline{\text{WAIT}}$
PX7			CLKOUT

2.2 Non-Port Pins

(1/4)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 15	P00
TO101			P01
TO110			P10
TO111			P11
TO120			P100
TO121			P101
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TO150			P120
TO151			P121
TCLR10	Input	External clear signal input for timers 10 to 15	P02
TCLR11			P12
TCLR12			P102
TCLR13			P32
TCLR14			P112
TCLR15			P122
TI10	Input	External count clock input for timers 10 to 15	P03
TI11			P13
TI12			P103
TI13			P33
TI14			P113
TI15			P123
INTP100	Input	External maskable interrupt request input, shared as external capture trigger input for timer 10	P04/$\overline{\text{DMARQ0}}$
INTP101			P05/$\overline{\text{DMARQ1}}$
INTP102			P06/$\overline{\text{DMARQ2}}$
INTP103			P07/$\overline{\text{DMARQ3}}$
INTP110	Input	External maskable interrupt request input, shared as external capture trigger input for timer 11	P14/$\overline{\text{DMAAK0}}$
INTP111			P15/$\overline{\text{DMAAK1}}$
INTP112			P16/$\overline{\text{DMAAK2}}$
INTP113			P17/$\overline{\text{DMAAK3}}$
INTP120	Input	External maskable interrupt request input, shared as external capture trigger input for timer 12	P104/$\overline{\text{TC0}}$
INTP121			P105/$\overline{\text{TC1}}$
INTP122			P106/$\overline{\text{TC2}}$
INTP123			P107/$\overline{\text{TC3}}$

(2/4)

Pin Name	I/O	Function	Alternate Function
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
INTP131			P35/SO2
INTP132			P36/SI2
INTP133			P37/$\overline{\text{SCK2}}$
INTP140	Input	External maskable interrupt request input, shared as external capture trigger input for timer 14	P114
INTP141			P115/SO3
INTP142			P116/SI3
INTP143			P117/$\overline{\text{SCK3}}$
INTP150	Input	External maskable interrupt request input, shared as external capture trigger input for timer 15	P124
INTP151			P125
INTP152			P126
INTP153			P127/ADTRG
SO0	Output	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P35/INTP131
SO3			P115/INTP141
SI0	Input	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P36/INTP132
SI3			P116/INTP142
$\overline{\text{SCK0}}$	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P37/INTP133
$\overline{\text{SCK3}}$			P117/INTP143
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	P40 to P47
D8 to D15			P50 to P57
A0 to A7	Output	24-bit address bus for external memory	PA0 to PA7
A8 to A15			PB0 to PB7
A16 to A23			P60 to P67
$\overline{\text{LWR}}$	Output	Lower byte write-enable signal output for external data bus	P90/$\overline{\text{LCAS}}$
$\overline{\text{UWR}}$	Output	Higher byte write-enable signal output for external data bus	P91/$\overline{\text{UCAS}}$
$\overline{\text{RD}}$	Output	Read strobe signal output for external data bus	P92
$\overline{\text{WE}}$	Output	Write enable signal output for DRAM	P93
$\overline{\text{OE}}$	Output	Output enable signal output for DRAM	P95

(3/4)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{LCAS}}$	Output	Column address strobe signal output for DRAM's lower data	P90/$\overline{\text{LWR}}$
$\overline{\text{UCAS}}$	Output	Column address strobe signal output for DRAM's higher data	P91/$\overline{\text{UWR}}$
$\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$	Output	Low address strobe signal output for DRAM	P80/$\overline{\text{CS0}}$ to P83/$\overline{\text{CS3}}$
$\overline{\text{RAS4}}$			P84/$\overline{\text{CS4}}$/$\overline{\text{IOWR}}$
$\overline{\text{RAS5}}$			P85/$\overline{\text{CS5}}$/$\overline{\text{IORD}}$
$\overline{\text{RAS6}}$			P86/$\overline{\text{CS6}}$
$\overline{\text{RAS7}}$			P87/$\overline{\text{CS7}}$
$\overline{\text{BCYST}}$	Output	Strobe signal output indicating start of bus cycle	P94
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	Output	Chip select signal output	P80/$\overline{\text{RAS0}}$ to P83/$\overline{\text{RAS3}}$
$\overline{\text{CS4}}$			P84/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$
$\overline{\text{CS5}}$			P85/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$
$\overline{\text{CS6}}$			P86/$\overline{\text{RAS6}}$
$\overline{\text{CS7}}$			P87/$\overline{\text{RAS7}}$
$\overline{\text{WAIT}}$	Input	Control signal input for inserting waits in bus cycle	PX6
$\overline{\text{REFRQ}}$	Output	Refresh request signal output for DRAM	PX5
$\overline{\text{IOWR}}$	Output	DMA write strobe signal output	P84/$\overline{\text{RAS4}}$/$\overline{\text{CS4}}$
$\overline{\text{IORD}}$	Output	DMA read strobe signal output	P85/$\overline{\text{RAS5}}$/$\overline{\text{CS5}}$
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$	Input	DMA request signal input	P04/INTP100 to P07/INTP103
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$	Output	DMA acknowledge signal output	P14/INTP110 to P17/INTP113
$\overline{\text{TC0}}$ to $\overline{\text{TC3}}$	Output	DMA end (terminal count) signal output	P104/INTP120 to P107/INTP123
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	P96
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P97
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	–
MODE0 to MODE3	Input	Specify operation modes	–
$\overline{\text{RESET}}$	Input	System reset input	–
X1	Input	Oscillator connection for system clock. Input is via X1 when using an external clock.	–
X2	–		–
ADTRG	Input	A/D converter external trigger input	P127/INTP153
AV_{REF}	Input	Reference voltage input for A/D converter	–
AV_{DD}	–	Positive power supply for A/D converter	–
AV_{SS}	–	Ground potential for A/D converter	–

(4/4)

Pin Name	I/O	Function	Alternate Function
CV_{DD}	–	Positive power supply for dedicated clock generator	–
CV_{SS}	–	Ground potential for dedicated clock generator	–
V_{DD}	–	Positive power supply (power supply for internal units)	–
HV_{DD}	–	Positive power supply (power supply for external pins)	–
V_{SS}	–	Ground potential	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

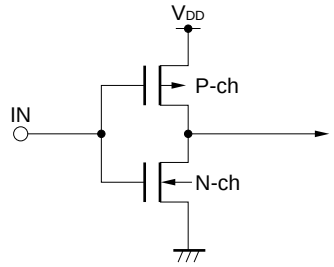
Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100, P01/TO101	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P02/TCLR10, P03/TI10	5-K	
P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$		
P10/TO110, P11/TO111	5	
P12/TCLR11, P13/TI11	5-K	
P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$		
P20/NMI	2	Connect directly to V_{SS}
P21	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P22/TXD0/SO0		
P23/RXD0/SI0	5-K	
P24/$\overline{\text{SCK0}}$		
P25/TXD1/SO1	5	
P26/RXD1/SI1	5-K	
P27/$\overline{\text{SCK1}}$		
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13	5-K	
P34/INTP130		
P35/INTP131/SO2		
P36/INTP132/SI2		
P37/INTP133/$\overline{\text{SCK2}}$		
P40/D0 to P47/D7	5	
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V_{SS}
P80/$\overline{\text{CS0}}$/$\overline{\text{RAS0}}$ to P83/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P84/$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$, P85/$\overline{\text{CS5}}$/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$		
P86/$\overline{\text{CS6}}$/$\overline{\text{RAS6}}$, P87/$\overline{\text{CS7}}$/$\overline{\text{RAS7}}$		
P90/$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$		
P91/$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

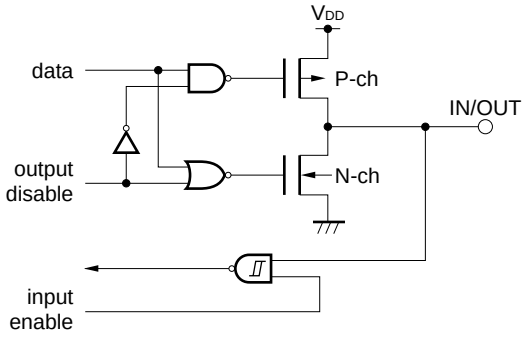
Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P92/$\overline{RD}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P93/$\overline{WE}$		
P94/$\overline{BCYST}$		
P95/$\overline{OE}$		
P96/$\overline{HLDAK}$		
P97/$\overline{HLDRQ}$		
P100/TO120, P101/TO121		
P102/TCLR12, P103/TI12	5-K	
P104/INTP120/$\overline{TC0}$ to P107/INTP123/$\overline{TC3}$		
P110/TO140, P111/TO141	5	
P112/TCLR14, P113/TI14	5-K	
P114/INTP140		
P115/INTP141/SO3		
P116/INTP142/SI3		
P117/INTP143/$\overline{SCK3}$		
P120/TO150, P121/TO151	5	
P122/TCLR15, P123/TI15	5-K	
P124/INTP150 to P126/INTP152		
P127/INTP153/ADTRG		
PA0/A0 to PA7/A7	5	
PB0/A8 to PB7/A15		
PX5/$\overline{REFRQ}$		
PX6/$\overline{WAIT}$		
PX7/CLKOUT		
CKSEL	1	Connect directly to HV_{DD}
$\overline{RESET}$	2	–
MODE0 to MODE2		
MODE3		Connect to V_{SS} via a resistor (R_{VPP})
AV_{REF}, AV_{SS}	–	Connect directly to V_{SS}
AV_{DD}	–	Connect directly to HV_{DD}

Figure 2-1. Pin I/O Circuits

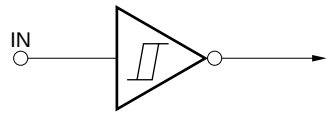
Type 1



Type 5-K

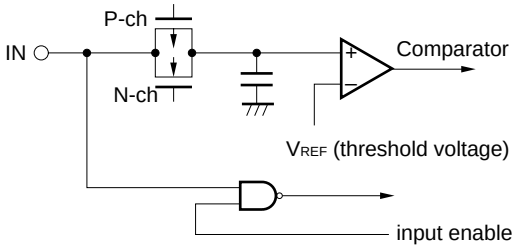


Type 2

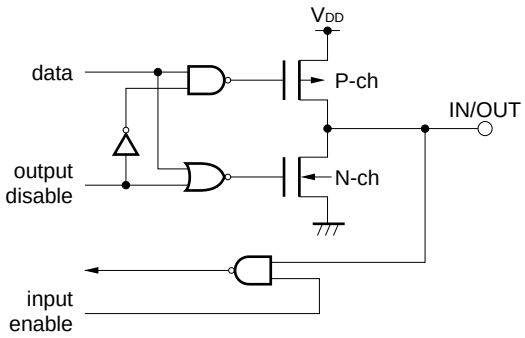


Schmitt-triggered input with hysteresis characteristics

Type 9



Type 5



Caution Replace V_{DD} by HV_{DD} when referencing the circuit diagrams shown above.

★ 3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage	V_{DD}	V_{DD} pin		–0.5 to +4.6	V
	HV_{DD}	HV_{DD} pin, $HV_{DD} \geq V_{DD}$		–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin		–0.5 to +4.6	V
	CV_{SS}	CV_{SS} pin		–0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		–0.5 to HV_{DD} + 0.5	V
	AV_{SS}	AV_{SS} pin		–0.5 to +0.5	V
Input voltage	V_I	X1 pin, except MODE3 pin		–0.5 to HV_{DD} + 0.5	V
		MODE3 pin		–0.5 to V_{DD} + 0.5	V
Clock input voltage	V_K	X1, V_{DD} = 3.0 to 3.6 V		–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin		4.0	mA
		Total of all pins		100	mA
Output current, high	I_{OH}	1 pin		–4.0	mA
		Total of all pins		–100	mA
Output voltage	V_O	HV_{DD} = 5.0 V ±10 %		–0.5 to HV_{DD} + 0.5	V
Analog input voltage	V_{IAN}	P70/ANI0 to P77/ANI7 pins	$AV_{DD} > HV_{DD}$	–0.5 to HV_{DD} + 0.5	V
			$HV_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5	V
A/D converter reference input voltage	AV_{REF}	$AV_{DD} > HV_{DD}$		–0.5 to HV_{DD} + 0.5	V
		$HV_{DD} \geq AV_{DD}$		–0.5 to AV_{DD} + 0.5	V
Operating ambient temperature	T_A	μPD703100-40		–40 to +70	°C
		μPD703100-33, 703101-33, 703102-33		–40 to +85	°C
Storage temperature	T_{stg}			–60 to +150	°C

Cautions 1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to V_{DD}, V_{CC}, or GND. However, the open drain pins or the open collector pins can be directly connected with each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to high-impedance state.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = HV_{DD} = CV_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_c = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)		Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD}, HV_{DD})
Direct mode	μPD703100-40	2 to 40 MHz	−40 to +70°C	V_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 V ±10%
	μPD703100-33, 703101-33, 703102-33	2 to 33 MHz	−40 to +85°C	
PLL mode Note 1	μPD703100-40 Note 2	20 to 40 MHz	−40 to +70°C	
	μPD703100-33, 703101-33, 703102-33 Note 3	20 to 33 MHz	−40 to +85°C	

Notes 1. The internal operating clock frequency in PLL mode is the value for 5× operation. When used for 1× or 1/2× operation as set by the CKDIVn (n = 0, 1) bit of the CKC register, operation at a frequency of 20 MHz or less is possible.

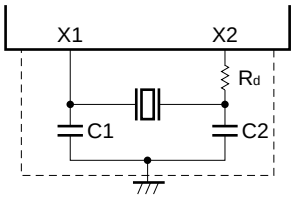
2. Set the input clock frequency used in PLL mode to 4.0 to 8.0 MHz.

3. Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

Recommended Oscillator

(a) Ceramic resonator (T_A = –40 to +70°C … μPD703100-40,
T_A = –40 to +85°C … μPD703100-33, 703101-33, 703102-33)

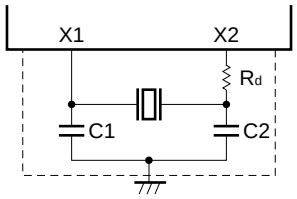
(i) Murata Mfg. Co., Ltd. (T_A = –40 to +85°C)



Type	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Surface mounting	CSAC4.00MGC040	4.0	100	100	0	3.0	3.6	0.5
	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CSAC5.00MGC040	5.0	100	100	0	3.0	3.6	0.4
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.2
	CSAC6.60MT	6.6	30	30	0	3.0	3.6	0.2
	CSTCC6.60MG0H6	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSAC8.00MT	8.0	30	30	0	3.0	3.6	0.2
	CSTCC8.00MG0H6	8.0	On-chip	On-chip	0	3.0	3.6	0.3
Lead	CSA4.00MG040	4.0	100	100	0	3.0	3.6	0.5
	CST4.00MGW040	4.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA5.00MG040	5.0	100	100	0	3.0	3.6	0.5
	CST5.00MGW040	5.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA6.60MTZ	6.6	30	30	0	3.0	3.6	0.1
	CST6.60MTW	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSA8.00MTZ	8.0	30	30	0	3.0	3.6	0.1
	CST8.00MTW	8.0	On-chip	On-chip	0	3.0	3.6	0.1

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

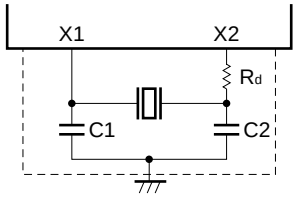
(ii) TDK (T_A = –40 to +85°C)



Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
TDK	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.17
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.15
	CCR8.0MC5	8.0	On-chip	On-chip	0	3.0	3.6	0.11

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

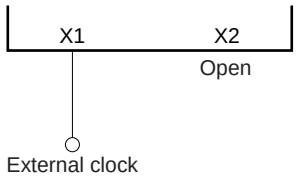
(iii) Kyocera Corporation (T_A = –20 to +80°C)



Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Kyocera	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.00BR-A	6.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.60BR-A	6.6	On-chip	On-chip	0	3.0	3.6	0.06

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703100-33, 703100-40, 703101-33, 703102-33 and the resonator.

(b) External clock input (T_A = –40 to +70°C ... μPD703100-40,
T_A = –40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33)



Caution Input CMOS-level voltage to the X1 pin.

DC Characteristics (T_A = –40 to +70°C ... μPD703100-40, T_A = –40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 ±10%, V_{SS} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	Except **Note 1**		2.2		HV_{DD} + 0.3	V
		Note 1		0.8HV_{DD}		HV_{DD} + 0.3	V
Input voltage, low	V_{IL}	Except **Note 1** and **Note 2**		–0.5		+0.8	V
		Note 1		–0.5		0.2HV_{DD}	V
Clock input voltage, high	V_{XH}	X1 pin	Direct mode	0.8V_{DD}		V_{DD} + 0.3	V
			PLL mode	0.8V_{DD}		V_{DD} + 0.3	V
Clock input voltage, low	V_{XL}	X1 pin	Direct mode	–0.3		0.15V_{DD}	V
			PLL mode	–0.3		0.15V_{DD}	V
Schmitt-triggered input threshold voltage	HV_T^+	**Note 1**, rising edge			3.0		V
	HV_T^-	**Note 1**, falling edge			2.0		V
Schmitt-triggered input hysteresis width	$HV_T^+ - HV_T^-$	**Note 1**		0.5			V
Output voltage, high	V_{OH}	I_{OH} = –2.5 mA		0.7HV_{DD}			V
		I_{OH} = –100 μA		HV_{DD} – 0.4			V
Output voltage, low	V_{OL}	I_{OL} = 2.5 mA				0.45	V
Input leakage current, high	I_{LIH}	Except V_I = HV_{DD} or **Note 2**				10	μA
Input leakage current, low	I_{LIL}	Except V_I = 0 V or **Note 2**				–10	μA
Output leakage current, high	I_{LOH}	V_O = HV_{DD}				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA

Notes 1. P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

2. When the P70/ANI0 to P77/ANI7 pins are used as analog input.

Remark TYP. values are reference values for when T_A = 25°C, V_{DD} = CV_{DD} = 3.3 V, and HV_{DD} = 5.0 V.

DC Characteristics (T_A = –40 to +70°C ... μPD703100-40, T_A = –40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 ±10%, V_{SS} = 0 V)

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit
Power supply current	Normal mode	I_{DD1}		V_{DD} + CV_{DD}		2.0 × fx	3.6 × fx	mA
				HV_{DD}		1.8 × fx	3.0 × fx	mA
	HALT mode	I_{DD2}		V_{DD} + CV_{DD}		1.4 × fx	2.5 × fx	mA
				HV_{DD}		0.8 × fx	1.6 × fx	mA
	IDLE mode	I_{DD3}		V_{DD} + CV_{DD}		1.5	3.0	mA
				HV_{DD}		10	50	μA
	STOP mode	I_{DD4}	μPD703100-40	V_{DD} + CV_{DD}		1.0	3.0	mA
				HV_{DD}		10	50	μA
			μPD703100-33, 703101-33, 703102-33	V_{DD} + CV_{DD}		20	100	μA
				HV_{DD}		10	50	μA

Remarks 1. TYP. values are reference values for when T_A = 25°C, V_{DD} = CV_{DD} = 3.3 V, and HV_{DD} = 5.0 V.

2. Direct mode:

f_X = 2 to 40 MHz (μPD703100-40)

f_X = 2 to 33 MHz (μPD703100-33, μPD703101-33, μPD703102-33)

PLL mode:

f_X = 20 to 40 MHz (μPD703100-40)

f_X = 20 to 33 MHz (μPD703100-33, μPD703101-33, μPD703102-33)

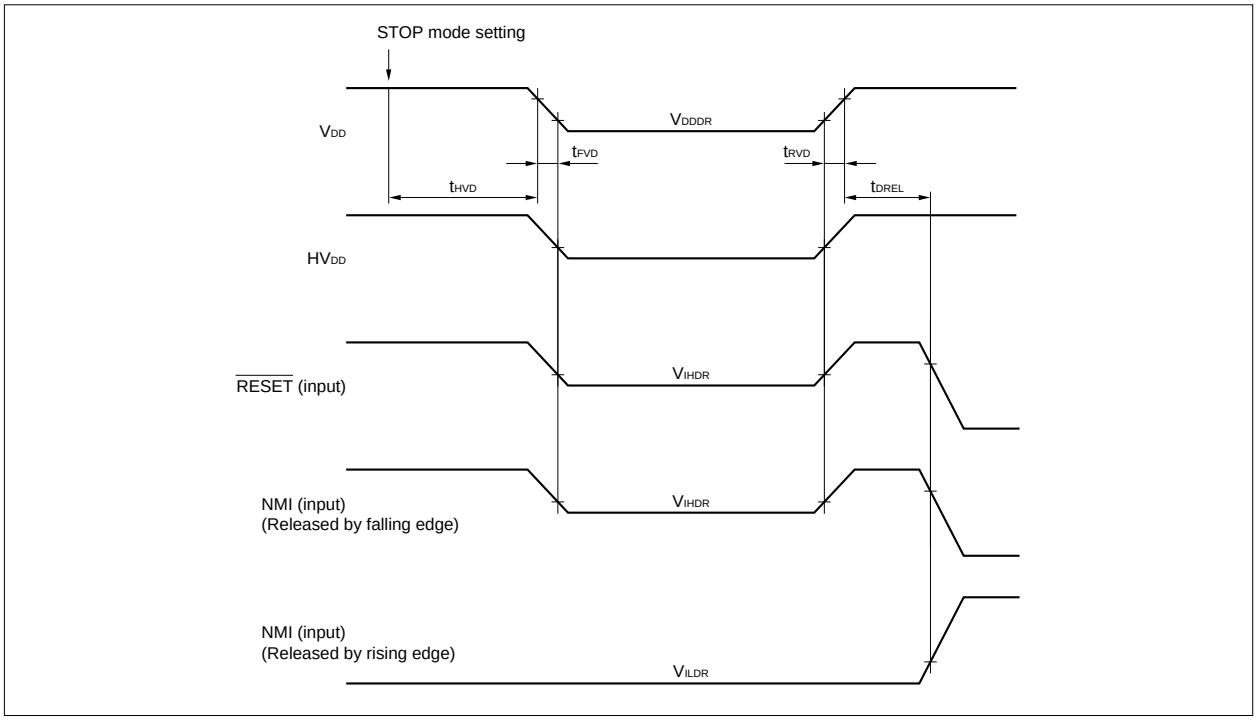
3. The unit for f_X is MHz.

Data Hold Characteristics (T_A = –40 to +70°C ... μPD703100-40, T_A = –40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode, $V_{DD} = V_{DDDR}$		1.5		3.6	V
	HV_{DDDR}	STOP mode, $HV_{DD} = HV_{DDDR}$		V_{DDDR}		5.5	V
Data hold current	I_{DDDR}	μPD703100-40	$V_{DD} = V_{DDDR}$		1.0	3.0	mA
		μPD703100-33, 703101-33, 703102-33	$V_{DD} = V_{DDDR}$		30	150	μA
Power supply voltage rise time	t_{RVD}			200			μs
Power supply voltage fall time	t_{FVD}			200			μs
Power supply voltage hold time (to STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold high-level input voltage	V_{IHDR}	**Note**		0.8HV_{DDDR}		HV_{DDDR}	V
Data hold low-level input voltage	V_{ILDR}	**Note**		0		0.2HV_{DDDR}	V

Note P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, Pl16/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

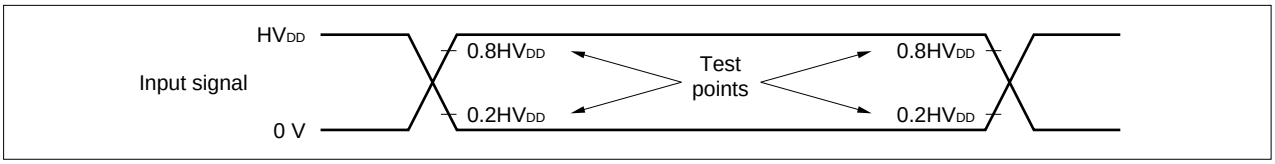
Remark TYP. values are reference values for when T_A = 25°C.


STOP mode setting
VDD
VDDDR
tFVD
tRVD
tHVD
tDREL
HVDD
RESET (input)
VIHDR
NMI (input)
(Released by falling edge)
VIHDR
NMI (input)
(Released by rising edge)
VILDR

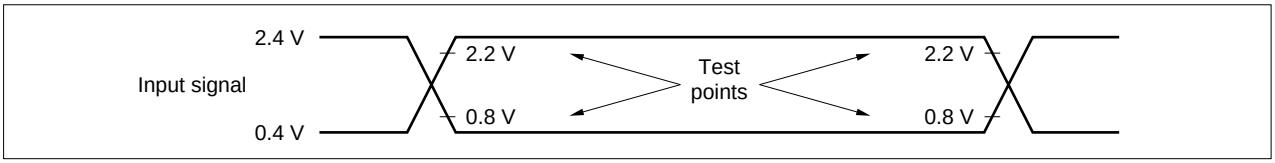
AC Characteristics (T_A = –40 to +70°C ... μPD703100-40, T_A = –40 to +85°C ... μPD703100-33, μPD703101-33, μPD703102-33, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 ±10%, V_{SS} = 0 V, output pin load capacitance: C_L = 50 pF)

AC Test Input Waveform

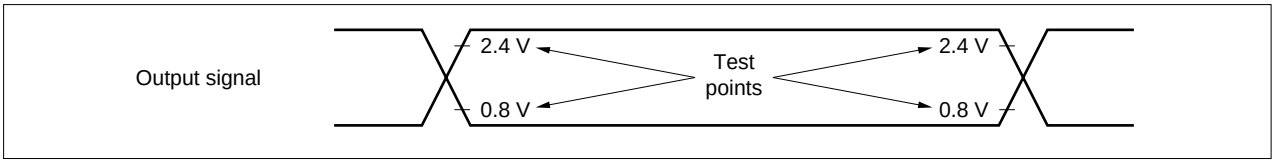
(a) P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$



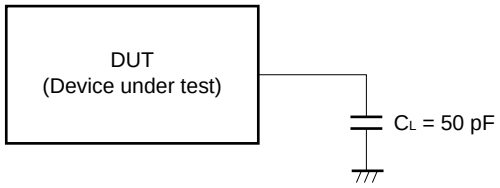
(b) Pins other than those listed in (a) above



AC Test Output Test Points



Load Condition

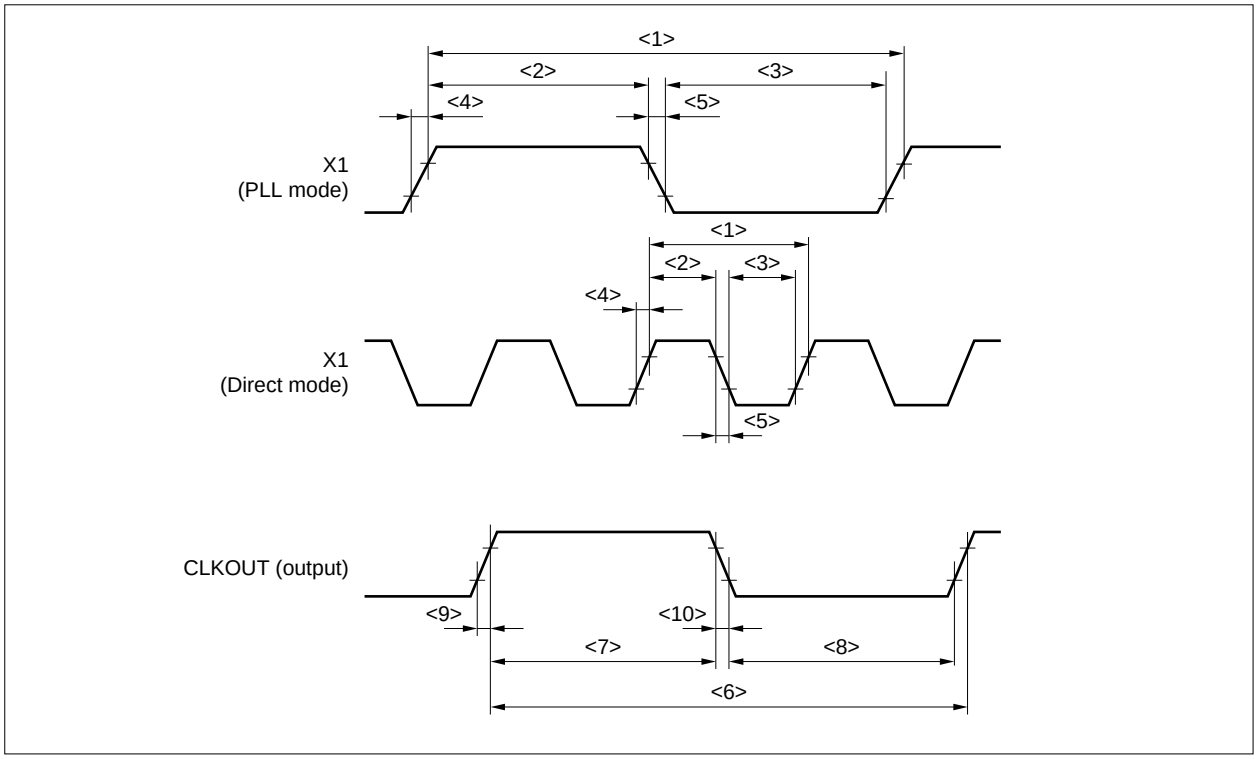


Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance 50 pF.

(1) Clock timing

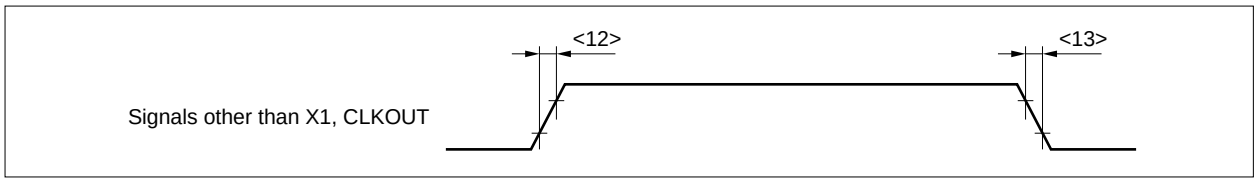
Parameter	Symbol		Condition		MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	μPD703100-40	12.5	250	ns
				μPD703100-33, 703101-33, 703102-33	15	250	ns
			PLL mode	μPD703100-40	125	250	ns
				μPD703100-33, 703101-33, 703102-33	150	250	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode		5		ns
			PLL mode		50		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode		5		ns
			PLL mode		50		ns
X1 input rise time	<4>	t_{XR}	Direct mode			4	ns
			PLL mode			10	ns
X1 input fall time	<5>	t_{XF}	Direct mode			4	ns
			PLL mode			10	ns
CLKOUT output cycle	<6>	t_{CYK}	μPD703100-40		25	500	ns
			μPD703100-33, 703101-33, 703102-33		30	500	ns
CLKOUT high-level width	<7>	t_{WKH}			0.5T – 7		ns
CLKOUT low-level width	<8>	t_{WKL}			0.5T – 4		ns
CLKOUT rise time	<9>	t_{KR}				5	ns
CLKOUT fall time	<10>	t_{KF}				5	ns

Remark T = t_{CYK}



(2) Output waveform (other than X1, CLKOUT)

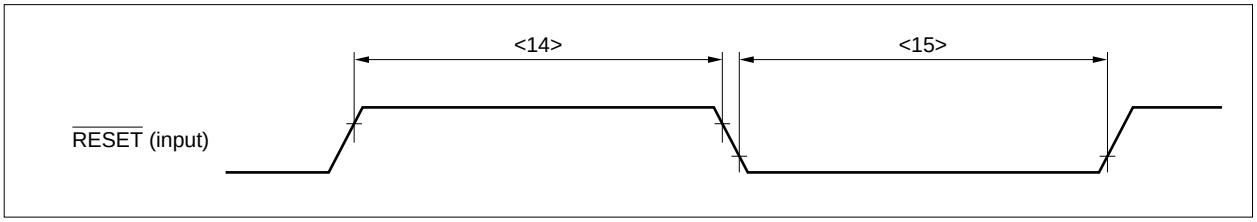
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t_{OR}			10	ns
Output fall time	<13>	t_{OF}			10	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t_{WRSL}	When power supply is on, and STOP mode has been released	500 + T_{OS}		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

Remark T_{OS}: Oscillation stabilization time



(4) SRAM, external ROM, or external I/O access timing

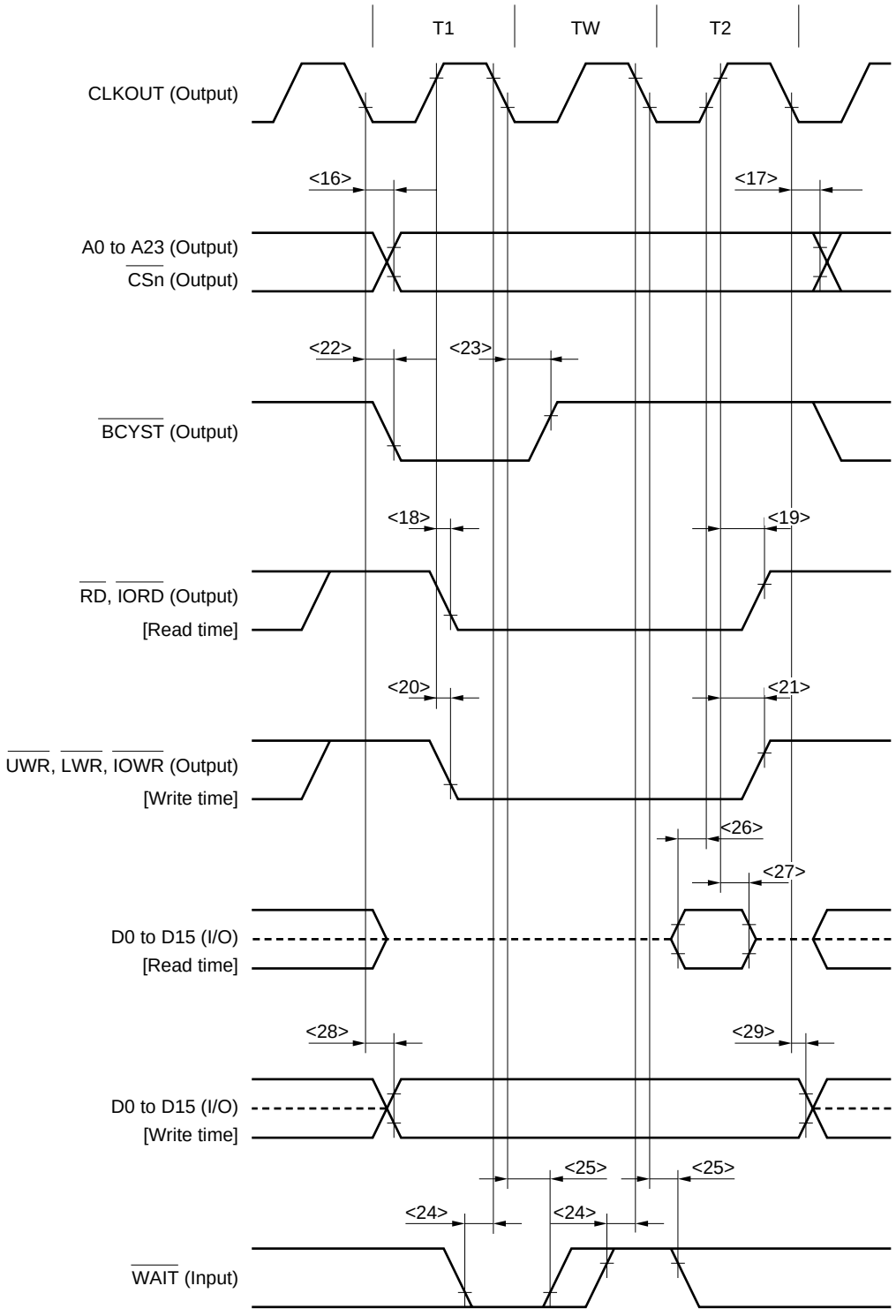
(a) Access timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT ↓)	<16>	t_{DKA}		2	10	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT ↓)	<17>	t_{HKA}		2	10	ns
$\overline{RD}$, $\overline{IORD}$ ↓ delay time (from CLKOUT ↑)	<18>	t_{DKRDL}		2	14	ns
$\overline{RD}$, $\overline{IORD}$ ↑ delay time (from CLKOUT ↑)	<19>	t_{HKRDH}		2	14	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↓ delay time (from CLKOUT ↑)	<20>	t_{DKWRL}		2	10	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑ delay time (from CLKOUT ↑)	<21>	t_{HKWRH}		2	10	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT ↓)	<22>	t_{DKBSL}		2	10	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT ↓)	<23>	t_{HKBSH}		2	10	ns
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Data output delay time (from CLKOUT ↓)	<28>	t_{DKOD}		2	10	ns
Data output hold time (from CLKOUT ↓)	<29>	t_{HKOD}		2	10	ns

Remarks 1. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

2. n = 0 to 7

(a) Access timing (SRAM, external ROM, or external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(b) Read timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w)T - 32$	ns
$\overline{RD}$, $\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$, $\overline{IORD}$ ↓	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{RD}$, $\overline{IORD}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Data input hold time (from $\overline{RD}$, $\overline{IORD}$ ↑)	<36>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$, $\overline{IORD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

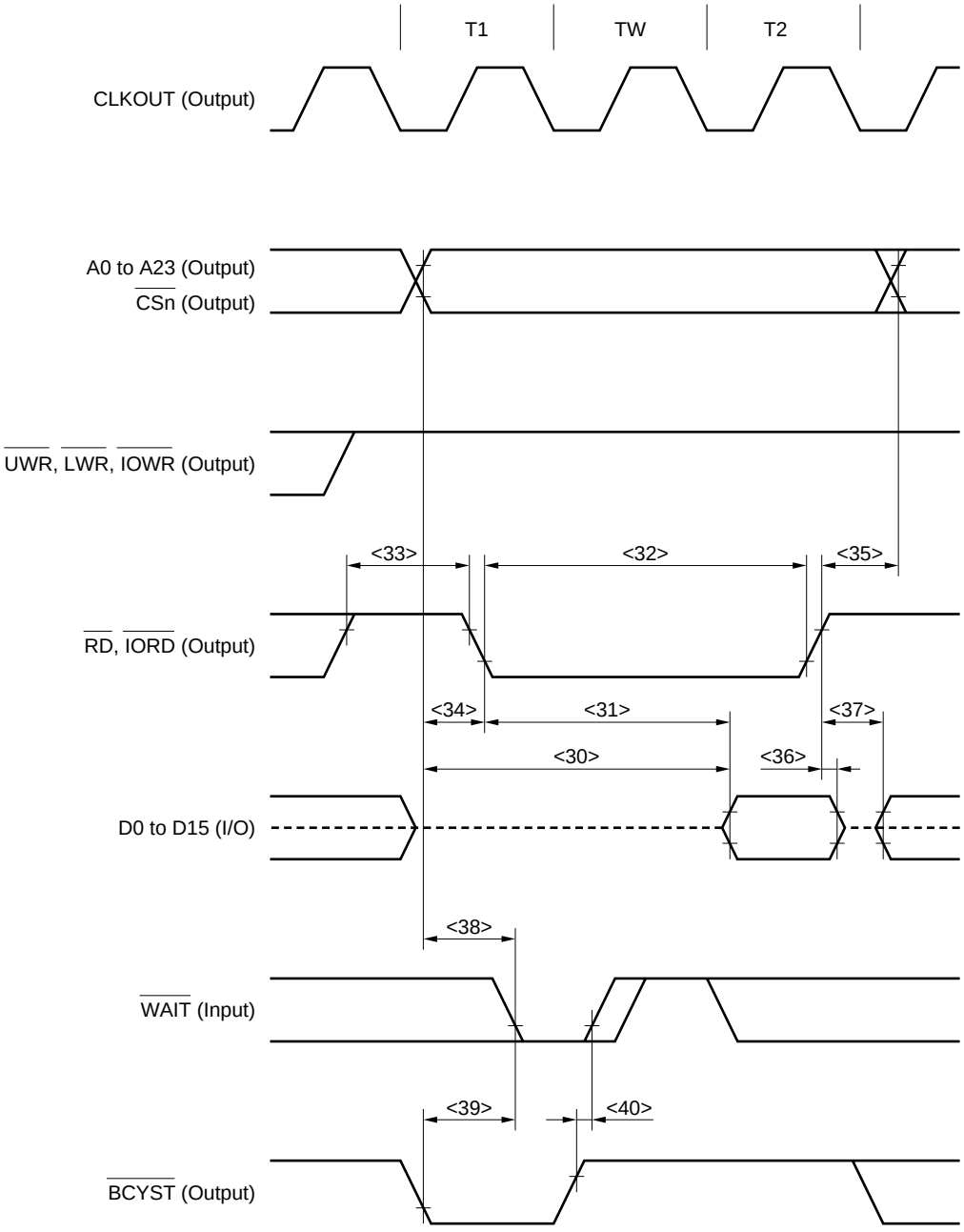
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. i: the number of idle states that are inserted when a write cycle follows a read cycle.

5. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

6. n = 0 to 7

(b) Read timing (SRAM, external ROM, or external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(c) Write timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 25	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		T – 25	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address, $\overline{CSn}$ to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↓	<41>	t_{DAWR}		0.5T – 10		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		(1.5 + w_D + w)T – 10		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑ to address	<43>	t_{DWRA}		0.5T – 10		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ low-level width	<45>	t_{WWRL}		($1 + w_D$ + w)T – 10		ns
Data output setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<46>	t_{SODWR}		(1.5 + w_D + w)T – 10		ns
Data output hold time (from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ ↑)	<47>	t_{HWROD}		0.5T – 10		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

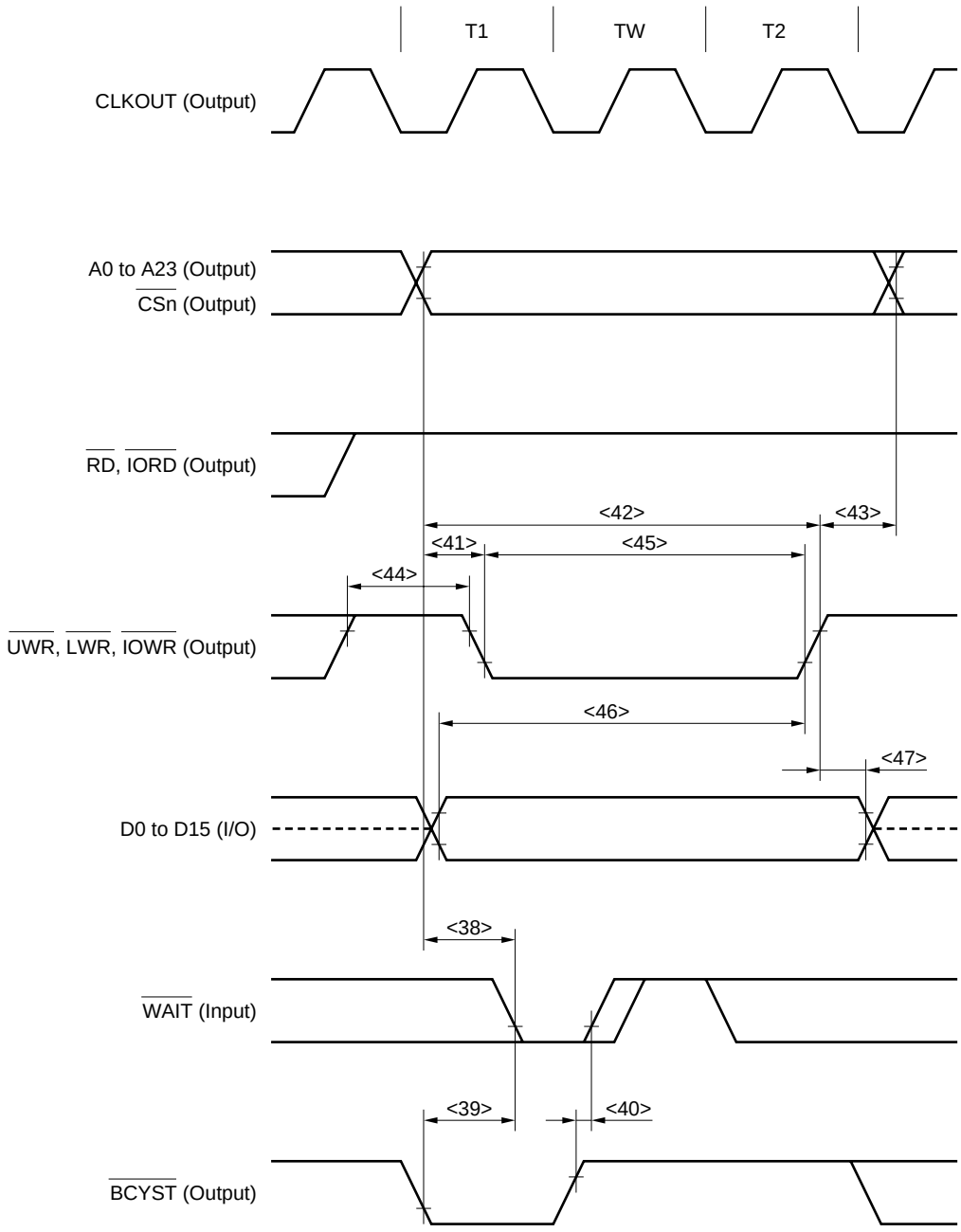
Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. n = 0 to 7

(c) Write timing (SRAM, external ROM, or external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{RD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{RD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$ ↓	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{RD}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Delay time from $\overline{RD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address to $\overline{IOWR}$ ↓	<41>	t_{DAWR}		$0.5T - 10$		ns
Address setup time (to $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{IOWR}$ ↑ to address	<43>	t_{DWRA}		$0.5T - 10$		ns
$\overline{IOWR}$ high-level width	<44>	t_{WWRH}		$T - 10$		ns
$\overline{IOWR}$ low-level width	<45>	t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{IOWR}$ ↑ to $\overline{RD}$ ↑	<48>	t_{DWRRD}	$w_F = 0$	0		ns
			$w_F = 1$	$T - 10$		ns
Delay time from $\overline{DMAAKm}$ ↓ to $\overline{IOWR}$ ↓	<49>	t_{DDAWR}		$0.5T - 10$		ns
Delay time from $\overline{IOWR}$ ↑ to $\overline{DMAAKm}$ ↑	<50>	t_{DWRDA}		$(0.5 + w_F)T - 10$		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

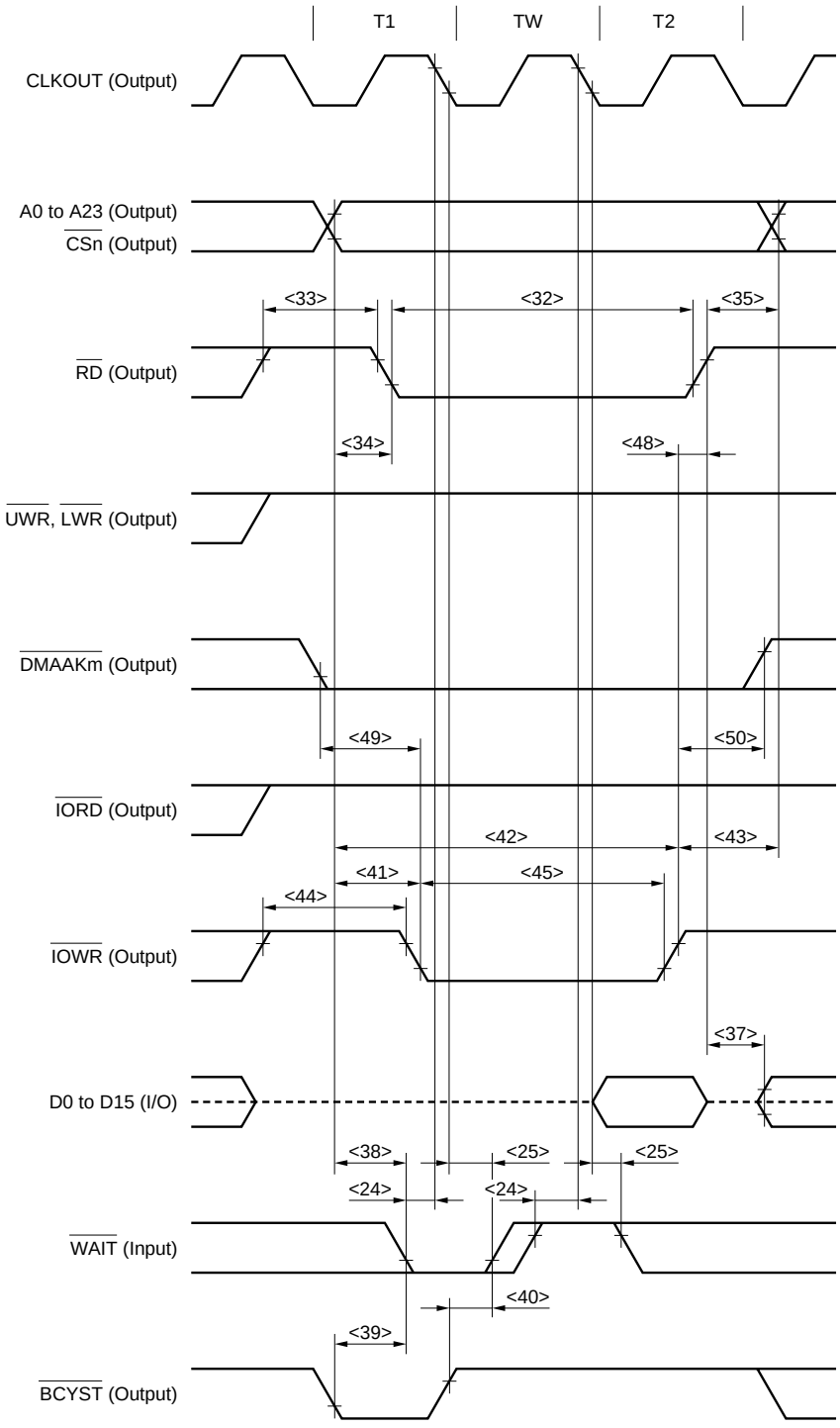
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0 to 7, m = 0 to 3

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{IORD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{IORD}$ ↓	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{IORD}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Delay time from $\overline{IORD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address to $\overline{UWR}$, $\overline{LWR}$ ↓	<41>	t_{DAWR}		$0.5T - 10$		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$ ↑)	<42>	t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$ to address	<43>	t_{DWRA}		$0.5T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$ high-level width	<44>	t_{WWRH}		$T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$ low-level width	<45>	t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$↑ to $\overline{IORD}$ ↑	<48>	t_{DWRRD}	$w_F = 0$	0		ns
			$w_F = 1$	$T - 10$		ns
Delay time from $\overline{DMAAKm}$ ↓ to $\overline{IORD}$ ↓	<51>	t_{DDARD}		$0.5T - 10$		ns
Delay time from $\overline{IORD}$ ↑ to $\overline{DMAAKm}$ ↑	<52>	t_{DRDDA}		$0.5T - 10$		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

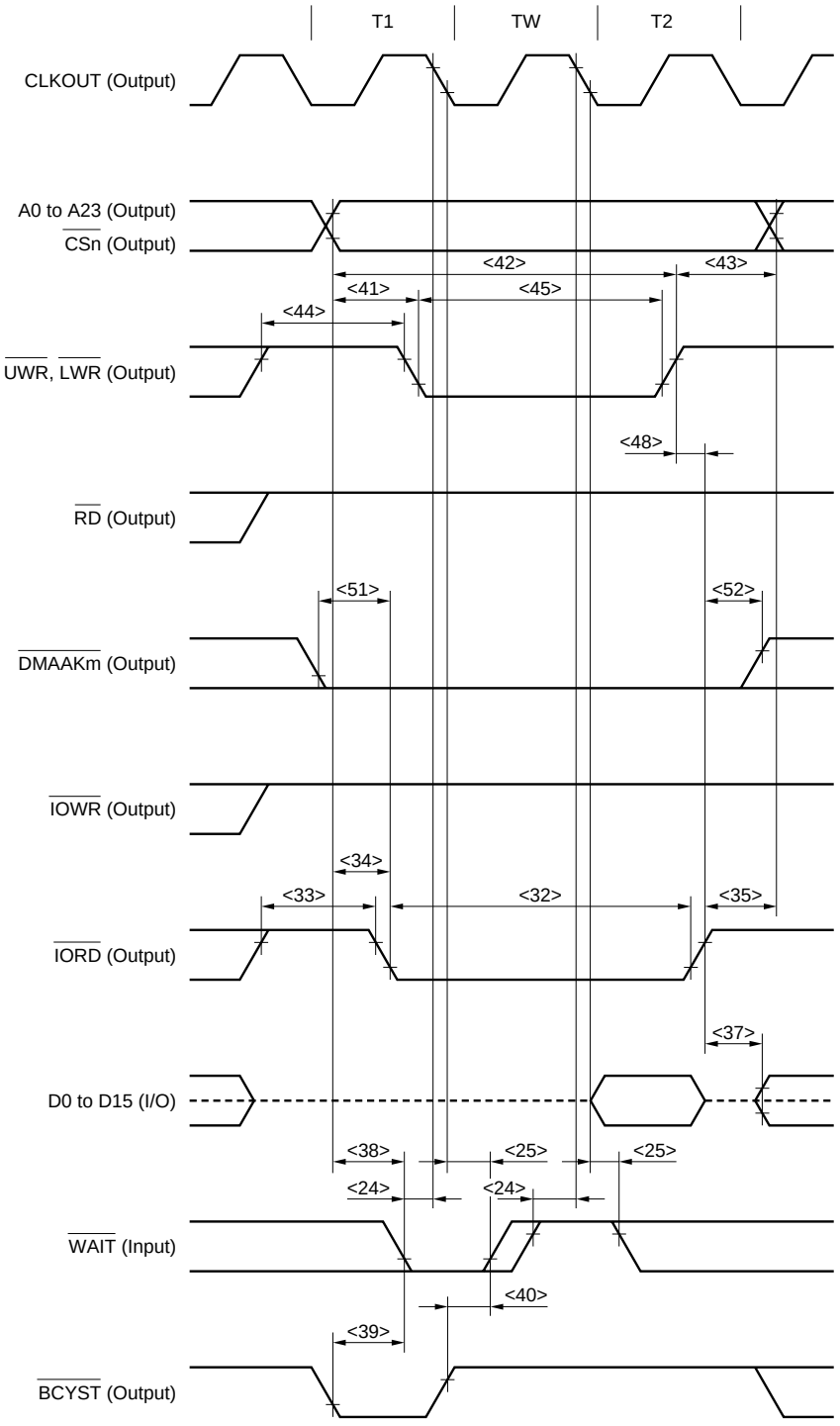
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(5) Page ROM access timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Off-page data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Off-page data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w)T - 32$	ns
Off-page $\overline{RD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{RD}$ high-level width	<33>	t_{WRDH}		$0.5T - 10$		ns
Data input hold time (from $\overline{RD}$)	<36>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
On-page $\overline{RD}$ low-level width	<53>	t_{WORDL}		$(1.5 + w_{PR} + w)T - 10$		ns
On-page data input setup time (to address)	<54>	t_{SOAID}			$(1.5 + w_{PR} + w)T - 28$	ns
On-page data input setup time (to $\overline{RD}$)	<55>	t_{SORDID}			$(1.5 + w_{PR} + w)T - 32$	ns

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

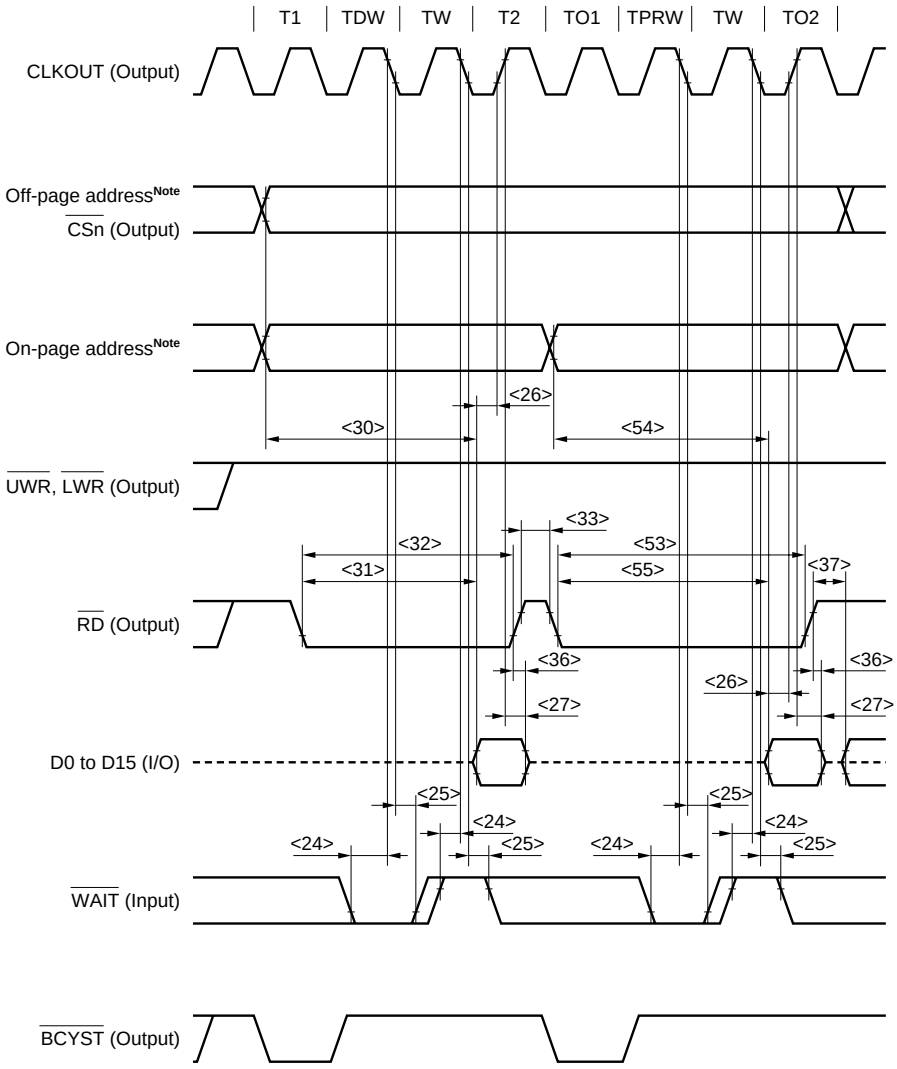
3. w_D: the number of waits due to the DWC1 and DWC2 registers.

4. w_{PR}: the number of waits due to the PRC register.

5. i: the number of idle states that are inserted when a write cycle follows a read cycle.

6. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

(5) Page ROM access timing (2/2)



Note On-page and off-page addresses are as follows.

PRC Register			On-page Addresses	Off-page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

Remarks 1. This is the timing for the following case.
Number of waits due to the DWC1 and DWC2 registers (TDW): 1
Number of waits due to the PRC register (TPRW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Row address setup time	<56>	t_{ASR}		(0.5 + w_{RP})T – 10		ns
Row address hold time	<57>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA} + w)T – 10		ns
Read/write cycle time	<60>	t_{RC}		(3 + w_{RP} + w_{RH} + w_{DA} + w)T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		(0.5 + w_{RP})T – 10		ns
$\overline{RAS}$ pulse time	<62>	t_{RAS}		(2.5 + w_{RH} + w_{DA} + w)T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA} + w)T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{DA} + w)T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA} + w)T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		(1 + w_{RP})T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		(2 + w_{RH} + w_{DA} + w)T – 10		ns
$\overline{WE}$ setup time	<68>	t_{RCS}		(2 + w_{RP} + w_{RH})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t_{RCH}		T – 10		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		(2 + w_{RP} + w_{RH})T – 10		ns
Output enable access time	<72>	t_{OEA}			(2 + w_{RP} + w_{RH} + w_{DA} + w)T – 28	ns
$\overline{RAS}$ access time	<73>	t_{RAC}			(2 + w_{RH} + w_{DA} + w)T – 28	ns
Access time from column address	<74>	t_{AA}			(1.5 + w_{DA} + w)T – 28	ns
$\overline{CAS}$ access time	<75>	t_{CAC}			(1 + w_{DA} + w)T – 28	ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: the number of idle states that are inserted when a write cycle follows a read cycle.

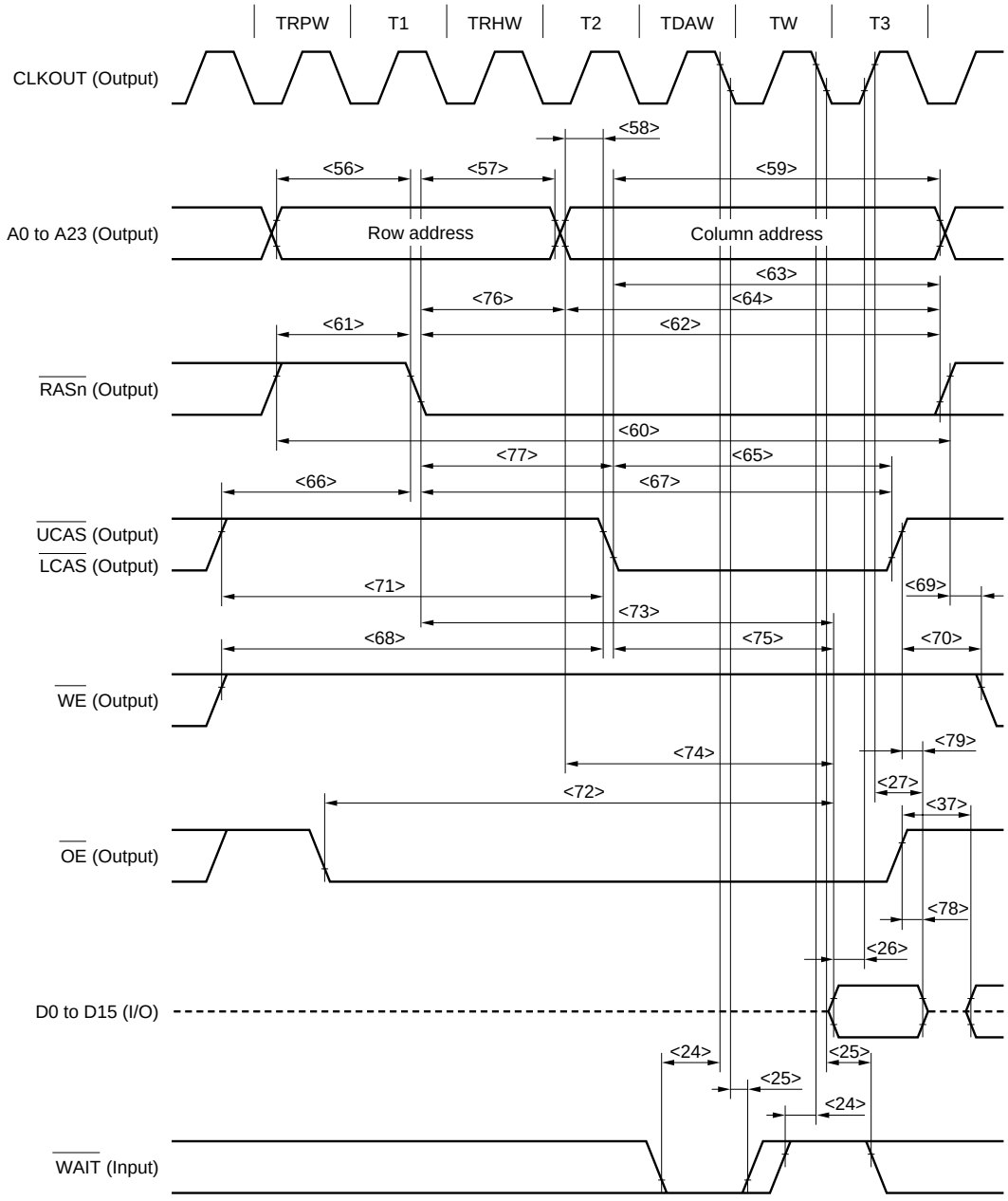
(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{RAS}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)	<79>	t_{OFF}		0		ns

Remarks 1. $T = t_{CYK}$

2. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

[MEMO]

(b) Read timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Column address setup time	<58>	t_{ASC}		(0.5 + w_{CP})T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA})T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA})T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{CP} + w_{DA})T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA})T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<68>	t_{RCS}		(1 + w_{CP})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)	<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)	<70>	t_{RCH}		T – 10		ns
Output enable access time	<72>	t_{OEA}			(1 + w_{CP} + w_{DA})T – 28	ns
Access time from column address	<74>	t_{AA}			(1.5 + w_{CP} + w_{DA})T – 28	ns
$\overline{CAS}$ access time	<75>	t_{CAC}			(1 + w_{DA})T – 28	ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)	<79>	t_{OFF}		0		ns
Access time from $\overline{CAS}$ precharge	<80>	t_{ACP}			(2 + w_{CP} + w_{DA})T – 28	ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		(1 + w_{CP})T – 10		ns
High-speed page mode cycle time	<82>	t_{PC}		(2 + w_{CP} + w_{DA})T – 10		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		(2.5 + w_{CP} + w_{DA})T – 10		ns

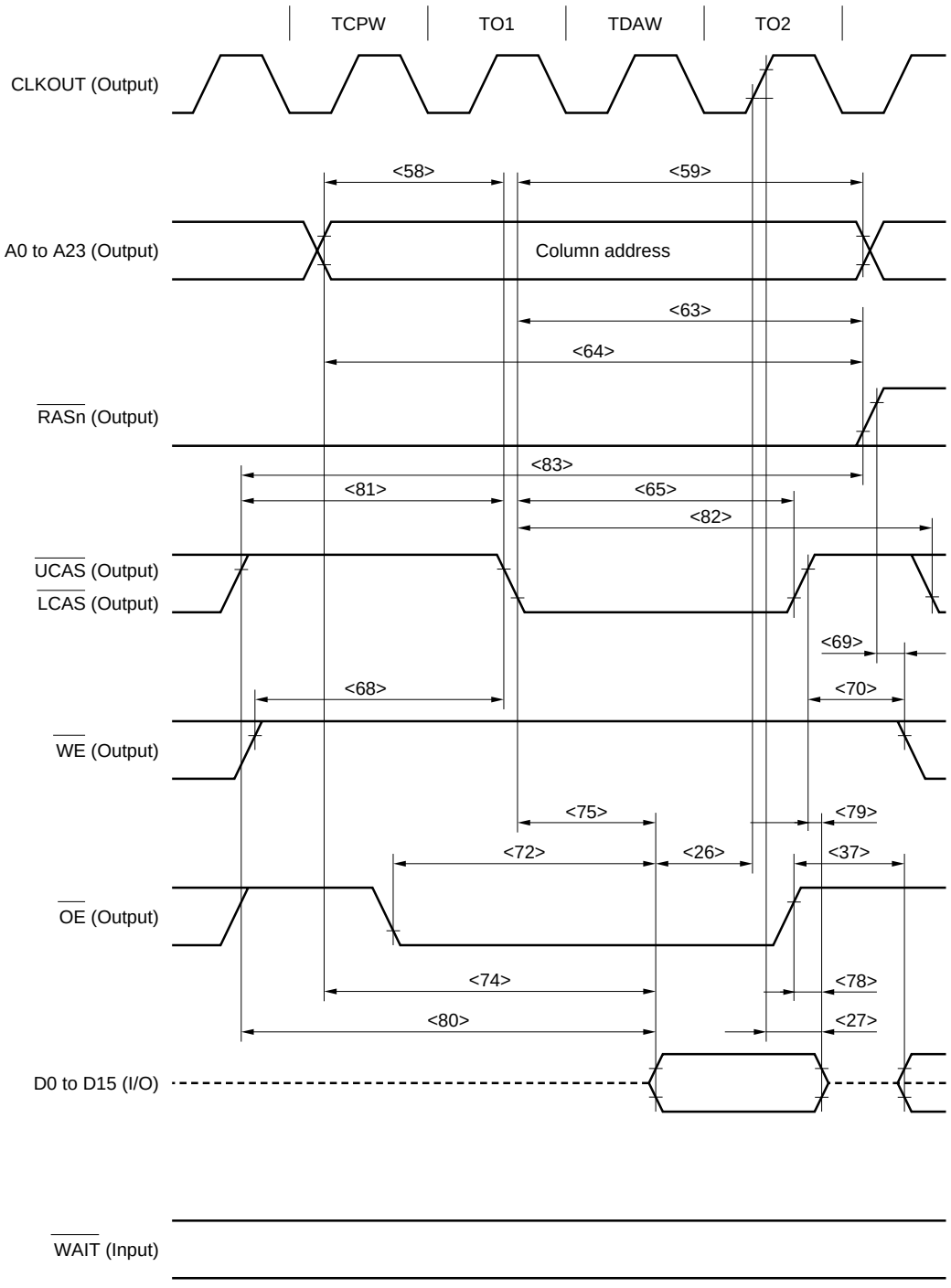
Remarks 1. T = t_{CYK}

2. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(b) Read timing (high-speed page DRAM access: on-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time	<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w)T - 10$		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{RAS}$ pulse time	<62>	t_{RAS}		$(2.5 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w)T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t_{RAL}		$(2 + w_{DA} + w)T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w)T - 10$		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		$(1 + w_{RH})T - 10$		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})T - 10$		ns
$\overline{RAS}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<84>	t_{WCS}		$(1 + w_{RP} + w_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA} + w)T - 10$		ns
Data setup time (to $\overline{CAS}$ ↓)	<86>	t_{DS}		$(1.5 + w_{RP} + w_{RH})T - 10$		ns
Data hold time (from $\overline{CAS}$ ↓)	<87>	t_{DH}		$(1.5 + w_{DA} + w)T - 10$		ns

Remarks 1. $T = t_{CYK}$

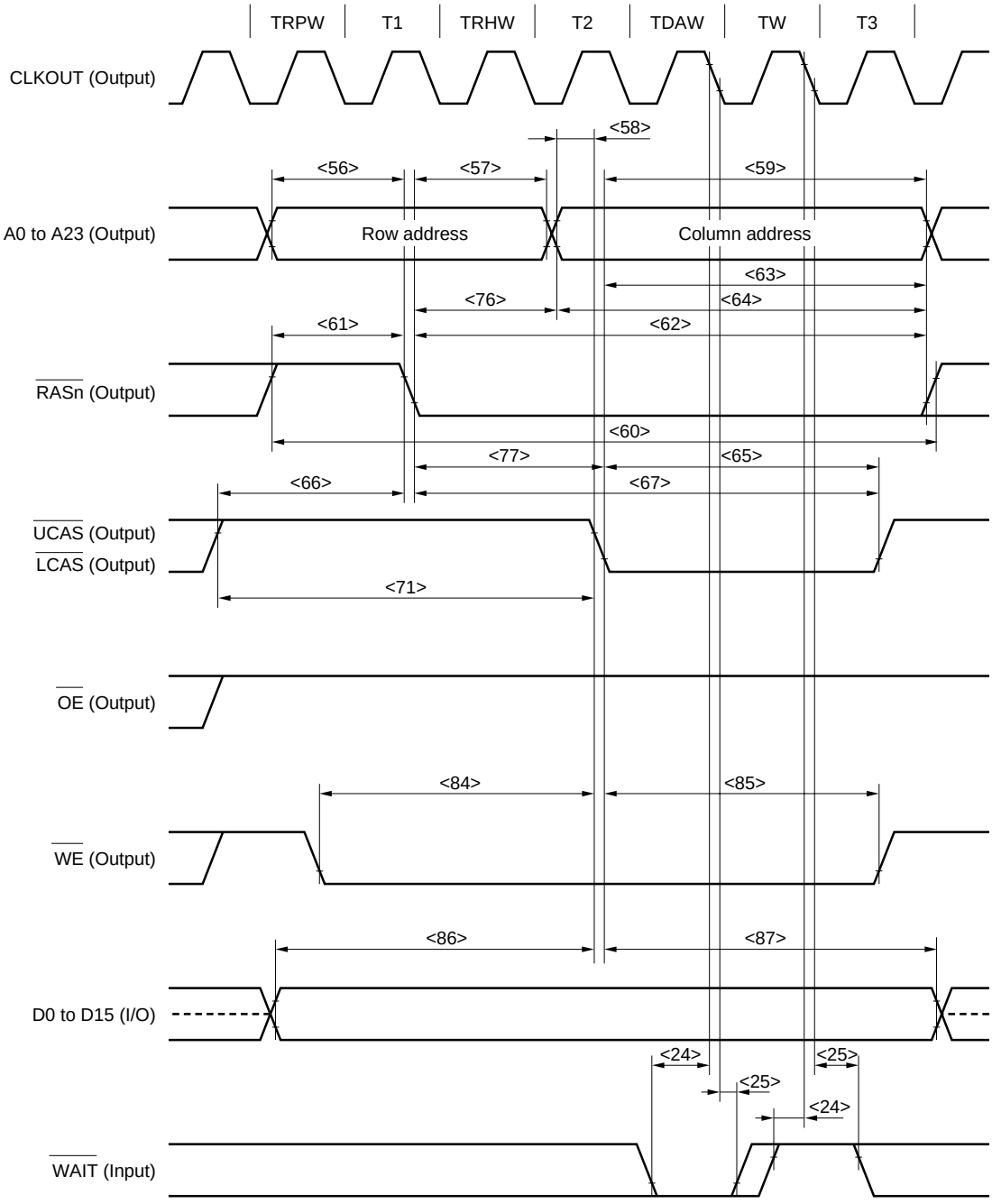
2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(d) Write timing (high-speed page DRAM access: on-page) (1/2)

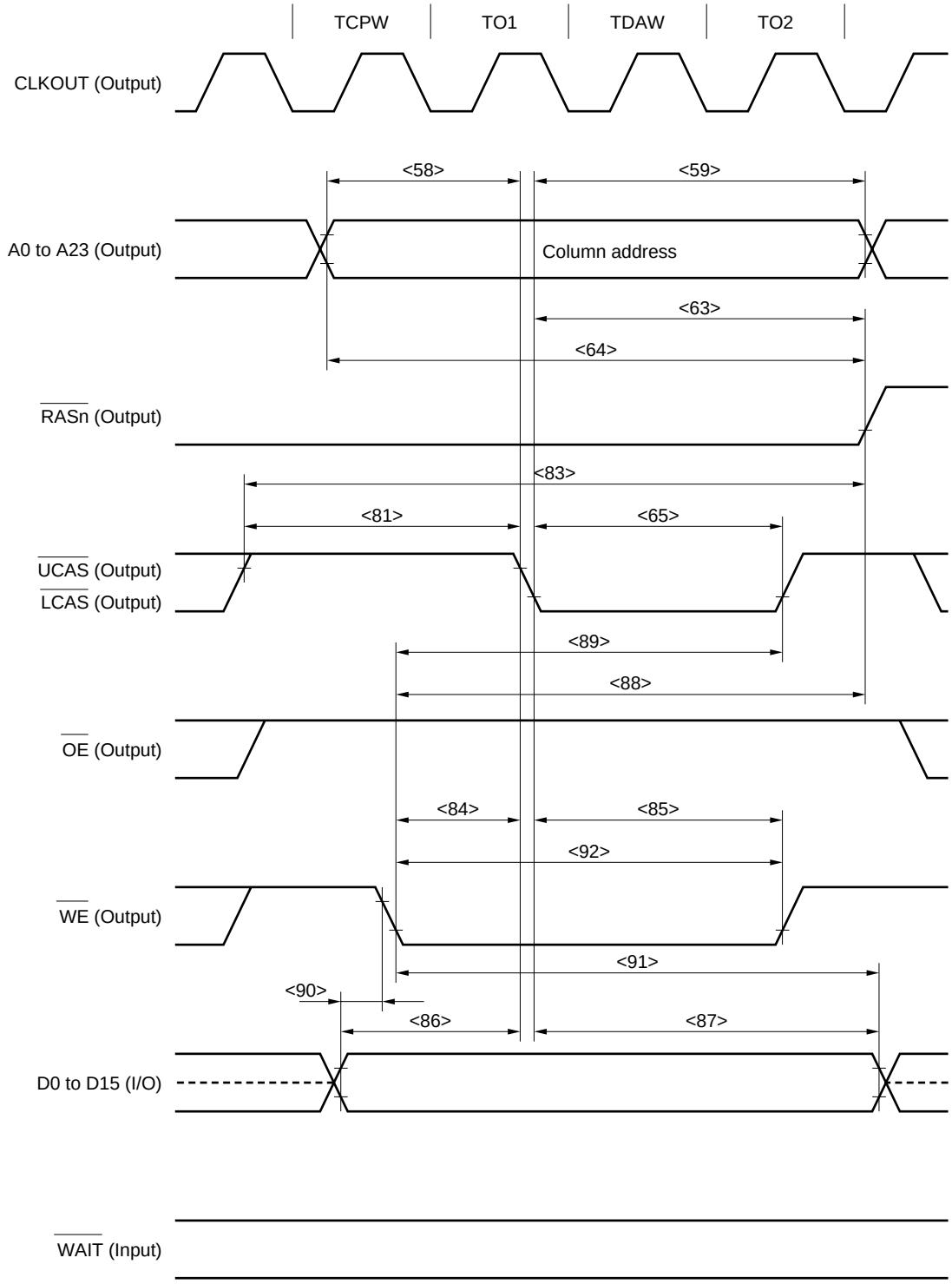
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Column address setup time	<58>	t_{ASC}		$(0.5 + w_{CP})T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA})T - 10$		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA})T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA})T - 10$		ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		$(1 + w_{CP})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<84>	t_{WCS}	$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Data setup time (to $\overline{CAS}$ ↓)	<86>	t_{DS}		$(0.5 + w_{CP})T - 10$		ns
Data hold time (from $\overline{CAS}$ ↓)	<87>	t_{DH}		$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)	<89>	t_{CWL}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns
Data setup time (to $\overline{WE}$ ↓)	<90>	t_{DSWE}	$w_{CP} = 0$	$0.5T - 10$		ns
Data hold time (from $\overline{WE}$ ↓)	<91>	t_{DHWE}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ pulse width	<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(d) Write timing (high-speed page DRAM access: on-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(e) Read timing (EDO DRAM) (1/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)		<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)		<27>	t_{HKID}		2		ns
Delay time from $\overline{OE}$ ↑ to data output		<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Row address setup time		<56>	t_{ASR}		(0.5 + w_{RP})T – 10		ns
Row address hold time		<57>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time		<58>	t_{ASC}		0.5T – 10		ns
Column address hold time		<59>	t_{CAH}		(0.5 + w_{DA})T – 10		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		(0.5 + w_{RP})T – 10		ns
Column address read time (from $\overline{RAS}$ ↑)		<64>	t_{RAL}		(2 + w_{CP} + w_{DA})T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		(1 + w_{RP})T – 10		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		(1.5 + w_{RH} + w_{DA})T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)		<68>	t_{RCS}		(2 + w_{RP} + w_{RH})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)		<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)		<70>	t_{RCH}		1.5T – 10		ns
$\overline{RAS}$ access time		<73>	t_{RAC}			(2 + w_{RH} + w_{DA})T – 28	ns
Access time from column address		<74>	t_{AA}			(1.5 + w_{DA})T – 28	ns
$\overline{CAS}$ access time		<75>	t_{CAC}			(1 + w_{DA})T – 28	ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}		(0.5 + w_{RH})T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		(1 + w_{RH})T – 10		ns
Output buffer turn-off delay time (from $\overline{OE}$)		<78>	t_{OEZ}		0		ns
Access time from $\overline{CAS}$ precharge		<80>	t_{ACP}			(1.5 + w_{CP} + w_{DA})T – 28	ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		(0.5 + w_{CP})T – 10		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		(2 + w_{CP} + w_{DA})T – 10		ns
Read cycle time		<93>	t_{HPC}		(1 + w_{DA} + w_{CP})T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		(2.5 + w_{RH} + w_{DA})T – 10		ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		(0.5 + w_{DA})T – 10		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<96>	t_{OCH1}		(2 + w_{RH} + w_{DA})T – 10		ns
	On-page	<97>	t_{OCH2}		(0.5 + w_{DA})T – 10		ns
Data input hold time (from $\overline{CAS}$ ↓)		<98>	t_{DHC}		0		ns

Remarks 1. T = t_{CYK}

2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t_{OEA1}			$(2 + w_{RP} + w_{RH} + w_{DA})T - 28$	ns
	On-page	<100>	t_{OEA2}			$(1 + w_{CP} + w_{DA})T - 28$	ns

Remarks 1. $T = t_{CYK}$

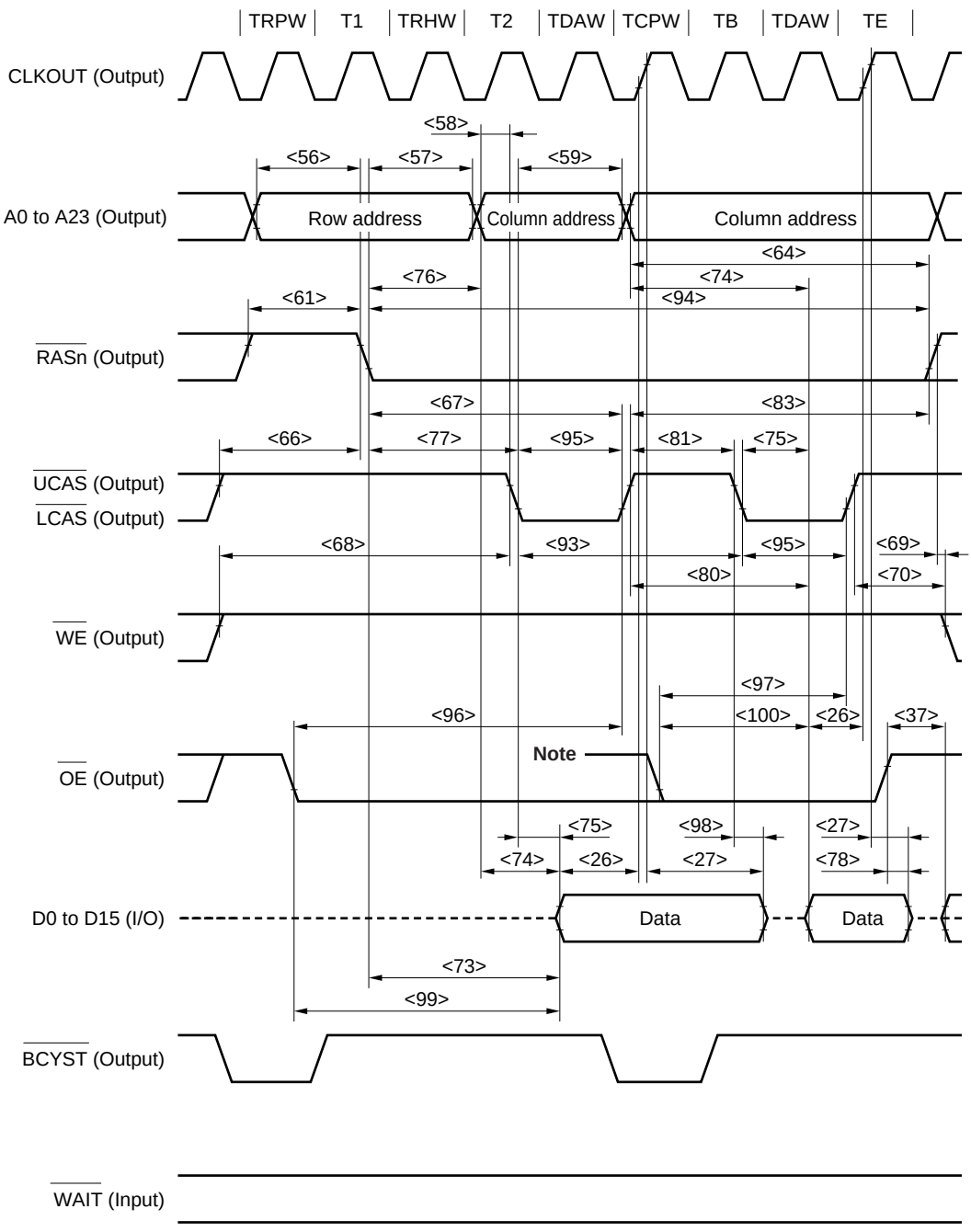
2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(e) Read timing (EDO DRAM) (3/3)



Note For on-page access from another cycle during the $\overline{\text{RASn}}$ low-level signal.

Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

[MEMO]

(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Row address setup time		<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time		<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time		<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time		<59>	t_{CAH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{RAS}$ hold time		<63>	t_{RSH}		$(1.5 + w_{DA})T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)		<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		$(1 + w_{RP})T - 10$		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		$(1.5 + w_{RH} + w_{DA})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)		<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Data hold time (from $\overline{CAS}$ ↓)		<87>	t_{DH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	On-page	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)	On-page	<89>	t_{CWL}	$w_{CP} = 0$	$(0.5 + w_{DA})T - 10$		ns
$\overline{WE}$ pulse width	On-page	<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns
Write cycle time		<93>	t_{HPC}		$(1 + w_{DA} + w_{CP})T - 10$		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA})T - 10$		ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		$(0.5 + w_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	Off-page	<101>	t_{WCS1}		$(1 + w_{RP} + w_{RH})T - 10$		ns
	On-page	<102>	t_{WCS2}	$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
Data setup time (to $\overline{CAS}$ ↓)	Off-page	<103>	t_{DS1}		$(1.5 + w_{RP} + w_{RH})T - 10$		ns
	On-page	<104>	t_{DS2}		$(0.5 + w_{CP})T - 10$		ns

Remarks 1. $T = t_{CYK}$

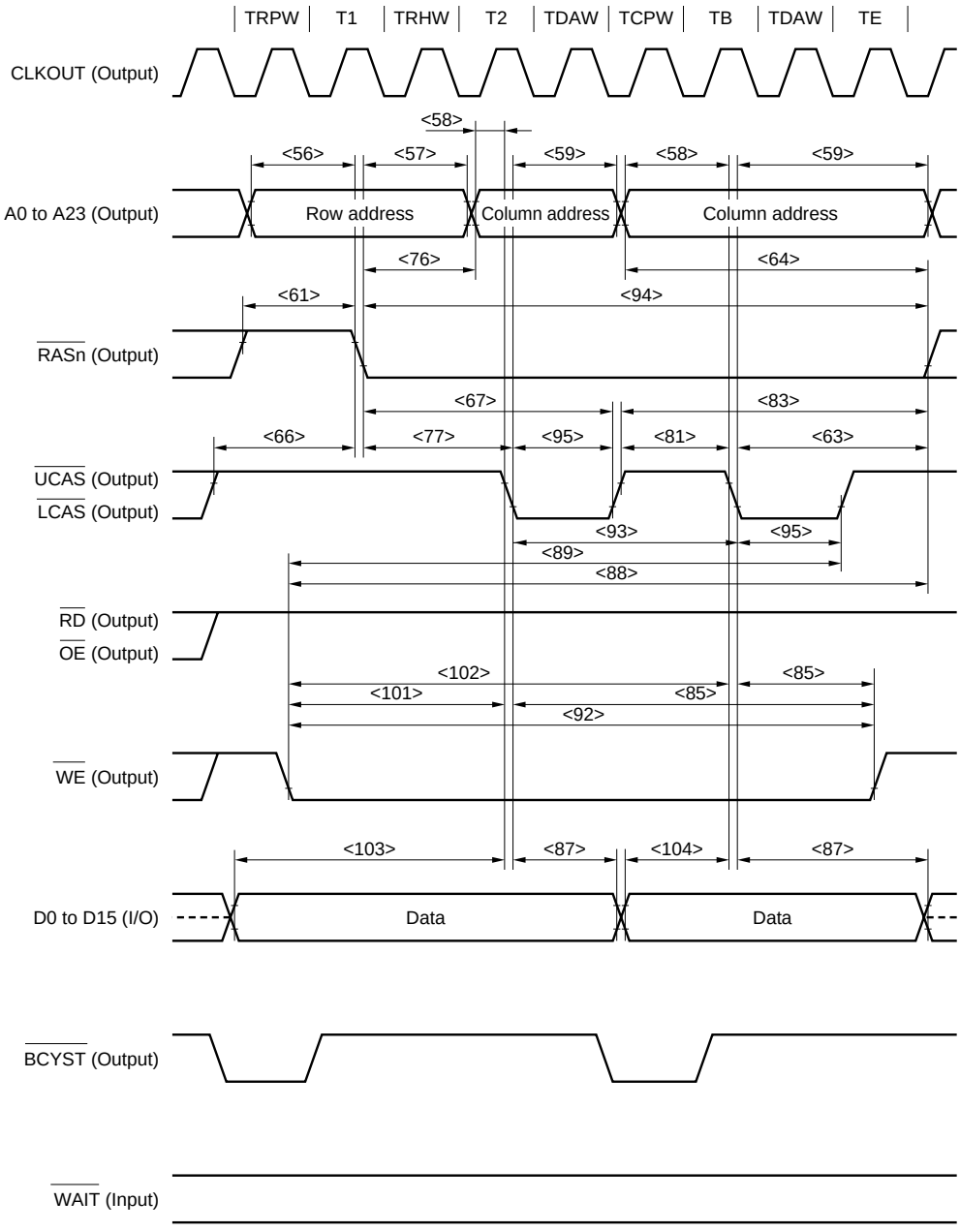
2. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(f) Write timing (EDO DRAM) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Delay time from address to $\overline{IOWR}$ ↓	<41>	t_{DAWR}		(0.5 + w_{RP})T – 10		ns
Address setup time (to $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		(2 + w_{RP} + w_{RH} + w_{DA} + w)T – 10		ns
Delay time from $\overline{IOWR}$ ↑ to address	<43>	t_{DWRA}		0.5T – 10		ns
Delay time from $\overline{IOWR}$ ↑ to $\overline{RD}$ ↑	<48>	t_{DWRRD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns
$\overline{IOWR}$ low-level width	<50>	t_{WWRL}		(2 + w_{RH} + w_{DA} + w)T – 10		ns
Row address setup time	<56>	t_{ASR}		(0.5 + w_{RP})T – 10		ns
Row address hold time	<57>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA} + w_F + w)T – 10		ns
Read/write cycle time	<60>	t_{RC}		(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		(0.5 + w_{RP})T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA} + w_F + w)T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{CP} + w_{DA} + w_F + w)T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA} + w_F + w)T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		(1 + w_{RP})T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		(2 + w_{RH} + w_{DA} + w_F + w)T – 10		ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. i: the number of idle states that are inserted when a write cycle follows a read cycle.

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)		<68>	t_{RCS}		$(2 + w_{RP} + w_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)		<69>	t_{RRH}		$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)		<70>	t_{RCH}		$1.5T - 10$		ns
$\overline{CAS}$ precharge time		<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)		<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)		<79>	t_{OFF}		0		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})T - 10$		ns
High-speed page mode cycle time		<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$ (from $\overline{CAS}$ ↑)	Off-page	<96>	t_{OCH1}		$(2.5 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
	On-page	<97>	t_{OCH2}		$(1.5 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
Delay time from $\overline{DMAAKm}$ ↓ to $\overline{CAS}$ ↓		<105>	t_{DDACS}		$(1.5 + w_{RH})T - 10$		ns
Delay time from $\overline{IOWR}$ ↓ to $\overline{CAS}$ ↓		<106>	t_{DRDCS}		$(1 + w_{RH})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

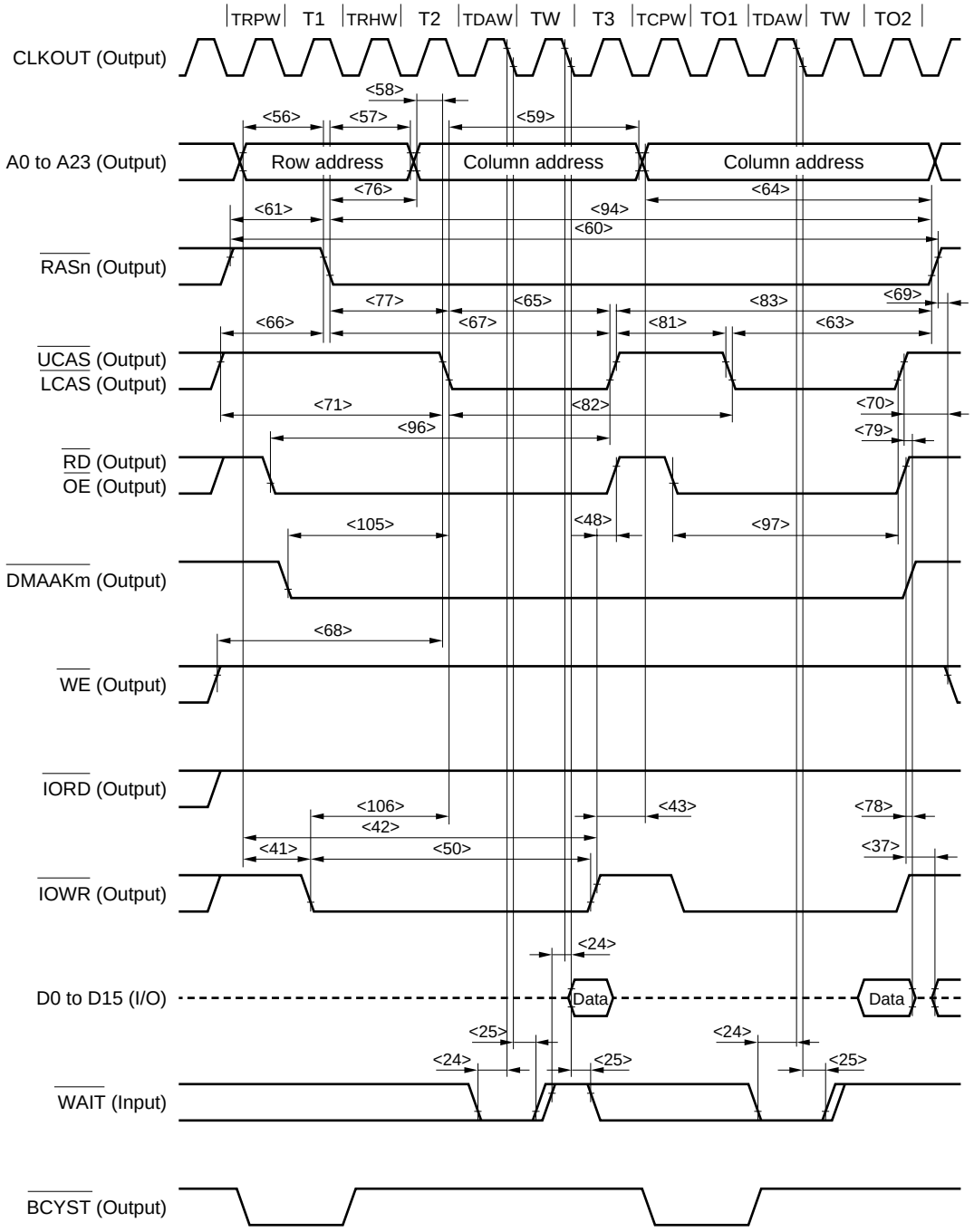
5. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. m = 0 to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(2 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{IORD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address to $\overline{IORD}$ ↑	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{IORD}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time	<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w_F)T - 10$		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w_F)T - 10$		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w_F)T - 10$		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		$(1 + w_{RP})T - 10$		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{CAS}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH} + w)T - 10$		ns
Delay time from $\overline{RAS}$ to column address	<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time	<77>	t_{RCD}		$(1 + w_{RH} + w)T - 10$		ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		$(0.5 + w_{CP} + w)T - 10$		ns
High-speed page mode cycle time	<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w)T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA} + w)T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. i: the number of idle states that are inserted when a write cycle follows a read cycle.

9. n = 0 to 7

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)		<89>	t_{CWL}	w_{CP} = 0	(1 + w_{DA} + w)T – 10		ns
$\overline{WE}$ pulse width		<92>	t_{WP}	w_{CP} = 0	(1 + w_{DA} + w)T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		(2.5 + w_{RH} + w_{DA} + w_F + w)T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	Off-page	<101>	t_{WCS1}	w_{CP} = 0	(1 + w_{RH} + w_{RP} + w)T – 10		ns
	On-page	<102>	t_{WCS2}	w_{CP} ≥ 1	w_{CP}T – 10		ns
Delay time from $\overline{DMAAKm}$ ↓ to $\overline{CAS}$ ↓		<105>	t_{DDACS}		(1.5 + w_{RH} + w)T – 10		ns
Delay time from $\overline{IORD}$ ↓ to $\overline{CAS}$ ↓		<106>	t_{DRDCS}		(1 + w_{RH} + w)T – 10		ns
Delay time from $\overline{WE}$ ↑ to $\overline{IORD}$ ↑		<107>	t_{DWERD}	w_F = 0	0		ns
				w_F = 1	T – 10		ns

Remarks 1. T = t_{CYK}

2. w: the number of waits due to $\overline{WAIT}$.

3. w_{RH}: the number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: the number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

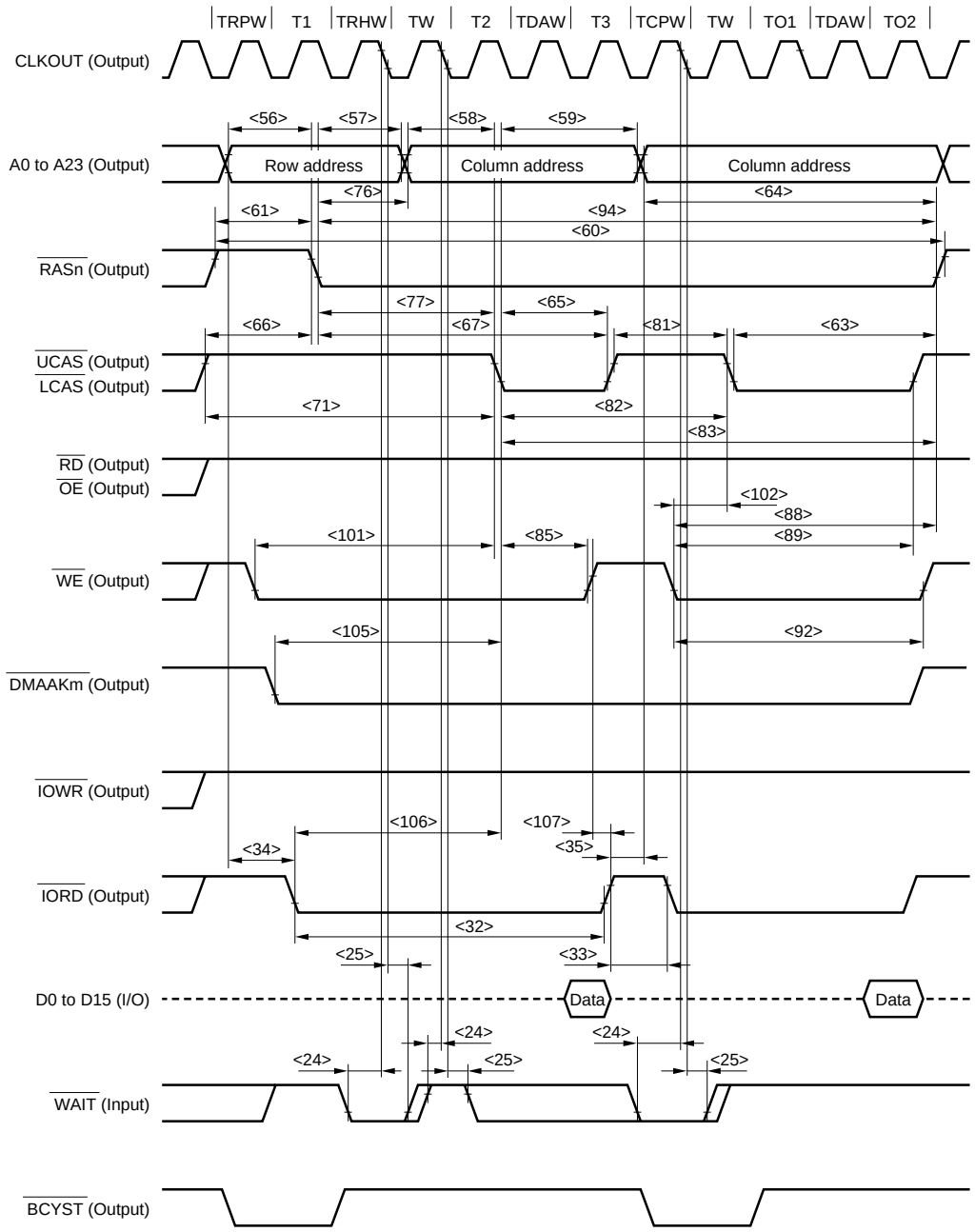
5. w_{RP}: the number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. w_{CP}: the number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

7. w_F: the number of waits that are inserted for a source-side access during a DMA flyby transfer.

8. m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(i) CBR refresh timing

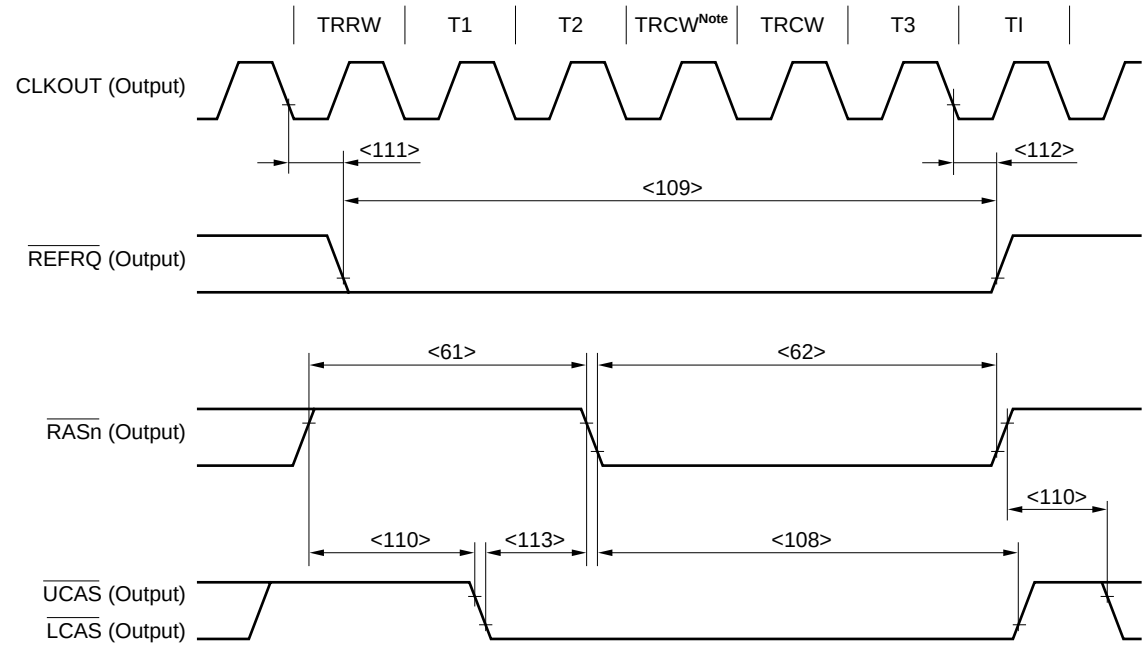
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{RAS}$ precharge time	<61>	t_{RP}		$(1.5 + w_{RRW})T - 10$		ns
$\overline{RAS}$ pulse width	<62>	t_{RAS}		$(1.5 + w_{RCW}^{Note})T - 10$		ns
$\overline{CAS}$ hold time	<108>	t_{CHR}		$(1.5 + w_{RCW}^{Note})T - 10$		ns
$\overline{REFRQ}$ pulse width	<109>	t_{WRFL}		$(3 + w_{RRW} + w_{RCW}^{Note})T - 10$		ns
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	<110>	t_{RPC}		$(0.5 + w_{RRW})T - 10$		ns
$\overline{REFRQ}$ active delay time (from CLKOUT ↓)	<111>	t_{DKRF}		2	10	ns
$\overline{REFRQ}$ inactive delay time (from CLKOUT ↓)	<112>	t_{HKRF}		2	10	ns
$\overline{CAS}$ setup time	<113>	t_{CSR}		T – 10		ns

Note At least one clock cycle is inserted by default for w_{RCW} regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. $T = t_{CYK}$

2. w_{RRW}: the number of waits due to the RRW0 and RRW1 bits of the RWC register.

3. w_{RCW}: the number of waits due to the RCW0 to RCW2 bits of the RWC register.



Note This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.
Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1
Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 2

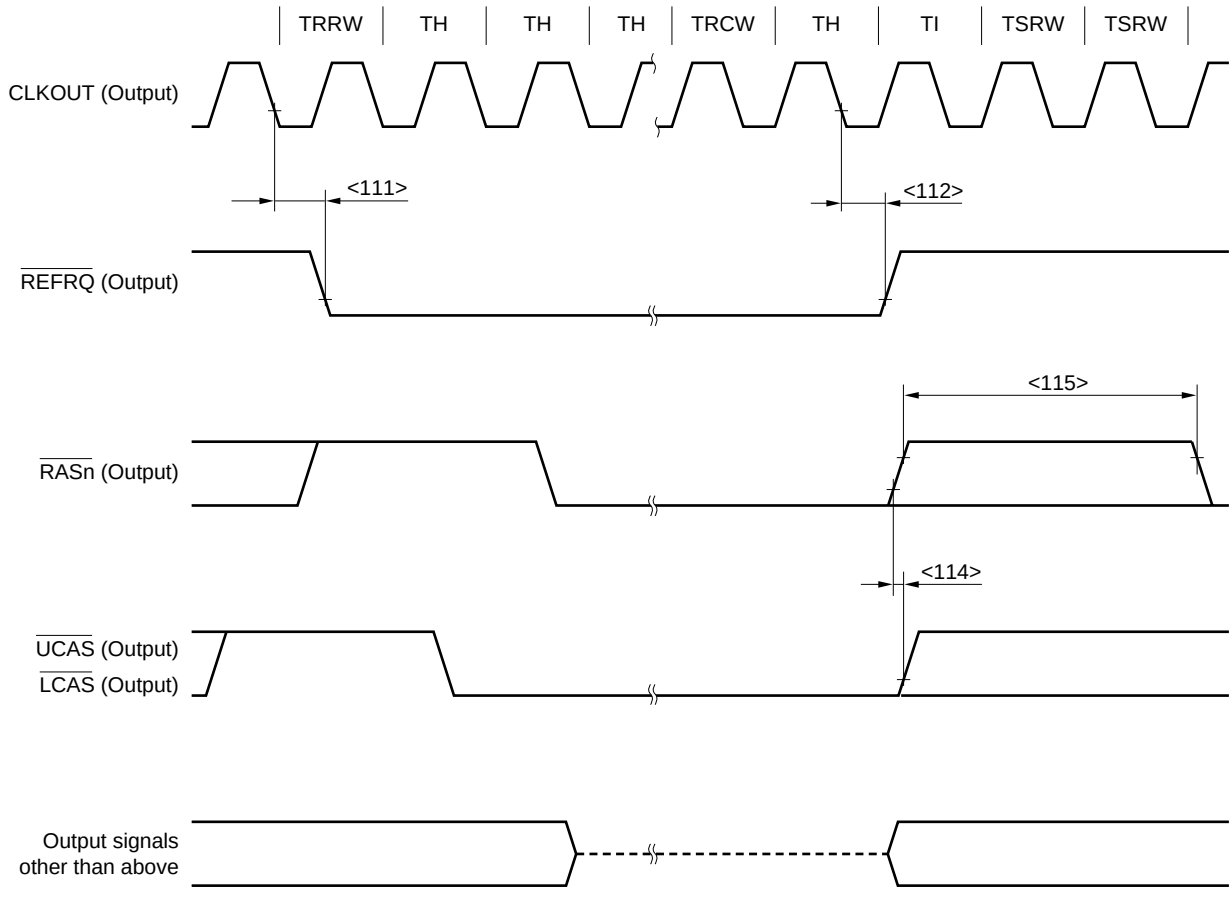
2. n = 0 to 7

(j) CBR self-refresh timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT ↓)	<111>	t_{DKRF}		2	10	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT ↓)	<112>	t_{HKRF}		2	10	ns
$\overline{\text{CAS}}$ hold time	<114>	t_{CHS}		–5		ns
$\overline{\text{RAS}}$ precharge time	<115>	t_{RPS}		$(1 + 2w_{SRW})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w_{SRW}: the number of waits due to the SRW0 to SRW2 bits of the RWC register.



Remarks 1. This is the timing for the following case.
Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1
Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 1
Number of waits due to the SRW0 to SRW2 bits of the RWC register (TSRW): 2

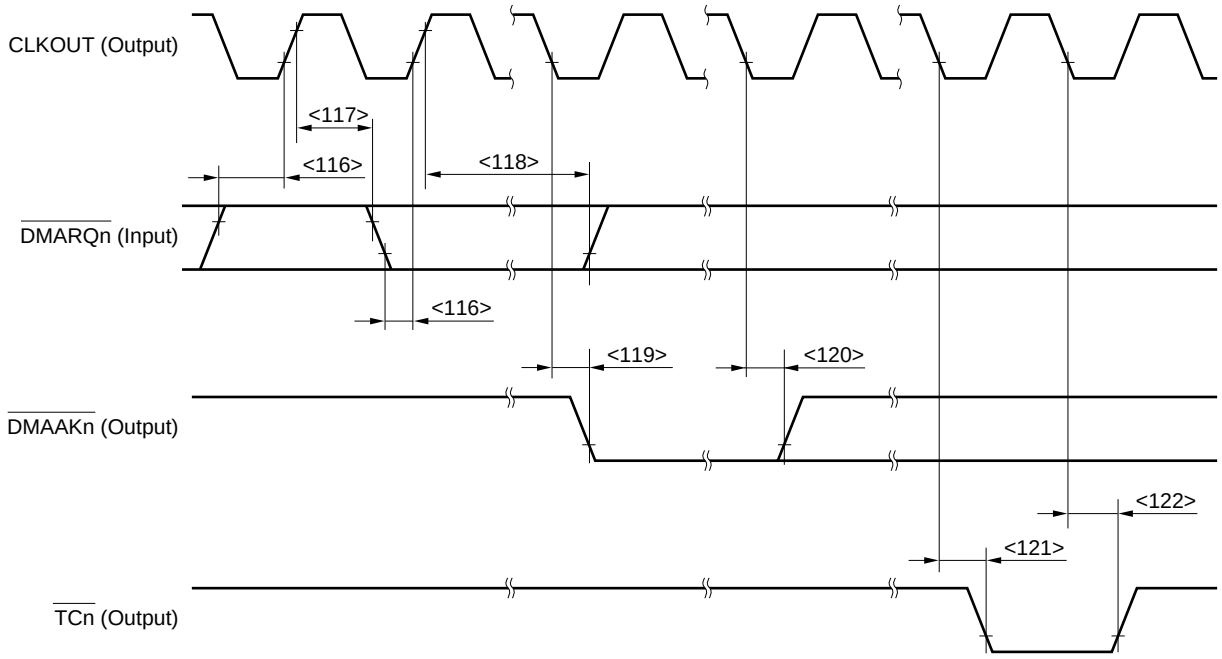
2. The broken lines indicate high impedance.

3. n = 0 to 7

(7) DMAC timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT ↑)	<116>	t_{SDRK}		15		ns
$\overline{\text{DMARQn}}$ hold time (from CLKOUT ↑)	<117>	t_{HKDR1}		2		ns
	<118>	t_{HKDR2}		Until $\overline{\text{DMAAKn}}$ ↓		ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT ↓)	<119>	t_{DKDA}		2	10	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT ↓)	<120>	t_{HKDA}		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT ↓)	<121>	t_{DKTC}		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT ↓)	<122>	t_{HKTC}		2	10	ns

Remark n = 0 to 3



Remark n = 0 to 3

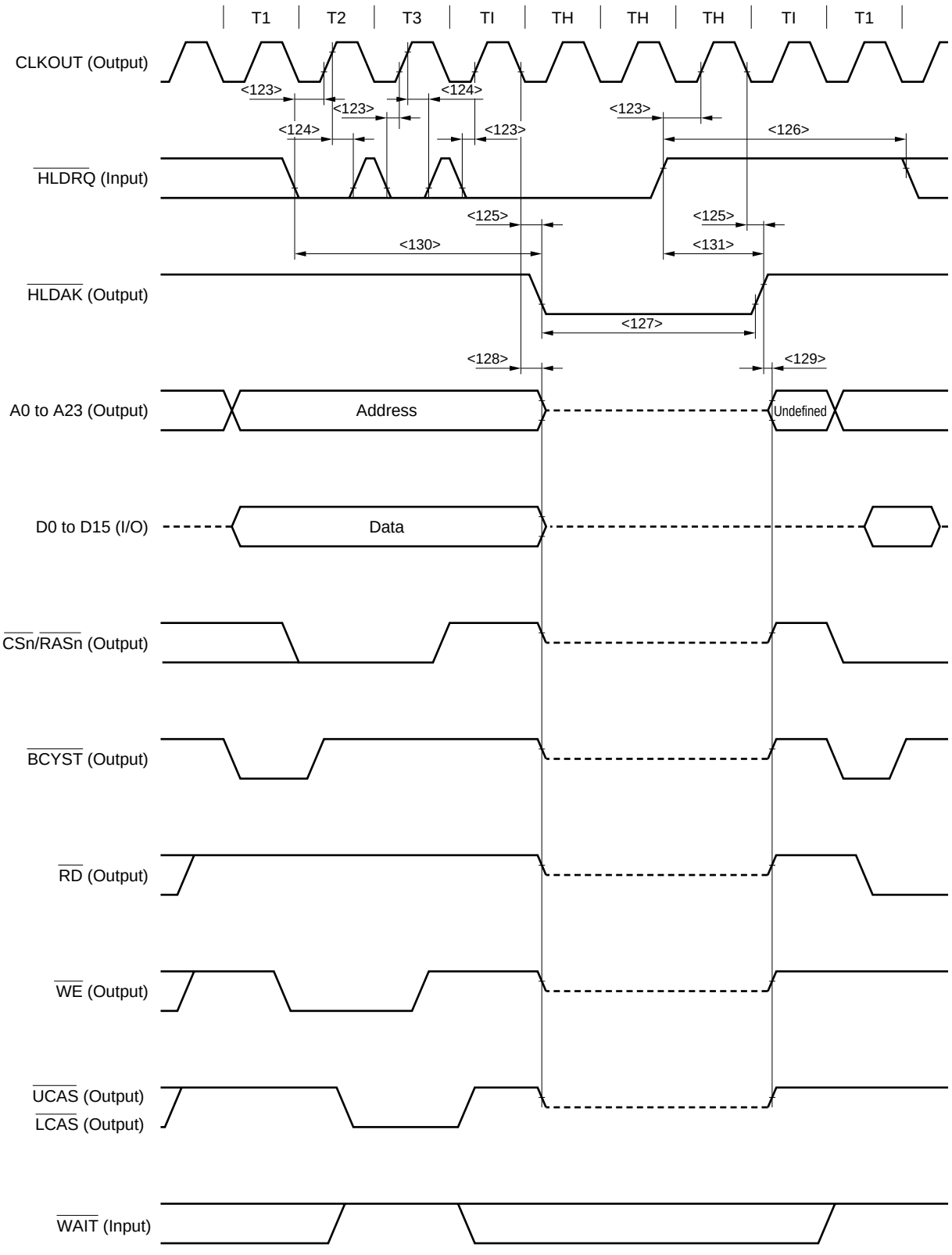
[MEMO]

(8) Bus hold timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↑)	<123>	t_{SHRK}		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↑)	<124>	t_{HKHR}		2		ns
Delay time from CLKOUT ↓ to $\overline{\text{HLDAK}}$	<125>	t_{DKHA}		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126>	t_{WHQH}		T + 17		ns
$\overline{\text{HLDAK}}$ low-level width	<127>	t_{WHAL}		T – 8		ns
Delay time from $\overline{\text{CLKOUT}}$ ↓ to bus float	<128>	t_{DKCF}			10	ns
Delay time from $\overline{\text{HLDAK}}$ ↑ to bus output	<129>	t_{DHAC}		0		ns
Delay time from $\overline{\text{HLDRQ}}$ ↓ to $\overline{\text{HLDAK}}$ ↓	<130>	t_{DHQHA1}		2.5T		ns
Delay time from $\overline{\text{HLDRQ}}$ ↑ to $\overline{\text{HLDAK}}$ ↑	<131>	t_{DHQHA2}		0.5T	1.5T	ns

Remark T = t_{CYK}

(8) Bus hold timing (2/2)



Remarks 1. The broken lines indicate high impedance.

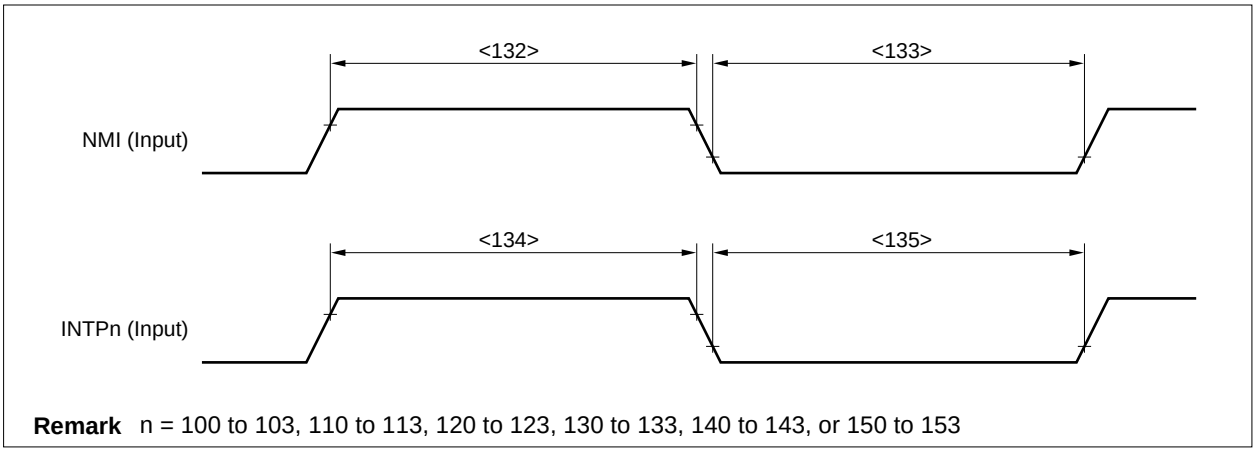
2. n = 0 to 7

(9) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<132>	t_{WNIH}		500		ns
NMI low-level width	<133>	t_{WNIL}		500		ns
INTPn high-level width	<134>	t_{WITH}		4T + 10		ns
INTPn low-level width	<135>	t_{WITL}		4T + 10		ns

Remarks 1. n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

2. T = t_{CYK}



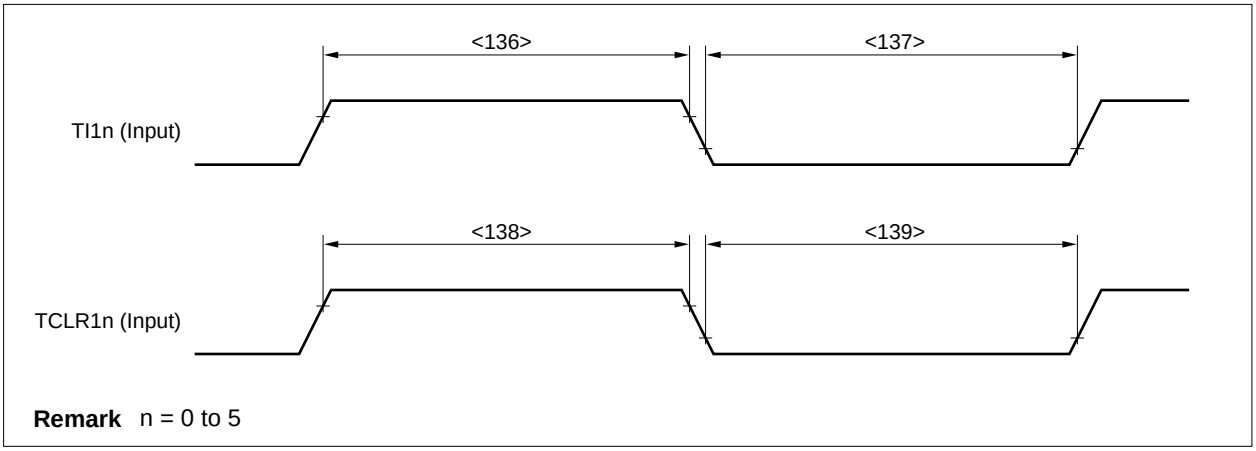
Remark n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1n high-level width	<136>	t_{WTIH}		3T + 18		ns
TI1n low-level width	<137>	t_{WTIL}		3T + 18		ns
TCLR1n high-level width	<138>	t_{WTCH}		3T + 18		ns
TCLR1n low-level width	<139>	t_{WTCL}		3T + 18		ns

Remarks 1. n = 0 to 5

2. T = t_{CYK}

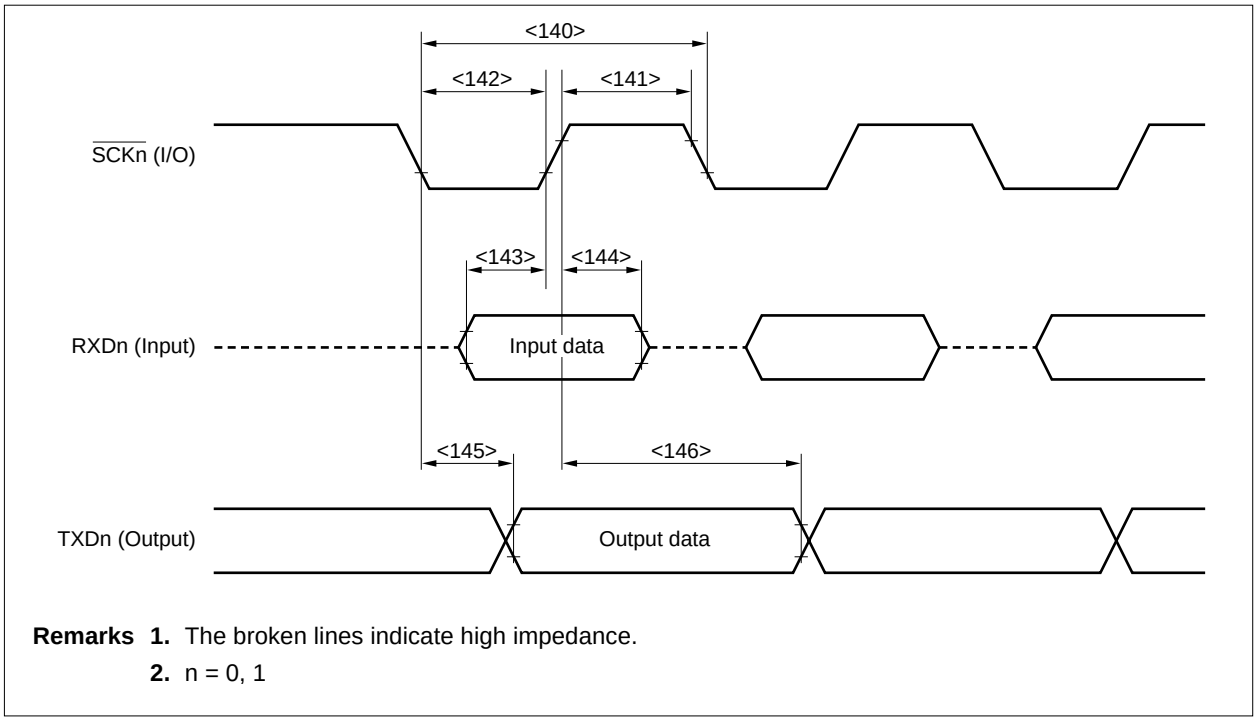


Remark n = 0 to 5

(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<140>	t_{CYSK0}	Output	250		ns
$\overline{SCKn}$ high-level width	<141>	t_{WSK0H}	Output	$0.5t_{CYSK0} - 20$		ns
$\overline{SCKn}$ low-level width	<142>	t_{WSK0L}	Output	$0.5t_{CYSK0} - 20$		ns
RXDn setup time (to $\overline{SCKn}$ ↑)	<143>	t_{SRXSK}		30		ns
RXDn hold time (from $\overline{SCKn}$ ↑)	<144>	t_{HSKRX}		0		ns
TXDn output delay time (from $\overline{SCKn}$ ↓)	<145>	t_{DSKTX}			20	ns
TXDn output hold time (from $\overline{SCKn}$ ↑)	<146>	t_{HSKTX}		$0.5t_{CYSK0} - 5$		ns

Remark n = 0, 1



Remarks 1. The broken lines indicate high impedance.

2. n = 0, 1

(12) CSI0 to CSI3 timing

(a) Master mode

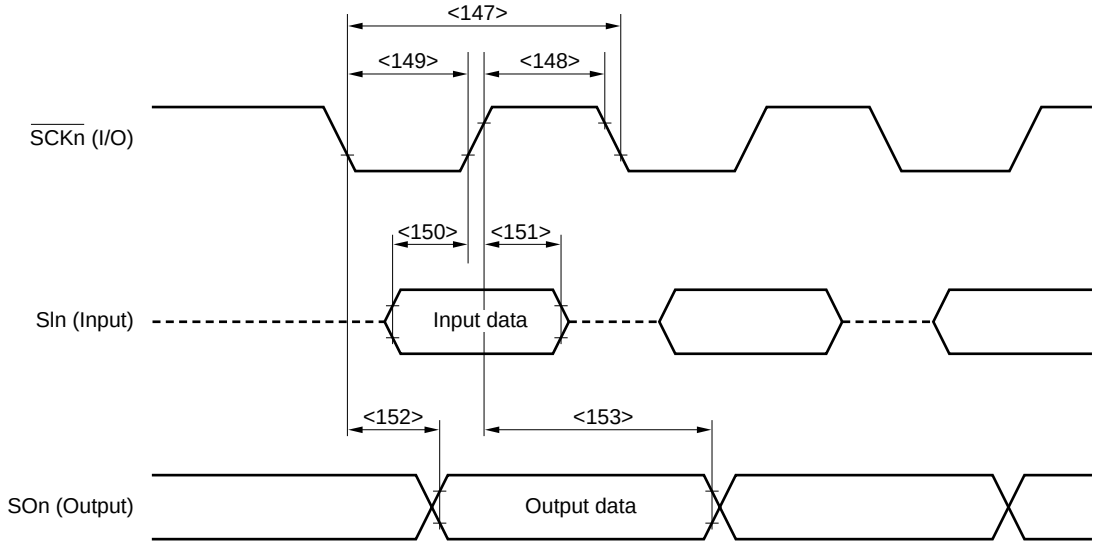
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147>	t_{CYSK1}	Output	100		ns
$\overline{SCKn}$ high-level width	<148>	t_{WSK1H}	Output	$0.5t_{CYSK1}$ – 20		ns
$\overline{SCKn}$ low-level width	<149>	t_{WSK1L}	Output	$0.5t_{CYSK1}$ – 20		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<150>	t_{SSISK}		30		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<151>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<152>	t_{DSKSO}			20	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<153>	t_{HSKSO}		$0.5t_{CYSK1}$ – 5		ns

Remark n = 0 to 3

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147>	t_{CYSK1}	Input	100		ns
$\overline{SCKn}$ high-level width	<148>	t_{WSK1H}	Input	30		ns
$\overline{SCKn}$ low-level width	<149>	t_{WSK1L}	Input	30		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<150>	t_{SSISK}		10		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<151>	t_{HSKSI}		10		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<152>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<153>	t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0 to 3



Remarks 1. The broken lines indicate high impedance.

2. n = 0 to 3

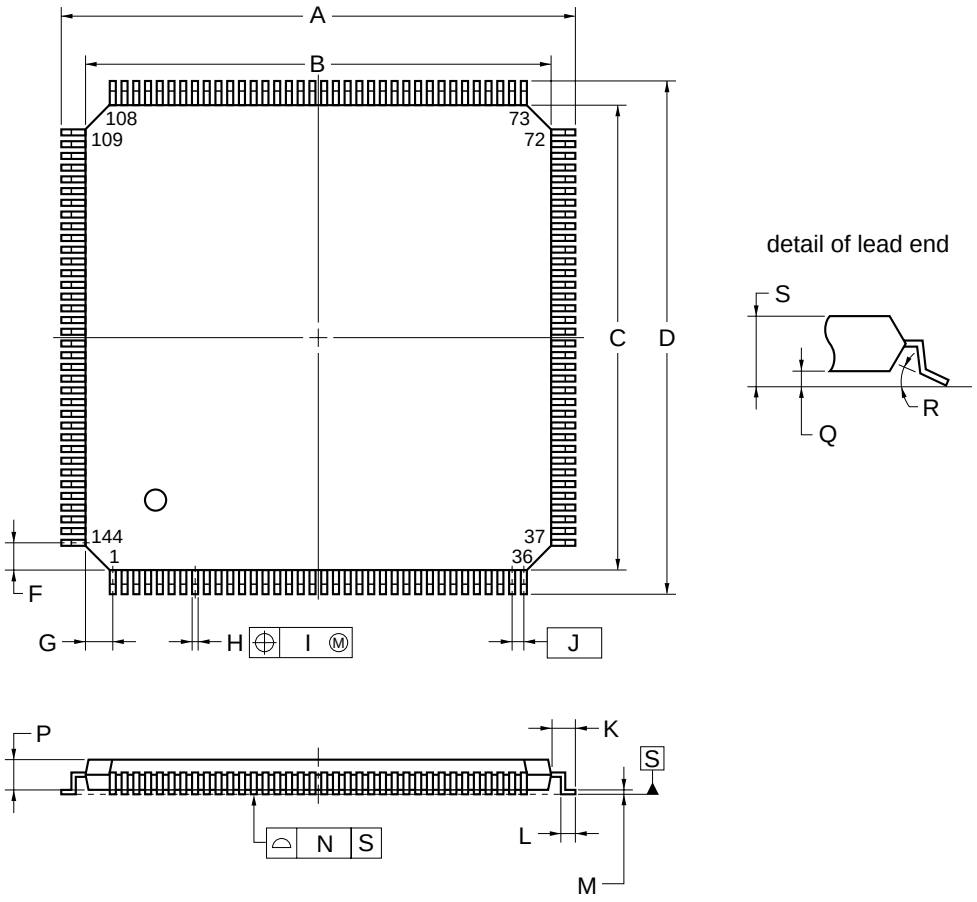
A/D Converter Characteristics (T_A = –40 to +70°C ... μPD703100-40,
T_A = –40 to +85°C ... μPD703100-33, 703101-33, 703102-33,
V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 V ±10%, V_{SS} = 0 V,
HV_{DD} – 0.5 V ≤ AV_{DD} ≤ HV_{DD}, output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Total error	–				±4	LSB
Quantization error	–				±1/2	LSB
Conversion time	t_{CONV}		5		10	μs
Sampling time	t_{SAMP}		Conversion clock[Note]/6			ns
Zero scale error	–				±4	LSB
Scale error	–				±4	LSB
Linearity error	–				±3	LSB
Analog input voltage	V_{IAN}		–0.3		AV_{REF} + 0.3	V
Analog input resistance	R_{AN}			2		MΩ
AV_{REF} input voltage	AV_{REF}	AV_{REF} = AV_{DD}	4.5		5.5	V
AV_{REF} input current	AI_{REF}				2.0	mA
AV_{DD} current	AI_{DD}				6	mA

Note Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

★ 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

5. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 5-1. Surface Mounting Type Soldering Conditions

★ **μPD703100GJ-40-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)**
★ **μPD703100GJ-33-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)**
★ **μPD703101GJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)**
★ **μPD703102GJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
★ VPS	Package peak temperature: 215°C, Time: 25 to 40 sec. Max. (at 200°C or higher), Count: two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related documents μPD70F3102-33 Data Sheet (U13844E)
μPD703100A-33, 703100A-40, 703101A-33, 703102A-33 Data Sheet (U14168E)
μPD70F3102A-33 Data Sheet (U13845E)

Reference materials Electrical Characteristics for Microcomputer (U15170J[Note])

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Madrid Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP Brasil
Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

J00.7

The export of these products from Japan is regulated by the Japanese government. The export of some or all of these products may be prohibited without governmental license. To export or re-export some or all of these products from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

License not needed: μPD703100-33, 703100-40

The customer must judge the need for license: μPD703101-33, 703102-33

- **The information in this document is current as of August, 2000. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4