

MOS INTEGRATED CIRCUIT

μ PD703038, 703038Y, 703039, 703039Y, 703040, 703040Y, 703041, 703041Y

V850/SV1™

32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μ PD703038, 703038Y, 703039, 703039Y, 703040, 703040Y, 703041, and 703041Y (collectively known as the V850/SV1) are products in the low-power series of V850 Family™ products, which are NEC's single-chip microcontrollers for real-time control.

The V850/SV1 employs the CPU core of the V850 Family, and has on-chip peripheral functions such as large capacity ROM/RAM, a multi-function timer/counter, serial interface, A/D converter, DMA controller, PWM, and a Vsync/Hsync separation circuit.

The V850/SV1 not only realizes the low power consumption necessary for applications such as camcorders, but also has an extremely high cost performance.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SV1 User's Manual Hardware: U14462E
V850 Family User's Manual Architecture: U10243E

FEATURES

- Number of instructions: 74
- ★ ○ Minimum instruction execution time: 50 ns (@ 20 MHz operation with main system clock)
- General-purpose registers: 32 bits × 32 registers
- Instruction set (signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions)
- Memory space: 16 MB linear address space
Memory block allocation function: 2 MB per block
- External bus: 16-bit multiplexed bus
- ★ ○ Internal memory:
 - μ PD703038, 703038Y (ROM: 384 KB, RAM: 16 KB)
 - μ PD703039, 703039Y (ROM: 256 KB, RAM: 8 KB)
 - μ PD703040, 703040Y (ROM: 256 KB, RAM: 16 KB)
 - μ PD703041, 703041Y (ROM: 192 KB, RAM: 8 KB)
- I/O lines Total: 151
- 10-bit resolution A/D converter: 16 channels
- Timer/counter 24-bit: 2 channels, 16-bit: 2 channels
8-bit: 8 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- DMA controller: 6 channels
- Interrupts and exceptions
 - Non-maskable interrupts: 2 sources
 - Maskable interrupts: μ PD703038, 703039, 703040, 703041 (51 sources)
 μ PD703038Y, 703039Y, 703040Y, 703041Y (52 sources)
 - Software exceptions: 32 sources
 - Exception trap: 1 source
- Serial interface (SIO)
 - Asynchronous serial interface (UART)
 - Clocked serial interface (CSI)
 - 3-wire variable-length serial interface (CSI4)
 - I²C bus interface (I²C) (μ PD703039Y, 703040Y, 703041Y)
- RTP: 8 bits × 2 channels or 4 bits × 4 channels

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

- PWM output: 4 channels
- Vsync/Hsync separation circuit
- On-chip key return function
- On-chip clock generator
- Power saving function: HALT/IDLE/STOP modes
- ROM correction: 4 points
- Package: 176-pin plastic LQFP (24 × 24)

APPLICATIONS

- Camcorders (including DVC)

★ ORDERING INFORMATION

Part Number	Package
μ PD703038F1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703038YF1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703039GM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)
μ PD703039F1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703039YGM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)
μ PD703039YF1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703040GM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)
μ PD703040F1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703040YGM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)
μ PD703040YF1-xxx-EN2	180-pin plastic FBGA (13 × 13)
μ PD703041GM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)
μ PD703041YGM-xxx-UEU	176-pin plastic LQFP (fine pitch) (24 × 24)

Remark xxx indicates ROM code suffix.

DIFFERENCES BETWEEN V850/SV1 PRODUCTS

	Internal ROM	Internal RAM	I ² C	V _{PP} Pin	
★ μ PD703038	384 KB (mask ROM)	16 KB	None	None	
★ μ PD703038Y			Provided		
μ PD703039	256 KB (mask ROM)	8 KB	None		
μ PD703039Y			Provided		
μ PD703040			16 KB		None
μ PD703040Y	Provided				
μ PD703041	192 KB (mask ROM)	8 KB	None		
μ PD703041Y			Provided		
★ μ PD70F3038	384 KB (flash memory)	16 KB	None		Provided
★ μ PD70F3038Y			Provided		
μ PD70F3040	256 KB (flash memory)	16 KB	None		
μ PD70F3040Y			Provided		

PIN CONFIGURATION

176-pin plastic LQFP (fine pitch) (24 × 24)

μPD703039GM-xxx-UEU

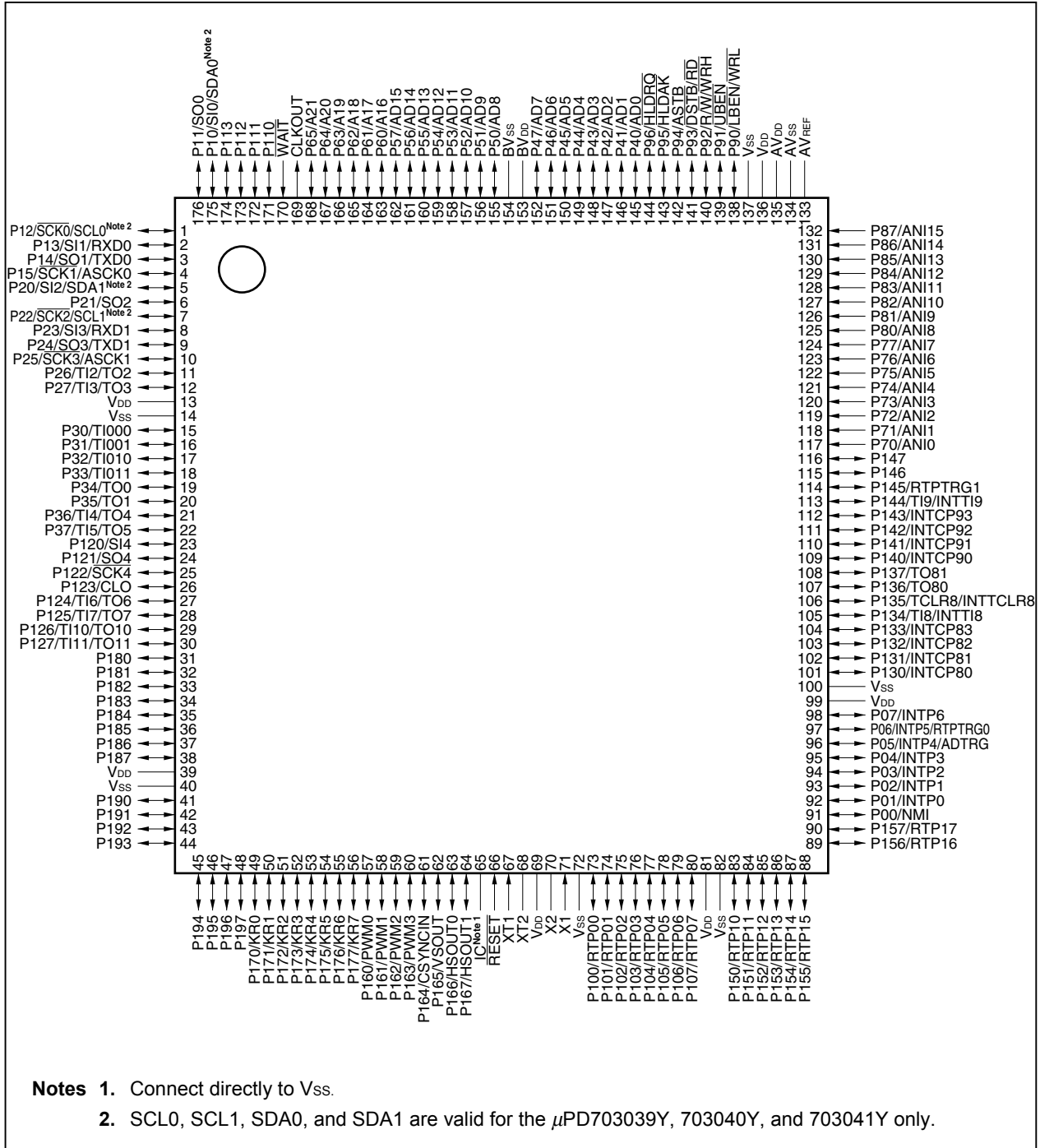
μPD703039YGM-xxx-UEU

μPD703040GM-xxx-UEU

μPD703040YGM-xxx-UEU

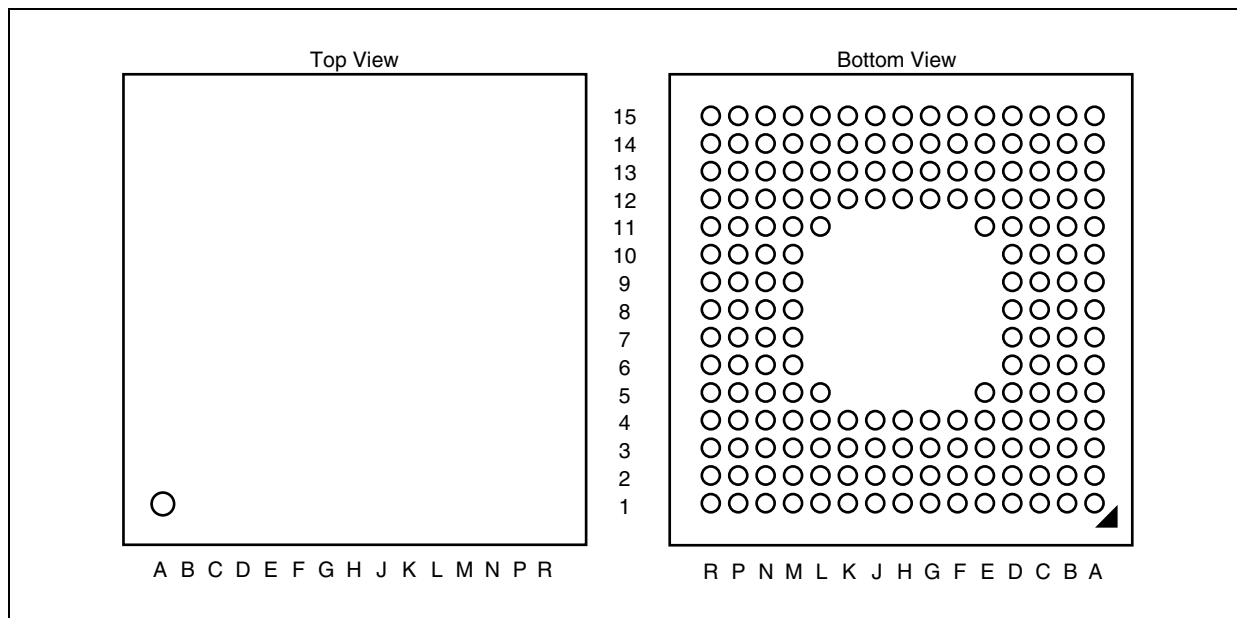
μPD703041GM-xxx-UEU

μPD703041YGM-xxx-UEU



Notes 1. Connect directly to Vss.
 2. SCL0, SCL1, SDA0, and SDA1 are valid for the μPD703039Y, 703040Y, and 703041Y only.

- ★ 180-pin plastic FBGA (13 × 13)
 - μ PD703038F1-xxx-EN2
 - μ PD703038YF1-xxx-EN2
 - μ PD703039F1-xxx-EN2
 - μ PD703039YF1-xxx-EN2
 - μ PD703040F1-xxx-EN2
 - μ PD703040YF1-xxx-EN2



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A1	NC ^{Note 1}	B1	P13/SI1/RXD0	C1	P15/SCK1/ASCK0	D1	P23/SI3/RXD1
A2	P11/SO0	B2	P12/SCK0/SCL0 ^{Note 2}	C2	P20/SI2/SDA1 ^{Note 2}	D2	P21/SO2
A3	P10/SI0/SDA0 ^{Note 2}	B3	P113	C3	P14/SO1/TXD0	D3	P22/SCK2/SCL1 ^{Note 2}
A4	P112	B4	P110	C4	P111	D4	P24/SO3/TXD1
A5	CLKOUT	B5	P64/A20	C5	P65/A21	D5	WAIT
A6	P62/A18	B6	P60/A16	C6	P63/A19	D6	P61/A17
A7	P57/AD15	B7	P54/AD12	C7	P56/AD14	D7	P55/AD13
A8	P53/AD11	B8	P50/AD8	C8	P52/AD10	D8	P51/AD9
A9	BV _{SS}	B9	P46/AD6	C9	BV _{DD}	D9	P47/AD7
A10	P45/AD5	B10	P42/AD2	C10	P44/AD4	D10	P43/AD3
A11	P41/AD1	B11	P94/ASTB	C11	P40/AD0	D11	P96/HLDRQ
A12	V _{SS}	B12	P91/UBEN	C12	P93/DSTB/RD	D12	P90/LBEN/WRL
A13	AV _{SS}	B13	AV _{DD}	C13	P82/ANI10	D13	P81/ANI9
A14	AV _{REF}	B14	V _{DD}	C14	P86/ANI14	D14	P84/ANI12
A15	NC ^{Note 1}	B15	P87/ANI15	C15	P85/ANI13	D15	P83/ANI11

Notes 1. Leave the NC pin open.

2. SCL0, SCL1, SDA0, and SDA1 are valid only for μ PD703038Y, 703039Y, and 703040Y.

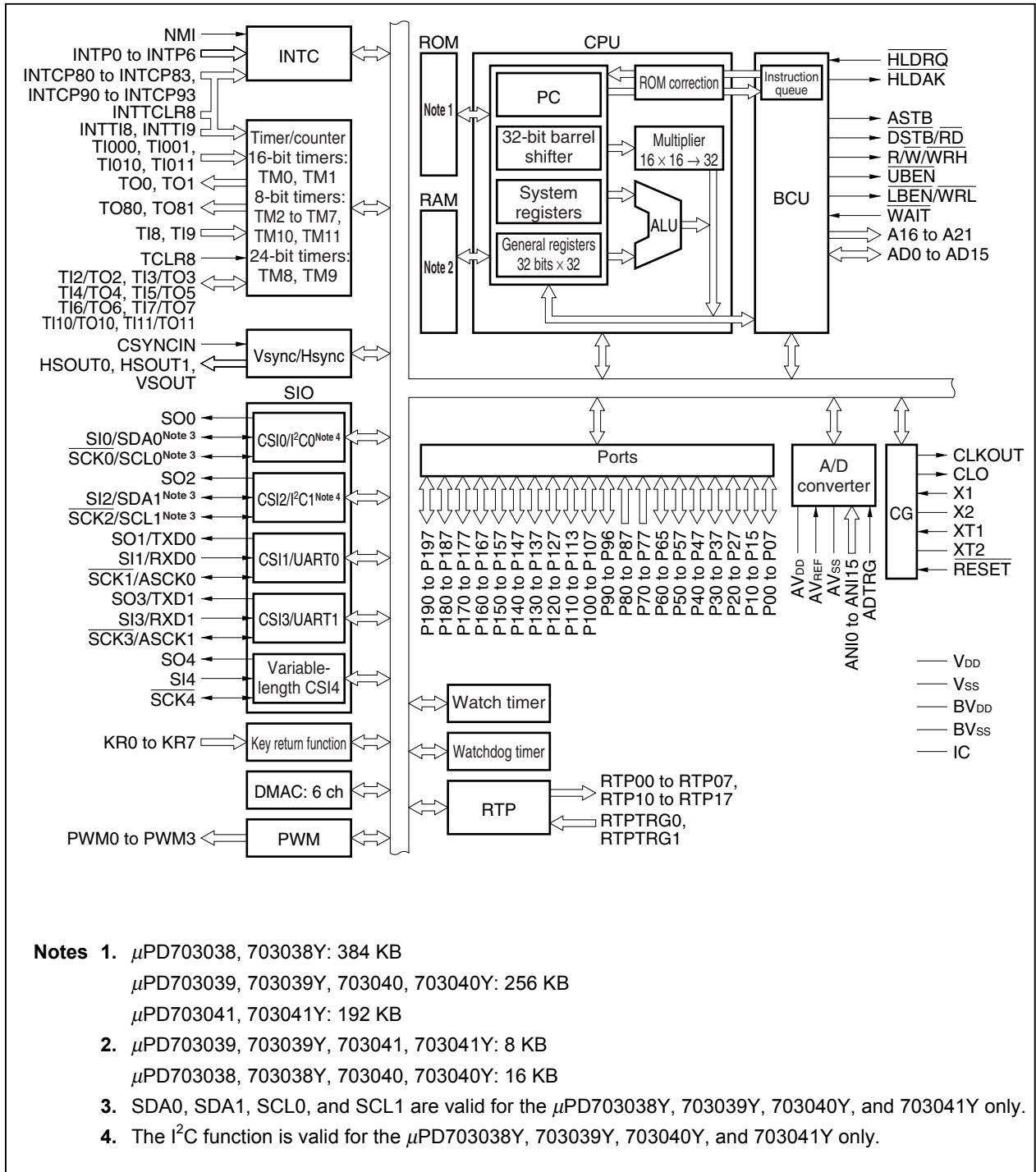
Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
E1	P27/TI3/TO3	H12	P144/TI9/INTTI9	M1	V _{DD}	P1	P193
E2	P25/SCK3/ASCK1	H13	P143/INTCP93	M2	P186	P2	P195
E3	P26/TI2/TO2	H14	P146	M3	P170/KR0	P3	P196
E4	V _{SS}	H15	P141/INTCP91	M4	P174/KR4	P4	P176/KR6
E5	V _{DD}	J1	P125/TI7/TO7	M5	P177/KR7	P5	P160/PWM0
E11	P95/HLDAK	J2	P124/TI6/TO6	M6	P163/PWM3	P6	P164/CSYNCIN
E12	P92/R \overline{W} /WRH	J3	P126/TI10/TO10	M7	P167/HSOUT1	P7	IC ^{Note 1}
E13	P76/ANI6	J4	P127/TI11/TO11	M8	RESET $\overline{}$	P8	X2
E14	P77/ANI7	J12	P140/INTCP90	M9	V _{SS}	P9	P100/RTP00
E15	P80/ANI8	J13	P137/TO81	M10	P103/RTP03	P10	P104/RTP04
F1	P30/TI000	J14	P142/INTCP92	M11	P01/INTP0	P11	P107/RTP07
F2	P31/TI001	J15	P135/TCLR8/INTTCLR8	M12	P04/INTP3	P12	P150/RTP10
F3	P32/TI010	K1	P181	M13	P05/INTP4/ADTRG	P13	P152/RTP12
F4	P33/TI011	K2	P180	M14	P03/INTP2	P14	P153/RTP13
F12	P74/ANI4	K3	P182	M15	P06/INTP5/RTPTRG0	P15	P156/RTP16
F13	P72/ANI2	K4	P183	N1	P191	R1	NC ^{Note 2}
F14	P75/ANI5	K12	P134/TI8/INTTI8	N2	P192	R2	P194
F15	P70/ANI0	K13	P133/INTCP83	N3	P197	R3	P171/KR1
G1	P35/TO1	K14	P136/TO80	N4	P173/KR3	R4	P172/KR2
G2	P34/TO0	K15	P132/INTCP82	N5	P175/KR5	R5	P161/PWM1
G3	P36/TI4/TO4	L1	P185	N6	P162/PWM2	R6	P165/VSOUT
G4	P37/TI5/TO5	L2	P184	N7	P166/HSOUT0	R7	XT1
G12	P73/ANI3	L3	P187	N8	V _{DD}	R8	XT2
G13	P147	L4	V _{SS}	N9	X1	R9	P101/RTP01
G14	P71/ANI1	L5	P190	N10	P102/RTP02	R10	P105/RTP05
G15	P145/RTPTRG1	L11	V _{DD}	N11	P106/RTP06	R11	V _{SS}
H1	P121/SO4	L12	V _{SS}	N12	V _{DD}	R12	P151/RTP11
H2	P120/SI4	L13	P07/INTP6	N13	P157/RTP17	R13	P154/RTP14
H3	P122/SCK4	L14	P131/INTCP81	N14	P00/NMI	R14	P155/RTP15
H4	P123/CLO	L15	P130/INTCP80	N15	P02/INTP1	R15	NC ^{Note 2}

- Notes
1. Connect the IC pin directly to V_{SS}.
 2. Leave the NC pin open.

PIN IDENTIFICATION

A16 to A21:	Address bus	P110 to P113:	Port 11
AD0 to AD15:	Address/data bus	P120 to P127:	Port 12
ADTRG:	AD trigger input	P130 to P137:	Port 13
ANI0 to ANI15:	Analog input	P140 to P147:	Port 14
ASCK0, ASCK1:	Asynchronous serial clock	P150 to P157:	Port 15
ASTB:	Address strobe	P160 to P167:	Port 16
AV _{DD} :	Analog power supply	P170 to P177:	Port 17
AV _{REF} :	Analog reference voltage	P180 to P187:	Port 18
AV _{SS} :	Analog ground	P190 to P197:	Port 19
BV _{DD} :	Bus interface power supply	PWM0 to PWM3:	Pulse width modulation
BV _{SS} :	Bus interface ground	\overline{RD} :	Read
CLKOUT:	Clock output	\overline{RESET} :	Reset
CLO:	Clock output (divided)	RTP00 to RTP07,:	Real-time output port
CSYNCIN:	Csync input	RTP10 to RTP17	
\overline{DSTB} :	Data strobe	RTPTRG0, RTPTRG1:	RTP trigger input
\overline{HLDAK} :	Hold acknowledge	R \overline{W} :	Read/write status
\overline{HLDRQ} :	Hold request	RXD0, RXD1:	Receive data
HSOUT0, HSOUT1:	Hsync output	$\overline{SCK0}$ to $\overline{SCK4}$:	Serial clock
IC:	Internally connected	SCL0, SCL1:	Serial clock
INTCP80 to INTPC83,:	Interrupt request from peripherals	SDA0, SDA1:	Serial data
INTCP90 to INTPC93,		SI0 to SI4:	Serial input
INTP0 to INTP6,		SO0 to SO4:	Serial output
INTTCLR8,		TCLR8:	Timer clear
INTTI8, INTTI9		TI000, TI001, TI010,:	Timer input
KR0 to KR7:	Key return	TI011, TI2 to TI11	
\overline{LBEN} :	Lower byte enable	TO0 to TO7, TO80,:	Timer output
NMI:	Non-maskable interrupt request	TO81, TO10, TO11	
P00 to P07:	Port 0	TXD0, TXD1:	Transmit data
P10 to P15:	Port 1	\overline{UBEN} :	Upper byte enable
P20 to P27:	Port 2	V _{DD} :	Power supply
P30 to P37:	Port 3	VSOUT:	Vsync output
P40 to P47:	Port 4	V _{SS} :	Ground
P50 to P57:	Port 5	\overline{WAIT} :	Wait
P60 to P65:	Port 6	\overline{WRH} :	Write strobe high level data
P70 to P77:	Port 7	\overline{WRL} :	Write strobe low level data
P80 to P87:	Port 8	X1, X2:	Crystal for main system clock
P90 to P96:	Port 9	XT1, XT2:	Crystal for subsystem clock
P100 to P107:	Port 10		

INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS.....	9
1.1 Port Pins	9
1.2 Non-Port Pins	13
1.3 Pin I/O Circuits, I/O Buffer Supply, and Recommended Connection of Unused Pins.....	16
2. ELECTRICAL SPECIFICATIONS	20
3. PACKAGE DRAWING	42
4. RECOMMENDED SOLDERING CONDITIONS	44

1. PIN FUNCTIONS

1.1 Port Pins

(1/4)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG0
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output mode can be specified in 1-bit units.	SI0/SDA0
P11				SO0
P12				SCK0/SCL0
P13				SI1/RXD0
P14				SO1/TXD0
P15				SCK1/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output mode can be specified in 1-bit units.	SI2/SDA1
P21				SO2
P22				SCK2/SCL1
P23				SI3/RXD1
P24				SO3/TXD1
P25				SCK3/ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output mode can be specified in 1-bit units.	TI000
P31				TI001
P32				TI010
P33				TI011
P34				TO0
P35				TO1
P36				TI4/TO4
P37				TI5/TO5
P40	I/O	No	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD0
P41				AD1
P42				AD2
P43				AD3
P44				AD4

Remark PULL: On-chip pull-up resistor

(2/4)

Pin Name	I/O	PULL	Function	Alternate Function
P45	I/O	No	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD5
P46				AD6
P47				AD7
P50	I/O	No	Port 5 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD8
P51				AD9
P52				AD10
P53				AD11
P54				AD12
P55				AD13
P56				AD14
P57				AD15
P60				I/O
P61	A17			
P62	A18			
P63	A19			
P64	A20			
P65	A21			
P70	Input	No	Port 7 8-bit input port	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	Input	No	Port 8 8-bit input port	ANI8
P81				ANI9
P82				ANI10
P83				ANI11
P84				ANI12
P85				ANI13
P86				ANI14
P87				ANI15
P90	I/O	No	Port 9 7-bit I/O port Input/output mode can be specified in 1-bit units.	LBEN/WRL
P91				UBEN
P92				R/W/WRH
P93				DSTB/RD

Remark PULL: On-chip pull-up resistor

Pin Name	I/O	PULL	Function	Alternate Function
P94	I/O	No	Port 9 7-bit I/O port Input/output mode can be specified in 1-bit units.	ASTB
P95				HLDKAK
P96				HLDKRD
P100	I/O	Yes	Port 10 8-bit I/O port Input/output mode can be specified in 1-bit units.	RTP00
P101				RTP01
P102				RTP02
P103				RTP03
P104				RTP04
P105				RTP05
P106				RTP06
P107				RTP07
P110	I/O	No	Port 11 4-bit I/O port Input/output mode can be specified in 1-bit units.	—
P111				—
P112				—
P113				—
P120	I/O	No	Port 12 8-bit I/O port Input/output mode can be specified in 1-bit units.	SI4
P121				SO4
P122				SCK4
P123				CLO
P124				TI6/TO6
P125				TI7/TO7
P126				TI10/TO10
P127				TI11/TO11
P130	I/O	No	Port 13 8-bit I/O port Input/output mode can be specified in 1-bit units.	INTCP80
P131				INTCP81
P132				INTCP82
P133				INTCP83
P134				TI8/INTTI8
P135				TCLR8/INTTCLR8
P136				TO80
P137				TO81
P140	I/O	No	Port 14 8-bit I/O port Input/output mode can be specified in 1-bit units.	INTCP90
P141				INTCP91
P142				INTCP92
P143				INTCP93
P144				TI9/INTTI9
P145				RTPTRG1
P146				—
P147				—

Remark PULL: On-chip pull-up resistor

(4/4)

Pin Name	I/O	PULL	Function	Alternate Function
P150	I/O	No	Port 15 8-bit I/O port Input/output mode can be specified in 1-bit units.	RTP10
P151				RTP11
P152				RTP12
P153				RTP13
P154				RTP14
P155				RTP15
P156				RTP16
P157				RTP17
P160	I/O	No	Port 16 8-bit I/O port Input/output mode can be specified in 1-bit units.	PWM0
P161				PWM1
P162				PWM2
P163				PWM3
P164				CSYNCIN
P165				VSOUT
P166				HSOUT0
P167				HSOUT1
P170	I/O	Yes	Port 17 8-bit I/O port Input/output mode can be specified in 1-bit units.	KR0
P171				KR1
P172				KR2
P173				KR3
P174				KR4
P175				KR5
P176				KR6
P177				KR7
P180	I/O	No	Port 18 8-bit I/O port Input/output mode can be specified in 1-bit units.	–
P181				–
P182				–
P183				–
P184				–
P185				–
P186				–
P187				–
P190	I/O	No	Port 19 8-bit I/O port Input/output mode can be specified in 1-bit units.	–
P191				–
P192				–
P193				–
P194				–
P195				–
P196				–
P197				–

Remark PULL: On-chip pull-up resistor

1.2 Non-Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
A16 to A21	Output	No	Address bus 16 to 21	P60 to P65
AD0 to AD7	I/O	No	Address/data multiplexed bus 0 to 15	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI15	Input	No		P80 to P87
ASCK0	Input	Yes	Baud rate clock input for UART0 and UART1	P15/SCK1
ASCK1				P25/SCK3
ASTB	Output	No	External address strobe signal output	P94
AV _{DD}	–	–	Positive power supply for A/D converter and ports used for alternate functions	–
AV _{REF}	Input	–	Reference voltage input for A/D converter	–
AV _{SS}	–	–	Ground potential for A/D converter and ports used for alternate functions	–
BV _{DD}	–	–	Positive power supply for bus interface and ports used for alternate functions	–
BV _{SS}	–	–	Ground potential for bus interface and ports used for alternate functions	–
CLKOUT	Output	–	Internal system clock output	–
CLO	Output	No	CLO output signal	P123
CSYNCIN	Input	No	Csync signal input	P164
$\overline{\text{DSTB}}$	Output	No	External data strobe signal output	P93/ $\overline{\text{RD}}$
$\overline{\text{HLDK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
HSOUT0	Output	No	Hsync signal output before revision	P166
HSOUT1			Hsync signal output after revision	P167
IC	–	–	Internal connection (connect directly to V _{SS})	–
INTCP80 to INTCP83	Input	No	External capture input for CC80 to CC83	P130 to P133
INTCP90 to INTCP93	Input	No	External capture input for CP90 to CP93	P140 to P143
INTP0 to INTP3	Input	Yes	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5			External interrupt request input (digital noise elimination supporting remote controller)	P06/RTPTRG0
INTP6				P07

Remark PULL: On-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
INTTCLR8	Input	No	External interrupt request input (digital noise elimination)	P135/TCLR8
INTTI8	Input	No		P134/TI8
INTTI9				P144/TI9
KR0 to KR7	Input	Yes	Key return input	P170 to P177
$\overline{\text{LBEN}}$	Output	No	Lower byte enable signal output for external data bus	P90/ $\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
PWM0 to PWM3	Output	No	Output of PWM channels 0 to 3	P160 to P163
$\overline{\text{RD}}$	Output	No	Bus read strobe signal output	P93/ $\overline{\text{DSTB}}$
$\overline{\text{RESET}}$	Input	–	System reset input	–
RTP00 to RTP07	Output	Yes	Real-time output port	P100 to P107
RTP10 to RTP17		No		P150 to P157
RTPTRG0	Input	Yes	RTP external trigger input	P06
RTPTRG1		No		P145
$\overline{\text{R/W}}$	Output	No	External read/write status output	P92/ $\overline{\text{WRH}}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23/SI3
$\overline{\text{SCK0}}$	I/O	Yes	Serial clock I/O for CSI0 to CSI3 (3-wire mode)	P12/ $\overline{\text{SCL0}}$
$\overline{\text{SCK1}}$				P15/ $\overline{\text{ASCK0}}$
$\overline{\text{SCK2}}$				P22/ $\overline{\text{SCL1}}$
$\overline{\text{SCK3}}$				P25/ $\overline{\text{ASCK1}}$
$\overline{\text{SCK4}}$		No	Variable-length CSI4 serial clock I/O	P122
$\overline{\text{SCL0}}$	I/O	Yes	Serial clock I/O for I ² C0 and I ² C1 (μ PD703038Y, 703039Y, 703040Y and 703041Y)	P12/ $\overline{\text{SCK0}}$
$\overline{\text{SCL1}}$				P22/ $\overline{\text{SCK2}}$
$\overline{\text{SDA0}}$	I/O	Yes	Serial transmit/receive data I/O for I ² C0 and I ² C1 (μ PD703038Y, 703039Y, 703040Y and 703041Y)	P10/SI0
$\overline{\text{SDA1}}$				P20/SI2
SI0	Input	Yes	Serial receive data input for CSI0 to CSI3 (3-wire mode)	P10/ $\overline{\text{SDA0}}$
SI1				P13/ $\overline{\text{RXD0}}$
SI2				P20/ $\overline{\text{SDA1}}$
SI3				P23/ $\overline{\text{RXD1}}$
SI4		No	Variable-length CSI4 serial receive data input	P120
SO0	Output	Yes	Serial transmit data output for CSI0 to CSI3	P11
SO1				P14/ $\overline{\text{TXD0}}$
SO2				P21
SO3				P24/ $\overline{\text{TXD1}}$
SO4		No	Variable-length CSI4 serial transmit data output	P121
TCLR8	Input	No	External clear input for TM8	P135/INTTCLR8
TI000	Input	Yes	External count clock input/external capture trigger input for TM0	P30

Remark PULL: On-chip pull-up resistor

Pin Name	I/O	PULL	Function	Alternate Function	
TI001	Input	Yes	External capture trigger input for TM0	P31	
TI010			External count clock input/external capture trigger input for TM1	P32	
TI011			External capture trigger input for TM1	P33	
TI2			External count clock input for TM2	P26/TO2	
TI3			External count clock input for TM3	P27/TO3	
TI4			External count clock input for TM4	P36/TO4	
TI5			External count clock input for TM5	P37/TO5	
TI6		No	External count clock input for TM6	P124/TO6	
TI7			External count clock input for TM7	P125/TO7	
TI8			External count clock input for TM8	P134/INTTI8	
TI9			External count clock input for TM9	P144/INTTI9	
TI10			External count clock input for TM10	P126/TO10	
TI11			External count clock input for TM11	P127/TO11	
TO0		Output	Yes	Pulse signal output for TM0	P34
TO1	Pulse signal output for TM1			P35	
TO2	Pulse signal output for TM2			P26/TI2	
TO3	Pulse signal output for TM3			P27/TI3	
TO4	Pulse signal output for TM4			P36/TI4	
TO5	Pulse signal output for TM5			P37/TI5	
TO6	No			Pulse signal output for TM6	P124/TI6
TO7			Pulse signal output for TM7	P125/TI7	
TO80			Pulse signal output 0 for TM8	P136	
TO81			Pulse signal output 1 for TM8	P137	
TO10			Pulse signal output for TM10	P126/TI10	
TO11			Pulse signal output for TM11	P127/TI11	
TXD0			Output	Yes	Serial transmit data output for UART0 and UART1
TXD1	P24/SO3				
$\overline{\text{UBEN}}$	Output	No	Higher byte enable signal output for external data bus	P91	
V _{DD}	–	–	Positive power supply pin	–	
VSOUT	Output	No	Vsync signal output	P165	
V _{SS}	–	–	Ground potential	–	
$\overline{\text{WAIT}}$	Input	–	External $\overline{\text{WAIT}}$ signal input	–	
WRH	Output	No	Higher byte write strobe signal output for external data bus	P92/ $\overline{\text{R/W}}$	
$\overline{\text{WRL}}$				P90/ $\overline{\text{LBEN}}$	
X1	Input	–	Resonator connection for main system clock	–	
X2				–	
XT1	Input	–	Resonator connection for subsystem clock	–	
XT2				–	

Remark PULL: On-chip pull-up resistor

1.3 Pin I/O Circuits, I/O Buffer Supply, and Recommended Connection of Unused Pins

Table 1-1 shows the I/O circuit type of each pin and the recommended connection of unused pins.

For the I/O circuit configuration of each type, refer to Figure 1-1.

Table 1-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection Method
P00	NMI	5-W	V _{DD}	Input: Independently connect to V _{DD} or V _{SS} via a resistor Output: Leave open
P01 to P04	INTP0 to INTP3			
P05	INTP4/ADTRG			
P06	INTP5/RTPTRG0			
P07	INTP6			
P10	SI0/SDA0	10-F	V _{DD}	
P11	SO0	10-E		
P12	SCK0/SCL0	10-F		
P13	SI1/RXD0	5-W		
P14	SO1/TXD0	10-E		
P15	SCK1/ASCK0	10-F		
P20	SI2/SDA1	10-F	V _{DD}	
P21	SO2	10-E		
P22	SCK2/SCL1	10-F		
P23	SI3/RXD1	5-W		
P24	SO3/TXD1	10-E		
P25	SCK3/ASCK1	10-F		
P26, P27	TI2/TO2, TI3/TO3	5-W	V _{DD}	
P30, P31	TI000, TI001	5-W		
P32, P33	TI010, TI011			
P34, P35	TO0, TO1	5-A		
P36	TI4/TO4	5-W		
P37	TI5/TO5			
P40 to P47	AD0 to AD7	5	BV _{DD}	Input: Independently connect to BV _{DD} or BV _{SS} via a resistor Output: Leave open
P50 to P57	AD8 to AD15	5	BV _{DD}	
P60 to P65	A16 to A21	5	BV _{DD}	
P70 to P77	ANI0 to ANI7	9	AV _{DD}	Connect to AV _{SS}
P80 to P87	ANI8 to ANI15	9	AV _{DD}	
P90	LBEN/WRL	5	BV _{DD}	Input: Independently connect to BV _{DD} or BV _{SS} via a resistor Output: Leave open
P91	UBEN			
P92	R/W/WRH			
P93	DSTB/RD			
P94	ASTB			
P95	HLDK			
P96	HLDRQ			
P100 to P107	RTP00 to RTP07	10-E	V _{DD}	Input: Independently connect to V _{DD} or V _{SS} via a resistor Output: Leave open
P110 to P113	–	5	V _{DD}	
P120	SI4	5-K	V _{DD}	

Table 1-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection Method
P121	SO4	10-G	V _{DD}	Input: Independently connect to V _{DD} or V _{SS} via a resistor Output: Leave open
P122	$\overline{\text{SCK4}}$	10-H		
P123	CLO	5		
P124	TI6/TO6	5-K		
P125	TI7/TO7			
P126	TI10/TO10			
P127	TI11/TO11			
P130 to P133	INTCP80 to INTCP83	5-K	V _{DD}	
P134	TI8/INTTI8			
P135	TCLR8/INTTCLR8			
P136, P137	TO80, TO81	5		
P140 to P143	INTCP90 to INTCP93	5-K	V _{DD}	
P144	TI9/INTTI9			
P145	RTPTRG1			
P146, P147	–	5		
P150 to P157	RTP10 to RTP17	5	V _{DD}	
P160 to P163	PWM0 to PWM3	5	V _{DD}	
P164	CSYNCIN	5-K		
P165	VSOUT	5		
P166	HSOUT0			
P167	HSOUT1			
P170 to P177	KR0 to KR7	5-K	V _{DD}	
P180 to P187	–	5	V _{DD}	
P190 to P197	–	5	V _{DD}	
CLKOUT	–	4	BV _{DD}	Leave open
$\overline{\text{WAIT}}$	–	1	BV _{DD}	Connect to V _{DD} via a resistor
$\overline{\text{RESET}}$	–	2	V _{DD}	–
X1	–	–	V _{DD}	–
X2	–	–	V _{DD}	Leave open
XT1	–	16-A	V _{DD}	Connect to V _{SS}
XT2	–	16-A	V _{DD}	Leave open
AV _{REF}	–	–	–	Connect to AV _{SS}
IC	–	–	–	Connect directly to V _{SS}
V _{DD}	–	–	–	–
V _{SS}	–	–	–	–
AV _{DD}	–	–	–	Connect to V _{DD}
AV _{SS}	–	–	–	Connect to V _{SS}
BV _{DD}	–	–	–	Connect to V _{DD}
BV _{SS}	–	–	–	Connect to V _{SS}

Figure 1-1. Pin I/O Circuits (1/2)

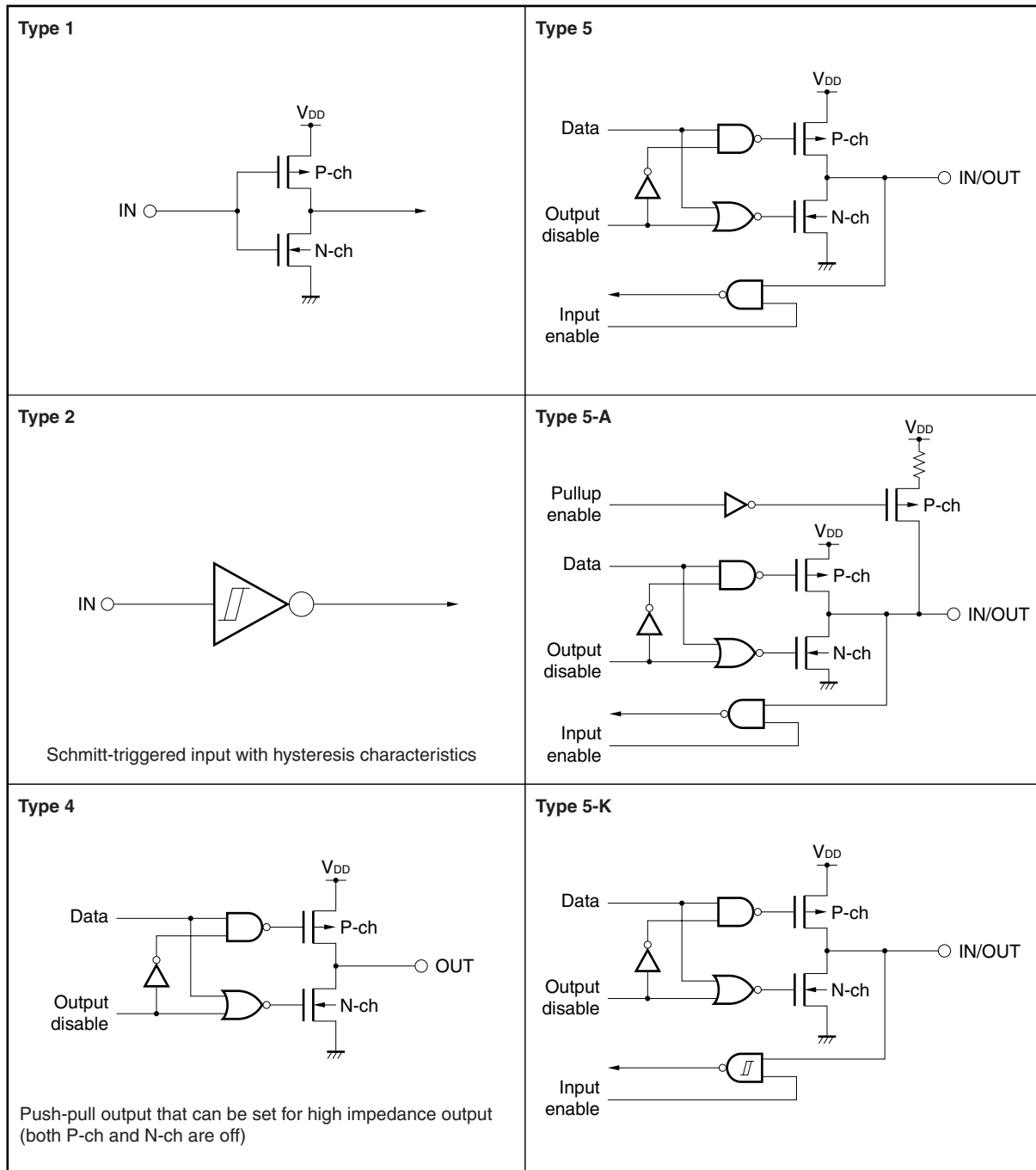
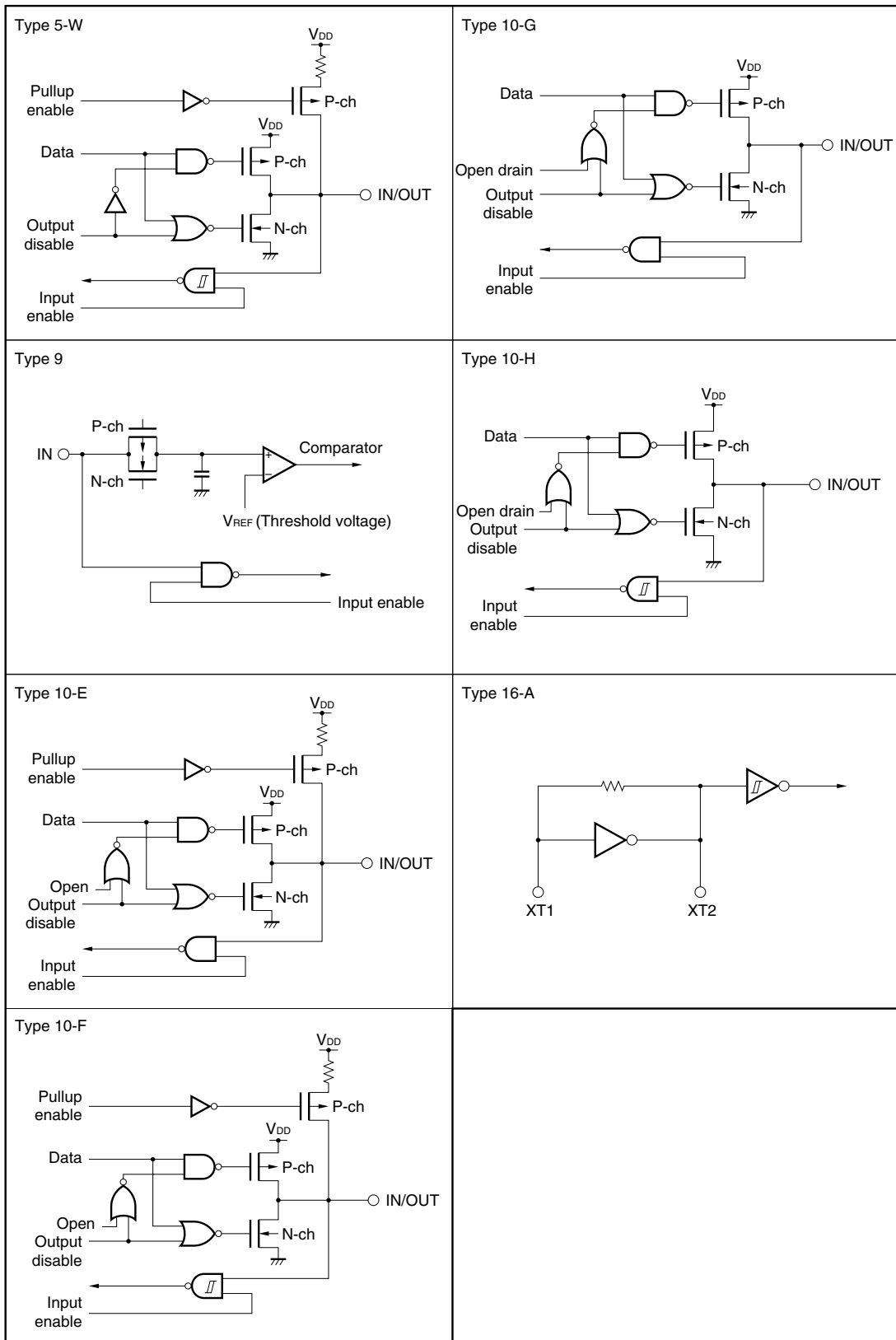


Figure 1-1. Pin I/O Circuits (2/2)



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +4.6	V
	AV _{DD}		-0.5 to +4.6	V
	BV _{DD}		-0.5 to +4.6	V
	V _{SS}		-0.5 to +0.5	V
	AV _{SS}		-0.5 to +0.5	V
	BV _{SS}		-0.5 to +0.5	V
Input voltage	V _{I1}	Note 1 , $\overline{\text{RESET}}$ (V _{DD})	-0.5 to V _{DD} + 0.5 ^{Note 4}	V
	V _{I2}	Note 2 , $\overline{\text{WAIT}}$ (BV _{DD})	-0.5 to BV _{DD} + 0.5 ^{Note 4}	V
Clock input voltage	V _K	X1, V _{DD} = 2.7 to 3.6 V	-0.5 to V _{DD} + 1.0 ^{Note 4}	
Analog input voltage	V _{IAN}	Note 3 (AV _{DD})	-0.5 to AV _{DD} + 0.5 ^{Note 4}	V
Analog reference input voltage	AV _{REF}	AV _{REF} pin	-0.5 to AV _{DD} + 0.5 ^{Note 4}	V
Output current, low	I _{OL}	Per pin	4.0	mA
		Total for P00 to P07, P150 to P157	25	mA
		Total for P100 to P107, P160 to P167	25	mA
		Total for P170 to P177, P190 to P197	25	mA
		Total for P124 to P127, P180 to P187	25	mA
		Total for P30 to P37, P120 to P123	25	mA
		Total for P12 to P15, P20 to P27, P110 to P113	25	mA
		Total for P50 to P57, P60 to P65, CLKOUT	25	mA
		Total for P40 to P47, P90 to P96	25	mA
		Total for P130 to P137, P140 to P147	25	mA
Output current, high	I _{OH}	Per pin	-4.0	mA
		Total for P00 to P07, P150 to P157	-25	mA
		Total for P100 to P107, P160 to P167	-25	mA
		Total for P170 to P177, P190 to P197	-25	mA
		Total for P124 to P127, P180 to P187	-25	mA
		Total for P30 to P37, P120 to P123	-25	mA
		Total for P12 to P15, P20 to P27, P110 to P113	-25	mA
		Total for P50 to P57, P60 to P65, CLKOUT	-25	mA
		Total for P40 to P47, P90 to P96	-25	mA
		Total for P130 to P137, P140 to P147	-25	mA
* Output voltage	V _{O1}	Note 1 , V _{DD} = 2.7 to 3.6 V	-0.5 to V _{DD} + 0.5 ^{Note 4}	V
	V _{O2}	Note 2 , CLKOUT, BV _{DD} = 2.7 to 3.6 V	-0.5 to BV _{DD} + 0.5 ^{Note 4}	V
Operating ambient temperature	T _A		-40 to +85	°C
Storage temperature	T _{stg}		-65 to +150	°C

Notes 1. Ports 0, 1, 2, 3, 10, 11, 12, 13, 14, 15, 16, 17, 18, and 19 (includes alternate function pins)

2. Ports 4, 5, 6, and 9 (includes alternate function pins)

3. Ports 7 and 8 (includes alternate function pins)
4. Be sure not to exceed each absolute maximum rating (MAX.).

Cautions

1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, direct connections among open-drain and open-collector pins are possible, as are direct connections to external circuits that have timing designed to prevent output contention with pins that become high-impedance.
2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance ($T_A = 25^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = V_{SS} = AV_{SS} = BV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_i	$f_c = 1\text{ MHz}$ Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{iO}				15	pF
Output capacitance	C_o				15	pF

★ **Operating Conditions**

(1) CPU operating frequency

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU operating frequency	f_{CPU}	$V_{DD} = 2.7\text{ to }3.6\text{ V}$	0.5		16	MHz
		$V_{DD} = 3.1\text{ to }3.6\text{ V}$	0.5		20	MHz

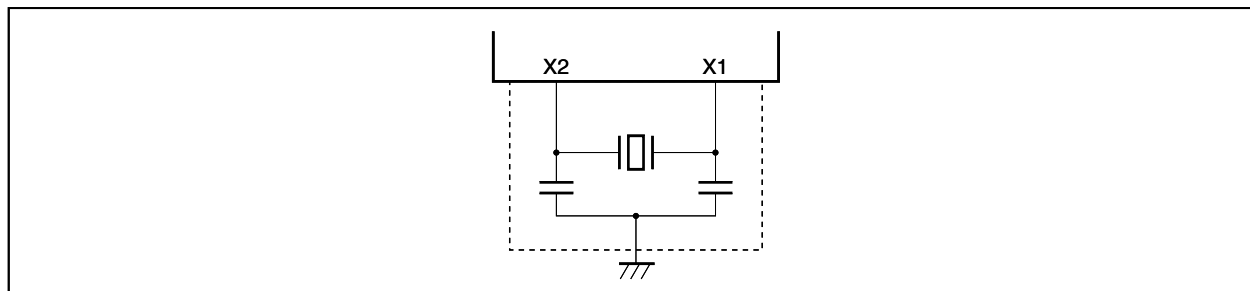
(2) Operating frequency for each supply voltage

Operating Frequency	Supply Voltage ($V_{DD} = AV_{DD} = BV_{DD}$)
$4\text{ MHz} \leq f_{xx} \leq 16\text{ MHz}$	2.7 to 3.6 V
$4\text{ MHz} \leq f_{xx} \leq 20\text{ MHz}$	3.1 to 3.6 V
$f_{XT} = 32.768\text{ kHz}$ (watch operation only)	2.7 to 3.6 V

Recommended Oscillator

(1) Main clock oscillator ($T_A = -40$ to $+85^\circ\text{C}$)

(a) Ceramic oscillator or crystal resonator connection

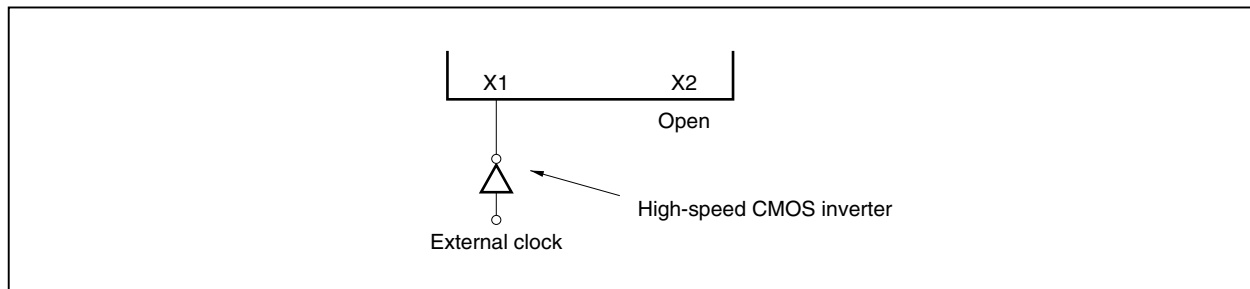


Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Oscillation frequency	f_{xx}	$V_{DD} = 2.7$ to 3.6 V	4		16	MHz
		$V_{DD} = 3.1$ to 3.6 V	4		20	MHz
Oscillation stabilization time		After reset release		$2^{19}/f_{xx}$		s
		After STOP mode release		Note		s

Note Values vary depending on the settings of the oscillation stabilization time selection register (OSTS).

- Remarks**
1. Place the oscillator as close as possible to X1 and X2.
 2. Do not wire other signal lines within the broken lines.
 3. For resonator selection and oscillation constants, customers are advised to either evaluate the oscillation themselves, or apply to the resonator manufacturer for evaluation.

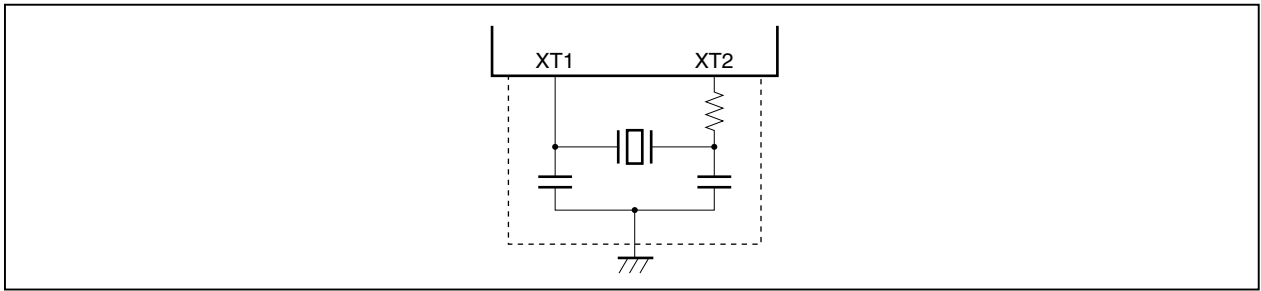
★ (b) External clock input



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_{xx}	$V_{DD} = 2.7$ to 3.6 V	4		16	MHz
		$V_{DD} = 3.1$ to 3.6 V	4		20	MHz

- Cautions**
1. Place the high-speed CMOS inverter as close as possible to the X1 pin.
 2. Perform a sufficient evaluation to determine whether the μ PD703038, 703038Y, 703039, 703039Y, 703040, 703040Y, 703041, or 703041Y matches the high-speed CMOS inverter.

(2) Subclock oscillator ($T_A = -40$ to $+85^\circ\text{C}$)



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}	$V_{DD} = 2.7$ to 3.6 V	32	32.768	35	kHz
Oscillation stabilization time				10		s

- Remarks**
1. Place the oscillator as close as possible to XT1 and XT2.
 2. Do not wire other signal lines within the broken lines.
 3. For resonator selection and oscillation constants, customers are advised to either evaluate the oscillation themselves, or apply to the resonator manufacturer for evaluation.

★ DC Characteristics

(1) 16 MHz operation

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins in Note 1 , $\overline{\text{WAIT}}$	$0.7BV_{DD}$		BV_{DD}	V
	V_{IH2}	Pins in Note 2	$0.7V_{DD}$		V_{DD}	V
	V_{IH3}	Pins in Note 3 , $\overline{\text{RESET}}$	$0.75V_{DD}$		V_{DD}	V
	V_{IH4}	Pins in Note 4	$0.7AV_{DD}$		AV_{DD}	V
	V_{IH5}	X1	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	Pins in Note 1 , $\overline{\text{WAIT}}$	BV_{SS}		$0.3BV_{DD}$	V
	V_{IL2}	Pins in Note 2	V_{SS}		$0.3V_{DD}$	V
	V_{IL3}	Pins in Note 3 , $\overline{\text{RESET}}$	V_{SS}		$0.2V_{DD}$	V
	V_{IL4}	Pins in Note 4	AV_{SS}		$0.3AV_{DD}$	V
	V_{IL5}	X1	V_{SS}		$0.2V_{DD}$	V
Output voltage, high	V_{OH1}	Note 1 , CLKOUT	$I_{OH} = -3$ mA	$0.8BV_{DD}$		V
	V_{OH2}	Notes 2, 3	$I_{OH} = -1$ mA	$0.8V_{DD}$		V
Output voltage, low	V_{OL1}	Note 1 , CLKOUT	$I_{OL} = 1.6$ mA		0.4	V
	V_{OL2}	Notes 2, 3 (except P10, P12, P20, P22)	$I_{OL} = 1.6$ mA		0.4	V
	V_{OL3}	P10, P12, P20, P22	$I_{OL} = 3$ mA		0.4	V
Input leakage current, high	I_{LH1}	$V_I = V_{DD} = AV_{DD} = BV_{DD}$	Other than X1		5	μA
	I_{LH2}		X1		20	μA
Input leakage current, low	I_{LIL1}	$V_I = 0$ V	Other than X1		-5	μA
	I_{LIL2}		X1		-20	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD} = AV_{DD} = BV_{DD}$			5	μA
Output leakage current, low	I_{LOL}	$V_O = 0$ V			-5	μA
Supply current ^{Note 5}	I_{DD1}	Normal operation mode ($f_{xx} = 16$ MHz)		22	40	mA
	I_{DD2}	HALT mode ($f_{xx} = 16$ MHz)		13	27	mA
	I_{DD3}	IDLE mode ($f_{xx} = 16$ MHz)		1.2	4	mA
	I_{DD4}	STOP mode (subclock operation: $f_{XT} = 32.768$ kHz, watch timer operation)		10	70	μA
		STOP mode (subclock stopped, $XT1 = V_{SS}$)		1	60	μA
Pull-up resistor	R_L	$V_{IN} = 0$ V	10	30	100	k Ω

Notes 1. Ports 4, 5, 6, and 9 (includes alternate function pins)

2. P11, P14, P21, P24, P34, P35, P100 to P107, P110 to P113, P121, P123, P136, P137, P146, P147, P150 to P157, P160 to P163, P165 to P167, P180 to P187, and P190 to P197 (includes alternate function pins)

3. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, P120, P122, P124 to P127, P130 to P135, P140 to P145, P164, and P170 to P177 (includes alternate function pins)

4. Ports 7 and 8 (includes alternate function pins)

Caution The typical values listed are those when $V_{DD} = 3.3$ V. The current that is consumed at output buffers is not included.

(2) 20 MHz operation

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 3.1$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins in Note 1 , $\overline{\text{WAIT}}$	$0.7BV_{DD}$		BV_{DD}	V
	V_{IH2}	Pins in Note 2	$0.7V_{DD}$		V_{DD}	V
	V_{IH3}	Pins in Note 3 , RESET	$0.75V_{DD}$		V_{DD}	V
	V_{IH4}	Pins in Note 4	$0.7AV_{DD}$		AV_{DD}	V
	V_{IH5}	X1	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	Pins in Note 1 , $\overline{\text{WAIT}}$	BV_{SS}		$0.3BV_{DD}$	V
	V_{IL2}	Pins in Note 2	V_{SS}		$0.3V_{DD}$	V
	V_{IL3}	Pins in Note 3 , RESET	V_{SS}		$0.2V_{DD}$	V
	V_{IL4}	Pins in Note 4	AV_{SS}		$0.3AV_{DD}$	V
	V_{IL5}	X1	V_{SS}		$0.2V_{DD}$	V
Output voltage, high	V_{OH1}	Note 1 , CLKOUT	$I_{OH} = -3$ mA	$0.8BV_{DD}$		V
	V_{OH2}	Notes 2, 3	$I_{OH} = -1$ mA	$0.8V_{DD}$		V
Output voltage, low	V_{OL1}	Note 1 , CLKOUT	$I_{OL} = 1.6$ mA		0.4	V
	V_{OL2}	Notes 2, 3 (except P10, P12, P20, P22)	$I_{OL} = 1.6$ mA		0.4	V
	V_{OL3}	P10, P12, P20, P22	$I_{OL} = 3$ mA		0.4	V
Input leakage current, high	I_{LIH1}	$V_i = V_{DD} = AV_{DD} = BV_{DD}$	Other than X1		5	μA
	I_{LIH2}	BV_{DD}	X1		20	μA
Input leakage current, low	I_{LIL1}	$V_i = 0$ V	Other than X1		-5	μA
	I_{LIL2}		X1		-20	μA
Output leakage current, high	I_{LOH}	$V_o = V_{DD} = AV_{DD} = BV_{DD}$			5	μA
Output leakage current, low	I_{LOL}	$V_o = 0$ V			-5	μA
Supply current	I_{DD1}	Normal operation mode ($f_{xx} = 20$ MHz)		25	45	mA
	I_{DD2}	HALT mode ($f_{xx} = 20$ MHz)		14	30	mA
	I_{DD3}	IDLE mode ($f_{xx} = 20$ MHz)		1.4	4.5	mA
	I_{DD4}	STOP mode (subclock operation: $f_{XT} = 32.768$ kHz, watch timer operation)		10	70	μA
		STOP mode (subclock stopped, $XT1 = V_{SS}$)		1	60	μA
Pull-up resistor	R_L	$V_{IN} = 0$ V	10	30	100	k Ω

Notes 1. Ports 4, 5, 6, and 9 (includes alternate function pins)

2. P11, P14, P21, P24, P34, P35, P100 to P107, P110 to P113, P121, P123, P136, P137, P146, P147, P150 to P157, P160 to P163, P165 to P167, P180 to P187, and P190 to P197 (includes alternate function pins)

3. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, P120, P122, P124 to P127, P130 to P135, P140 to P145, P164, and P170 to P177 (includes alternate function pins)

4. Ports 7 and 8 (includes alternate function pins)

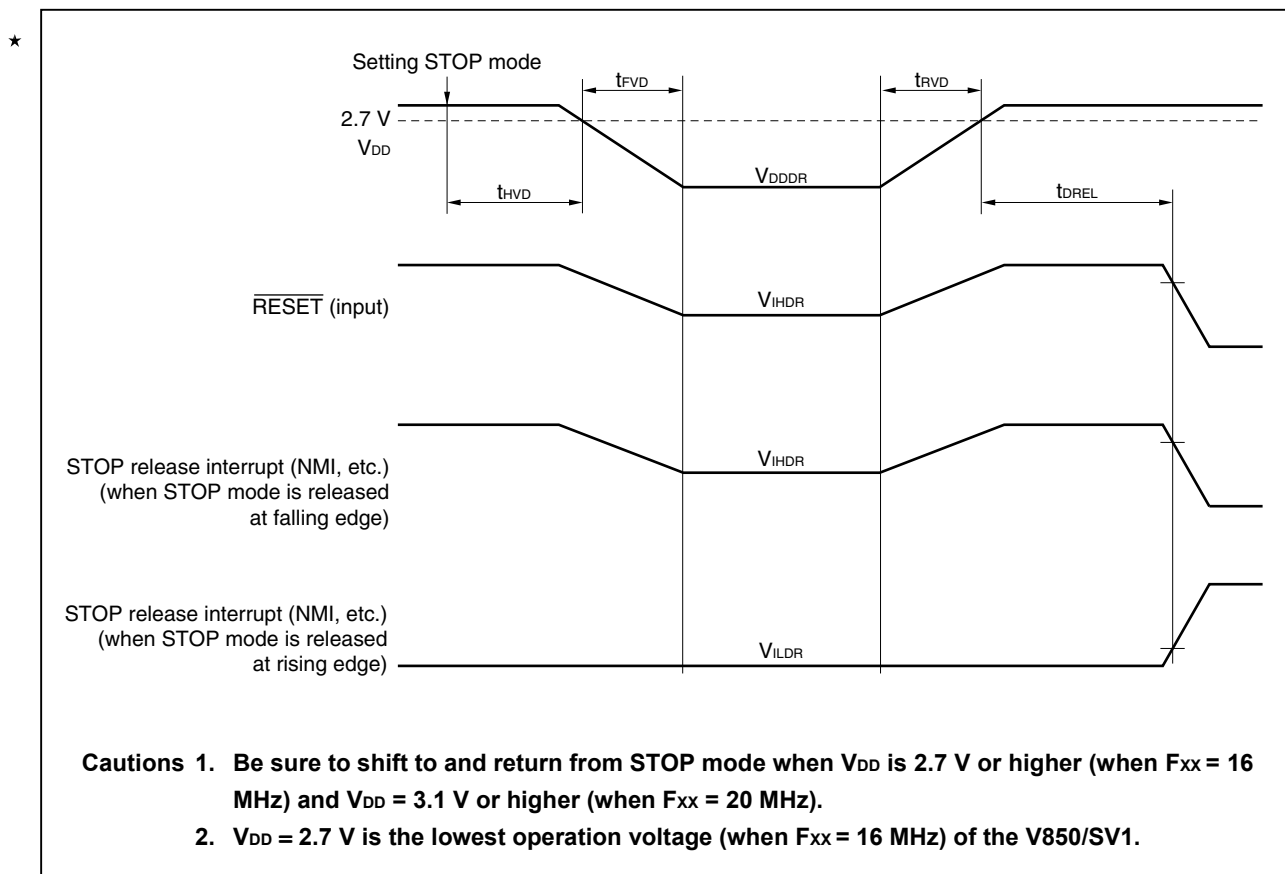
Caution The typical values listed are those when $V_{DD} = 3.3$ V. The current that is consumed at output buffers is not included.

Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

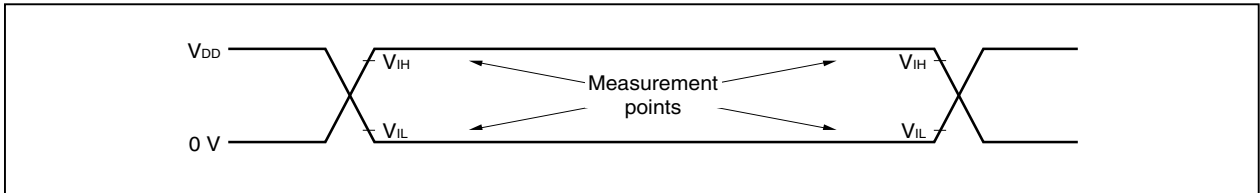
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	1.8		3.6	V
Data retention current	I_{DDDR}	V_{DDDR} [V], $XT1 = V_{SS}$		1	60	μA
Supply voltage rise time	t_{rVD}		200			μs
Supply voltage fall time	t_{fVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{hVD}		0			ms
STOP release signal input time	t_{dREL}		0			ms
Data retention high-level input voltage	V_{IHDR}	All input ports	V_{IHn}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports	0		V_{ILn}	V

Remark n = 1 to 5

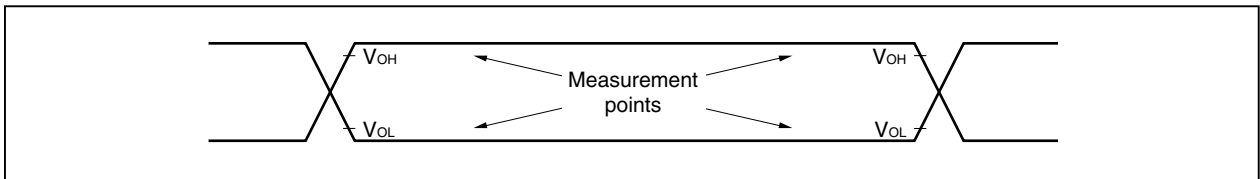


AC Characteristics

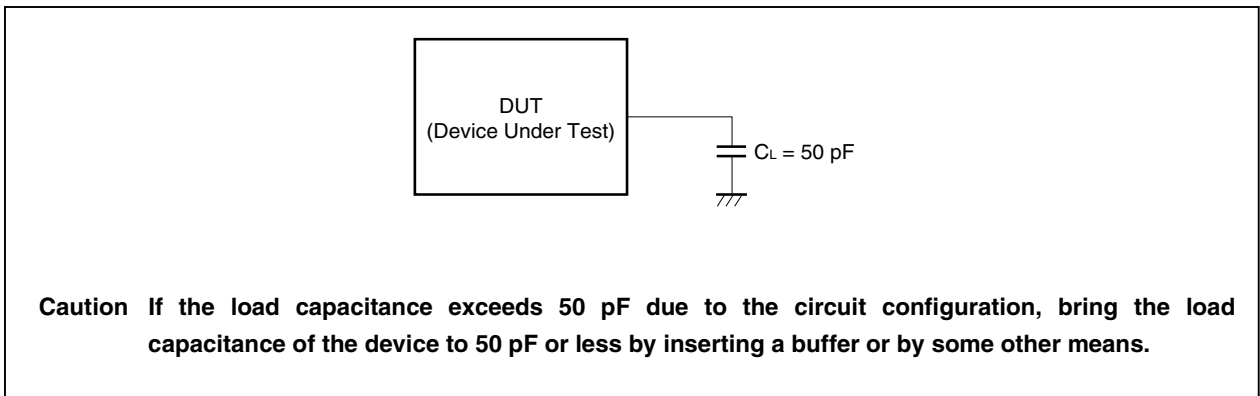
AC test input measurement points (V_{DD} , BV_{DD} , AV_{DD})



AC test output measurement points (BV_{DD})



Load conditions



★ Clock Timing

(1) 16 MHz operation

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		62.5	250	ns
X1 input high-level width	t_{WXH}	<2>		28.2		ns
X1 input low-level width	t_{WXL}	<3>		31.2		ns
X1 input rise time	t_{XR}	<4>			$0.5(<1> - <2> - <3>)$	ns
X1 input fall time	t_{XF}	<5>			$0.5(<1> - <2> - <3>)$	ns
CLKOUT output cycle	t_{CYK}	<6>		62.5 ns	$2 \mu\text{s}$	
CLKOUT high-level width	t_{WKH}	<7>		$0.4t_{CYK} - 10$		ns
CLKOUT low-level width	t_{WKL}	<8>		$0.4t_{CYK} - 10$		ns
CLKOUT rise time	t_{KR}	<9>			10	ns
CLKOUT fall time	t_{KF}	<10>			10	ns

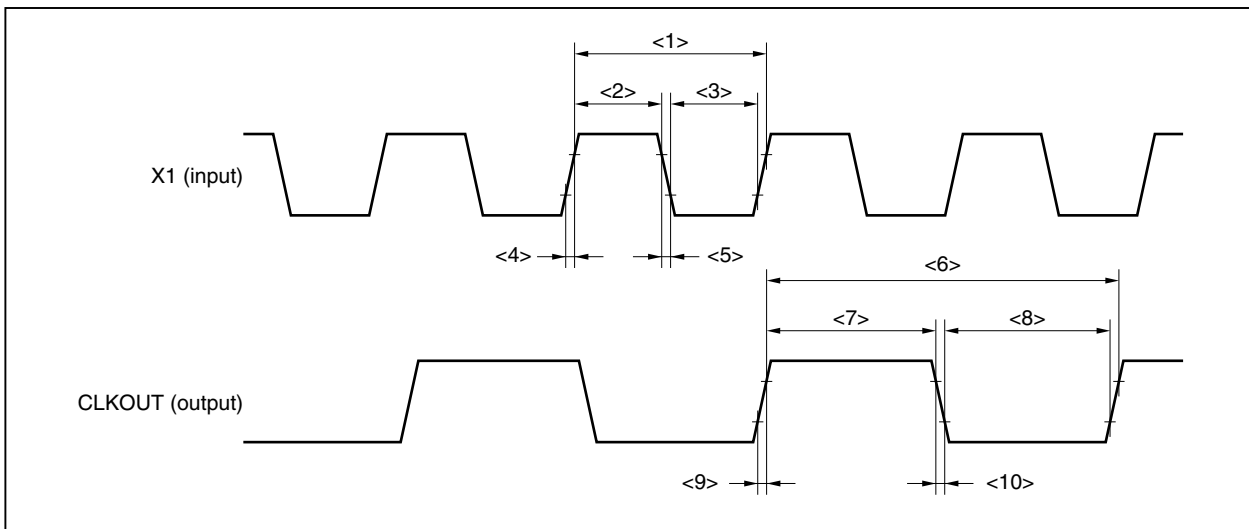
Remark T = t_{CYK}

(2) 20 MHz operation

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 3.1$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		50.0	250	ns
X1 input high-level width	t_{WXH}	<2>		22.5		ns
X1 input low-level width	t_{WXL}	<3>		22.5		ns
X1 input rise time	t_{XR}	<4>			$0.5(<1> - <2> - <3>)$	ns
X1 input fall time	t_{XF}	<5>			$0.5(<1> - <2> - <3>)$	ns
CLKOUT output cycle	t_{CYK}	<6>		50 ns	$2 \mu\text{s}$	
CLKOUT high-level width	t_{WKH}	<7>		$0.4t_{CYK} - 10$		ns
CLKOUT low-level width	t_{WKL}	<8>		$0.4t_{CYK} - 10$		ns
CLKOUT rise time	t_{KR}	<9>			10	ns
CLKOUT fall time	t_{KF}	<10>			10	ns

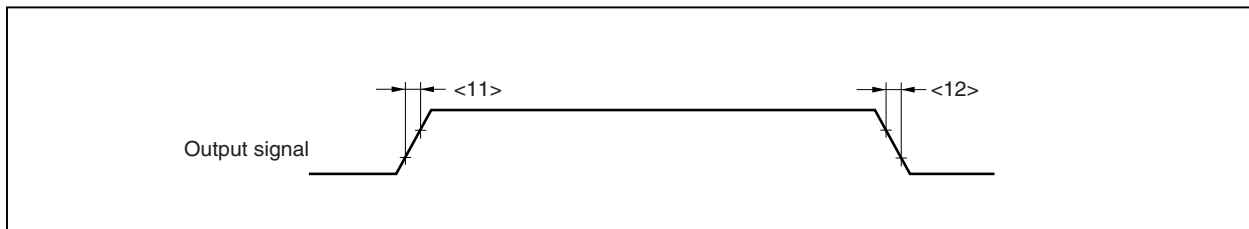
Clock Timing



Output Timing of Pins Other Than CLKOUT, P4, P5, P6, and P9

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	t_{OR}	<11>		20	ns
Output fall time	t_{OF}	<12>		20	ns



★

Bus Timing (CLKOUT Asynchronous)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{\text{ASTB}}\downarrow$)	t_{SAST}	<13>	$0.5T - 20$		ns
Address hold time (from $\overline{\text{ASTB}}\downarrow$)	t_{HSTA}	<14>	$0.5T - 15$		ns
Address float delay time from $\overline{\text{DSTB}}\downarrow$	t_{FDA}	<15>		2	ns
Data input setup time from address	t_{SAID}	<16>		$(2 + n)T - 30$	ns
Data input setup time from $\overline{\text{DSTB}}\downarrow$	t_{SDID}	<17>		$(1 + n)T - 30$	ns
Delay time from $\overline{\text{ASTB}}\downarrow$ to $\overline{\text{DSTB}}\downarrow$	t_{DSTD}	<18>	$0.5T - 15$		ns
Data input hold time (from $\overline{\text{DSTB}}\uparrow$)	t_{HDID}	<19>	0		ns
Address output time from $\overline{\text{DSTB}}\uparrow$	t_{DDA}	<20>	$(1 + i)T - 15$		ns
Delay time from $\overline{\text{DSTB}}\uparrow$ to $\overline{\text{ASTB}}\uparrow$	t_{DDST1}	<21>	$0.5T - 15$		ns
Delay time from $\overline{\text{DSTB}}\uparrow$ to $\overline{\text{ASTB}}\downarrow$	t_{DDST2}	<22>	$(1.5 + i)T - 15$		ns
$\overline{\text{DSTB}}$ low-level width	t_{WDL}	<23>	$(1 + n)T - 15$		ns
$\overline{\text{ASTB}}$ high-level width	t_{WSTH}	<24>	$T - 15$		ns
Data output time from $\overline{\text{DSTB}}\downarrow$	t_{DDOD}	<25>		15	ns
Data output setup time (to $\overline{\text{DSTB}}\uparrow$)	t_{SODD}	<26>	$(1 + n)T - 20$		ns
Data output hold time (from $\overline{\text{DSTB}}\uparrow$)	t_{HDOD}	<27>	$T - 15$		ns
$\overline{\text{WAIT}}$ setup time (to address)	t_{SAWT1}	<28>	$n \geq 1$	$1.5T - 30$	ns
	t_{SAWT2}	<29>		$(1 + n)T - 30$	ns
$\overline{\text{WAIT}}$ hold time (from address)	t_{HAWT1}	<30>	$n \geq 1$	$(0.5 + n)T$	ns
	t_{HAWT2}	<31>		$(1.5 + n)T$	ns
★ $\overline{\text{WAIT}}$ setup time (to $\overline{\text{ASTB}}\downarrow$)	t_{SSTWT1}	<32>	$n \geq 1$	$T - 25$	ns
	t_{SSTWT2}	<33>		$(1 + n)T - 25$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{ASTB}}\downarrow$)	t_{HSTWT1}	<34>	$n \geq 1$	$nT + 5$	ns
	t_{HSTWT2}	<35>		$(1 + n)T + 5$	ns
$\overline{\text{HLDRQ}}$ high-level width	t_{WHQH}	<36>	$T + 10$		ns
$\overline{\text{HLDAK}}$ low-level width	t_{WHAL}	<37>	$T - 15$		ns
Bus output delay time from $\overline{\text{HLDAK}}\uparrow$	t_{DHAC}	<38>	0		ns
★ Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	t_{DHQHA1}	<39>		$(2n + 7.5)T + 25$	ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	t_{DHQHA2}	<40>	$0.5T$	$1.5T + 25$	ns

Remarks 1. $T = 1/f_{\text{CPU}}$ (f_{CPU} : CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.

The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle states inserted after the read cycle (0 or 1).

4. The specifications described above are the values of when a clock with a duty ratio of 1:1 is input from X1.

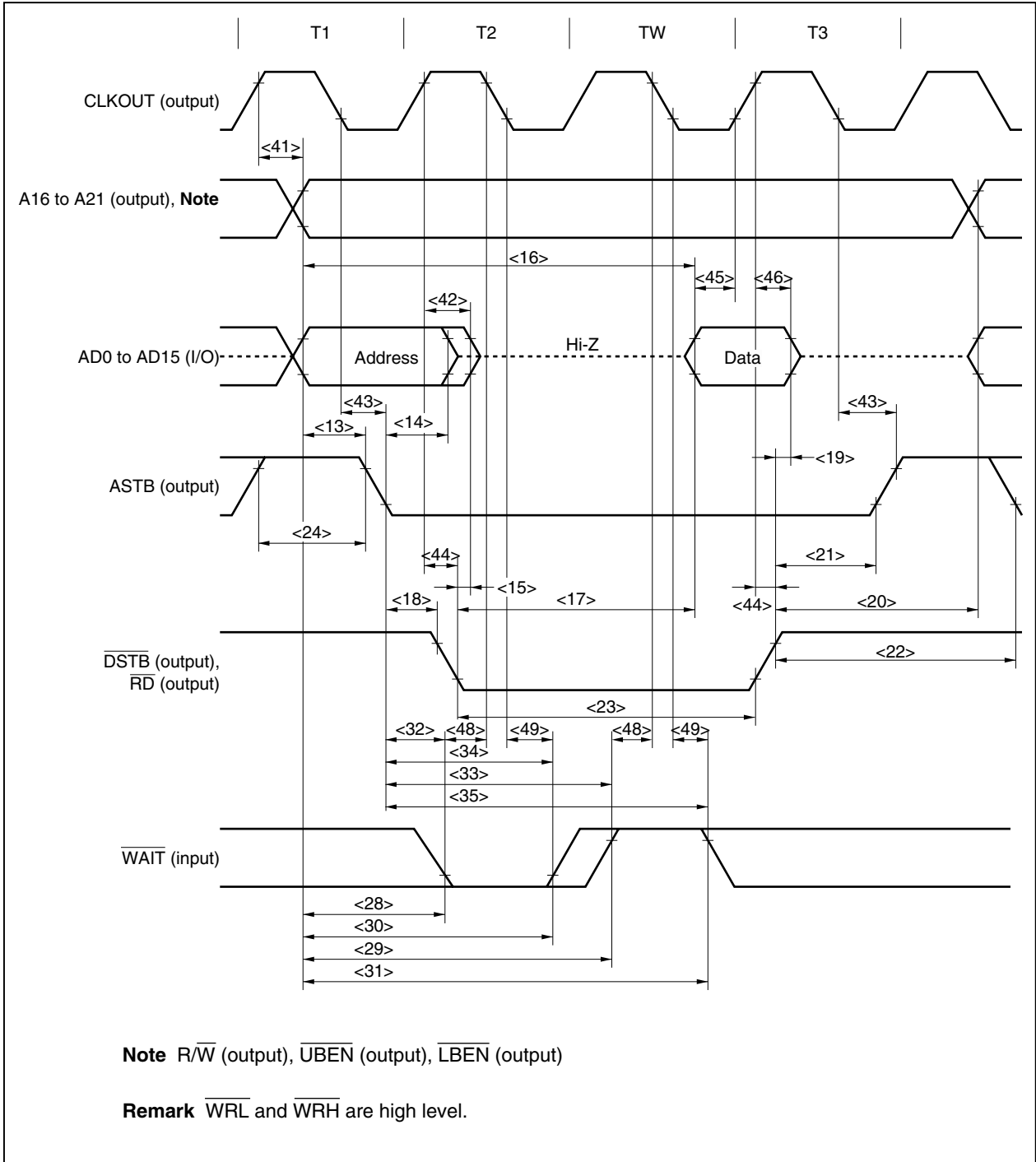
Bus Timing (CLKOUT Synchronous)

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

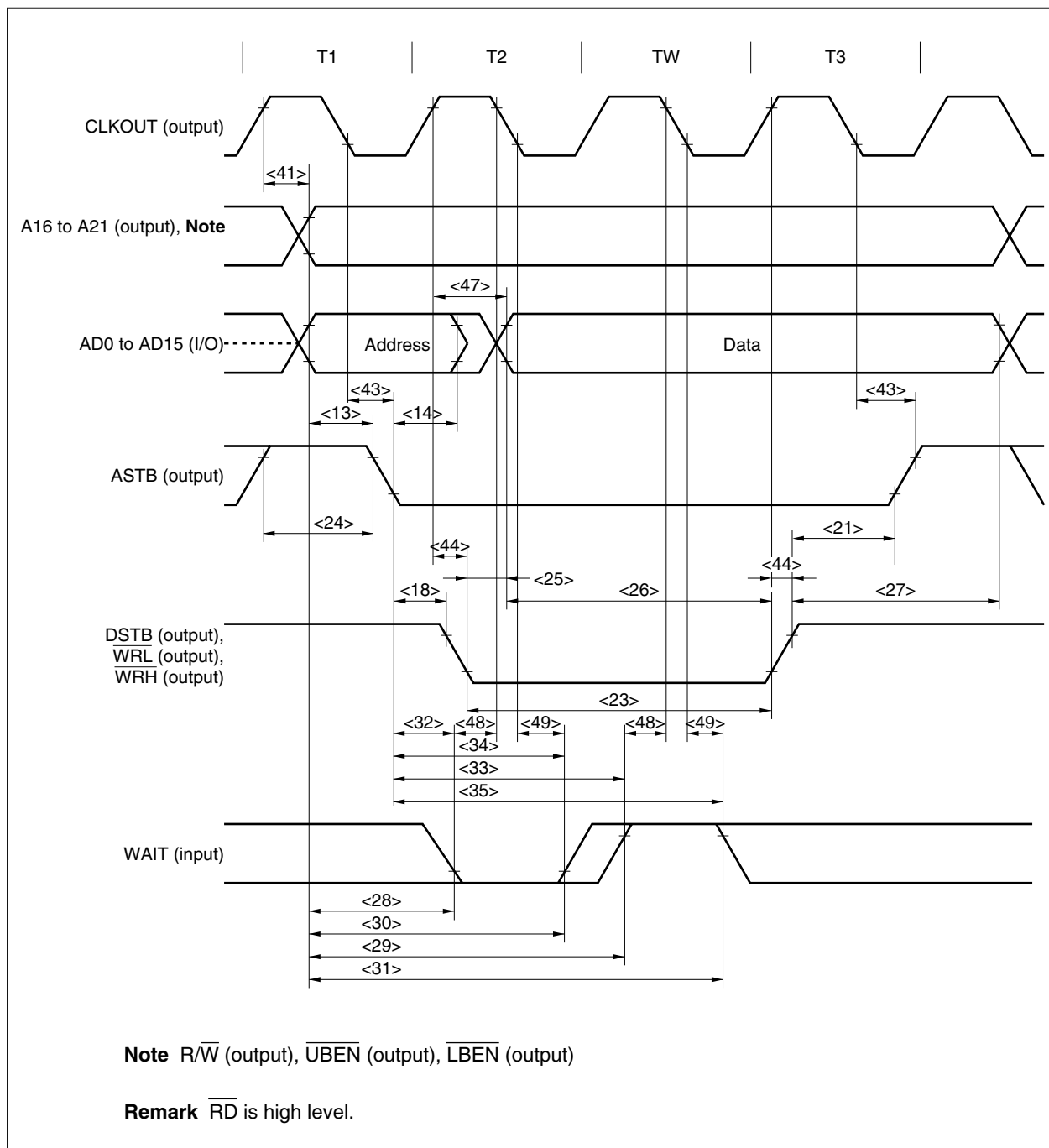
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address delay time from CLKOUT \uparrow	t_{DKA}	<41>		0	19	ns
Address float delay time from CLKOUT \uparrow	t_{FKA}	<42>		-12	7	ns
Delay time from CLKOUT \downarrow to ASTB \downarrow	t_{DKST}	<43>		-12	7	ns
Delay time from CLKOUT \uparrow to \overline{DSTB} \uparrow	t_{DKD}	<44>		-5	14	ns
Data input setup time (to CLKOUT \uparrow)	t_{SIDK}	<45>		15		ns
Data input hold time (from CLKOUT \uparrow)	t_{HKID}	<46>		5		ns
Data output delay time from CLKOUT \uparrow	t_{DKOD}	<47>			19	ns
\overline{WAIT} setup time (to CLKOUT \downarrow)	t_{SWTK}	<48>		15		ns
\overline{WAIT} hold time (from CLKOUT \downarrow)	t_{HKWT}	<49>		5		ns
\overline{HLDRQ} setup time (to CLKOUT \downarrow)	t_{SHQK}	<50>		15		ns
\overline{HLDRQ} hold time (from CLKOUT \downarrow)	t_{HKHQ}	<51>		5		ns
Float delay time from CLKOUT \uparrow	t_{DKF}	<52>			19	ns
Delay time from CLKOUT \uparrow to HLDA \overline{K}	t_{DKHA}	<53>			19	ns

Remark The specifications described above are the values of when a clock with a duty ratio of 1:1 is input from X1.

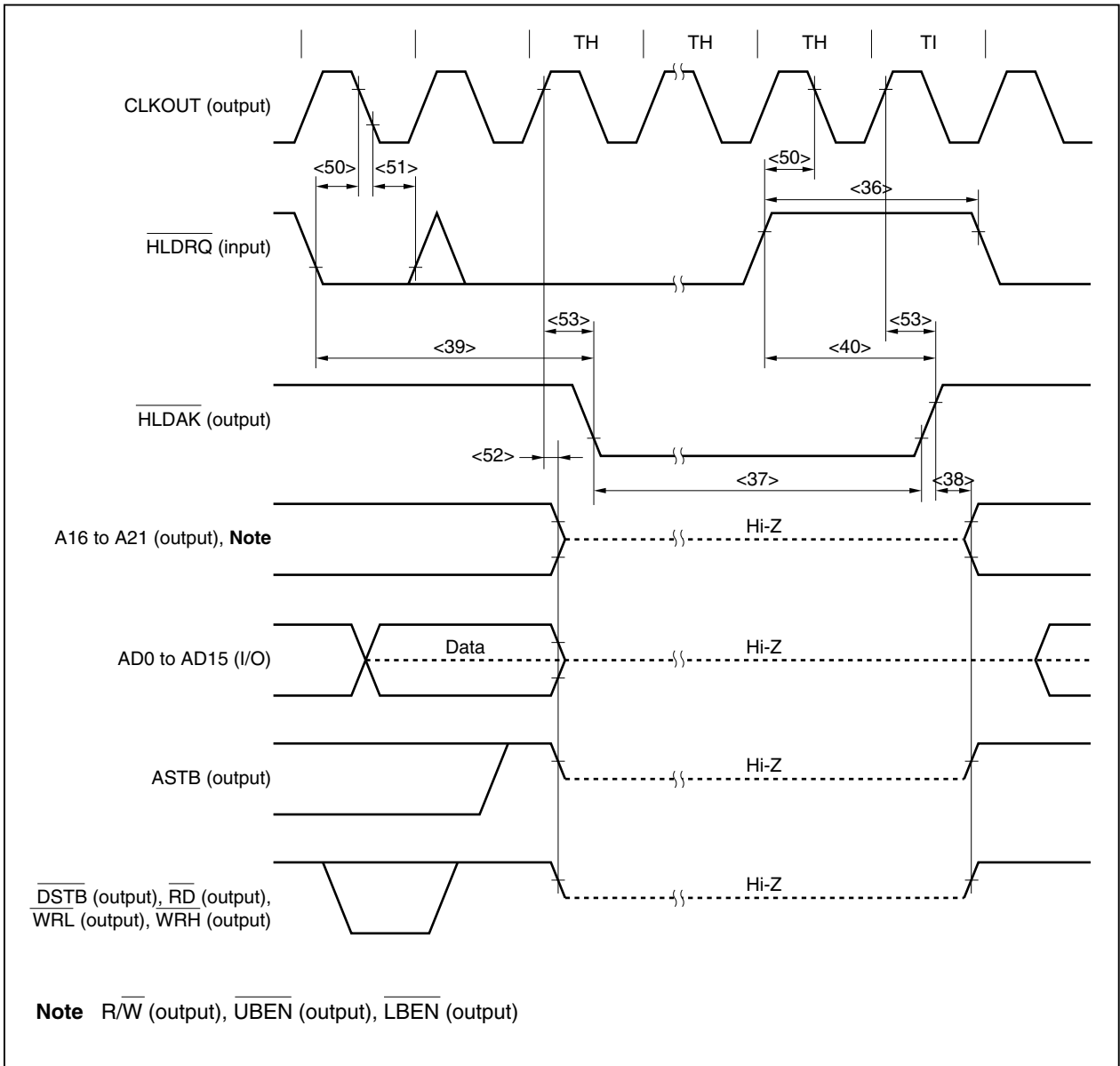
Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait)



Bus Hold

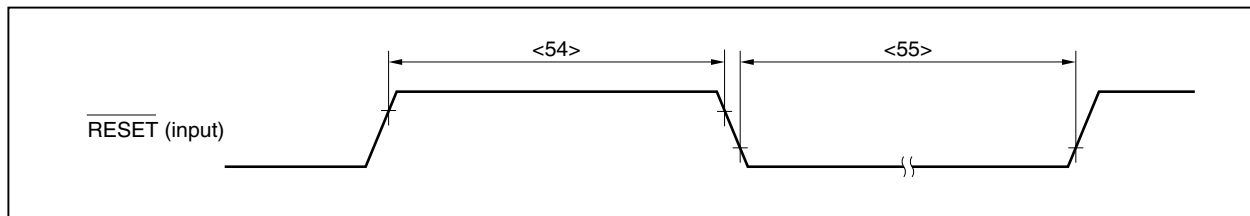


Reset/Interrupt Timing ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

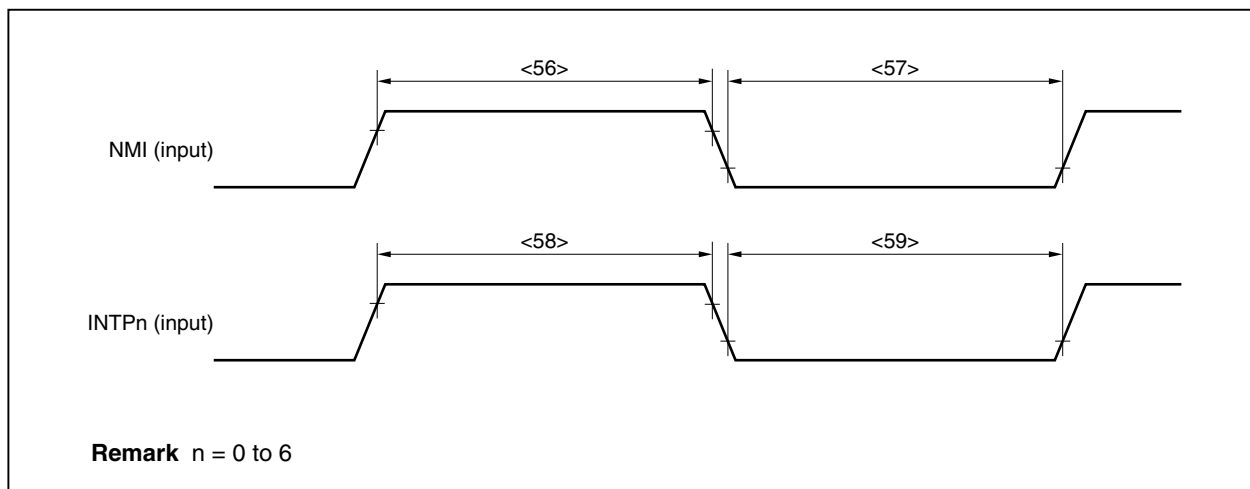
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RESE \bar{T} high-level width	t_{WRSH}	<54>	500		ns
RESE \bar{T} low-level width	t_{WRSL}	<55>	500		ns
NMI high-level width	t_{WNIH}	<56>	500		ns
NMI low-level width	t_{WNIL}	<57>	500		ns
INTP \bar{n} high-level width	t_{WITH}	<58> n = 0 to 3, analog noise elimination	500		ns
		n = 4, 5, digital noise elimination	$3T + 20$		ns
		n = 6, digital noise elimination	$3T_{smp} + 20$		ns
INTP \bar{n} low-level width	t_{WITL}	<59> n = 0 to 3, analog noise elimination	500		ns
		n = 4, 5, digital noise elimination	$3T + 20$		ns
		n = 6, digital noise elimination	$3T_{smp} + 20$		ns

- Remarks**
1. $T = 1/f_{xx}$
 2. T_{smp} = Noise elimination sampling clock frequency

Reset



Interrupt



TIn Input Timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Tl0n0, Tl0n1 (n = 00, 01) high-level width	t _{TIH}	<60>	$2T_{\text{sam}} + 20^{\text{Note}}$		ns
TIn (n = 2 to 7, 10, 11) high-level width			$3T + 20$		ns
Tl0n0, Tl0n1 (n = 00, 01) low-level width	t _{TIL}	<61>	$2T_{\text{sam}} + 20^{\text{Note}}$		ns
TIn (n = 2 to 7, 10, 11) low-level width			$3T + 20$		ns

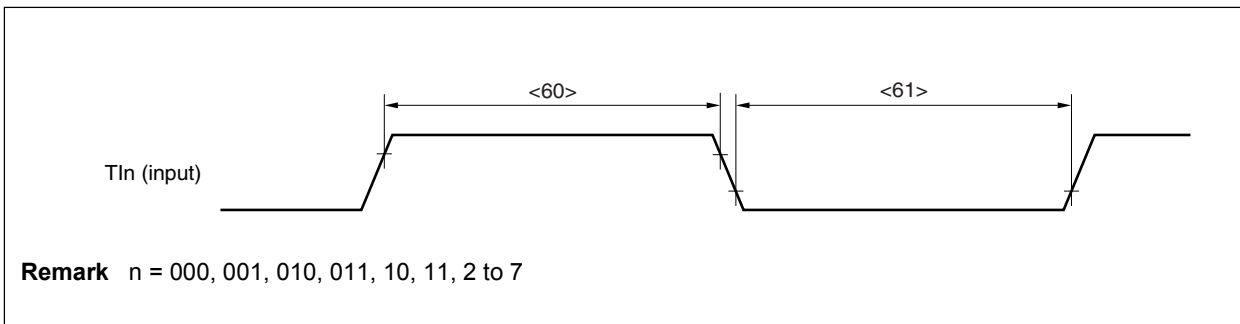
Note T_{sam} can be selected by setting bits PRMn2 to PRMn0 of prescaler mode registers n0, n1 (PRMn0, PRMn1) (n = 0, 1).

TM0 (PRM00, PRM01 registers): $T_{\text{sam}} = 2T, 4T, 16T, 64T, 256T, 1/\text{INTWTDN}$ period

TM1 (PRM10, PRM11 registers): $T_{\text{sam}} = 2T, 4T, 16T, 32T, 128T, 256T$

However, when the Tl0n0 valid edge is selected as the count clock, $T_{\text{sam}} = 2T$ (n = 0, 1).

Remark T: $1/f_{\text{xx}}$



Remark n = 000, 001, 010, 011, 10, 11, 2 to 7

3-Wire SIO Timing

(1) Master mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

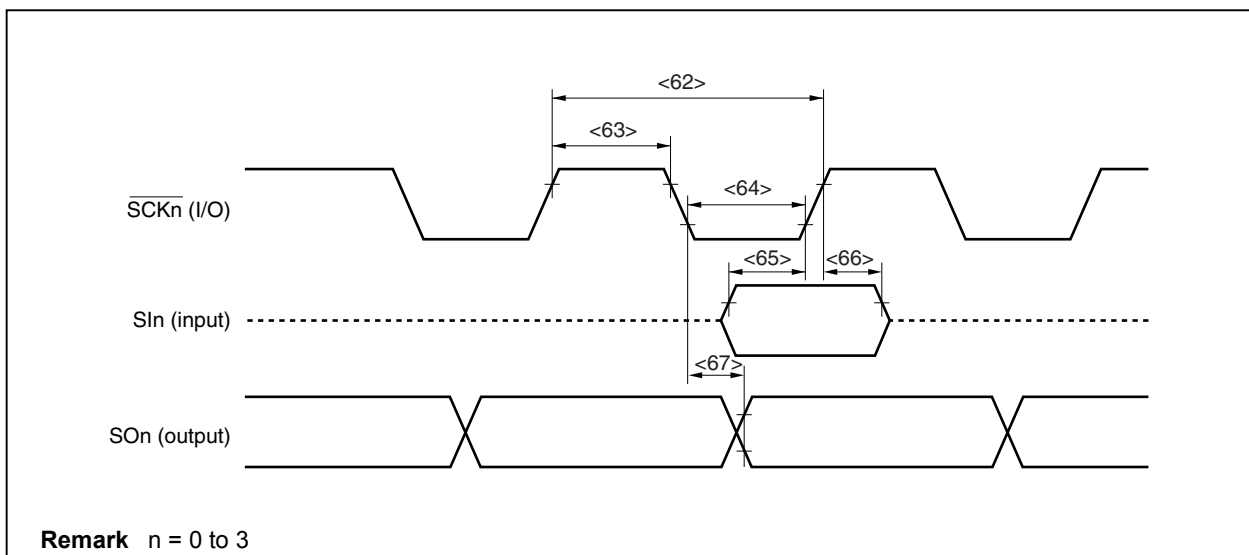
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle time	t_{KCY1}	<62>		400		ns
$\overline{\text{SCKn}}$ high-level width	t_{KH1}	<63>		140		ns
$\overline{\text{SCKn}}$ low-level width	t_{KL1}	<64>		140		ns
SIn setup time (to $\overline{\text{SCKn}}\uparrow$)	t_{SIK1}	<65>		50		ns
SIn hold time (from $\overline{\text{SCKn}}\downarrow$)	t_{KSI1}	<66>		50		ns
SO _n output delay time from $\overline{\text{SCKn}}\downarrow$	t_{KSO1}	<67>			60	ns

Remark n = 0 to 3

(2) Slave mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle time	t_{KCY2}	<62>		400		ns
★ $\overline{\text{SCKn}}$ high-level width	t_{KH2}	<63>		180		ns
★ $\overline{\text{SCKn}}$ low-level width	t_{KL2}	<64>		180		ns
SIn setup time (to $\overline{\text{SCKn}}\uparrow$)	t_{SIK2}	<65>		50		ns
SIn hold time (from $\overline{\text{SCKn}}\downarrow$)	t_{KSI2}	<66>		50		ns
SO _n output delay time from $\overline{\text{SCKn}}\downarrow$	t_{KSO2}	<67>			60	ns

Remark n = 0 to 3



Remark n = 0 to 3

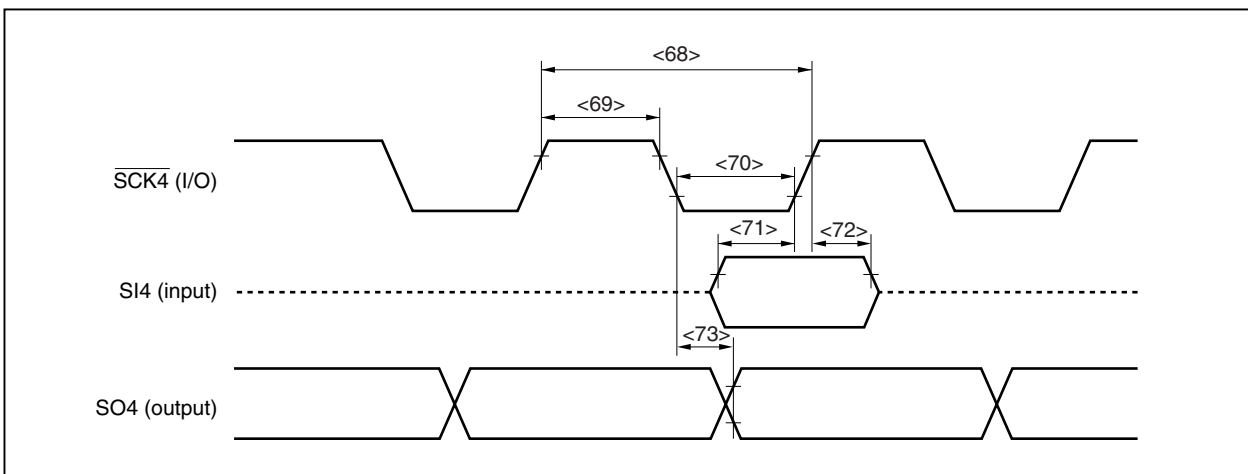
3-Wire Variable-Length CSI Timing

(1) Master mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCK4}}$ cycle time	t_{KCY1}	<68>	400		ns
$\overline{\text{SCK4}}$ high-level width	t_{KH1}	<69>	140		ns
$\overline{\text{SCK4}}$ low-level width	t_{KL1}	<70>	140		ns
SI4 setup time (to $\overline{\text{SCK4}}\uparrow$)	t_{SIK1}	<71>	50		ns
SI4 hold time (from $\overline{\text{SCK4}}\uparrow$)	t_{KSI1}	<72>	50		ns
SO4 output delay time from $\overline{\text{SCK4}}\downarrow$	t_{KSO1}	<73>		60	ns

(2) Slave mode ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{SCK4}}$ cycle time	t_{KCY2}	<68>	400		ns
* $\overline{\text{SCK4}}$ high-level width	t_{KH2}	<69>	180		ns
* $\overline{\text{SCK4}}$ low-level width	t_{KL2}	<70>	180		ns
SI4 setup time (to $\overline{\text{SCK4}}\uparrow$)	t_{SIK2}	<71>	50		ns
SI4 hold time (from $\overline{\text{SCK4}}\uparrow$)	t_{KSI2}	<72>	50		ns
SO4 output delay time from $\overline{\text{SCK4}}\downarrow$	t_{KSO2}	<73>		60	ns

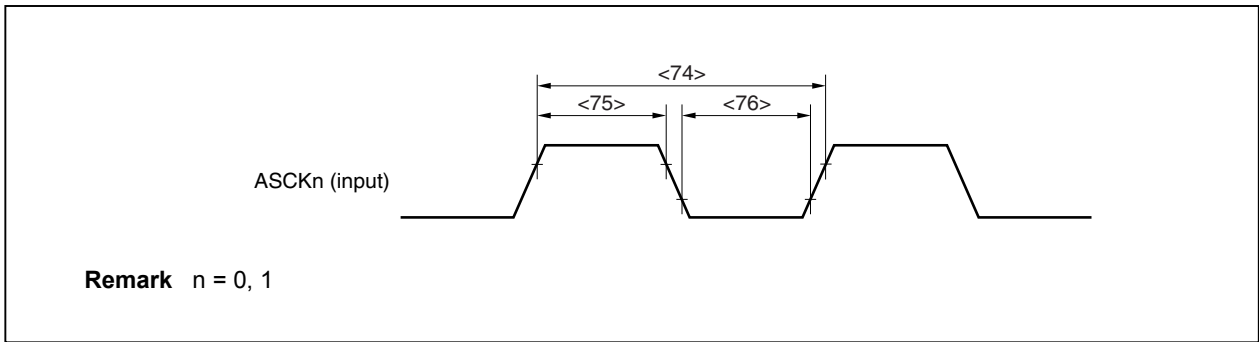


UART Timing

($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = BV_{DD} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS} = BV_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCKn cycle time	t_{kCY13}	<74>	200		ns
ASCKn high-level width	t_{kH13}	<75>	80		ns
ASCKn low-level width	t_{kL13}	<76>	80		ns

Remark n = 0, 1



I²C Bus Mode (Only for μ PD703038Y, 703039Y, 703040Y, and 703041Y)

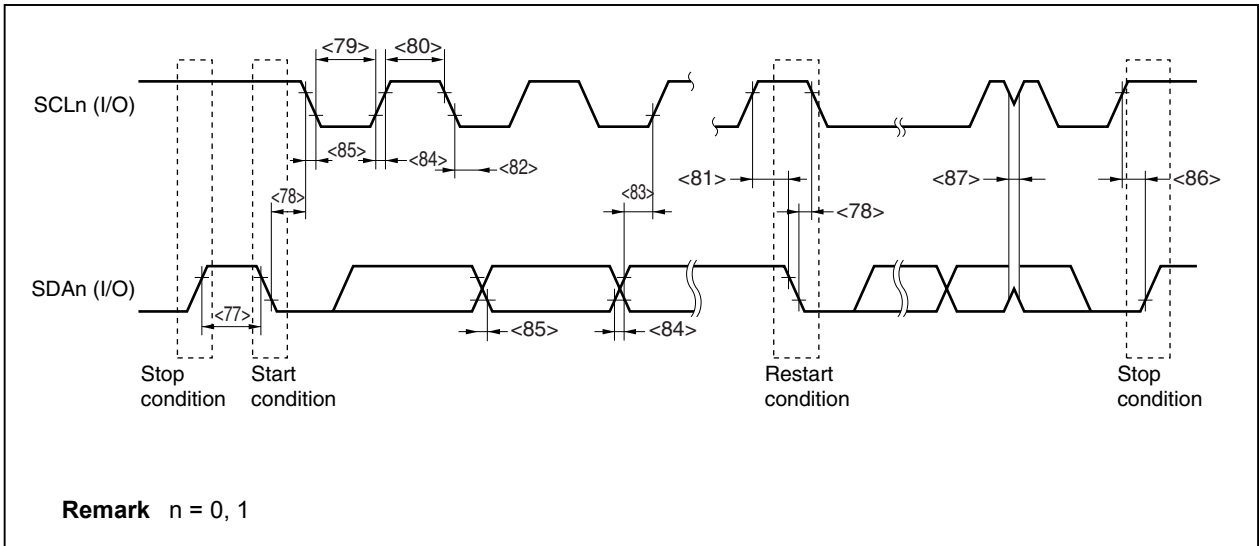
(T_A = -40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = 0 V, C_L = 50 pF)

Parameter		Symbol		Standard Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		f _{CLK}		0	100	0	400	kHz
Bus free time (between stop and start conditions)		t _{BUF}	<77>	4.7		1.3		μs
Hold time ^{Note 1}		t _{HD : STA}	<78>	4.0		0.6		μs
SCLn clock low-level width		t _{LOW}	<79>	4.7		1.3		μs
SCLn clock high-level width		t _{HIGH}	<80>	4.0		0.6		μs
Setup time of start/restart conditions		t _{SU : STA}	<81>	4.7		0.6		μs
Data hold time	CBUS-compatible master	t _{HD : DAT}	<82>	5.0				μs
	I ² C bus mode			0 ^{Note 2}		0 ^{Note 2}	0.9 ^{Note 3}	μs
Data setup time		t _{SU : DAT}	<83>	250		100 ^{Note 4}		ns
Rise time of SDAn and SCLn signals		t _R	<84>		1000	20 + 0.1Cb ^{Note 5}	300	ns
Fall time of SDAn and SCLn signals		t _F	<85>		300	20 + 0.1Cb ^{Note 5}	300	ns
Setup time of stop condition		t _{SU : STO}	<86>	4.0		0.6		μs
Pulse width of spike suppressed by input filter		t _{SP}	<87>			0	50	ns
Load capacitance of bus lines		Cb			400		400	pF

- Notes**
- The first clock pulse in the start condition is generated after the hold time.
 - The system must internally provide at least 300 ns hold time for the SDAn signal (at V_{IHmin.} of the SCLn signal) in order to fill the undefined area that appears at the SCLn falling edge.
 - If the system does not extend the low hold time (t_{LOW}), only the maximum data hold time (t_{HD : DAT}) needs to be satisfied.
 - The high-speed I²C bus is available in a standard mode I²C bus system. In this case, the following conditions should be satisfied.
 - When the system does not extend the low-state hold time of the SCLn signal
t_{SU : DAT} ≥ 250 ns
 - When the system extends the low-state hold time of the SCLn signal
Send the next data bit to the SDAn line before the SCLn line is released (t_{Rmax.} + t_{SU : DAT} = 1000 + 250 = 1250 ns: Standard mode I²C bus specification).
 - Cb: Total capacitance of one bus line (Unit: pF)

- Remarks**
- N = 0, 1
 - The maximum operating frequency of I²C is f_{xx} = 17 MHz. However, when 16 MHz < f_{xx} ≤ 17 MHz, use a system with V_{DD} = 3.1 V to 3.6 V.

I²C Bus Mode (Only for μ PD703039Y, 703040Y, and 703041Y)



A/D Converter ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = AV_{REF} = 2.7$ to 3.6 V, $AV_{SS} = V_{SS} = 0$ V, $C_L = 50$ pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error ^{Note 1}					± 0.8	%FSR
Conversion time	t_{CONV}		5		100	μs
Zero-scale error ^{Note 1}					± 0.4	%FSR
Full-scale error ^{Note 1}					± 0.4	%FSR
Integral linearity error ^{Note 2}					± 4.0	LSB
Differential linearity error ^{Note 2}					± 4.0	LSB
Analog reference voltage	AV_{REF}	$AV_{REF} = AV_{DD}$	2.7		3.6	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} current	AI_{REF}			360	500	μA
Supply current	AI_{DD}	In normal operation mode		1	3	mA
	AI_{DDS}	In STOP mode		1	10	μA

Notes 1. Excluding quantization error ($\pm 0.05\%$ FSR)

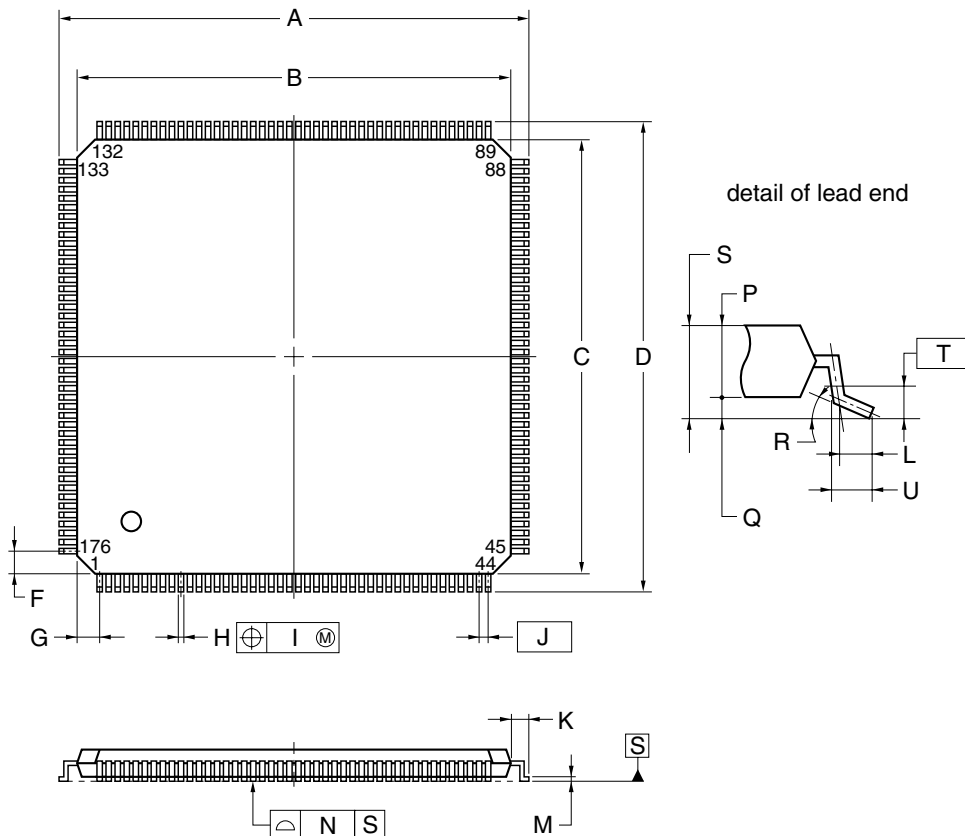
2. Excluding quantization error (± 0.5 LSB)

Remark LSB: Least Significant Bit

FSR: Full Scale Range

3. PACKAGE DRAWING

176-PIN PLASTIC LQFP (FINE PITCH) (24x24)



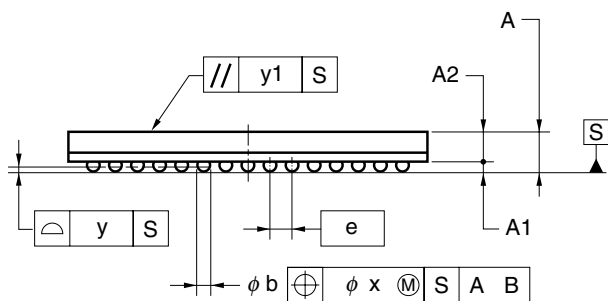
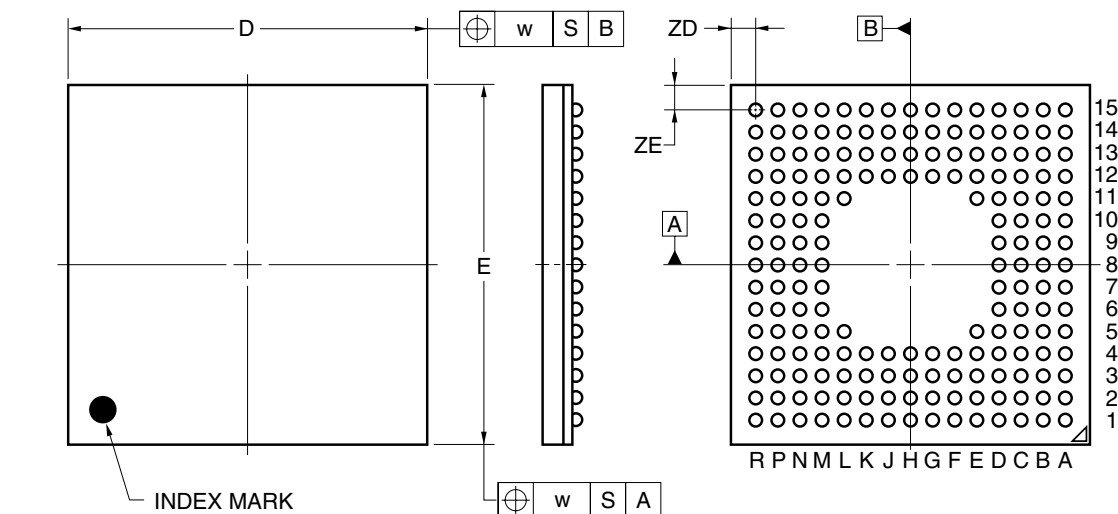
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	26.0±0.2
B	24.0±0.2
C	24.0±0.2
D	26.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.4
Q	0.1±0.05
R	3° ^{+4°} _{-3°}
S	1.5±0.1

S176GM-50-UEU

★ 180-PIN PLASTIC FBGA (13x13)



ITEM	MILLIMETERS
D	13.00±0.10
E	13.00±0.10
w	0.2
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	0.50±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.90
ZE	0.90

P180F1-80-EN2

4. RECOMMENDED SOLDERING CONDITIONS

The μ PD703038, 703038Y, 703039, 703039Y, 703040, 703040Y, 703041, and 703041Y should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

- (a) μ PD703039GM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)
- ★ μ PD703039YGM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)
- μ PD703040GM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)
- ★ μ PD703040YGM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)
- ★ μ PD703041GM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)
- ★ μ PD703041YGM-xxx-UEU: 176-pin plastic LQFP (fine pitch) (24 × 24)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 sec. max. (at 200°C or higher), Count: Twice or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

- ★ (b) μ PD703038F1-xxx-EN2: 180-pin plastic FBGA (13 × 13)
- μ PD703038YF1-xxx-EN2: 180-pin plastic FBGA (13 × 13)
- μ PD703039F1-xxx-EN2: 180-pin plastic FBGA (13 × 13)
- μ PD703039YF1-xxx-EN2: 180-pin plastic FBGA (13 × 13)
- μ PD703040F1-xxx-EN2: 180-pin plastic FBGA (13 × 13)
- μ PD703040YF1-xxx-EN2: 180-pin plastic FBGA (13 × 13)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: Twice or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 sec. (at 200°C or higher), Count: Twice or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Related document μ PD70F3038, 70F3038Y, 70F3040, 70F3040Y Data Sheet (U14622E)

Reference document Electrical Characteristics for Microcomputer (U15170J) ^{Note}

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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