DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, 70F3035AY

V850/SB2™

32-/16-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, and 70F3035AY (V850/SB2) are 32-/16-bit single-chip microcontrollers of the V850 Family™ for AV equipment. 32-bit CPU, ROM, RAM, timer/counters, serial interfaces, A/D converter, DMA controller, and so on are integrated on a single chip.

The μPD70F3035A and 70F3035AY have flash memory in place of the internal mask ROM of the μPD703035A and 703035AY. Because flash memory allows the program to be written and erased electrically with the device mounted on the board, these products are ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850/SB1™, V850/SB2 User's Manual Hardware: U13850E
V850 Family User's Manual Architecture: U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 76.9 ns (@ internal 13 MHz operation)
- General-purpose registers: 32 bits × 32 registers
- Instruction set: Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space: 16 MB linear address space
- Internal memory ROM: 128 KB (μPD703034A, 703034AY: mask ROM)
  256 KB (μPD703035A, 703035AY: mask ROM)
  256 KB (μPD70F3035A, 70F3035AY: flash memory)
  RAM: 12 KB (μPD703034A, 703034AY)
  16 KB (μPD703035A, 703035AY, 70F3035A, 70F3035AY)
- Interrupt/exception: μPD703034A, 703035A, 70F3035A (external: 8, internal: 32 sources, exception: 1 source)
  μPD703034AY, 703035AY, 70F3035AY (external: 8, internal: 33 sources, exception: 1 source)
- I/O lines Total: 83
- Timer/counters: 16-bit timer (2 channels: TM0, TM1)
  8-bit timer (6 channels: TM2 to TM7)
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- IEBus controller: 1 channel

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- Serial interface
  - Asynchronous serial interface (UART0, UART1)
  - Clocked serial interface (CSI0 to CSI3)
  - 3-wire variable length serial interface (CSI4)
  - I^2C bus interface (I^2C0, I^2C1) (μPD703034AY, 703035AY, 70F3035AY only)
- 10-bit resolution A/D converter: 12 channels
- DMA controller: 6 channels
- Real-time output port: 8 bits × 1 channel or 4 bits × 2 channels
- ROM correction: 4 places can be corrected
- Power-saving function: HALT/IDLE/STOP modes
- Packages: 100-pin plastic LQFP (fine pitch) (14 × 14)
  100-pin plastic QFP (14 × 20)
- μPD70F3035A, 70F3035AY
  - Can be replaced with μPD703035A and 703035AY (internal mask ROM) in mass production

APPLICATIONS

- AV equipment (audio, car audio, VCR, TV, etc.)

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD703034AGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (128 KB)
μPD703034AYGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (128 KB)
μPD703034AGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (128 KB)
μPD703034AYGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (128 KB)
μPD703035AGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (256 KB)
μPD703035AYGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Mask ROM (256 KB)
μPD703035AGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (256 KB)
μPD703035AYGF-×××-3BA	100-pin plastic QFP (14 × 20)	Mask ROM (256 KB)
μPD70F3035AGC-8EU[Note]	100-pin plastic LQFP (fine pitch) (14 × 14)	Flash memory (256 KB)
μPD70F3035AYGC-8EU[Note]	100-pin plastic LQFP (fine pitch) (14 × 14)	Flash memory (256 KB)
μPD70F3035AGF-3BA[Note]	100-pin plastic QFP (14 × 20)	Flash memory (256 KB)
μPD70F3035AYGF-3BA[Note]	100-pin plastic QFP (14 × 20)	Flash memory (256 KB)

Note Under development

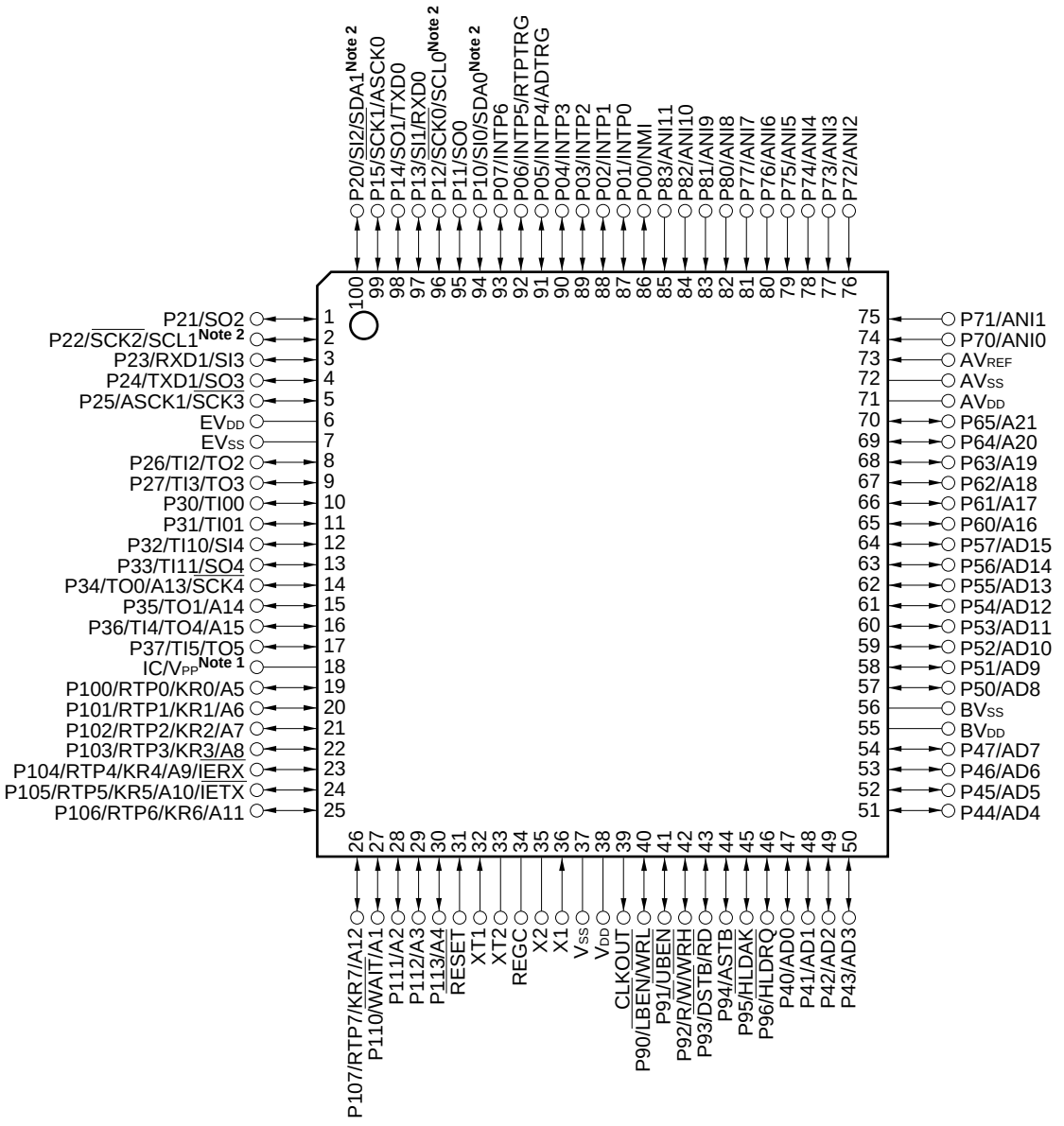
Remarks 1. ××× indicates ROM code suffix.

2. ROMless versions are not provided.

PIN CONFIGURATION (Top View)

100-pin plastic LQFP (fine pitch) (14 × 14)

- μPD703034AGC-×××-8EU
- μPD703034AYGC-×××-8EU
- μPD703035AGC-×××-8EU
- μPD703035AYGC-×××-8EU
- μPD70F3035AGC-8EU
- μPD70F3035AYGC-8EU

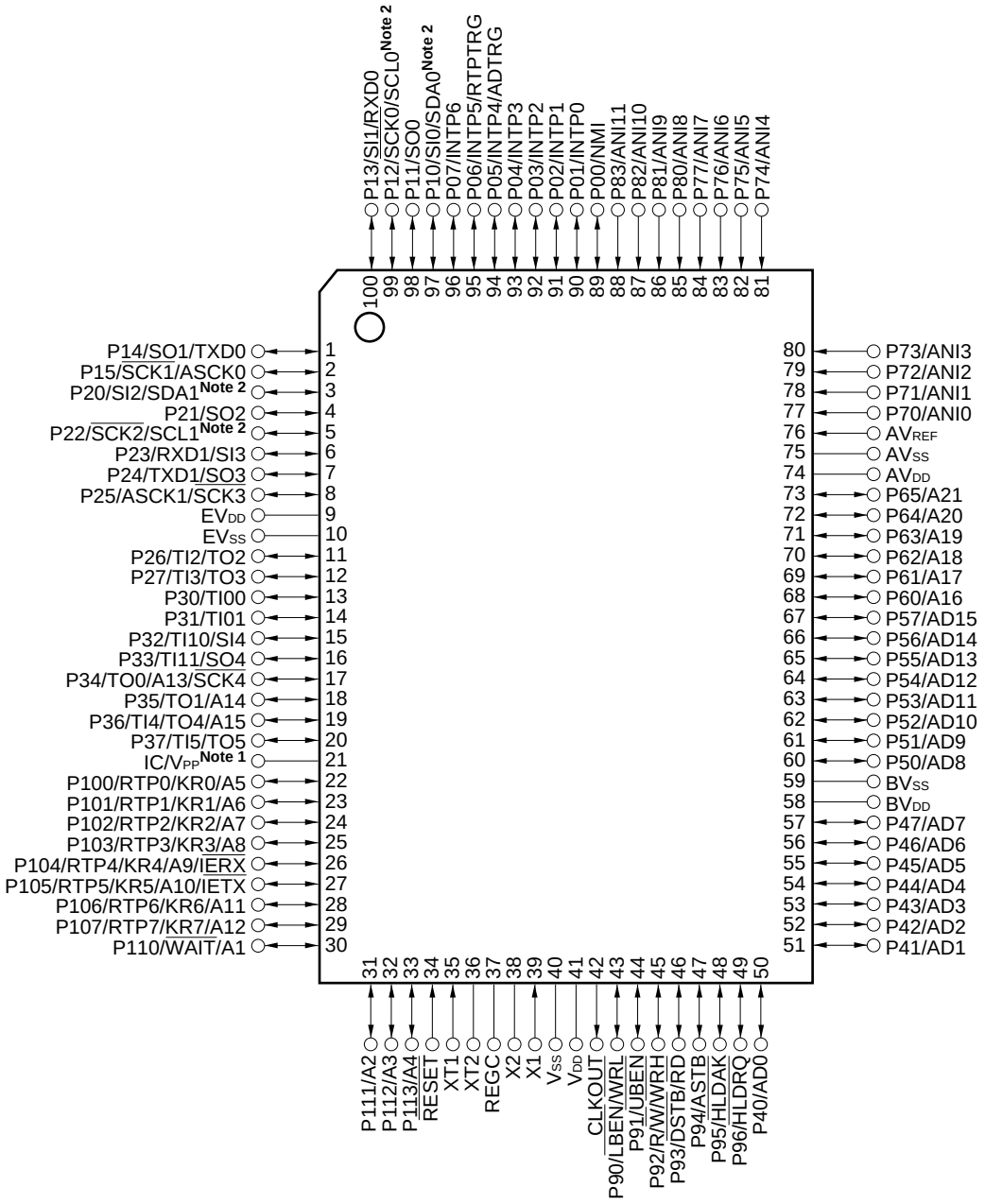


Notes 1. IC: Connect directly to VSS (μPD703034A, 703034AY, 703035A, 703035AY).
VPP: Connect to VSS in normal operation mode (μPD70F3035A, 70F3035AY).

2. SCL0, SCL1, SDA0, and SDA1 are available only in the μPD703034AY, 703035AY, and 70F3035AY.

100-pin plastic QFP (14 × 20)

- μPD703034AGF-×××-3BA
- μPD703034AYGF-×××-3BA
- μPD703035AGF-×××-3BA
- μPD703035AYGF-×××-3BA
- μPD70F3035AGF-3BA
- μPD70F3035AYGF-3BA



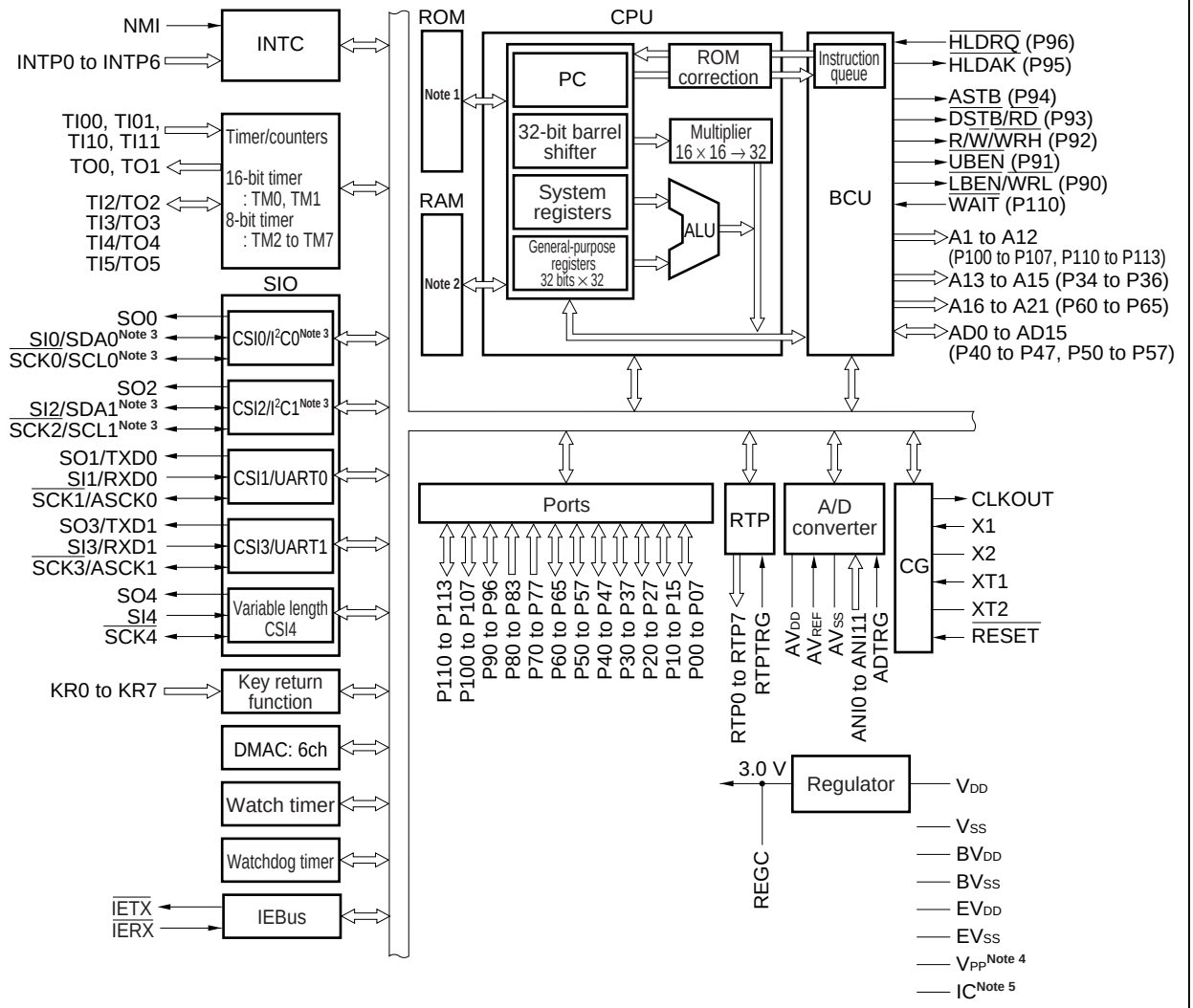
Notes 1. IC: Connect directly to VSS (μPD703034A, 703034AY, 703035A, 703035AY).
VPP: Connect to VSS in normal operation mode (μPD70F3035A, 70F3035AY).

2. SCL0, SCL1, SDA0, and SDA1 are available only in the μPD703034AY, 703035AY, and 70F3035AY.

PIN IDENTIFICATION

A1 to A21:	Address Bus	P70 to P77:	Port 7
AD0 to AD15:	Address/Data Bus	P80 to P83:	Port 8
ADTRG:	AD Trigger Input	P90 to P96:	Port 9
ANI0 to ANI11:	Analog Input	P100 to P107:	Port 10
ASCK0, ASCK1:	Asynchronous Serial Clock	P110 to P113:	Port 11
ASTB:	Address Strobe	$\overline{RD}$:	Read
AV_{DD}:	Analog Power Supply	REGC:	Regulator Clock
AV_{REF}:	Analog Reference Voltage	$\overline{RESET}$:	Reset
AV_{SS}:	Analog Ground	RTP0 to RTP7:	Real-time Output Port
BV_{DD}:	Power Supply for Bus Interface	RTPTRG:	RTP Trigger Input
BV_{SS}:	Ground for Bus Interface	R/$\overline{W}$:	Read/Write Status
CLKOUT:	Clock Output	RXD0, RXD1:	Receive Data
$\overline{DSTB}$:	Data Strobe	$\overline{SCK0}$ to $\overline{SCK4}$:	Serial Clock
EV_{DD}:	Power Supply for Port	SCL0, SCL1:	Serial Clock
EV_{SS}:	Ground for Port	SDA0, SDA1:	Serial Data
$\overline{HLDAK}$:	Hold Acknowledge	SI0 to SI4:	Serial Input
$\overline{HLDRQ}$:	Hold Request	SO0 to SO4:	Serial Output
IC:	Internally Connected	TI00, TI01, TI10, :	Timer Input
$\overline{IERX}$:	IEBus Receive Data	TI11, TI2 to TI5	
$\overline{IETX}$:	IEBus Transmit Data	TO0 to TO5:	Timer Output
INTP0 to INTP6:	Interrupt Request from Peripherals	TXD0, TXD1:	Transmit Data
KR0 to KR7:	Key Return	$\overline{UBEN}$:	Upper Byte Enable
$\overline{LBEN}$:	Lower Byte Enable	V_{DD}:	Power Supply
NMI:	Non-Maskable Interrupt Request	V_{PP}:	Programming Power Supply
P00 to P07:	Port 0	V_{SS}:	Ground
P10 to P15:	Port 1	$\overline{WAIT}$:	Wait
P20 to P27:	Port 2	$\overline{WRH}$:	Write Strobe High Level Data
P30 to P37:	Port 3	$\overline{WRL}$:	Write Strobe Low Level Data
P40 to P47:	Port 4	X1, X2:	Crystal for Main Clock
P50 to P57:	Port 5	XT1, XT2:	Crystal for Sub-clock
P60 to P65:	Port 6		

INTERNAL BLOCK DIAGRAM



Notes 1. μPD703034A, 703034AY: 128 KB (mask ROM)
μPD703035A, 703035AY: 256 KB (mask ROM)
μPD70F3035A, 70F3035AY: 256 KB (flash memory)

2. μPD703034A, 703034AY: 12 KB
μPD703035A, 703035AY, 70F3035A, 70F3035AY: 16 KB

3. I^2C bus interface and SDAn and SCLn pins are available only in the μPD703034AY, 703035AY, and 70F3035AY.

4. μPD70F3035A, 70F3035AY

5. μPD703034A, 703034AY, 703035A, 703035AY

CONTENTS

1. DIFFERENCES AMONG PRODUCTS

1.1 Differences of μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, and 70F3035AY

Item \ Part Number	μPD703034A	μPD703034AY	μPD703035A	μPD703035AY	μPD70F3035A	μPD70F3035AY
Internal ROM	128 KB (mask ROM)		256 KB (mask ROM)		256 KB (flash memory)	
Flash memory programming pin	None				Provided (V_{PP})	
Flash memory programming mode	None				Provided (V_{PP} = 7.8 V)	
I^2C bus interface pins (SCL0, SCL1, SDA0, SDA1)	None	Provided	None	Provided	None	Provided
Electrical specifications	Current consumption, etc. differs.					
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.					

Cautions 1. There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. When replacing the flash memory versions with mask ROM versions, write the same code in the empty area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	SI0/SDA0
P11				SO0
P12				$\overline{\text{SCK0}}$/SCL0
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	SI2/SDA1
P21				SO2
P22				$\overline{\text{SCK2}}$/SCL1
P23				SI3/RXD1
P24				SO3/TXD1
P25				$\overline{\text{SCK3}}$/ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TI00
P31				TI01
P32				TI10/SI4
P33				TI11/SO4
P34				TO0/A13/$\overline{\text{SCK4}}$
P35				TO1/A14
P36				TI4/TO4/A15
P37				TI5/TO5
P40 to P47	I/O	No	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	No	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8 to AD15

Remark PULL: On-chip pull-up resistor

(2/2)

Pin Name	I/O	PULL	Function	Alternate Function
P60 to P65	I/O	No	Port 6 6-bit I/O port Input/output can be specified in 1-bit units.	A16 to A21
P70 to P77	Input	No	Port 7 8-bit input port	ANI0 to ANI7
P80 to P83	Input	No	Port 8 4-bit input port	ANI8 to ANI11
P90	I/O	No	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}/\overline{\text{WRL}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93				$\overline{\text{DSTB}}/\overline{\text{RD}}$
P94				ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$
P100	I/O	Yes	Port 10 8-bit I/O port Input/output can be specified in 1-bit units.	RTP0/A5/KR0
P101				RTP1/A6/KR1
P102				RTP2/A7/KR2
P103				RTP3/A8/KR3
P104				RTP4/A9/KR4/$\overline{\text{IERX}}$
P105				RTP5/A10/KR5/$\overline{\text{IETX}}$
P106				RTP6/A11/KR6
P107				RTP7/A12/KR7
P110	I/O	Yes	Port 11 4-bit I/O port Input/output can be specified in 1-bit units.	A1/$\overline{\text{WAIT}}$
P111				A2
P112				A3
P113				A4

Remark PULL: On-chip pull-up resistor

2.2 Non-Port Pins

(1/4)

Pin Name	I/O	PULL	Function	Alternate Function
A1	Output	Yes	Low-order address bus used for external memory expansion	P110/$\overline{\text{WAIT}}$
A2				P111
A3				P112
A4				P113
A5				P100/RTP0/KR0
A6				P101/RTP1/KR1
A7				P102/RTP2/KR2
A8				P103/RTP3/KR3
A9				P104/RTP4/KR4/$\overline{\text{IERX}}$
A10				P105/RTP5/KR5/$\overline{\text{IETX}}$
A11				P106/RTP6/KR6
A12				P107/RTP7/KR7
A13				P34/TO0/$\overline{\text{SCK4}}$
A14				P35/TO1
A15				P36/TO4/TI4
A16 to A21	Output	No	High-order address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11				P80 to P83
ASCK0	Input	Yes	Baud rate clock input for UART0	P15/$\overline{\text{SCK1}}$
ASCK1			Baud rate clock input for UART1	P25/$\overline{\text{SCK3}}$
ASTB	Output	No	External address strobe output	P94
AV_{DD}	–	–	Positive power supply for A/D converter and alternate port	–
AV_{REF}	Input	–	Reference voltage input for A/D converter	–
AV_{SS}	–	–	Ground potential for A/D converter and alternate port	–
BV_{DD}	–	–	Positive power supply for bus interface and alternate port	–
BV_{SS}	–	–	Ground potential for bus interface and alternate port	–
CLKOUT	Output	–	Internal system clock output	–
$\overline{\text{DSTB}}$	Output	No	External data strobe output	P93/$\overline{\text{RD}}$
EV_{DD}	–	–	Positive power supply for I/O ports and alternate-function pins (except bus interface alternate port)	–
EV_{SS}	–	–	Ground potential for I/O ports and alternate-function pins (except bus interface alternate port)	–
$\overline{\text{HLDAK}}$	Output	No	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	No	Bus hold request input	P96
IC	–	–	Internally connected (μPD703034A, 703034AY, 703035A, 703035AY only)	–

Remark PULL: On-chip pull-up resistor

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Pin Name	I/O	PULL	Function	Alternate Function
$\overline{\text{IERX}}$	Input	Yes	IEBus data input	P104/RTP4/A9/KR4
$\overline{\text{IETX}}$	Output		IEBus data output	P105/RTP5/A10/KR5
INTP0	Input	Yes	External interrupt request input (analog noise elimination)	P01
INTP1				P02
INTP2				P03
INTP3				P04
INTP4	Input	Yes	External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG
INTP6	Input	Yes	External interrupt request input (digital noise elimination supporting remote controller)	P07
KR0	Input	Yes	Key return input	P100/RTP0/A5
KR1				P101/RTP1/A6
KR2				P102/RTP2/A7
KR3				P103/RTP3/A8
KR4				P104/RTP4/A9/$\overline{\text{IERX}}$
KR5				P105/RTP5/A10/$\overline{\text{IETX}}$
KR6				P106/RTP6/A11
KR7				P107/RTP7/A12
$\overline{\text{LBEN}}$	Output	No	External data bus's low-order byte enable output	P90/$\overline{\text{WRL}}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
$\overline{\text{RD}}$	Output	No	Read strobe output	P93/$\overline{\text{DSTB}}$
REGC	–	–	Regulator output stabilization capacitance connection	–
$\overline{\text{RESET}}$	Input	–	System reset input	–
RTP0	Output	Yes	Real-time output port	P100/KR0/A5
RTP1				P101/KR1/A6
RTP2				P102/KR2/A7
RTP3				P103/KR3/A8
RTP4				P104/KR4/A9/$\overline{\text{IERX}}$
RTP5				P105/KR5/A10/$\overline{\text{IETX}}$
RTP6				P106/KR6/A11
RTP7				P107/KR7/A12
RTPTRG	Input	Yes	Real-time output port external trigger input	P06/INTP5
R/$\overline{\text{W}}$	Output	No	External read/write status output	P92/$\overline{\text{WRH}}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23/SI3

Remark PULL: On-chip pull-up resistor

(3/4)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{SCK0}$	I/O	Yes	Serial clock I/O (3-wire type) for CSI0 to CSI3	P12/SCL0
$\overline{SCK1}$				P15/ASCK0
$\overline{SCK2}$				P22/SCL1
$\overline{SCK3}$				P25/ASCK1
$\overline{SCK4}$	I/O	Yes	Serial clock I/O (3-wire type) for variable length CSI4	P34/TO0/A13
SCL0	I/O	Yes	Serial clock I/O for I^2C0 and I^2C1 (μPD703034AY, 703035AY, 70F3035AY only)	P12/$\overline{SCK0}$
SCL1				P22/$\overline{SCK2}$
SDA0	I/O	Yes	Serial transmit/receive data I/O for I^2C0 and I^2C1 (μPD703034AY, 703035AY, 70F3035AY only)	P10/SI0
SDA1				P20/SI2
SI0	Input	Yes	Serial receive data input (3-wire type) for CSI0 to CSI3	P10/SDA0
SI1				P13/RXD0
SI2				P20/SDA1
SI3				P23/RXD1
SI4	Input	Yes	Serial receive data input (3-wire type) for variable length CSI4	P32/TI10
SO0	Output	Yes	Serial transmit data output (3-wire type) for CSI0 to CSI3	P11
SO1				P14/TXD0
SO2				P21
SO3				P24/TXD1
SO4	Output	Yes	Serial transmit data output (3-wire type) for variable length CSI4	P33/TI11
TI00	Input	Yes	External count clock input for TM0/external capture trigger input for TM0	P30
TI01			External capture trigger input for TM0	P31
TI10			External count clock input for TM1/external capture trigger input for TM1	P32/SI4
TI11			External capture trigger input for TM1	P33/SO4
TI2	Input	Yes	External count clock input for TM2 to TM5	P26/TO2
TI3				P27/TO3
TI4				P36/TO4/A15
TI5				P37/TO5
TO0	Output	Yes	Pulse signal output for TM0 and TM1	P34/A13/$\overline{SCK4}$
TO1				P35/A14
TO2	Output	Yes	Pulse signal output for TM2 to TM5	P26/TI2
TO3				P27/TI3
TO4				P36/TI4/A15
TO5				P37/TI5
TXD0	Output	Yes	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24/SO3
$\overline{UBEN}$	Output	No	High-order byte enable output for external data bus	P91
V_{DD}	–	–	Positive power supply pin	–

Remark PULL: On-chip pull-up resistor

(4/4)

Pin Name	I/O	PULL	Function	Alternate Function
V_{PP}	–	–	High voltage apply pin for program write/verify (μPD70F3035A, 70F3035AY only)	–
V_{SS}	–	–	Ground potential	–
$\overline{WAIT}$	Input	Yes	Control signal input for inserting wait in bus cycle	P110/A1
$\overline{WRH}$	Output	No	High-order byte write strobe signal output for external data bus	P92/R/$\overline{W}$
$\overline{WRL}$	Output	No	Low-order byte write strobe signal output for external data bus	P90/$\overline{LBEN}$
X1	Input	No	Resonator connection for main clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	–
XT2	–			–

Remark PULL: On-chip pull-up resistor

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are show in Table 2-1. For the input/output schematic circuit diagram of each type, refer to Figure 2-1.

Table 2-1. Types of Pin I/O Circuits (1/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P00	NMI	8-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P01	INTP0			
P02	INTP1			
P03	INTP2			
P04	INTP3			
P05	INTP4/ADTRG			
P06	INTP5/RTPTRG			
P07	INTP6			
P10	SI0/SDA0	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P11	SO0	26		
P12	$\overline{SCK0}$/SCL0	10-A		
P13	SI1/RXD0	8-A		
P14	SO0/TXD0	26		
P15	$\overline{SCK1}$/ASCK0	10-A		
P20	SI2/SDA1	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P21	SO2	26		
P22	$\overline{SCK2}$/SCL1	10-A		
P23	SI3/RXD1			
P24	SO3/TXD1	26		
P25	$\overline{SCK3}$/ASCK1	10-A		
P26	TI2/TO2	8-A		
P27	TI3/TO3			
P30	TI00	8-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P31	TI01			
P32	TI10/SI4			
P33	TI11/SO4			
P34	TO0/A13/$\overline{SCK4}$			
P35	TO1/A14	5-A		
P36	TI4/TO4/A15	8-A		
P37	TI5/TO5			
P40 to P47	AD0 to AD7	5	BV_{DD}	Input state: Independently connect to BV_{DD} or BV_{SS} via a resistor. Output state: Leave open.
P50 to P57	AD8 to AD15	5	BV_{DD}	
P60 to P65	A16 to A21	5	BV_{DD}	

Table 2-1. Types of Pin I/O Circuits (2/2)

Pin	Alternate Function	I/O Circuit Type	I/O Buffer Power Supply	Recommended Connection of Unused Pins
P70 to P77	ANI0 to ANI7	9	AV_{DD}	Independently connect to AV_{DD} or AV_{SS} via a resistor.
P80 to P83	ANI8 to ANI11	9	AV_{DD}	
P90	$\overline{LBEN}/\overline{WRL}$	5	BV_{DD}	Input state: Independently connect to BV_{DD} or BV_{SS} via a resistor. Output state: Leave open.
P91	$\overline{UBEN}$			
P92	$R/\overline{W}/\overline{WRH}$			
P93	$\overline{DSTB}/\overline{RD}$			
P94	ASTB			
P95	$\overline{HLDAK}$	26		
P96	$\overline{HLDRQ}$			
P100	RTP0/A5/KR0	10-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P101	RTP1/A6/KR1			
P102	RTP2/A7/KR2			
P103	RTP3/A8/KR3			
P104	RTP4/A9/KR4/$\overline{IERX}$			
P105	RTP5/A10/KR5/$\overline{IETX}$			
P106	RTP6/A11/KR6			
P107	RTP7/A12/KR7			
P110	A1/$\overline{WAIT}$	5-A	EV_{DD}	Input state: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output state: Leave open.
P111	A2			
P112	A3			
P113	A4			
CLKOUT	–	4	BV_{DD}	Leave open.
$\overline{RESET}$	–	2	EV_{DD}	–
XT1	–	16	–	Connect to V_{SS} via a resistor.
XT2	–	16	–	Leave open.
AV_{REF}	–	–	–	Connect to AV_{SS} via a resistor.
IC[Note 1]	–	–	–	Connect directly to V_{SS}.
V_{PP}[Note 2]	–	–	–	Connect to V_{SS}.

Notes 1. μPD703034A, 703034AY, 703035A, 703035AY

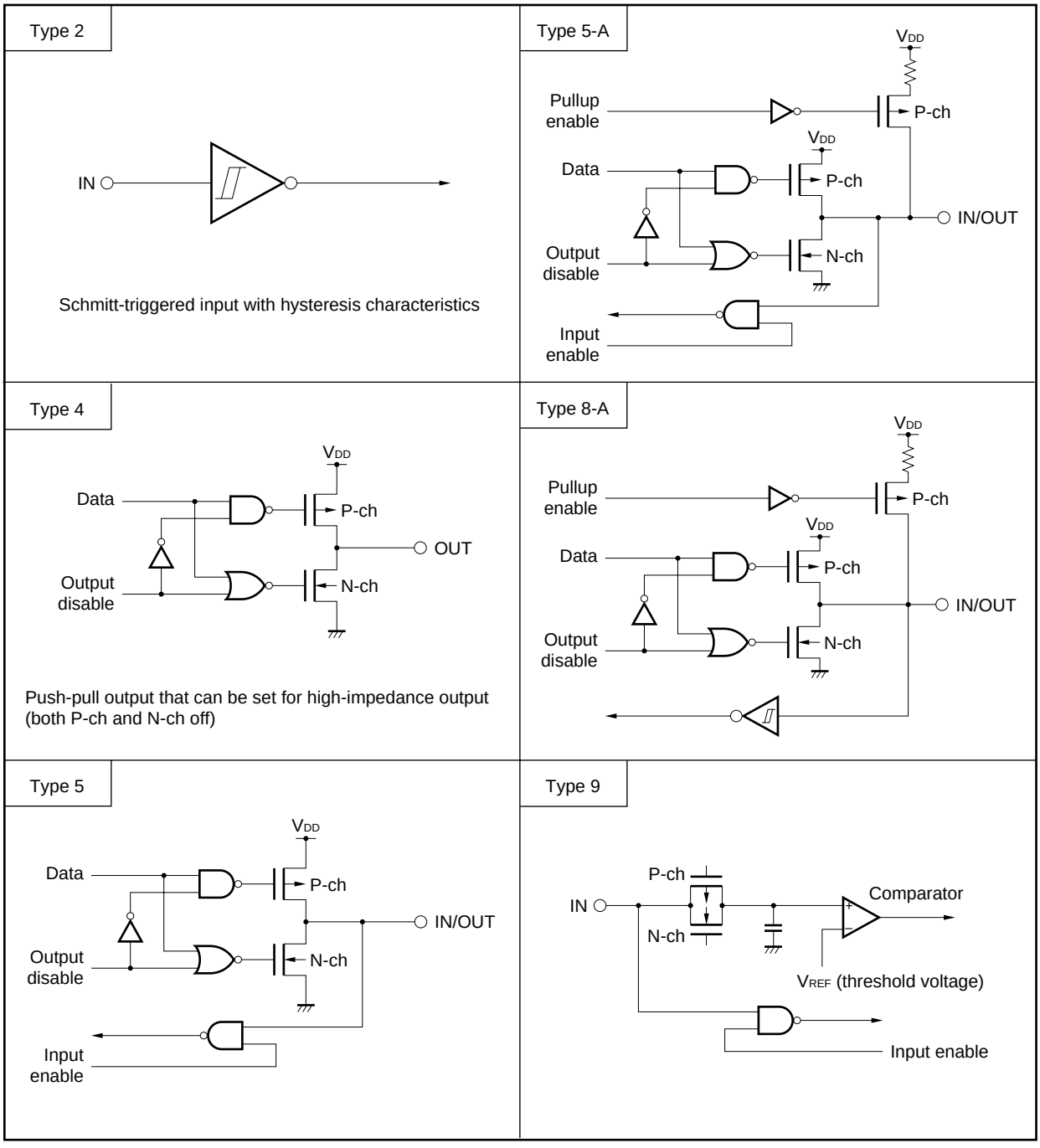
2. μPD70F3035A, 70F3035AY

Caution Three power supply systems are available to supply power to the I/O buffers of the V850/SB2's pins: EV_{DD}, BV_{DD}, and AV_{DD}. The voltage ranges that can be used for these I/O buffer power supplies are shown below.

EV_{DD}, BV_{DD}: 3.0 V to 5.5 V
AV_{DD}: 4.5 V to 5.5 V

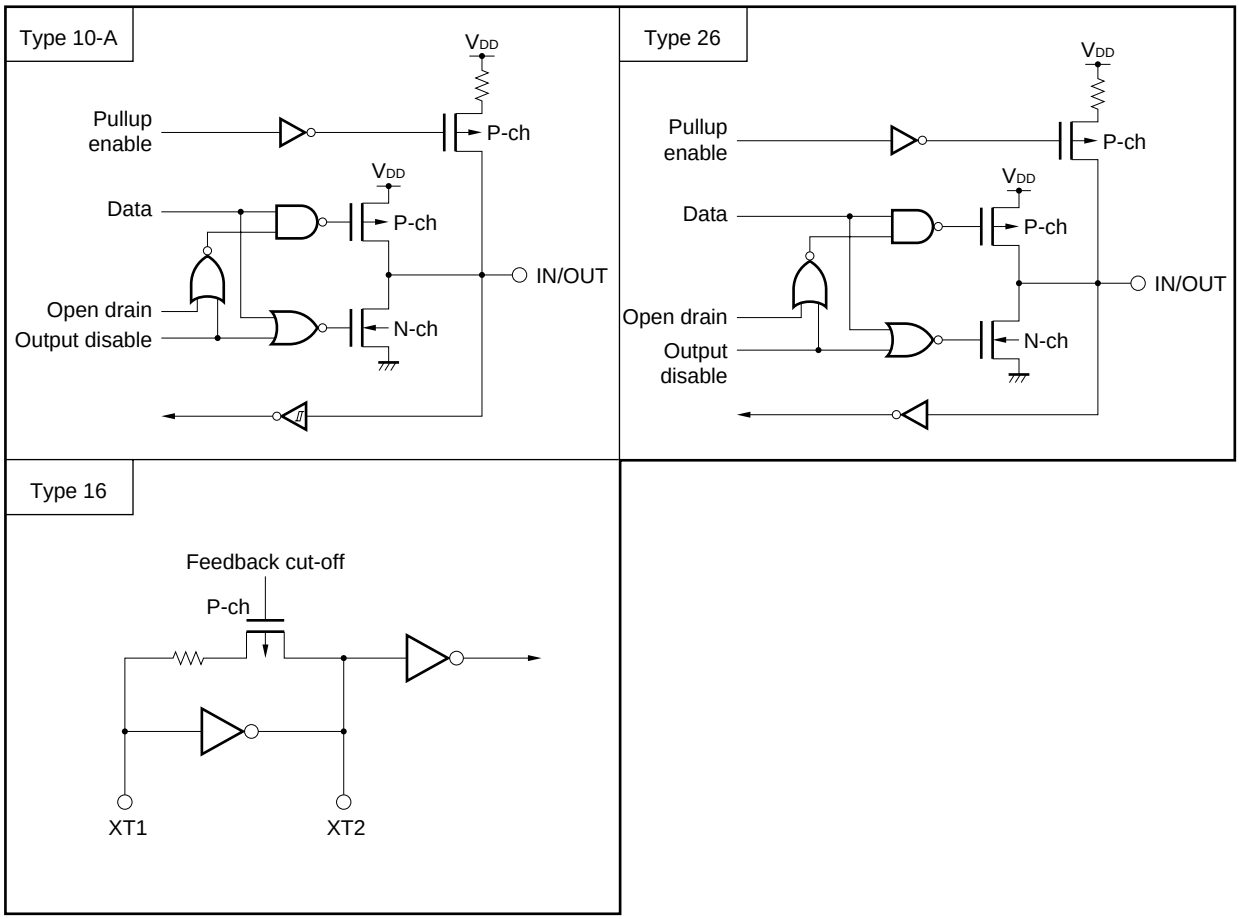
The electrical specifications differ depending on whether the power supply voltage range is 3.0 V to under 4.0 V, or 4.0 V to 5.5 V.

Figure 2-1. Pin Input/Output Circuits (1/2)



Caution V_{DD} in the circuit diagrams can be read as EV_{DD}, BV_{DD}, or AV_{DD}, as appropriate.

Figure 2-1. Pin Input/Output Circuits (2/2)



Caution V_{DD} in the circuit diagrams can be read as EV_{DD}, BV_{DD}, or AV_{DD}, as appropriate.

3. PROGRAMMING FLASH MEMORY (μPD70F3035A, 70F3035AY ONLY)

There are the following two methods for writing a program to the flash memory.

(1) On-board programming

Write a program to the flash memory using a dedicated flash programmer after the μPD70F3035A and 70F3035AY have been mounted on the target board. Also mount a connector, etc. on the target board to communicate with the dedicated flash programmer.

(2) Off-board programming

Write a program using a dedicated adapter before the μPD70F3035A and 70F3035AY have been mounted on the target board.

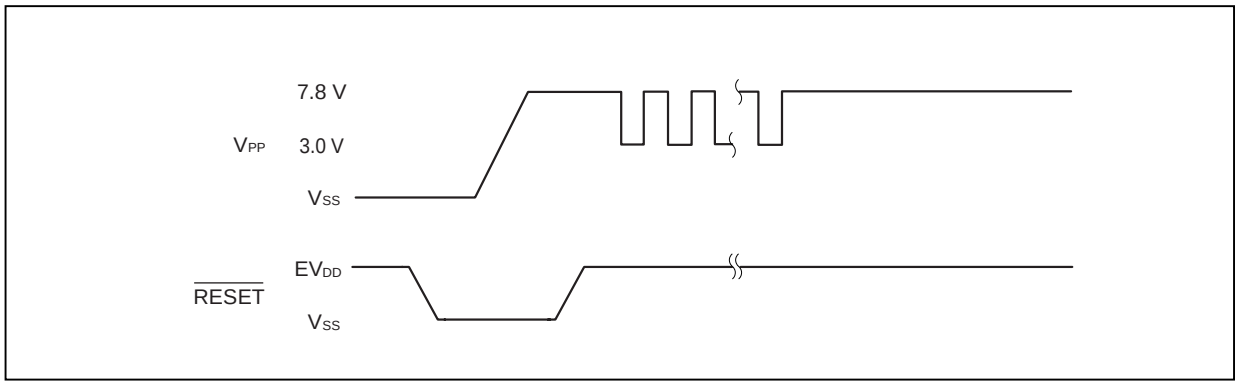
3.1 Selecting Communication Mode

To write the flash memory, use a dedicated flash programmer and serial communication. Select a serial communication mode from those listed in Table 3-1 in the format shown in Figure 3-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 3-1.

Table 3-1. Communication Modes

Communication Mode	Pins Used	Number of V_{PP} Pulses
CSI0	SO0 (serial data output) SI0 (serial data input) $\overline{SCK0}$ (serial clock input)	0
CSI0 + HS	SO0 (serial data output) SI0 (serial data input) $\overline{SCK0}$ (serial clock input) P15 (3-wire + handshake signal output of handshake communication)	3
UART0	TXD0 (serial data output) RXD0 (serial data input)	8

Figure 3-1. Communication Mode Selecting Format



3.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. The major functions are shown below.

Table 3-2. Major Functions of Flash Memory Programming

Function		Description
Category	Command	
Verify	Batch verify	Compares the contents of the entire memory and the input data.
Erase	Batch erase	Erases the contents of the entire memory.
	Write back	Writes back the contents which is overerased.
Blank check	Batch blank check	Checks the erase state of the entire memory.
Data write	High-speed write	Writes data by the specification of the write start address and the number of bytes to be written, and executes verify check.
	Continuous write	Writes data from the address following the high-speed write command executed immediately before, and executes verify check.
System setting/control	Status read out	Reads out the status of operations.
	Oscillation frequency setting	Sets the oscillation frequency.
	Erase time setting	Sets the erase time of batch erase.
	Write time setting	Sets the write time of data write.
	Write back time setting	Sets the write back time.
	Baud rate setting	Sets the baud rate when using UART0.
	Silicon signature	Reads out the silicon signature information.
	Reset	Restarts the system of flash programmer.

3.3 Connecting Dedicated Flash Programmer

The connection of the dedicated flash programmer and the μPD70F3035A and 70F3035AY differs according to the communication mode. The connections for each communication mode are shown below.

Figure 3-2. Connection of Dedicated Flash Programmer in CSI0 Mode

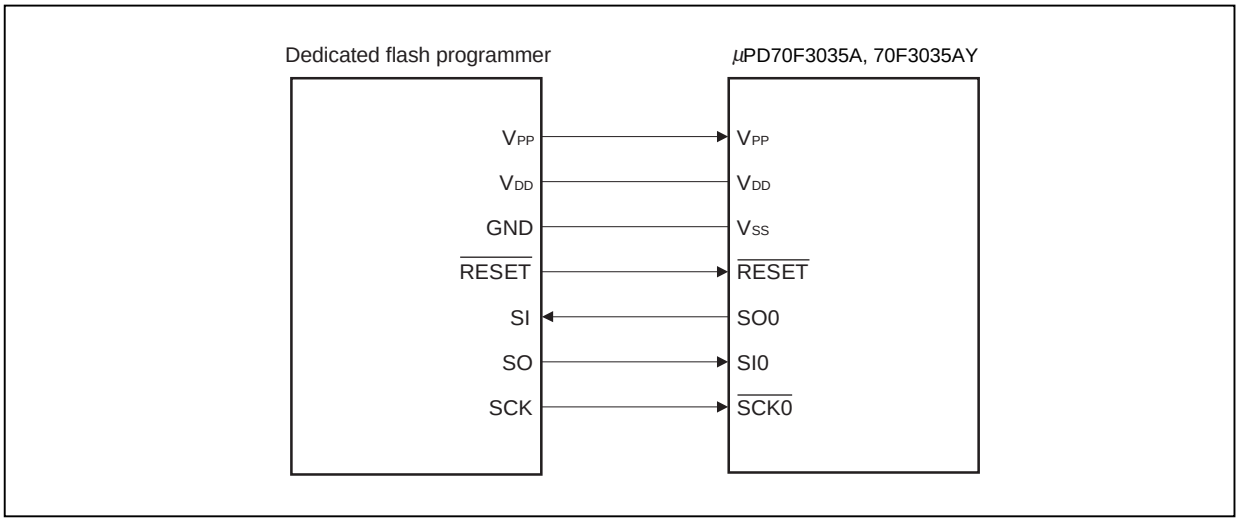


Figure 3-3. Connection of Dedicated Flash Programmer in CSI0 + HS Mode

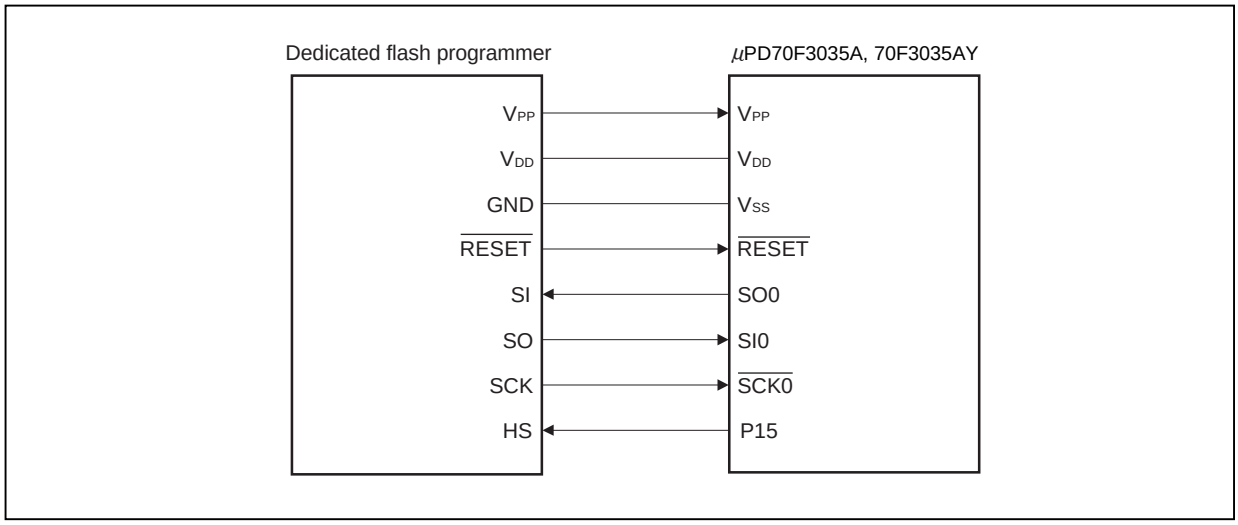
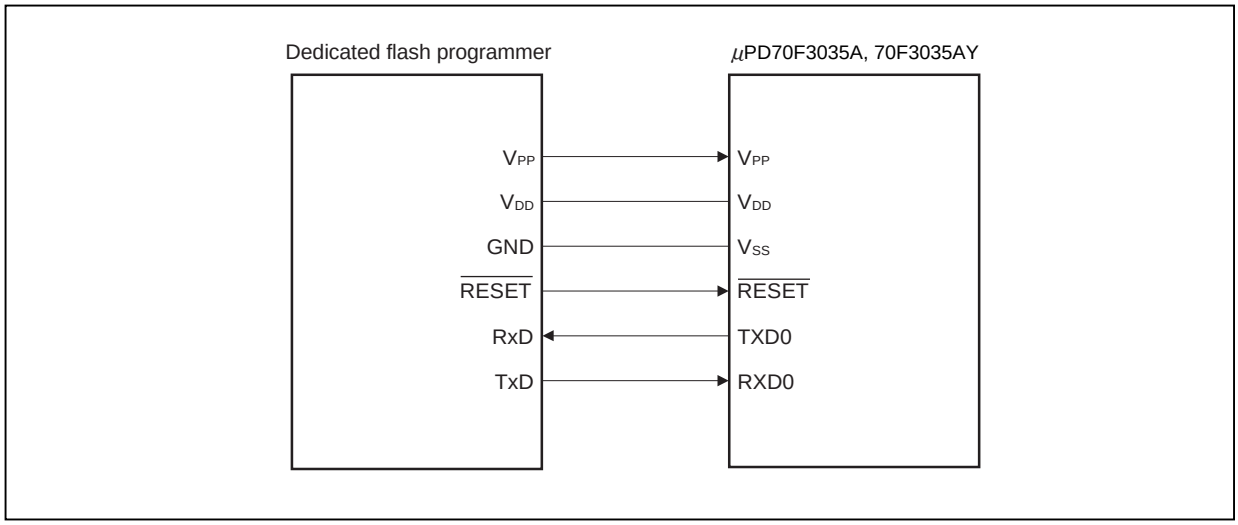


Figure 3-4. Connection of Dedicated Flash Programmer in UART0 Mode



4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
	AV_{DD}	AV_{DD} pin	–0.5 to +7.0	V
	BV_{DD}	BV_{DD} pin	–0.5 to +7.0	V
	EV_{DD}	EV_{DD} pin	–0.5 to +7.0	V
	AV_{SS}	AV_{SS} pin	–0.5 to +0.5	V
	BV_{SS}	BV_{SS} pin	–0.5 to +0.5	V
	EV_{SS}	EV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1** (BV_{DD} pin)	–0.5 to BV_{DD} + 0.5[Note 4]	V
	V_{I2}	**Note 2** (EV_{DD} pin)	–0.5 to EV_{DD} + 0.5[Note 4]	V
	V_{I3}	V_{PP} pin (μPD70F3035A, 70F3035AY only)	–0.5 to +8.5	V
Analog input voltage	V_{IAN}	**Note 3** (AV_{DD} pin)	–0.5 to AV_{DD} + 0.5[Note 4]	V
Analog reference input voltage	AV_{REF}	AV_{REF} pin	–0.5 to AV_{DD} + 0.5[Note 4]	V
Output current, low	I_{OL}	Per pin	4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	25	mA
		Total for P40 to P47, P90 to P96, CLKOUT	25	mA
		Total for P50 to P57, P60 to P65	25	mA
Output current, high	I_{OH}	Per pin	–4.0	mA
		Total for P00 to P07, P10 to P15, P20 to P25	–25	mA
		Total for P26, P27, P30 to P37, P100 to P107, P110 to P113	–25	mA
		Total for P40 to P47, P90 to P96, CLKOUT	–25	mA
		Total for P50 to P57, P60 to P65	–25	mA
Output voltage	V_{O1}	**Note 1** (BV_{DD} pin)	–0.5 to BV_{DD} + 0.5[Note 4]	V
	V_{O2}	**Note 2** (EV_{DD} pin)	–0.5 to EV_{DD} + 0.5[Note 4]	V
Operating ambient temperature	T_A	Normal operation mode	–40 to +85	°C
		Flash memory programming mode (μPD70F3035A, 70F3035AY only)	10 to 85	°C
Storage temperature	T_{stg}	μPD703034A, 703034AY	–65 to +150	°C
		μPD703035A, 703035AY		
		μPD70F3035A, 70F3035AY	–40 to +125	°C

Notes 1. Ports 4, 5, 6, 9, CLKOUT, and their alternate-function pins

2. Ports 0, 1, 2, 3, 10, 11, $\overline{\text{RESET}}$, and their alternate-function pins

3. Ports 7, 8, and their alternate-function pins

4. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Capacitance (T_A = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

(1) Operating frequency

Operating Frequency (f_{XX})		V_{DD}	AV_{DD}	BV_{DD}	EV_{DD}	Remark
2 to 13 MHz		4.0 to 5.5 V	4.5 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	**Note 1**
32.768 kHz	Other than IDLE mode	4.0 to 5.5 V	4.5 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	–
	IDLE mode	3.5 to 5.5 V	4.5 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	**Note 2**

Notes 1. During STOP mode (subsystem oscillator operating), V_{DD} = 3.5 to 5.5 V. Shifting to STOP mode or restoring from STOP mode must be performed at V_{DD} = 4.0 V min.

2. Shifting to IDLE mode or restoring from IDLE mode must be performed at V_{DD} = 4.0 V min.

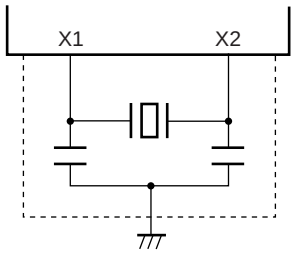
(2) CPU operating frequency

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU operating frequency	f_{CPU}	Main system clock operation	0.25		13	MHz
		Subsystem clock operation		32.768		kHz

Recommended Oscillator

(1) Main system clock oscillator (T_A = –40 to +85°C)

(a) Connection of ceramic resonator or crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XX}		2		13	MHz
Oscillation stabilization time	–	Upon reset release		$2^{19}/f_{XX}$		s
	–	Upon STOP mode release		**Note**		s

Note The TYP. value differs depending on the setting of the oscillation stabilization time select register (OSTS).

Cautions 1. Main system clock oscillator operates on the output voltage of the on-chip regulator. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

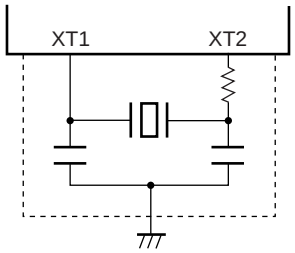
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Ensure that the duty of oscillation waveform is between 5.5 and 4.5.

4. Sufficiently evaluate the matching between the μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, 70F3035AY and the resonator.

(2) Subsystem clock oscillator (T_A = –40 to +85°C)

(a) Connection of crystal resonator



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{XT}		32	32.768	35	kHz
Oscillation stabilization time	–			10		s

Cautions 1. Subsystem clock oscillator operates on the output voltage of the on-chip regulator. External clock input is prohibited.

2. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

3. Sufficiently evaluate the matching between the μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, 70F3035AY and the resonator.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**	4.0 V ≤ BV_{DD} ≤ 5.5 V	0.7BV_{DD}		BV_{DD}	V
			3.0 V ≤ BV_{DD} < 4.0 V	0.8BV_{DD}		BV_{DD}	V
	V_{IH2}	**Note 2**	4.0 V ≤ EV_{DD} ≤ 5.5 V	0.7EV_{DD}		EV_{DD}	V
			3.0 V ≤ EV_{DD} < 4.0 V	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	**Note 3**	4.0 V ≤ EV_{DD} ≤ 5.5 V	0.7EV_{DD}		EV_{DD}	V
			3.0 V ≤ EV_{DD} < 4.0 V	0.8EV_{DD}		EV_{DD}	V
	V_{IH4}	**Note 4**	4.5 V ≤ AV_{DD} ≤ 5.5 V	0.7AV_{DD}		AV_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**		BV_{SS}		0.3BV_{DD}	V
	V_{IL2}	**Note 2**		EV_{SS}		0.3EV_{DD}	V
	V_{IL3}	**Note 3**		EV_{SS}		0.3EV_{DD}	V
	V_{IL4}	**Note 4**		AV_{SS}		0.3AV_{DD}	V
Output voltage, high	V_{OH1}	**Note 1**	3.0 V ≤ BV_{DD} ≤ 5.5 V, I_{OH} = –100 μA	BV_{DD}–0.5			V
			4.0 V ≤ BV_{DD} ≤ 5.5 V, I_{OH} = –3 mA	BV_{DD}–1.0			V
	V_{OH2}	**Notes 2, 3** (except $\overline{\text{RESET}}$)	3.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = –100 μA	EV_{DD}–0.5			V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = –3 mA	EV_{DD}–1.0			V
Output voltage, low	V_{OL}	I_{OL} = 3 mA, 3.0 V ≤ BV_{DD}, EV_{DD} ≤ 5.5 V				0.5	V
		I_{OL} = 3 mA, 4.0 V ≤ BV_{DD}, EV_{DD} ≤ 5.5 V				0.4	V
Input leakage current, high	I_{LIH}	V_I = V_{DD} = BV_{DD} = EV_{DD} = AV_{DD}				5	μA
Input leakage current, low	I_{LIL}	V_I = 0 V				–5	μA
Output leakage current, high	I_{LOH}					5	μA
Output leakage current, low	I_{LOL}					–5	μA

Notes 1. Ports 4, 5, 6, 9, CLKOUT, and their alternate-function pins

2. P11, P14, P21, P24, P34, P35, P110 to P113, and their alternate-function pins

3. P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, P100 to P107, $\overline{\text{RESET}}$, and their alternate-function pins

4. Ports 7, 8, and their alternate-function pins

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current	μPD703034A, μPD703034AY, μPD703035A, μPD703035AY	I_{DD1}	In normal operation mode[Note 1]			15	25	mA
		I_{DD2}	In HALT mode[Note 1]			6	13	mA
		I_{DD3}	In IDLE mode[Note 2]	Watch timer operating		1	4	mA
		I_{DD4}	In STOP mode	Watch timer, subsystem oscillator operating		13	70	μA
				Subsystem oscillator stopped, XT1 = V_{SS}		8	70	μA
		I_{DD5}	In normal operation mode (subsystem operation)[Note 3]			50	150	μA
		I_{DD6}	In IDLE mode (subsystem operation)[Note 3]			13	70	μA
	μPD70F3035A, μPD70F3035AY	I_{DD1}	In normal operation mode[Note 1]			25	48	mA
		I_{DD2}	In HALT mode[Note 1]			7	15	mA
		I_{DD3}	In IDLE mode[Note 2]	Watch timer operating		1	4	mA
		I_{DD4}	In STOP mode	Watch timer, subsystem oscillator operating		13	100	μA
				Subsystem oscillator stopped, XT1 = V_{SS}		8	100	μA
		I_{DD5}	In normal operation mode (subsystem operation)[Note 3]			200	600	μA
		I_{DD6}	In IDLE mode (subsystem operation)[Note 3]			90	180	μA
Pull-up resistance		R_L	V_{IN} = 0 V		10	30	100	kΩ

Notes 1. f_{CPU} = f_{XX} = 13 MHz, all peripheral functions operating, output buffer: OFF

2. f_{XX} = 13 MHz

3. f_{CPU} = f_{XT} = 32.768 kHz, main system clock oscillator stopped

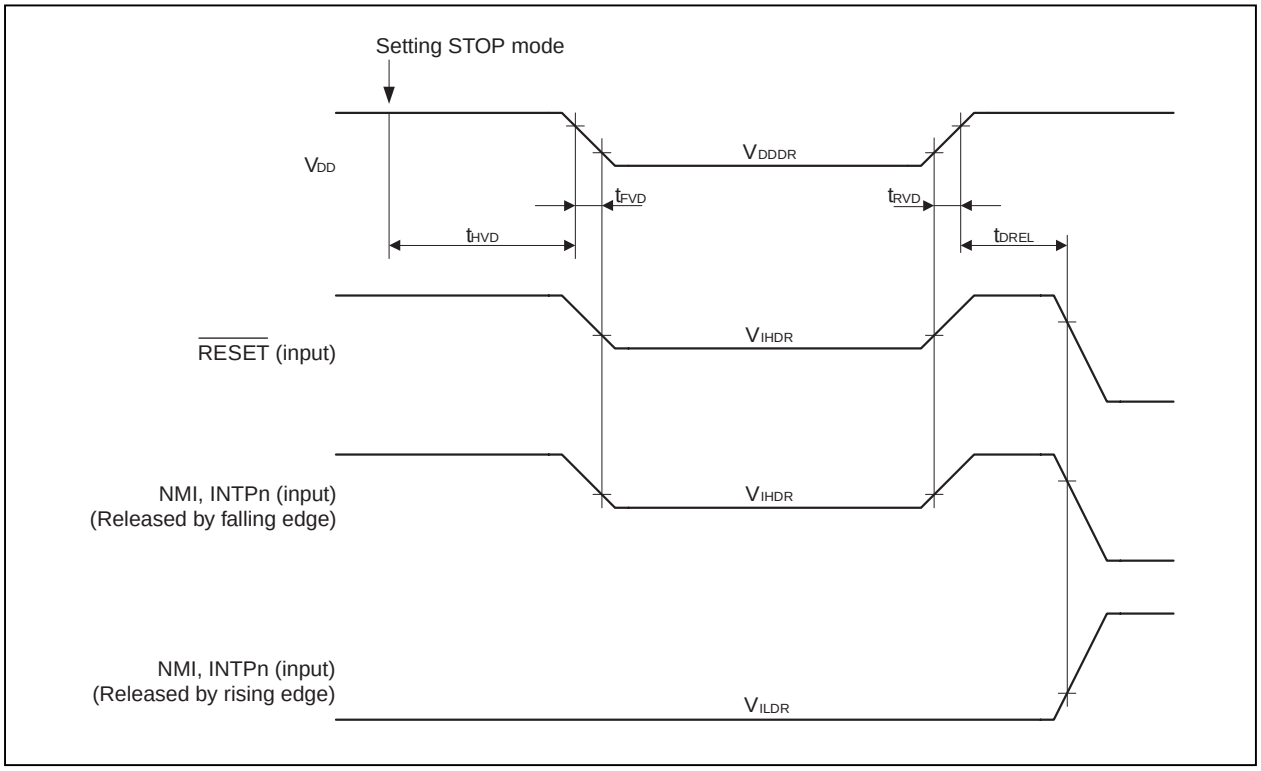
Remark TYP. values are reference values for when T_A = 25°C, V_{DD} = BV_{DD} = EV_{DD} = AV_{DD} = 5.0 V. The current consumed by the output buffer is not included.

Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode (all functions not operating)		3.0[Note]		5.5	V
Data retention current	I_{DDDR}	$V_{DD} = V_{DDDR}$, XT1 = V_{SS} (subsystem stopped)	μPD703034A, μPD703034AY, μPD703035A, μPD703035AY		8	70	μA
			μPD70F3035A, μPD70F3035AY		8	100	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}			0			ms
STOP release signal input time	t_{DREL}			0			ms
Data retention high-level input voltage	V_{IHDR}	All input ports		0.9V_{DDDR}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input ports		0		0.1V_{DDDR}	V

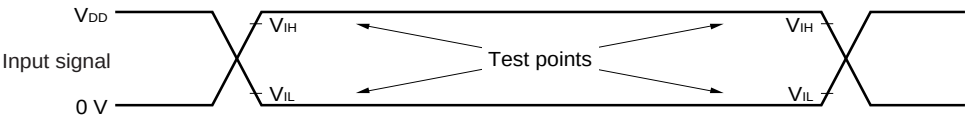
Note During STOP mode (subsystem oscillator operating), V_{DD} = 3.5 to 5.5 V. Shifting to STOP mode or restoring from STOP mode must be performed at V_{DD} = 4.0 V min.

Remark TYP. values are reference values for when T_A = 25°C.

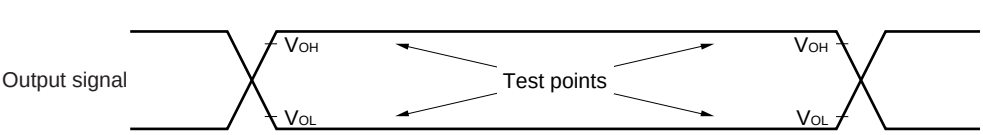


AC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

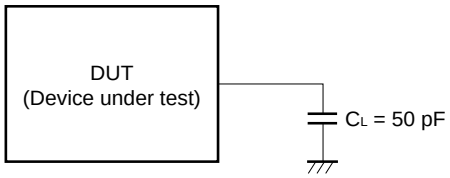
AC Test Input Waveform (V_{DD}: EV_{DD}, BV_{DD}, AV_{DD})



AC Test Output Test Points (EV_{DD}, BV_{DD})



Load Conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

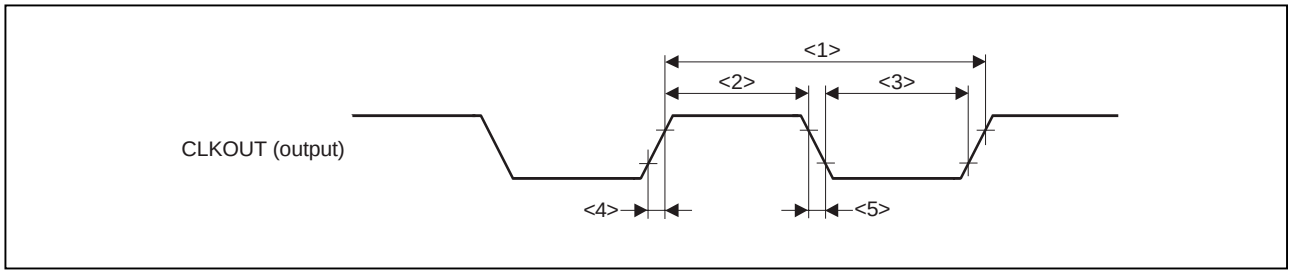
(1) Clock timing

(a) T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, V_{SS} = BV_{SS} = 0 V

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		76.9 ns	31.2 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 12		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 12		ns
CLKOUT rise time	<4>	t_{KR}			12	ns
CLKOUT fall time	<5>	t_{KF}			12	ns

(b) T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, V_{SS} = BV_{SS} = 0 V

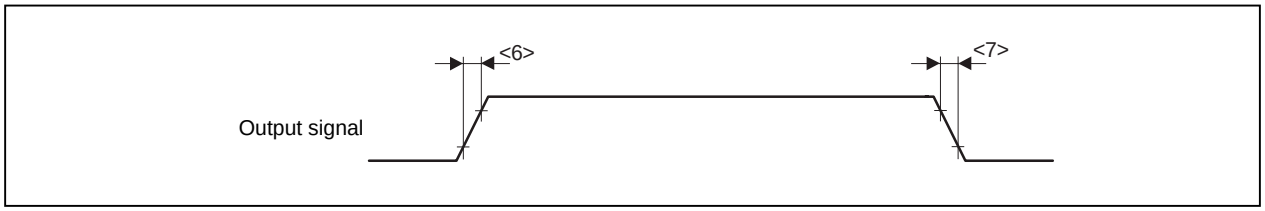
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
CLKOUT output cycle	<1>	t_{CYK}		76.9 ns	31.2 μs	
CLKOUT high-level width	<2>	t_{WKH}		$0.4t_{CYK}$ – 15		ns
CLKOUT low-level width	<3>	t_{WKL}		$0.4t_{CYK}$ – 15		ns
CLKOUT rise time	<4>	t_{KR}			15	ns
CLKOUT fall time	<5>	t_{KF}			15	ns



(2) Output waveform (other than port 4, port 5, port 6, port 9, X1, and CLKOUT)

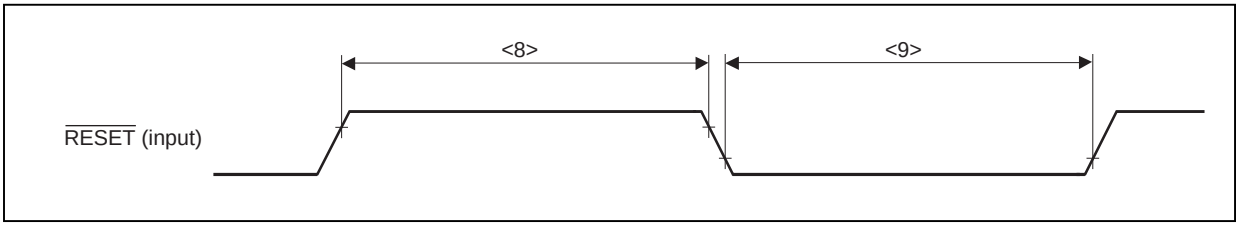
(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = EV_{DD} = 3.0 to 5.5 V, V_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<6>	t_{OR}			20	ns
Output fall time	<7>	t_{OF}			20	ns



(3) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ pin high-level width	<8>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ pin low-level width	<9>	t_{WRSL}		500		ns



(4) Bus timing

(a) Clock asynchronous (T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, V_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 16		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 15		ns
Address float from $\overline{DSTB}$↓	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 40	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 40	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<15>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<16>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<17>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<18>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<19>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<20>	t_{WDL}		(1 + n)T – 22		ns
ASTB high-level width	<21>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<22>	t_{DDOD}			10	ns
Data output setup time (to $\overline{DSTB}$↑)	<23>	t_{SODD}		(1 + n)T – 25		ns
Data output hold time (from $\overline{DSTB}$↑)	<24>	t_{HDOD}		T – 20		ns
$\overline{WAIT}$ setup time (to address)	<25>	t_{SAWT1}	n ≥ 1		1.5T – 40	ns
	<26>	t_{SAWT2}	n ≥ 1		(1.5 + n)T – 40	ns
$\overline{WAIT}$ hold time (from address)	<27>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<28>	t_{HAWT2}	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<29>	t_{SSTWT1}	n ≥ 1		T – 32	ns
	<30>	t_{SSTWT2}	n ≥ 1		(1 + n)T – 32	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<31>	t_{HSTWT1}	n ≥ 1	nT		ns
	<32>	t_{HSTWT2}	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<33>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<34>	t_{WHAL}		T – 15		ns
Bus output delay time from $\overline{HLDAK}$↑	<35>	t_{DHAC}		–6		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<36>	t_{DHQHA1}			(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<37>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle cycles inserted in the bus cycle.

4. The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(b) Clock asynchronous (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, V_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	<10>	t_{SAST}		0.5T – 20		ns
Address hold time (from ASTB↓)	<11>	t_{HSTA}		0.5T – 20		ns
Address float from $\overline{DSTB}$↓	<12>	t_{FDA}			0	ns
Data input setup time from address	<13>	t_{SAID}			(2 + n)T – 50	ns
Data input setup time from $\overline{DSTB}$↓	<14>	t_{SDID}			(1 + n)T – 50	ns
Delay time from ASTB↓ to $\overline{DSTB}$↓	<15>	t_{DSTD}		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↑)	<16>	t_{HDID}		0		ns
Address output time from $\overline{DSTB}$↑	<17>	t_{DDA}		(1 + i)T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↑	<18>	t_{DDST1}		0.5T – 15		ns
Delay time from $\overline{DSTB}$↑ to ASTB↓	<19>	t_{DDST2}		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	<20>	t_{WDL}		(1 + n)T – 35		ns
ASTB high-level width	<21>	t_{WSTH}		T – 15		ns
Data output time from $\overline{DSTB}$↓	<22>	t_{DDOD}			10	ns
Data output setup time (to $\overline{DSTB}$↑)	<23>	t_{SODD}		(1 + n)T – 35		ns
Data output hold time (from $\overline{DSTB}$↑)	<24>	t_{HDOD}		T – 25		ns
$\overline{WAIT}$ setup time (to address)	<25>	t_{SAWT1}	n ≥ 1		1.5T – 55	ns
	<26>	t_{SAWT2}	n ≥ 1		(1.5 + n)T – 55	ns
$\overline{WAIT}$ hold time (from address)	<27>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<28>	t_{HAWT2}	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	<29>	t_{SSTWT1}	n ≥ 1		T – 45	ns
	<30>	t_{SSTWT2}	n ≥ 1		(1 + n)T – 45	ns
$\overline{WAIT}$ hold time (from ASTB↓)	<31>	t_{HSTWT1}	n ≥ 1	nT		ns
	<32>	t_{HSTWT2}	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	<33>	t_{WHQH}		T + 10		ns
$\overline{HLDAK}$ low-level width	<34>	t_{WHAL}		T – 25		ns
Bus output delay time from $\overline{HLDAK}$↑	<35>	t_{DHAC}		–6		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	<36>	t_{DHQHA1}			(2n + 7.5)T + 25	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	<37>	t_{DHQHA2}		0.5T	1.5T + 25	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. i: Number of idle cycles inserted in the bus cycle.

4. The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(c) Clock synchronous (T_A = –40 to +85°C, V_{DD} = BV_{DD} = 4.0 to 5.5 V, V_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<38>	t_{DKA}		0	19	ns
Delay time from CLKOUT↑ to address float	<39>	t_{FKA}		–12	10	ns
Delay time from CLKOUT↓ to ASTB	<40>	t_{DKST}		0	19	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<41>	t_{DKD}		0	19	ns
Data input setup time (to CLKOUT↑)	<42>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<43>	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	<44>	t_{DKOD}			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<45>	t_{SWTK}		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<46>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<47>	t_{SHQK}		20		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<48>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<49>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<50>	t_{DKHA}			19	ns

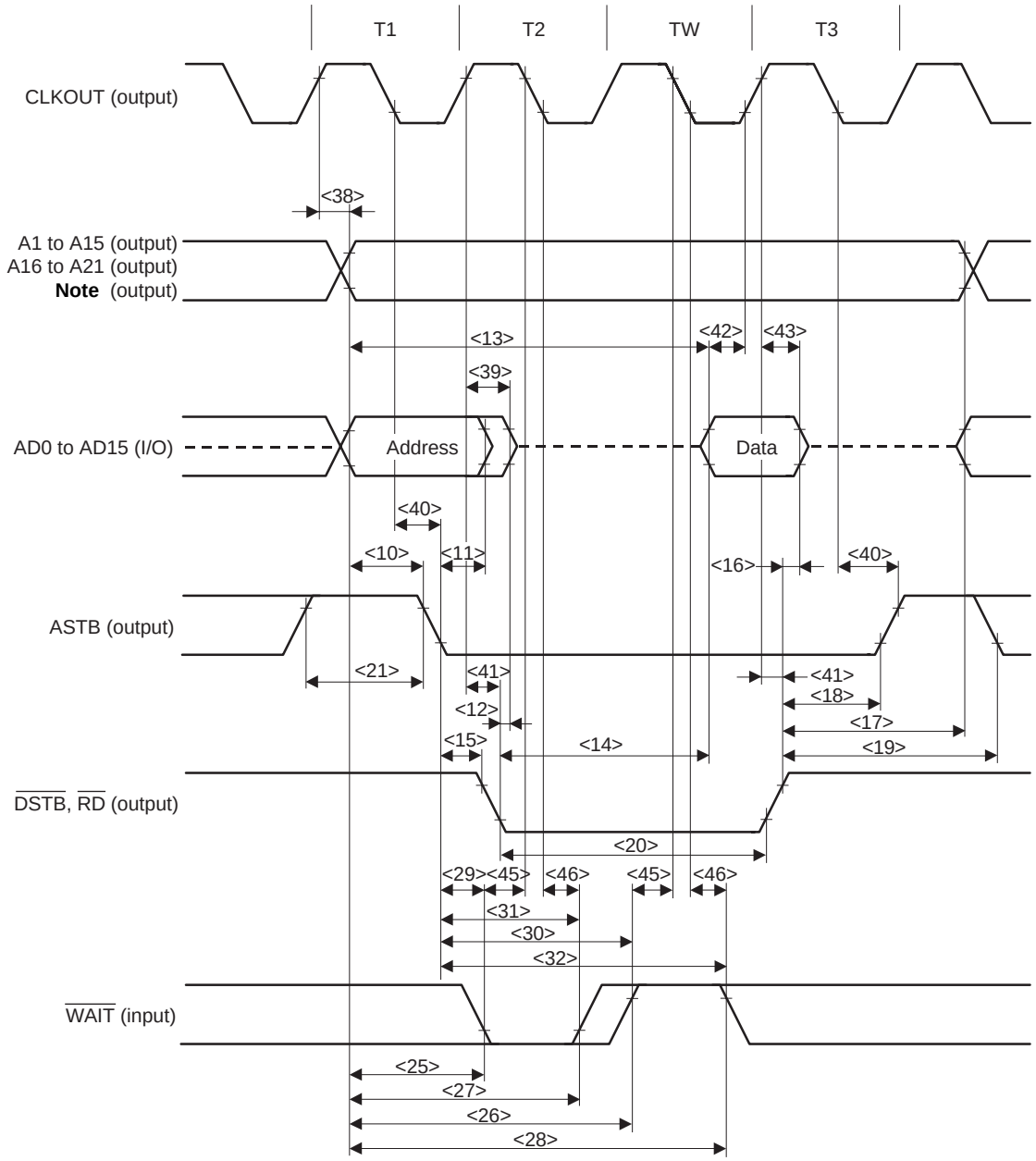
Remark The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

(d) Clock synchronous (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, BV_{DD} = 3.0 to 4.0 V, V_{SS} = BV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<38>	t_{DKA}		0	22	ns
Delay time from CLKOUT↑ to address float	<39>	t_{FKA}		–16	10	ns
Delay time from CLKOUT↓ to ASTB	<40>	t_{DKST}		0	19	ns
Delay time from CLKOUT↑ to $\overline{DSTB}$	<41>	t_{DKD}		0	22	ns
Data input setup time (to CLKOUT↑)	<42>	t_{SIDK}		20		ns
Data input hold time (from CLKOUT↑)	<43>	t_{HKID}		5		ns
Data output delay time from CLKOUT↑	<44>	t_{DKOD}			22	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<45>	t_{SWTK}		24		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<46>	t_{HKWT}		5		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<47>	t_{SHQK}		24		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<48>	t_{HKHQ}		5		ns
Delay time from CLKOUT↑ to address float (during bus hold)	<49>	t_{DKF}			19	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	<50>	t_{DKHA}			19	ns

Remark The values in the above specifications are values for when clocks with a 5:5 duty ratio are input from X1.

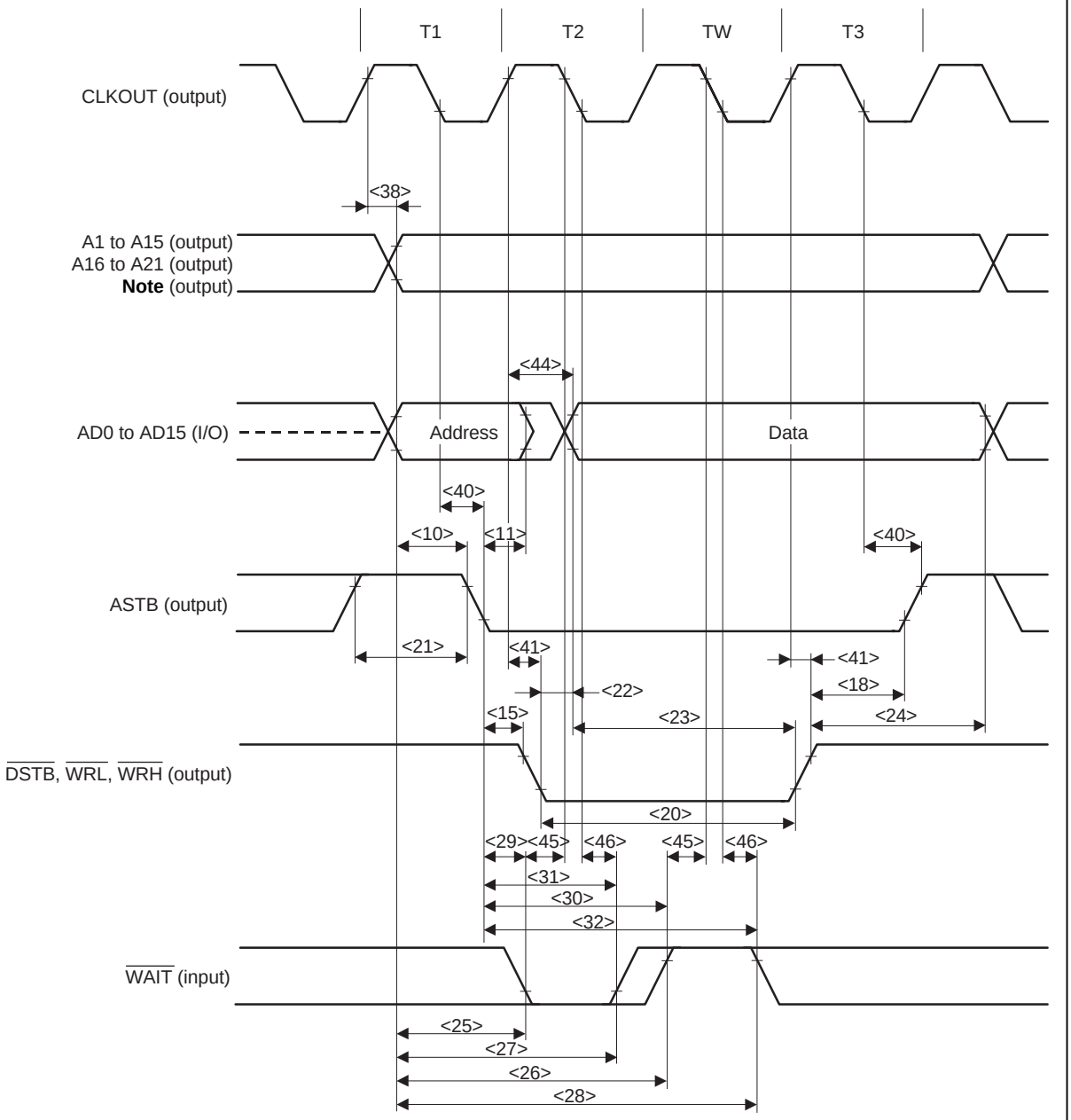
(e) Read cycle (CLKOUT synchronous/asynchronous, 1 wait)



Note R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$

Remark The broken lines indicate high impedance.

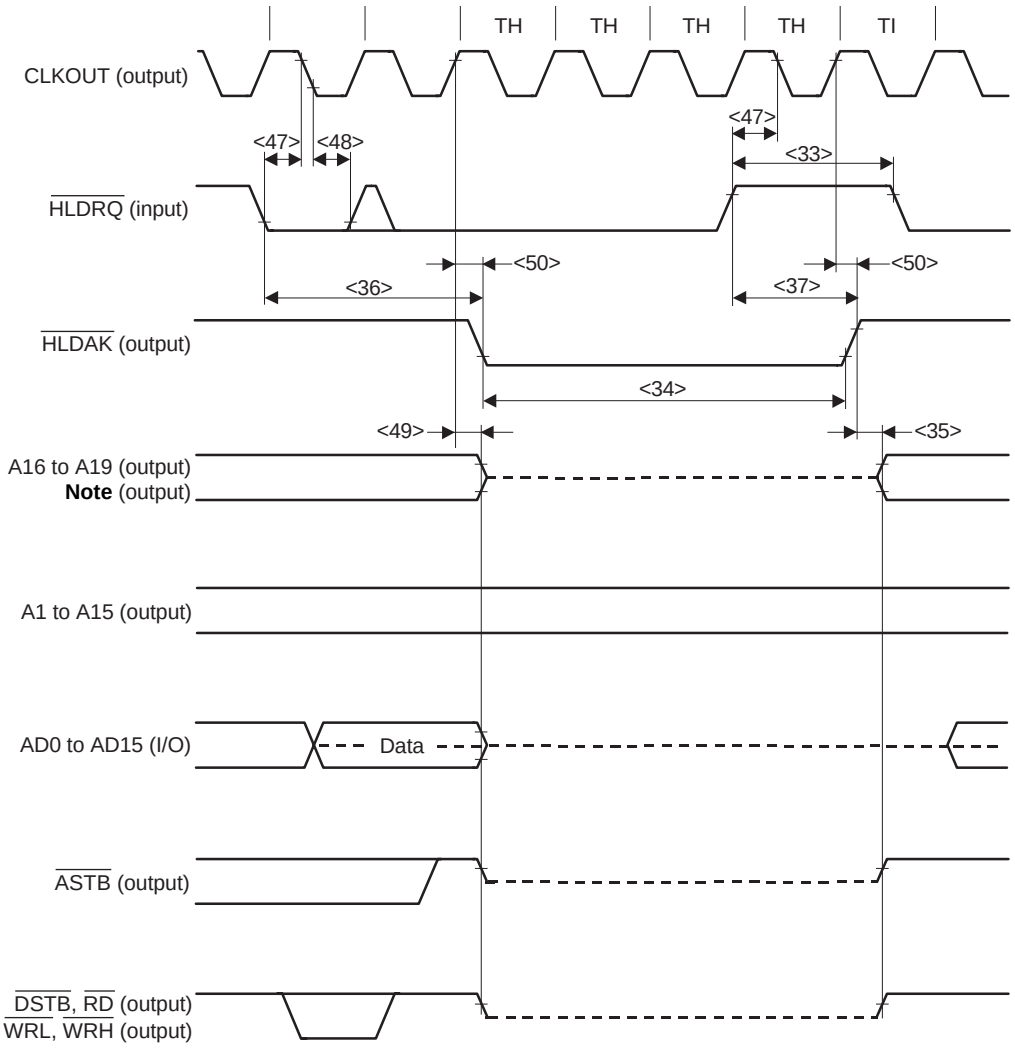
(f) Write cycle (CLKOUT synchronous/asynchronous, 1 wait)



Note R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$

Remark The broken lines indicate high impedance.

(g) Bus hold timing



Note R/W, UBEN, LBEN

Remark The broken lines indicate high impedance.

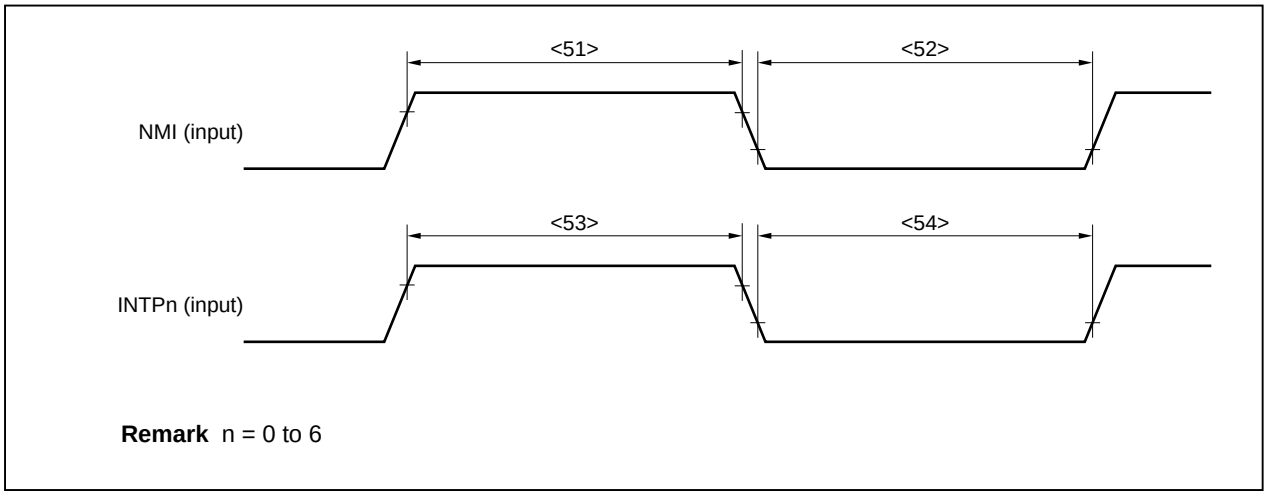
(5) Interrupt timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<51>	t_{WNIH}		500		ns
NMI low-level width	<52>	t_{WNIL}		500		ns
INTPn high-level width	<53>	t_{WITH}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns
INTPn low-level width	<54>	t_{WITL}	n = 0 to 3, analog noise elimination	500		ns
			n = 4, 5, digital noise elimination	3T + 20		ns
			n = 6, digital noise elimination	3Tsmp + 20		ns

Remarks 1. T = 1/f_{XX}

2. Tsmp = Noise elimination sampling clock cycle



Remark n = 0 to 6

(6) RPU timing (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = BV_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TIn0, TIn1 high-level width	<55>	t_{TIHn}	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIn0, TIn1 low-level width	<56>	t_{TILn}	n = 0, 1	$2T_{sam}$ + 20[Note]		ns
TIn high-level width	<57>	t_{TIHn}	n = 2 to 5	3T + 20		ns
TIn low-level width	<58>	t_{TILn}	n = 2 to 5	3T + 20		ns

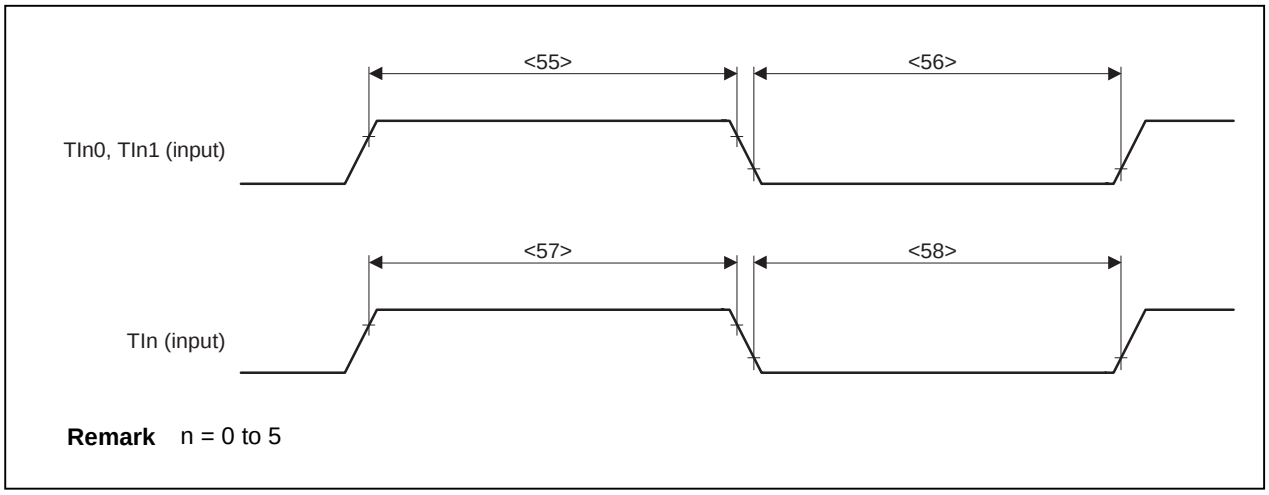
Note T_{sam} can select the following count clocks by setting the PRMn2 to PRMn0 bits of prescaler mode registers n0, n1 (PRMn0, PRMn1).

When n = 0 (TM0), T_{sam} = 2T, 4T, 16T, 64T, 256T, or 1/INTWTNI cycle

When n = 1 (TM1), T_{sam} = 2T, 4T, 16T, 32T, 128T, or 256T

However, when the TIn0 valid edge is selected as the count clock, T_{sam} = 4T.

Remark T = 1/f_{XX}



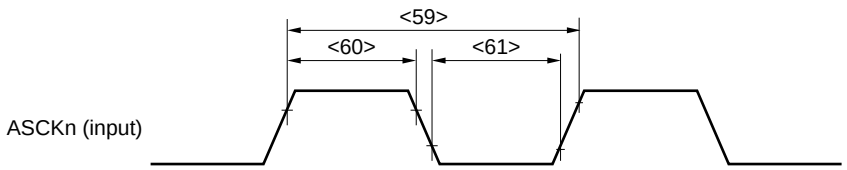
Remark n = 0 to 5

(7) Asynchronous serial interface (UART0, UART1) timing

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
ASCKn cycle time	<59>	t_{KCY13}		200		ns
ASCKn high-level width	<60>	t_{KH13}		80		ns
ASCKn low-level width	<61>	t_{KSO13}		80		ns

Remark n = 0, 1



Remark n = 0, 1

(8) 3-wire serial interface (CSI0 to CSI3) timing

(a) Master mode (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

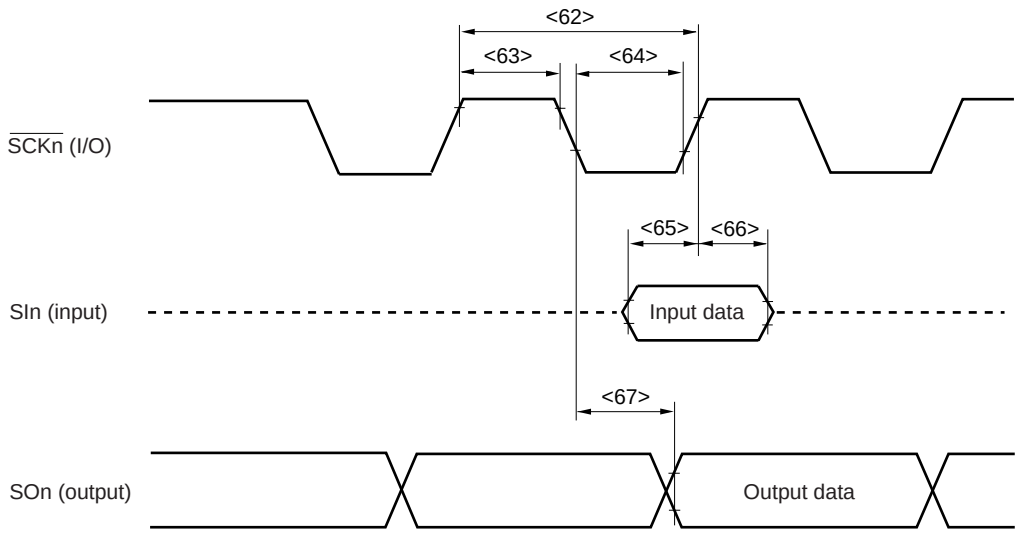
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<62>	t_{KCY1}		400		ns
$\overline{SCKn}$ high-level width	<63>	t_{KH1}		140		ns
$\overline{SCKn}$ low-level width	<64>	t_{KL1}		140		ns
SIn setup time (to $\overline{SCKn}$↑)	<65>	t_{SIK1}		50		ns
SIn hold time (from $\overline{SCKn}$↑)	<66>	t_{KSI1}		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	<67>	t_{KSO1}			60	ns

Remark n = 0 to 3

(b) Slave mode (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<62>	t_{KCY2}		400		ns
$\overline{SCKn}$ high-level width	<63>	t_{KH2}		140		ns
$\overline{SCKn}$ low-level width	<64>	t_{KL2}		140		ns
SIn setup time (to $\overline{SCKn}$↑)	<65>	t_{SIK2}		50		ns
SIn hold time (from $\overline{SCKn}$↑)	<66>	t_{KSI2}		50		ns
Delay time from $\overline{SCKn}$↓ to SOn output	<67>	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		60	ns
			3.0 V ≤ EV_{DD} < 4.0 V		100	ns

Remark n = 0 to 3



Remarks 1. The broken lines indicate high impedance.

2. n = 0 to 3

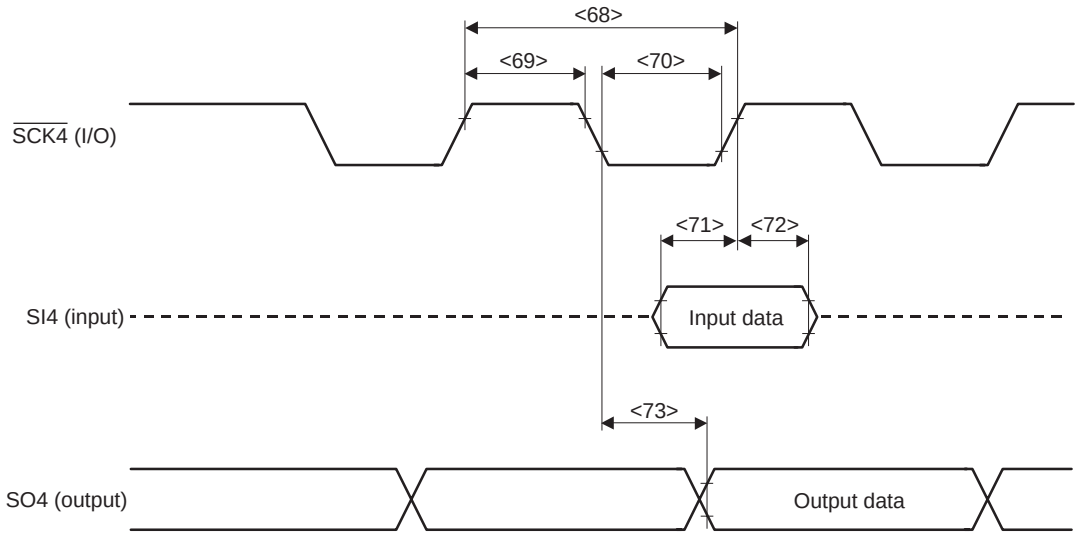
(9) 3-wire variable length serial interface (CSI4) timing

(a) Master mode (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle	<68>	t_{KCY1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	200		ns
			3.0 V ≤ EV_{DD} < 4.0 V	400		ns
$\overline{SCK4}$ high-level width	<69>	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
$\overline{SCK4}$ low-level width	<70>	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
SI4 setup time (to $\overline{SCK4}$↑)	<71>	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	25		ns
			3.0 V ≤ EV_{DD} < 4.0 V	50		ns
SI4 hold time (from $\overline{SCK4}$↑)	<72>	t_{KSI1}		20		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	<73>	t_{KSO1}			55	ns

(b) Slave mode (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK4}$ cycle	<68>	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	200		ns
			3.0 V ≤ EV_{DD} < 4.0 V	400		ns
$\overline{SCK4}$ high-level width	<69>	t_{KH2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
$\overline{SCK4}$ low-level width	<70>	t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	60		ns
			3.0 V ≤ EV_{DD} < 4.0 V	140		ns
SI4 setup time (to $\overline{SCK4}$↑)	<71>	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	25		ns
			3.0 V ≤ EV_{DD} < 4.0 V	50		ns
SI4 hold time (from $\overline{SCK4}$↑)	<72>	t_{KSI2}		20		ns
Delay time from $\overline{SCK4}$↓ to SO4 output	<73>	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		55	ns
			3.0 V ≤ EV_{DD} < 4.0 V		100	ns



Remark The broken lines indicate high impedance.

(10) I^2C bus mode (μPD703034AY, 703035AY, 70F3035AY only)

(T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		–	f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		<74>	t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		<75>	$t_{HD:STA}$	4.0	–	0.6	–	μs
SCLn clock low-level width		<76>	t_{LOW}	4.7	–	1.3	–	μs
SCLn clock high-level width		<77>	t_{HIGH}	4.0	–	0.6	–	μs
Setup time for start/restart conditions		<78>	$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	<79>	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		<80>	$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDAn and SCLn signal rise time		<81>	t_R	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDAn and SCLn signal fall time		<82>	t_F	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		<83>	$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		<84>	t_{SP}	–	–	0	50	ns
Capacitance load of each bus line		–	Cb	–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDAn signal (at $V_{IHmin.}$ of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

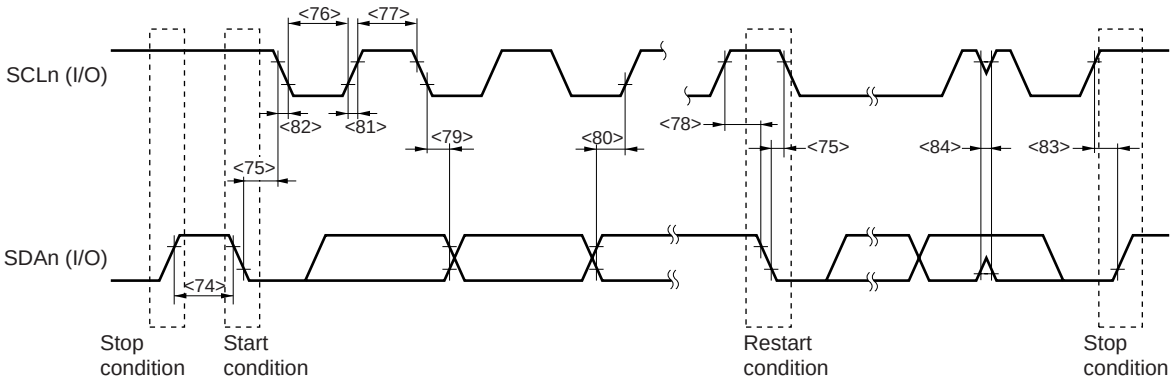
3. If the system does not extend the SCLn signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCLn signal's low state hold time:
  $t_{HD:DAT} \geq 250$ ns
- If the system extends the SCLn signal's low state hold time:
  Transmit the following data bit to the SDAn line prior to the SCLn line release ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0, 1



Remark n = 0, 1

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF}, V_{SS} = AV_{SS} = 0 V, Output pin load capacitance: C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10	10	10	bit
Overall error[Note 1]	–	ADM2 = 00H			±0.6	%FSR
		ADM2 = 01H			±1.0	%FSR
Conversion time	t_{CONV}		5		10	μs
Zero-scale error[Note 1]	AINL				±0.4	%FSR
Full-scale error[Note 1]	AINL	ADM2 = 00H			±0.4	%FSR
		ADM2 = 01H			±0.6	%FSR
Integral linearity error[Note 2]	INL	ADM2 = 00H			±4.0	LSB
		ADM2 = 01H			±6.0	LSB
Differential linearity error[Note 2]	DNL	ADM2 = 00H			±4.0	LSB
		ADM2 = 01H			±6.0	LSB
Analog reference voltage	AV_{REF}	AV_{REF} = AV_{DD}	4.5		5.5	V
Analog power supply voltage	AV_{DD}		4.5		5.5	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} input current	AI_{REF}			1	2	mA
AV_{DD} current	AI_{DD}	ADM2 = 00H		3	6	mA
		ADM2 = 01H		4	8	mA

Notes 1. Excluding quantization error (±0.05 %FSR)

2. Excluding quantization error (±0.5 LSB)

Remarks 1. LSB: Least Significant Bit
FSR: Full Scale Range

2. ADM2: A/D converter mode register 2

IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, EV_{DD} = 3.0 to 5.5 V, V_{SS} = EV_{SS} = 0 V)

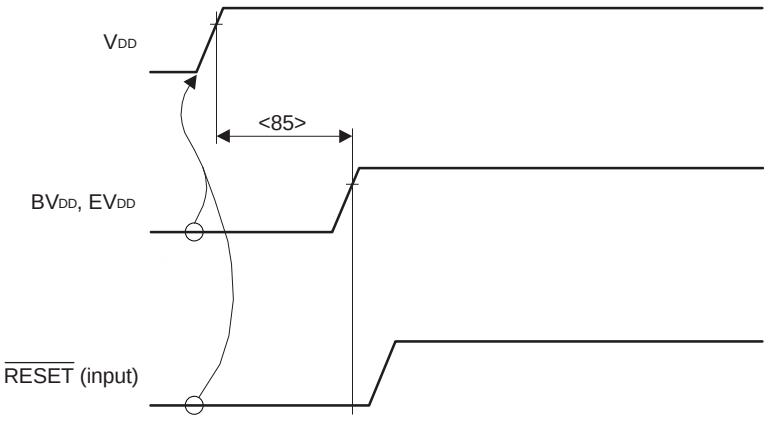
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_S	Communication mode: fixed to mode 1		6.0 Note 1		MHz
				6.29 Notes 1, 2		MHz

Notes 1. 6.0 MHz and 6.29 MHz can not be used together for the IEBus system clock frequency

2. Although the system clock specified in the IEBus specification is 6.0 MHz, operation is guaranteed at 6.29 MHz system clock in the V850/SB2.

Regulator (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
Output stabilization time	<85>	t_{REG}	Stabilization capacitance C = 1 μF (Connected to REGC pin)	1			ms



Cautions 1. Be sure to start inputting supply voltage (V_{DD}) when $\overline{RESET}$ = V_{SS} = EV_{SS} = BV_{SS} = 0 V (the above state), and make $\overline{RESET}$ high level after the t_{REG} period has elapsed.

2. If supply voltage (BV_{DD} or EV_{DD}) is input before the t_{REG} period has elapsed following the input of supply voltage (V_{DD}), data may be driven from the pins until the t_{REG} period has elapsed because the I/O buffers' power supply was turned on while the circuit was in an undefined state. To avoid this situation, it is recommended to input supply voltage (BV_{DD} or EV_{DD}) after the t_{REG} period has elapsed following the input of supply voltage (V_{DD}).

4.1 Flash Memory Programming Mode (μPD70F3035A, 70F3035AY only)

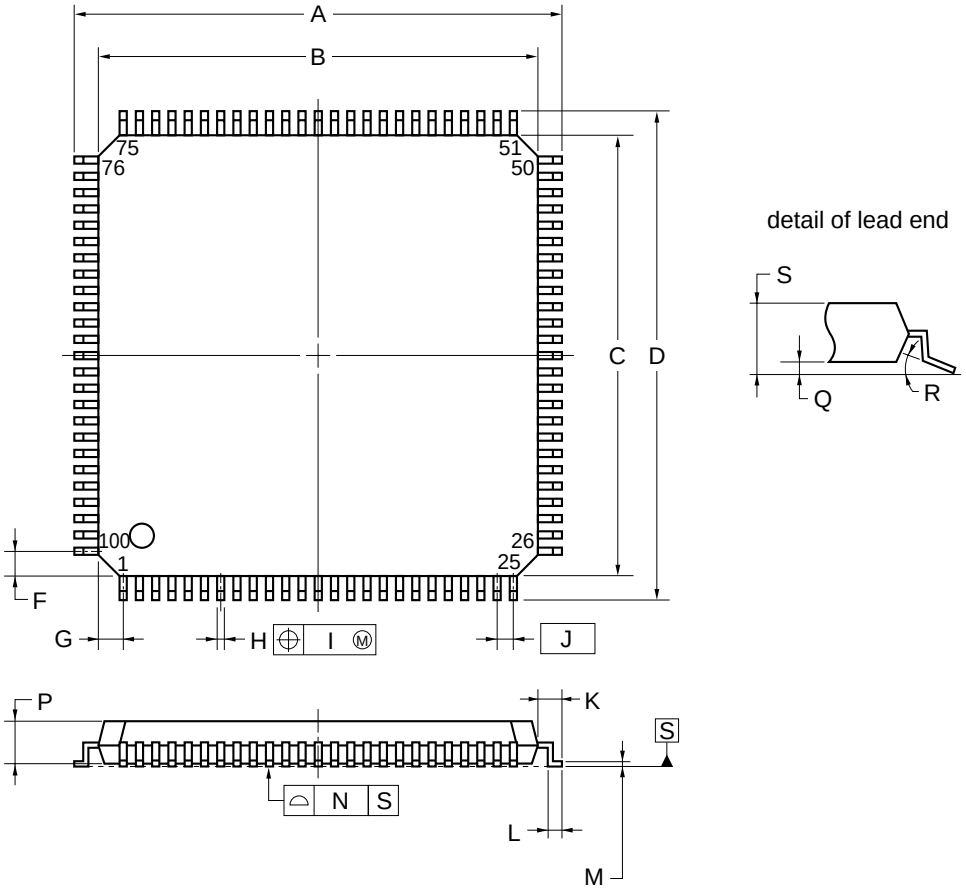
Basic characteristics (T_A = 10 to 85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Operating frequency	f_X			2		13	MHz
Power supply voltage	V_{DD}			4.5		5.5	V
Write current	I_{DDW}	When $V_{PP} = V_{PP1}$	V_{DD} pin			51	mA
	I_{PPW}		V_{PP} pin			50	mA
Erase current	I_{DDE}	When $V_{PP} = V_{PP1}$	V_{DD} pin			51	mA
	I_{PPE}		V_{PP} pin			100	mA
V_{PP} power supply voltage	V_{PP0}	During normal operation		0		0.54	V
	V_{PP1}	During flash memory programming		7.5	7.8	8.1	V
Write count[Note]	C_{WRT}			20	20	20	Times
Unit erase time	t_{ER}			0.2	0.2	0.2	s
Total erase time	t_{ERT}					20	s

Note Erase/write are regarded as 1 cycle.

5. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



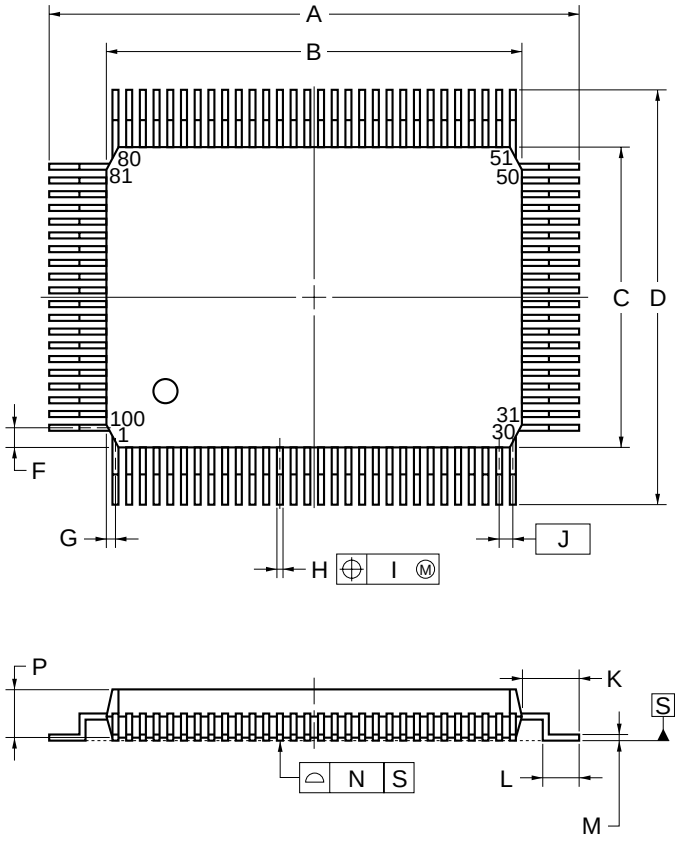
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

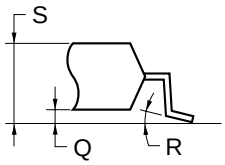
ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU-1

100-PIN PLASTIC QFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

6. RECOMMENDED SOLDERING CONDITIONS

The μPD703034A, 703034AY, 703035A, 703035AY, 70F3035A, and 70F3035AY should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 6-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD703034AGC-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703034AYGC-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703035AGC-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703035AYGC-×××-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD70F3035AGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3035AYGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 6-1. Surface Mounting Type Soldering Conditions (2/2)

(3) μPD703034AGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703034AYGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703035AGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD703035AYGF-xxx-3BA: 100-pin plastic QFP (14 × 20)
μPD70F3035AGF-3BA: 100-pin plastic QFP (14 × 20)
μPD70F3035AYGF-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-207-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Reference document Electrical Characteristics for Microcomputer (IEI-601)[Note]

Note This document number is that of the Japanese version.

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- Availability of related technical literature
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