NEC

MOS INTEGRATED CIRCUIT

μPD703015

V850/SA1™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD703015 (V850/SA1) is a 32-/16-bit single-chip microcontroller that includes the CPU core of the V850 Family™, and peripheral functions such as ROM/RAM, a timer/counter, a serial interface, an A/D converter, a timer, and a DMA controller.

In addition to its highly real-time responsiveness and one-clock-pitch execution of instructions, the V850/SA1 includes a hardware multiplier for multiplication instructions, saturation instructions, and bit manipulation instructions, all of which are instructions suited for digital servo control applications. As a real-time control system, this device provides a high-level cost performance suitable for applications ranging from low-power camcorders and other AV equipment to portable telephone equipment such as cellular phones and personal handyphone systems (PHS).

The functions of the V850/SA1 are explained in detail in the following manual. Be sure to refer to this manual when designing your system.

V850/SA1 User's Manual Hardware: (U12768E)
V850 Family User's Manual Architecture: (U10243E)

FEATURES

- Number of instructions: 74
- Minimum instruction execution time:
  59 ns (when main system clock (f_{XX}) is operating at 17 MHz)
  30.5 μs (when subsystem clock (f_{XT}) is operating at 32.768 kHz)
- General-purpose registers: 32 bits × 32 registers
- Instruction set:
  Signed multiplication, saturation operations, 32-bit shift instruction. bit manipulation instructions, load/store instructions
- Memory space:
  16-Mbyte linear address space
  Memory block allocation function: 2 Mbytes per block
- External bus interface: 16-bit data bus
  Address bus: separate output enabled
- Internal memory
  Mask ROM: 128 Kbytes
  RAM: 4 Kbytes
- Interrupts and exceptions
  External: 8, internal: 30, exception: 1
- I/O lines Total: 85
- Timer/counter
  16-bit timer: 2 channels
  8-bit timer: 4 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Serial interface (SIO)
  Asynchronous serial interface (UART)
  Clock-synchronized serial interface (CSI)
- A/D converter: 12 channels
- DMA controller: 3 channels
- RTP: 8 bits × 1 channel or 4 bits × 2 channels
- Power-saving functions: HALT/IDLE/STOP modes
- Packages: 100-pin plastic LQFP (14 × 14 mm)
  121-pin fine-pitch BGA (12 × 12 mm)

Document No. U13829EJ1V0DS00 (1st edition)
Date Published January 1999 N CP(K)
Printed in Japan

APPLICATIONS

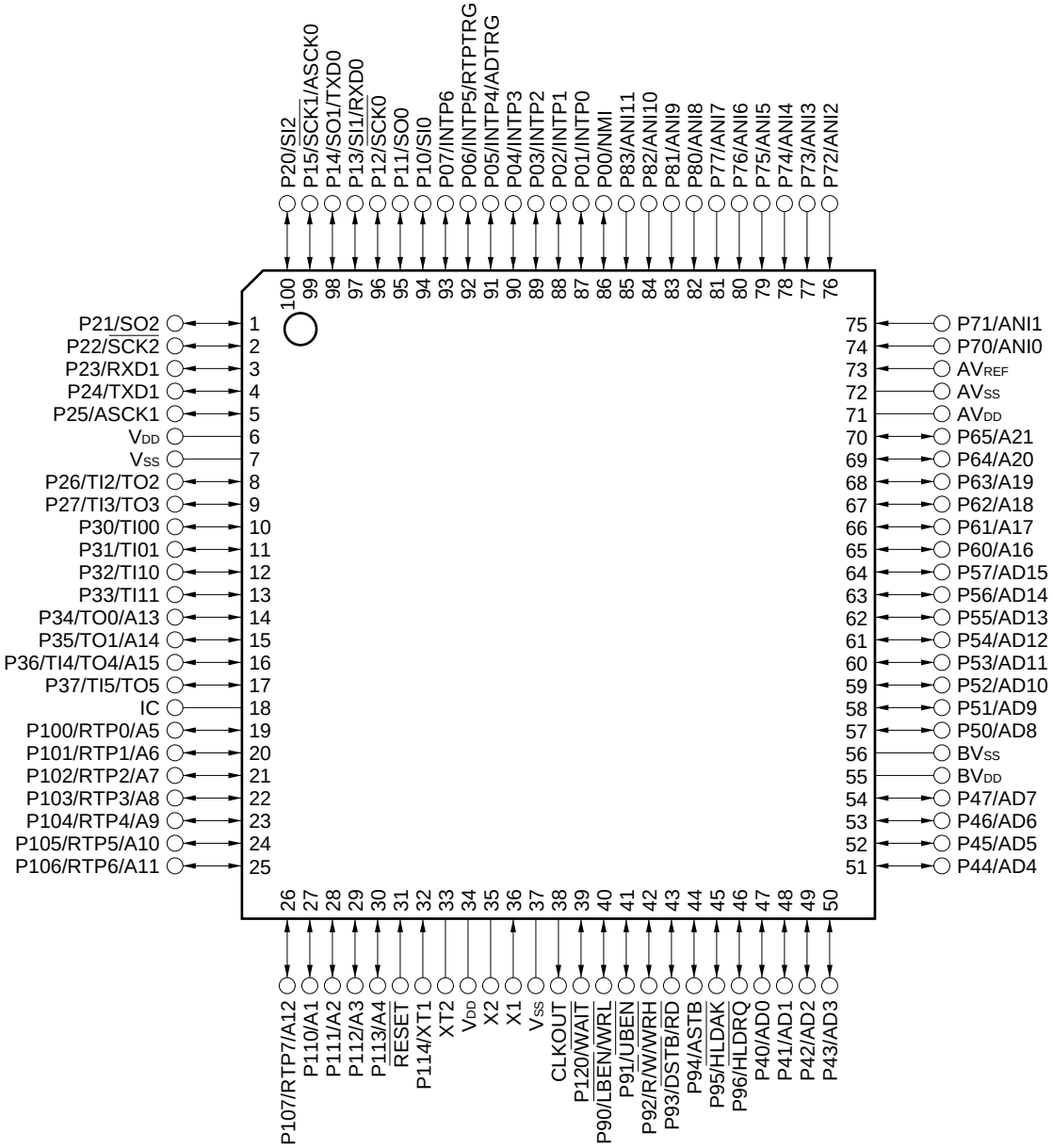
○ Low-power portable equipment
Cellular phones, PHSs, and camcorders

ORDERING INFORMATION

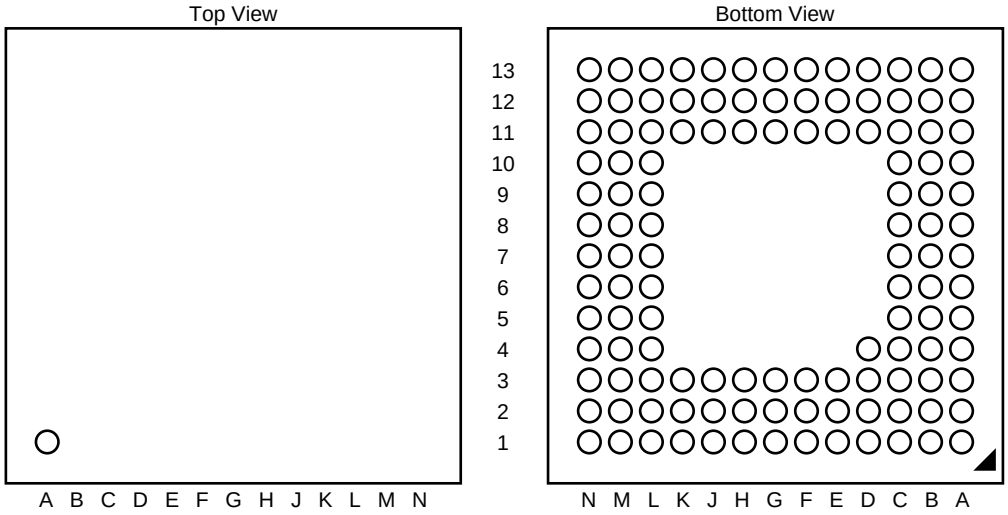
Part Number	Package
μPD703015GC-×××-8EU	100-pin plastic LQFP (fine-pitch) (14 × 14 mm)
μPD703015S1-×××-YJC	121-pin fine-pitch BGA (12 × 12 mm)

PIN CONFIGURATION

- 100-pin plastic LQFP (fine-pitch) (14 × 14 mm)
  μPD703015GC-×××-8EU



- 121-pin fine-pitch BGA (12 × 12 mm)
  μPD703015S1-×××-YJC



Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
A1	P20	B8	P83	D2	V_{DD}	G11	P60	K13	BV_{DD}	M7	V_{SS}
A2	P15	B9	P80	D3	V_{SS}	G12	P56	L1	P104	M8	V_{SS}
A3	V_{SS}	B10	P75	D11	AV_{DD}	G13	P57	L2	P105	M9	P92
A4	P13	B11	AV_{SS}	D12	AV_{DD}	H1	P34	L3	$\overline{\text{RESET}}$	M10	P95
A5	P11	B12	AV_{SS}	D13	AV_{DD}	H2	P37	L4	V_{DD}	M11	P41
A6	P06	B13	P71	E1	P25	H3	P35	L5	V_{SS}	M12	P45
A7	P03	C1	P22	E2	V_{DD}	H11	P55	L6	X2	M13	P44
A8	P00	C2	P23	E3	P30	H12	P53	L7	P90	N1	P107
A9	P81	C3	V_{SS}	E11	AV_{DD}	H13	P54	L8	P120	N2	P110
A10	P76	C4	P24	E12	P64	J1	IC	L9	P93	N3	P112
A11	P73	C5	P07	E13	P65	J2	IC	L10	P96	N4	V_{DD}
A12	P72	C6	P04	F1	P26	J3	P100	L11	BV_{SS}	N5	XT1
A13	AV_{SS}	C7	P01	F2	P27	J11	P52	L12	BV_{SS}	N6	V_{SS}
B1	P21	C8	P82	F3	P33	J12	P50	L13	BV_{SS}	N7	V_{SS}
B2	P14	C9	P77	F11	P63	J13	P51	M1	P106	N8	CLKOUT
B3	V_{SS}	C10	P74	F12	P61	K1	P101	M2	P111	N9	P91
B4	P12	C11	AV_{SS}	F13	P62	K2	P102	M3	P113	N10	P94
B5	P10	C12	P70	G1	P31	K3	P103	M4	V_{DD}	N11	P40
B6	P05	C13	AV_{REF}	G2	P32	K11	P46	M5	XT2	N12	P42
B7	P02	D1	V_{DD}	G3	P36	K12	P47	M6	X1	N13	P43

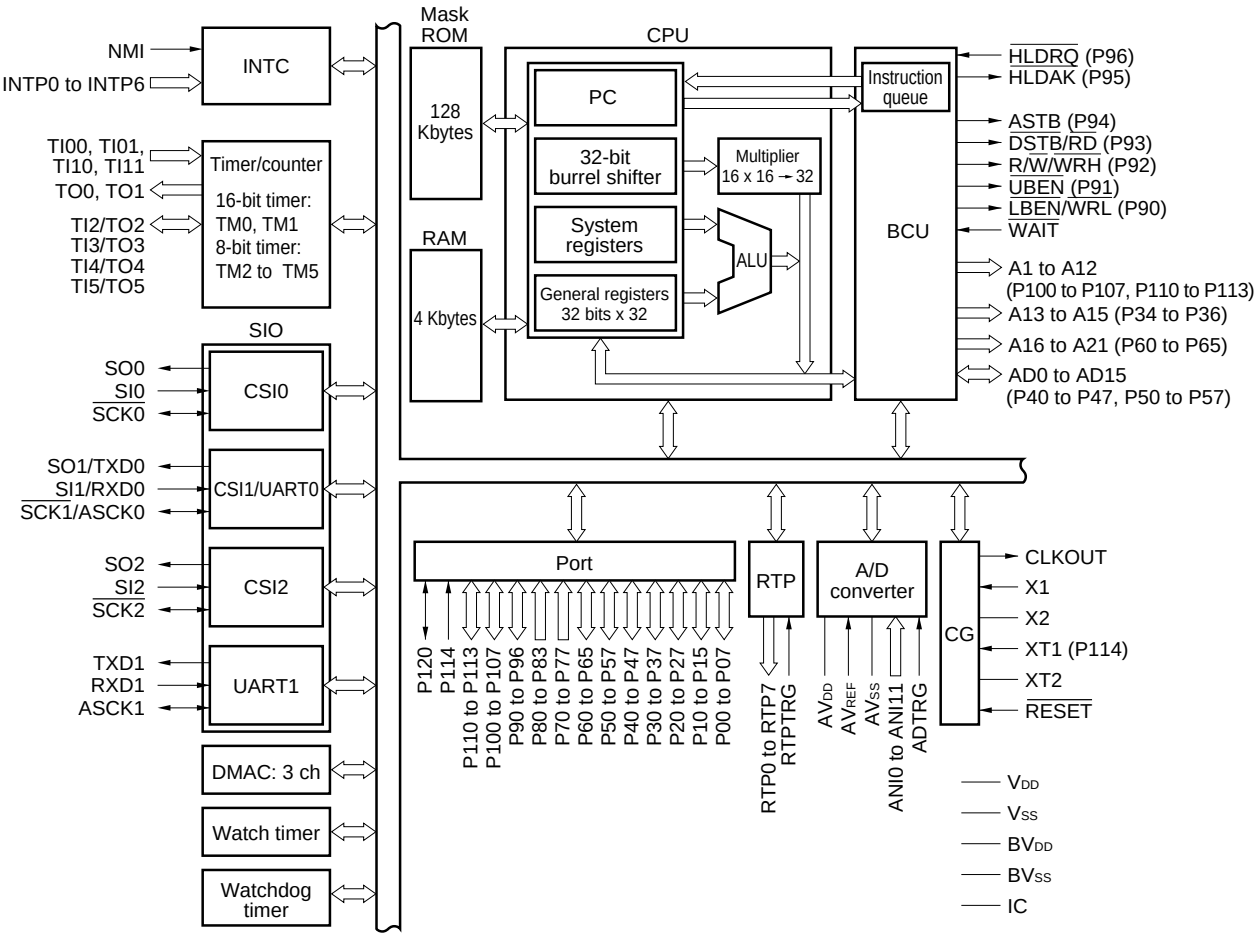
Remarks 1. Alternate function names are omitted. The alternate functions are identical to 100-pin plastic LQFP.

2. Directly connect D4 pin to V_{SS}.

PIN IDENTIFICATION

A1 to A21:	Address Bus	P80 to P83:	Port8
AD0 to AD15:	Address/Data Bus	P90 to P96:	Port9
ADTRG:	AD Trigger Input	P100 to P107:	Port10
ANI0 to ANI11:	Analog Input	P110 to P114:	Port11
ASCK0, ASCK1:	Asynchronous Serial Clock	P120:	Port12
ASTB:	Address Strobe	$\overline{RD}$:	Read
AV_{DD}:	Analog V_{DD}	$\overline{RESET}$:	Reset
AV_{REF}:	Analog Reference Voltage	RTP0 to RTP7:	Real-time Port
AV_{SS}:	Analog V_{SS}	RTPTRG:	RTP Trigger
BV_{DD}:	Power Supply for Bus Interface	R/$\overline{W}$:	Read/Write Status
BV_{SS}:	Ground for Bus Interface	RXD0, RXD1:	Receive Data
CLKOUT:	Clock Output	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
$\overline{DSTB}$:	Data Strobe	SI0 to SI2:	Serial Input
$\overline{HLDAK}$:	Hold Acknowledge	SO0 to SO2:	Serial Output
$\overline{HLDRQ}$:	Hold Request	TI00, TI01, TI10, :	Timer Input
IC:	Internally Connected	TI11, TI2 to TI5	
INTP0 to INTP6:	Interrupt Request From Peripherals	TO0 to TO5:	Timer Output
$\overline{LBEN}$:	Lower Byte Enable	TXD0,TXD1:	Transmit Data
NMI:	Non-maskable Interrupt Request	$\overline{UBEN}$:	Upper Byte Enable
P00 to P07:	Port0	V_{DD}:	Power Supply
P10 to P15:	Port1	V_{SS}:	Ground
P20 to P27:	Port2	$\overline{WAIT}$:	Wait
P30 to P37:	Port3	$\overline{WRH}$:	Write Strobe High Level Data
P40 to P47:	Port4	$\overline{WRL}$:	Write Strobe Low Level Data
P50 to P57:	Port5	X1, X2:	Crystal for Main System Clock
P60 to P65:	Port6	XT1, XT2:	Crystal for Subsystem clock
P70 to P77:	Port7		

INTERNAL BLOCK DIAGRAM



CONTENTS

1. LIST OF PIN FUNCTIONS

1.1 Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
P00	I/O	Yes	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units.	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P05				INTP4/ADTRG
P06				INTP5/RTPTRG
P07				INTP6
P10	I/O	Yes	Port 1 6-bit I/O port Input/output mode can be specified in 1-bit units.	SI0
P11				SO0
P12				$\overline{\text{SCK0}}$
P13				SI1/RXD0
P14				SO1/TXD0
P15				$\overline{\text{SCK1}}$/ASCK0
P20	I/O	Yes	Port 2 8-bit I/O port Input/output mode can be specified in 1-bit units.	SI2
P21				SO2
P22				$\overline{\text{SCK2}}$
P23				RXD1
P24				TXD1
P25				ASCK1
P26				TI2/TO2
P27				TI3/TO3
P30	I/O	Yes	Port 3 8-bit I/O port Input/output mode can be specified in 1-bit units.	TI00
P31				TI01
P32				TI10
P33				TI11
P34				TO0/A13
P35				TO1/A14
P36				TI4/TO4/A15
P37				TI5/TO5

Remark PULL: on-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
P40	I/O	No	Port 4 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD0
P41				AD1
P42				AD2
P43				AD3
P44				AD4
P45				AD5
P46				AD6
P47				AD7
P50	I/O	No	Port 5 8-bit I/O port Input/output mode can be specified in 1-bit units.	AD8
P51				AD9
P52				AD10
P53				AD11
P54				AD12
P55				AD13
P56				AD14
P57				AD15
P60	I/O	No	Port 6 6-bit I/O port Input/output mode can be specified in 1-bit units.	A16
P61				A17
P62				A18
P63				A19
P64				A20
P65				A21
P70	Input	No	Port 7 8-bit input port	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	Input	No	Port 8 4-bit input port	ANI8
P81				ANI9
P82				ANI10
P83				ANI11

Remark PULL: on-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
P90	I/O	No	Port 9 7-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{LBEN}}$/$\overline{\text{WRL}}$
P91				$\overline{\text{UBEN}}$
P92				R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93				$\overline{\text{DSTB}}$/$\overline{\text{RD}}$
P94				ASTB
P95				$\overline{\text{HLDAK}}$
P96				$\overline{\text{HLDRQ}}$
P100	I/O	Yes	Port 10 8-bit I/O port Input/output mode can be specified in 1-bit units.	RTP0/A5
P101				RTP1/A6
P102				RTP2/A7
P103				RTP3/A8
P104				RTP4/A9
P105				RTP5/A10
P106				RTP6/A11
P107				RTP7/A12
P110	I/O	Yes	Port 11 5-bit I/O port Input/output mode can be specified in 1-bit units. P114 is fixed as input only.	A1
P111				A2
P112				A3
P113				A4
P114	Input	No		XT1
P120	I/O	No	Port 12 1-bit I/O port	$\overline{\text{WAIT}}$

Remark PULL: on-chip pull-up resistor

1.2 Non-Port Pins

(1/3)

Pin Name	I/O	PULL	Function	Alternate Function
A1 to A4	Output	Yes	Low-order address bus used for external memory expansion	P110 to P113
A5 to A12				P100/RTP0 to P107/RTP7
A13				P34/TO0
A14				P35/TI1
A15				P36/TI4/TO4
A16 to A21	Output	No	High-order address bus used for external memory expansion	P60 to P65
AD0 to AD7	I/O	No	16-bit multiplexed address/data bus used for external memory expansion	P40 to P47
AD8 to AD15				P50 to P57
ADTRG	Input	Yes	A/D converter external trigger input	P05/INTP4
ANI0 to ANI7	Input	No	Analog input to A/D converter	P70 to P77
ANI8 to ANI11	Input	No		P80 to P83
ASCK0	Input	Yes	Serial clock input for UART0 and UART1	P15/$\overline{SCK1}$
ASCK1				P25
ASTB	Output	No	External address strobe signal output	P94
AV_{DD}	–	–	Positive power supply for A/D converter	–
AV_{REF}	Input	–	Reference voltage input for A/D converter	–
AV_{SS}	–	–	Ground potential for A/D converter	–
BV_{DD}	–	–	Positive power supply for bus interface	–
BV_{SS}	–	–	Ground potential for bus interface	–
CLKOUT	Output	–	Internal system clock output	–
$\overline{DSTB}$	Output	No	External data strobe signal output	P93/$\overline{RD}$
$\overline{HLDAK}$	Output	No	Bus hold acknowledge output	P95
$\overline{HLDRQ}$	Input	No	Bus hold request input	P96
INTP0 to INTP3	I/O	Yes	External interrupt request input (analog noise elimination)	P01 to P04
INTP4			External interrupt request input (digital noise elimination)	P05/ADTRG
INTP5				P06/RTPTRG
INTP6				P07
$\overline{LBEN}$	Output	No	External data bus's low-order byte enable signal output	P90/$\overline{WRL}$
NMI	Input	Yes	Non-maskable interrupt request input	P00
$\overline{RD}$	Output	No	Read strobe signal output	P93/$\overline{DSTB}$
$\overline{RESET}$	Input	–	System reset input	–
RTP0 to RTP7	Output	Yes	Real-time output port	P100/A5 to P107/A12

Remark PULL: on-chip pull-up resistor

(2/3)

Pin Name	I/O	PULL	Function	Alternate Function
RTPTRG	Input	Yes	RTP external trigger input	P06/INTP5
R/$\overline{W}$	Output	No	External read/write status output	P92/$\overline{WRH}$
RXD0	Input	Yes	Serial receive data input for UART0 and UART1	P13/SI1
RXD1				P23
$\overline{SCK0}$	I/O	Yes	Serial clock I/O (3-wire type) for CSI0 to CSI2	P12
$\overline{SCK1}$				P15/ASCK0
$\overline{SCK2}$				P22
SI0	Input	Yes	Serial receive data input (3-wire type) for CSI0 to CSI2	P10
SI1				P13/RXD0
SI2				P20
SO0	Output	Yes	Serial transmit data output (3-wire type) for CSI0 to CSI2	P11
SO1				P14/TXD0
SO2				P21
TI00	Input	Yes	External capture trigger input and external count clock input for TM0	P30
TI01			External capture trigger input for TM0	P31
TI10			External capture trigger input and external count clock input for TM1	P32
TI11			External capture trigger input for TM1	P33
TI2			External count clock input for TM2	P26/TO2
TI3			External count clock input for TM3	P27/TO3
TI4			External count clock input for TM4	P36/TO4/A15
TI5			External count clock input for TM5	P37/TO5
TO0, TO1	Output	Yes	Pulse signal output for TM0, TM1	P34/A13, P35/A14
TO2			Pulse signal output for TM2	P26/TI2
TO3			Pulse signal output for TM3	P27/TI3
TO4			Pulse signal output for TM4	P36/TI4/A15
TO5			Pulse signal output for TM5	P37/TI5
TXD0	Output	Yes	Serial transmit data output for UART0 and UART1	P14/SO1
TXD1				P24
$\overline{UBEN}$	Output	No	High-order byte enable signal output for external data bus	P91
V_{DD}	–	–	Positive power supply pin	–
V_{SS}	–	–	GND potential	–

Remark PULL: on-chip pull-up resistor

(3/3)

Pin Name	I/O	PULL	Function	Alternate Function
$\overline{\text{WAIT}}$	Input	No	Control signal input for inserting wait in bus cycle	P120
$\overline{\text{WRH}}$	Output	No	High-order byte write strobe signal output for external data bus	P92/R/$\overline{\text{W}}$
$\overline{\text{WRL}}$			Low-order byte write strobe signal output for external data bus	P90/$\overline{\text{LBEN}}$
X1	Input	No	Resonator connection for main clock	–
X2	–			–
XT1	Input	No	Resonator connection for subsystem clock	P114
XT2	–			–
IC	–	–	Internally connected	–

Remark PULL: on-chip pull-up resistor

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 1-1 shows the input/output circuit type of each pin and the recommended connection of unused pins, and Figure 1-1 shows the schematic circuit diagram for each I/O circuit type.

Table 1-1. Types of Pin I/O Circuit and Recommended Connection of Unused Pins (1/2)

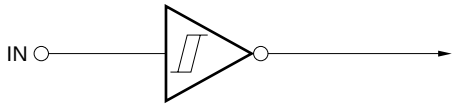
Pin	Alternate Function	I/O Circuit Type	Recommended Connection Method
P00	NMI	8-A	During input: Connect to V_{SS} During output: Leave open
P01 to P04	INTP0 to INTP3		
P05	INTP4/ADTRG		
P06	INTP5/RTPTRG		
P07	INTP6		
P10	SI0	10-A	During input: Connect to V_{DD} or V_{SS} During output: Leave open
P11	SO0	26	
P12	$\overline{SCK0}$	10-A	
P13	SI1/RXD0	8-A	
P14	SO1/TXD0	26	
P15	$\overline{SCK1}$/ASCK0	10-A	
P20	SI2	8-A	
P21	SO2	26	
P22	$\overline{SCK2}$	10-A	
P23	RXD1	8-A	
P24	TXD1	5-A	
P25	ASCK1	8-A	
P26, P27	TI2/TO2, TI3/TO3		
P30, P31	TI00, TI01		
P32, P33	TI10, TI11		
P34, P35	TO0/A13, TO1/A14	5-A	
P36	TI4/TO4/A15	8-A	
P37	TI5/TO5		
P40 to P47	AD0 to AD7	5	During input: Connect to BV_{DD} or BV_{SS} During output: Leave open
P50 to P57	AD8 to AD15		
P60 to P65	A16 to A21		
P70 to P77	ANI0 to ANI7	9	Connect to AV_{SS} or AV_{DD}
P80 to P83	ANI8 to ANI11		

Table 1-1. Types of Pin I/O Circuit and Recommended Connection of Unused Pins (2/2)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection Method
P90	$\overline{LBEN}/\overline{WRL}$	5	During input: Connect to BV_{DD} or BV_{SS} During output: Leave open
P91	$\overline{UBEN}$		
P92	R/$\overline{W}$/$\overline{WRH}$		
P93	$\overline{DSTB}/\overline{RD}$		
P94	ASTB		
P95	$\overline{HLDAK}$		
P96	$\overline{HLDRQ}$		
P100 to P107	RTP0/A5 to RTP7/A12	26	During input: Connect to V_{DD} or V_{SS} During output: Leave open
P110 to P113	A1 to A4	5-A	
P114	XT1	16	
P120	$\overline{WAIT}$	5	During input: Connect to BV_{DD} or BV_{SS} During output: Leave open
AV_{DD}	–	–	Connect to V_{DD}
AV_{SS}	–	–	Connect to V_{SS}
AV_{REF}	–	–	
CLKOUT	–	4	Leave open
$\overline{RESET}$	–	2	–
X2	–	–	Leave open (when external clock is input to X1 pin)
XT2	–	16	Leave open

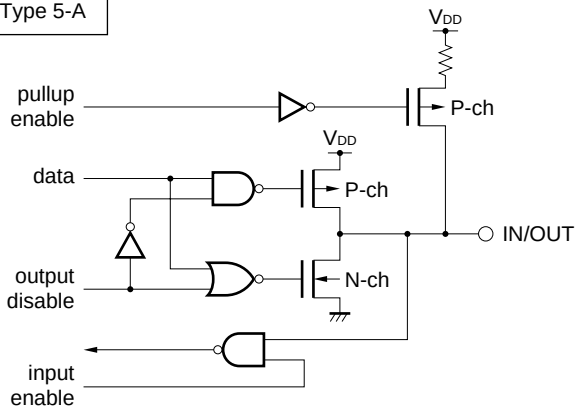
Figure 1-1. Pin Input/Output Circuits (1/2)

Type 2

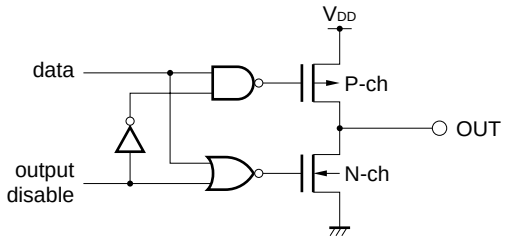


Schmitt-triggered input with hysteresis characteristic

Type 5-A

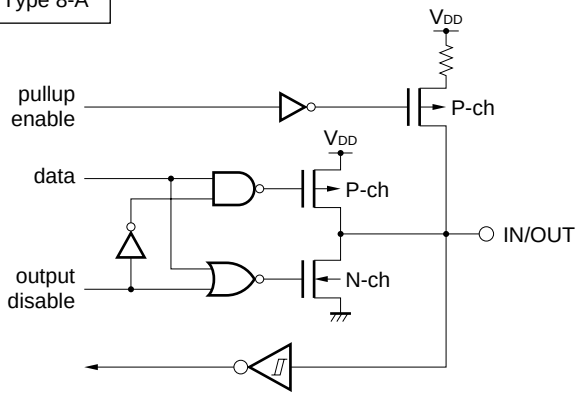


Type 4

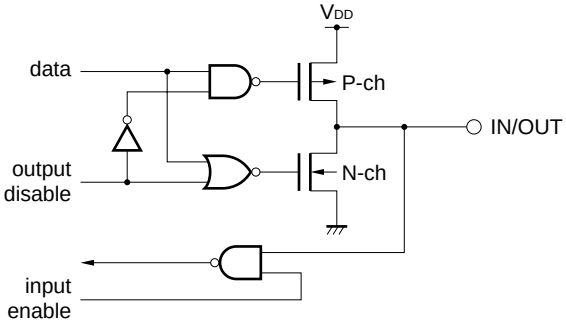


Push-pull output that can be set for high-impedance output (both P-ch and N-ch off)

Type 8-A



Type 5



Type 9

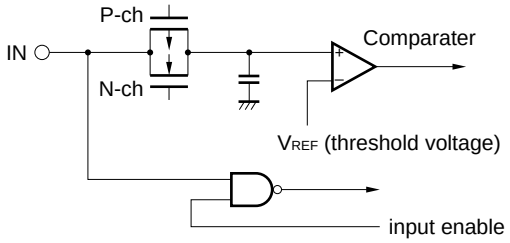
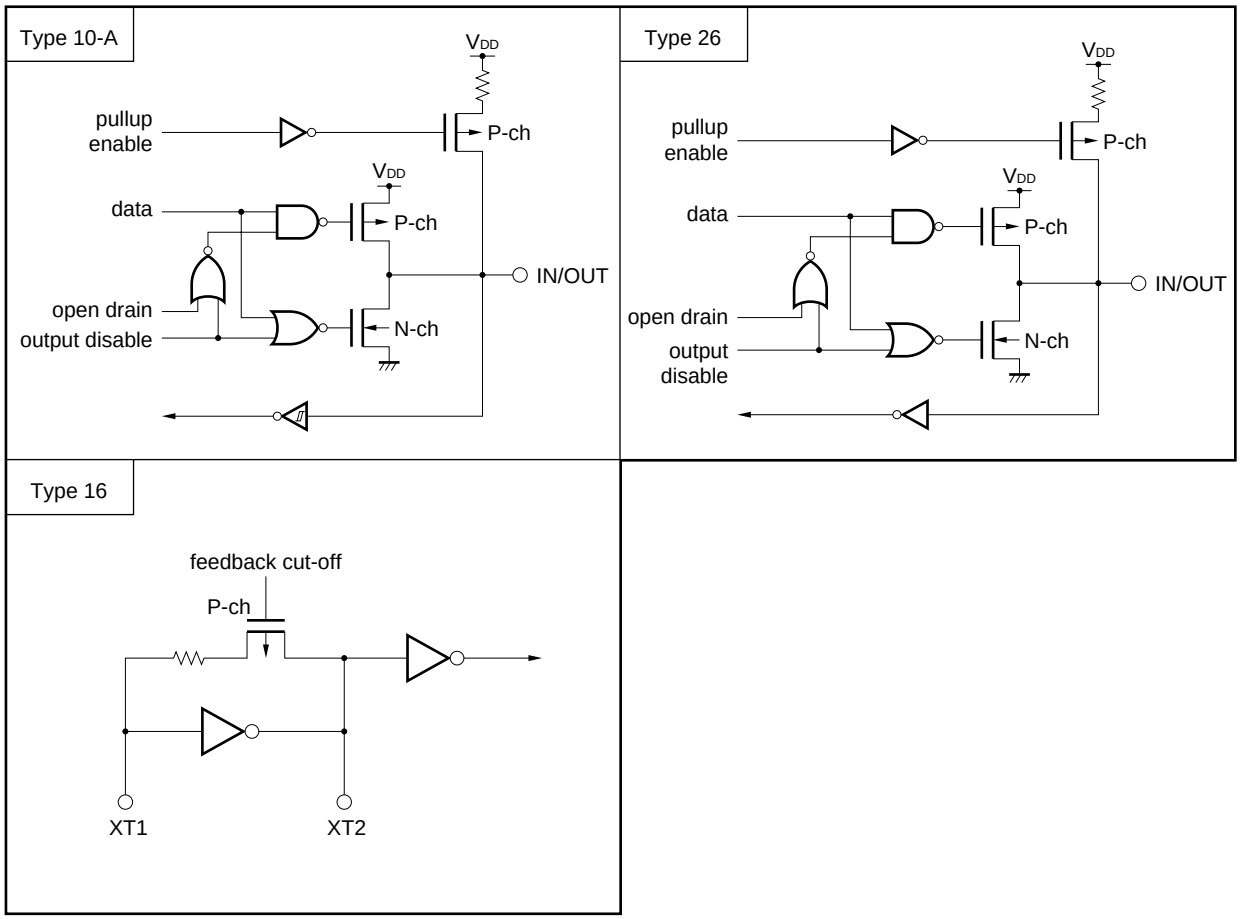


Figure 1-1. Pin Input/Output Circuits (2/2)



2. FUNCTION BLOCKS

2.1 On-Chip Units

(1) CPU

The CPU uses five-stage pipeline control to enable 1-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as the multiplier (16 bits × 16 bits → 32 bits) and the barrel shifter (32 bits) help accelerate processing of complex instructions.

(2) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU. When an instruction is fetched from external memory area and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an instruction queue.

The μPD703015 is equipped with BV_{DD} and BV_{SS} as power supply pins for the bus interface. These provide an external interface using a lower voltage level compared to the V_{DD} and V_{SS} pins.

(3) ROM

This consists of a 128-Kbyte mask ROM mapped to the address space starting at 00000000H. This area can be accessed by the CPU in 1-clock cycle when an instruction is fetched.

(4) RAM

This consists of a 4-Kbyte RAM mapped to the address space starting at FFFFE000H for a mask ROM version. This area can be accessed by the CPU in 1-clock cycle.

(5) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed for interrupt sources.

(6) Clock generator (CG)

The clock generator includes two types of oscillators, each for main system clock (f_{XX}) and for subsystem clock (f_{XT}), generates five types of clocks (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, and f_{XT}), and supplies one of them as operating clocks for the CPU (f_{CPU}).

(7) Timer/counter

A two-channel 16-bit timer/event counter and a four-channel 8-bit timer/event counter are both on chip, which enable measurement of pulse intervals and frequency as well as programmable pulse output.

The two-channel 8-bit timer/event counter can be connected via a cascade connection to enable use as a 16-bit timer.

(8) Watch timer

This timer counts the reference time period (0.5 seconds) for watch counting by using the 32.768-kHz subsystem clock or the 16.777-MHz main system clock. At the same time, the watch timer can also be used as an interval timer that uses the main system clock as a source clock.

(9) Watchdog timer

This timer detects program runaway, system abnormalities, etc.

It can also be used as an interval timer.

When used as a watchdog timer, it generates a non-maskable interrupt request (INTWDT) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request (INTWDTM) after an overflow occurs.

(10) Serial interface (SIO)

The μPD703015 includes two kinds of serial interfaces –asynchronous serial interface (UART) and a clock-synchronized serial interface (CSI)– comprising four channels. One of these channels is switchable between the UART and CSI. Other two channels are fixed as CSI, while the other one channel is fixed as UART.

For UART, data is transferred via the TXDn and RXDn pins (n = 0, 1).

For CSI, data is transferred via the SOn, SIn, and $\overline{\text{SCKn}}$ pins (n = 0 to 2).

UART has an on-chip two-channel dedicated baud rate generator.

(11) A/D converter

This high-speed, high-resolution 10-bit A/D converter includes 12 analog input pins. Conversion uses the successive approximation method.

(12) DMA controller

A three-channel DMA controller is on chip. This controller transfers data between the internal RAM and on-chip peripheral I/O devices in response to interrupt requests sent by on-chip peripheral I/O.

(13) Real-time output (RTP)

The RTP is a real-time output function that transfers previously set 8-bit data to an output latch when an external trigger signal occurs or when a match signal of timer's compare register occurs. RTP can also output an 8-bit data in 4-bit × 2-channel format.

(14) Ports

As shown below, following ports have general port functions and control pin functions.

Table 2-1. Port

Port	I/O	Port Function	Control Function
P0	8-bit I/O	General port	NMI, external interrupt, A/D converter trigger, RTP trigger
P1	6-bit I/O		Serial interface
P2	8-bit I/O		Serial interface, timer I/O
P3	8-bit I/O		Timer I/O, external address bus
P4	8-bit I/O		External address/data bus
P5			
P6	6-bit I/O		External address bus
P7	8-bit input		A/D converter analog input
P8	4-bit input		
P9	7-bit I/O		External bus interface control signal I/O
P10	8-bit I/O		Real-time output port, external address bus
P11	4-bit I/O, 1-bit input		External address bus, subsystem clock input
P12	1-bit I/O		Wait control

3. CPU FUNCTIONS

The CPU of the μPD703015 is based on the RISC architecture and executes most instructions in one clock cycle by using a 5-stage pipeline.

The followings show the characteristics of the CPU functions.

- Minimum instruction execution time: 58 ns (@ 17-MHz operation)
- Address space: 4-Mbyte linear
- Thirty-two 32-bit general registers
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- 1-clock 32-bit shift instruction
- Load/store instruction with long/short format
- Internal memory
  - Mask ROM: 128 Kbytes
  - RAM: 4 Kbytes
- Four types of bit manipulation instructions
  - Set
  - Clear
  - Not
  - Test

4. BUS CONTROL FUNCTION

The followings show the characteristics of the bus control function.

- Address bus (capable of separate output)
- 16-bit data bus
- Capable of connection with external devices via the pins that have alternate functions as ports
- WAIT function
  - Programmable wait function, capable of inserting up to three wait states per two blocks
  - External wait function with $\overline{\text{WAIT}}$ pin signal
- Idle state insertion function
- Bus mastership arbitration function
- Bus hold function

5. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The followings show the characteristics of the interrupt/exception processing function.

- Interrupt
  - Non-maskable interrupt: 2 sources
  - Maskable interrupt: 30 sources
  - 8-level programmable priority
  - Mask specification for the interrupt request according to priority
  - Mask specification for each maskable interrupt request
  - Noise elimination, edge detection, and valid edge specification of an external interrupt request
- Exception
  - Software exception: 32 sources
  - Exception trap: 1 source (illegal op code exception)

Table 5-1 shows the interrupt/exception sources.

Table 5-1. Interrupt Source List (1/2)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	Reset input	–	0000H	00000000H	Undefined	–
Non-maskable	Interrupt	–	NMI	NMI pin input	–	0010H	00000010H	nextPC	–
	Interrupt	–	INTWDT	WDTOVF non-maskable	WDT	0020H	00000020H	nextPC	–
Software exception	Exception	–	TRAP0n	TRAP instruction	–	004nH[Note]	0000004nH	nextPC	–
	Exception	–	TRAP1n	TRAP instruction	–	005nH[Note]	0000005nH	nextPC	–
Exception trap	Exception	–	ILGOP	Illegal instruction code	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM	WDTOVF maskable	WDT	0080H	00000080H	nextPC	WDTIC
		1	INTP0	INTP0 pin	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTWTI	Watch timer prescaler	WT	0100H	00000100H	nextPC	WTIIC
		9	INTTM00	INTTM00	TM0	0110H	00000110H	nextPC	TMIC00
		10	INTTM01	INTTM01	TM0	0120H	00000120H	nextPC	TMIC01
		11	INTTM10	INTTM10	TM1	0130H	00000130H	nextPC	TMIC10
		12	INTTM11	INTTM11	TM1	0140H	00000140H	nextPC	TMIC11
		13	INTTM2	TM2 compare match/ OVF	TM2	0150H	00000150H	nextPC	TMIC2
		14	INTTM3	TM3 compare match/ OVF	TM3	0160H	00000160H	nextPC	TMIC3
		15	INTTM4	TM4 compare match/ OVF	TM4	0170H	00000170H	nextPC	TMIC4
		16	INTTM5	TM5 compare match/ OVF	TM5	0180H	00000180H	nextPC	TMIC5
		17	INTCSI0	CSI0 transmit end	CSI0	0190H	00000190H	nextPC	CSIC0
		18	INTSER0	UART0 serial error	UART0	01A0H	000001A0H	nextPC	SERIC0
		19	INTSR0/ INTCSI1	UART0 receiving end/CSI1 transmit end	UART0/ CSI1	01B0H	000001B0H	nextPC	CSIC1
		20	INTST0	UART0 transmit end	UART0	01C0H	000001C0H	nextPC	STIC0
		21	INTCSI2	CSI2 transmit end	CSI2	01D0H	000001D0H	nextPC	CSIC2
		22	INTSER1	UART1 serial error	UART1	01E0H	000001E0H	nextPC	SERIC1

Table 5-1. Interrupt Source List (2/2)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	23	INTSR1	UART1 receiving end	UART1	01F0H	000001F0H	nextPC	SRIC1
		24	INTST1	UART1 transmit end	UART1	0200H	00000200H	nextPC	STIC1
		25	INTAD	A/D conversion end	A/D	0210H	00000210H	nextPC	ADIC
		26	INTDMA0	DMA0 transfer end	DMA0	0220H	00000220H	nextPC	DMAIC0
		27	INTDMA1	DMA1 transfer end	DMA1	0230H	00000230H	nextPC	DMAIC1
		28	INTDMA2	DMA2 transfer end	DMA2	0240H	00000240H	nextPC	DMAIC2
		29	INTWT	Watch timer OVF	WT	0250H	00000250H	nextPC	WTIC

Note n: value of 0 to FH

Remarks 1. Default Priority: Priority that takes precedence when two or more maskable interrupt requests occur at the same time. The highest priority is 0.

Restored PC: The value of the restored PC saved to EIPC or FEPC when interrupt/exception processing is started. However, the value of the PC saved when an interrupt is granted during the DIVH (division) instruction execution is the value of the PC of the current instruction (DIVH).

2. The execution address of the illegal instruction when an illegal op code exception occurs is calculated with (Restored PC – 4).

3. Restored PC of the interrupt/exception other than $\overline{\text{RESET}}$ is the value of the PC (when an event occurred) + 1.

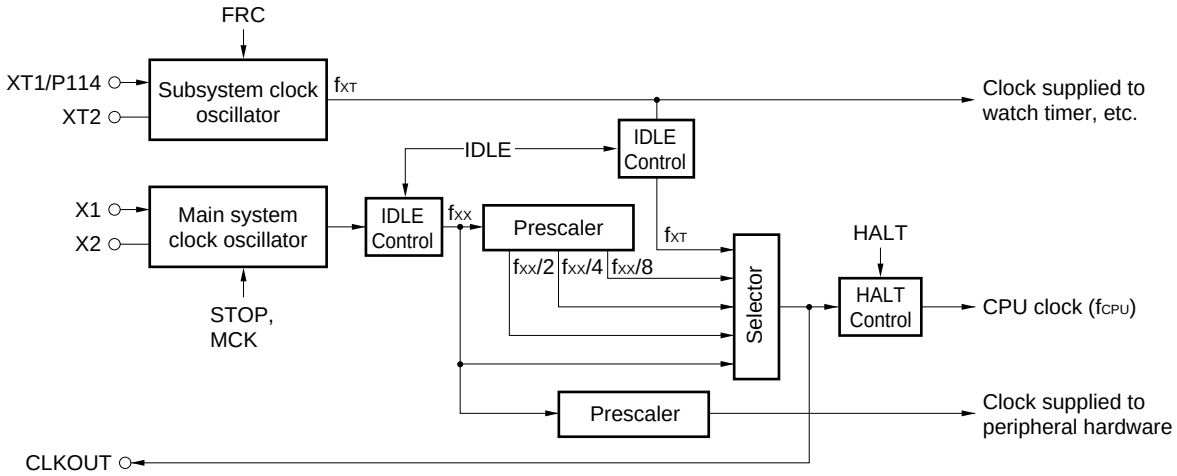
4. Non-maskable interrupt (INTWDT) and maskable interrupt (INTWDTM) are set by the WDTM4 bit of the watchdog timer mode register (WDTM).

6. CLOCK GENERATION FUNCTION

The followings show the characteristics of the clock generation function.

- Clock division function (capable of selecting CPU operation clock)
- CPU operation with subsystem clock is available
- Power saving mode
  - HALT mode
  - IDLE mode
  - Software STOP mode

The following figure shows the configuration of the clock generation function.



Remark f_{XX}: Main system clock frequency
f_{XT}: Subsystem clock frequency

7. TIMER/COUNTER FUNCTION

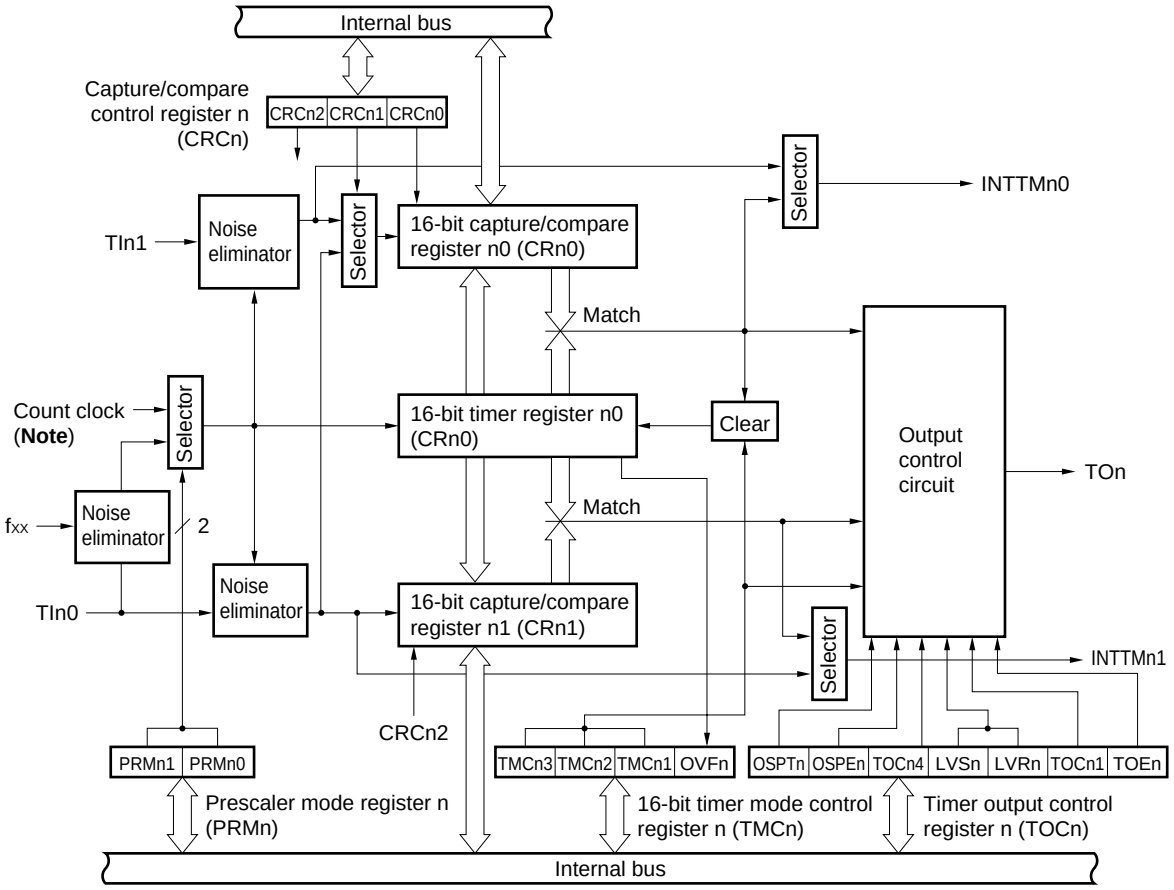
The followings show the characteristics of the timer/counter function.

- 16-bit timers (TM0 and TM1)
  - Interval timer
  - PPG output
  - Pulse width measurement
  - External event counter
  - Square wave output
  - One-shot pulse output
  - 16-bit capture/compare register: 2/each (CRn0 and CRn1)
  - Independent capture/trigger input: 2/each (TIn0 and TIn1)
  - Capable of outputting capture/match interrupt request signal (INTTMn0 and INTTMn1)
  - Event input (alternate function of TIn0) via the digital noise elimination circuit, capable of specifying its valid edge
  - Timer output that starts operation at match detection: 1/each (TO0 and TO1)

- 8-bit timers (TM2 to TM5)
  - Individual mode (mode using a timer alone)
    Interval timer
    External even counter
    Square wave output
    PWM output
  - Cascade connection mode (mode using the cascade connection: 16-bit resolution)
    16-bit resolution interval timer
    16-bit resolution external event counter
    16-bit resolution square wave output

The following figure shows the configuration of the timer/counter function.

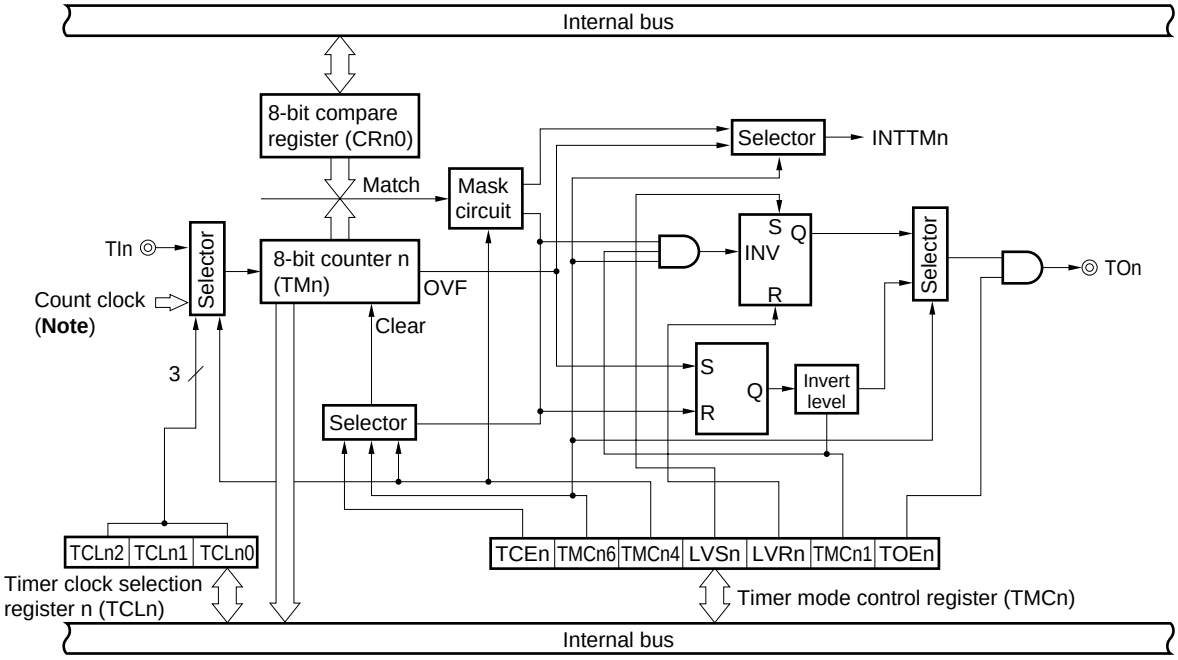
(1) TM0 and TM1



Note Count clock is selected by setting the PRMn register.

Remark n = 0, 1

(2) TM2 to TM5



Note Count clock is selected by setting the TCLn register.

Remarks 1. ——◎ indicates a signal that can be directly connected to a port.

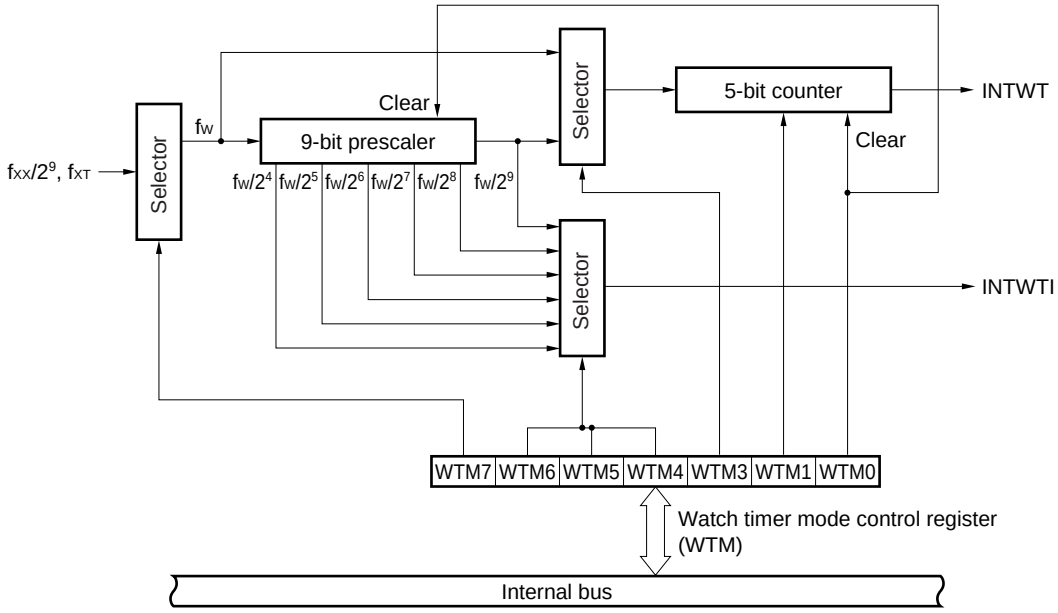
2. n = 2 to 5

8. WATCH TIMER FUNCTION

The watch timer has the following functions.

- Watch timer
- Interval timer

The following figure shows the configuration of the watch timer function.



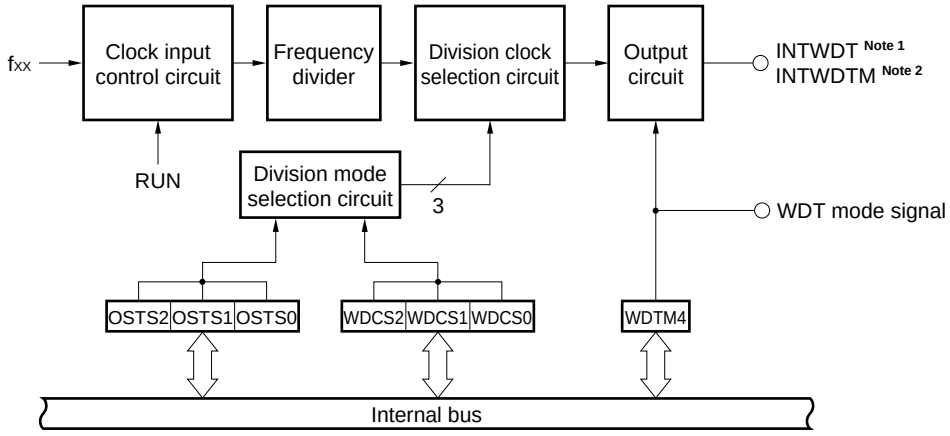
Remark f_{XX}: Main system clock frequency
f_{XT}: Subsystem clock frequency
f_W: Watch timer clock frequency

9. WATCHDOG TIMER FUNCTION

The watchdog timer has the following functions.

- Watchdog timer
- Interval timer
- Selection of oscillation stabilization time

The following figure shows the configuration of the watchdog timer function



Notes 1. In watchdog timer mode
2. In interval timer mode

Remark fxx: Main system clock frequency

10. SERIAL INTERFACE FUNCTION

10.1 Serial Interfaces

The μPD703015 supports the following four independent serial interfaces.

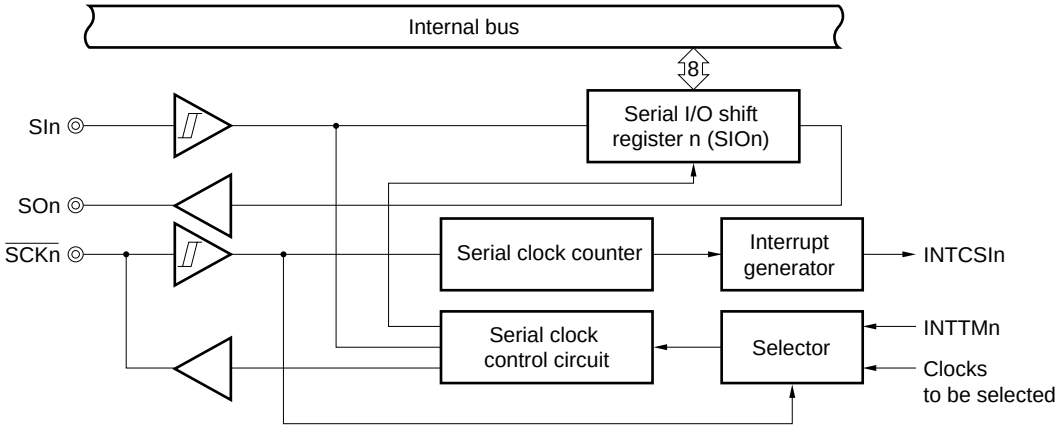
- Channel 0: 3-wire serial I/O (CSI0)
- Channel 1: 3-wire serial I/O (CSI1)/Asynchronous serial interface (UART0)
- Channel 2: 3-wire serial I/O (CSI2)
- Channel 3: Asynchronous serial interface (UART1)

10.2 3-wire Serial I/O (CSI0 to CSI2)

The followings show the characteristics of the 3-wire serial I/O (CSI0 to CSI2).

- Two types of modes
  - Operation stop mode (used when serial transfers are not performed)
  - 3-wire serial I/O mode (MSB-first fixed)
- Number of channels: 3 (CSI0 to CSI2)
- Using 3 types of pins
  - SO0 to SO2: Serial data output pins
  - SI0 to SI2: Serial data input pins
  - $\overline{SCK0}$ to $\overline{SCK2}$: Serial clock I/O pins
- 3 interrupt sources
  - Interrupt request signals (INTCSI0 to INTCSI2)

The following figure shows the configuration of the 3-wire serial I/O (CSI0 to CSI2).



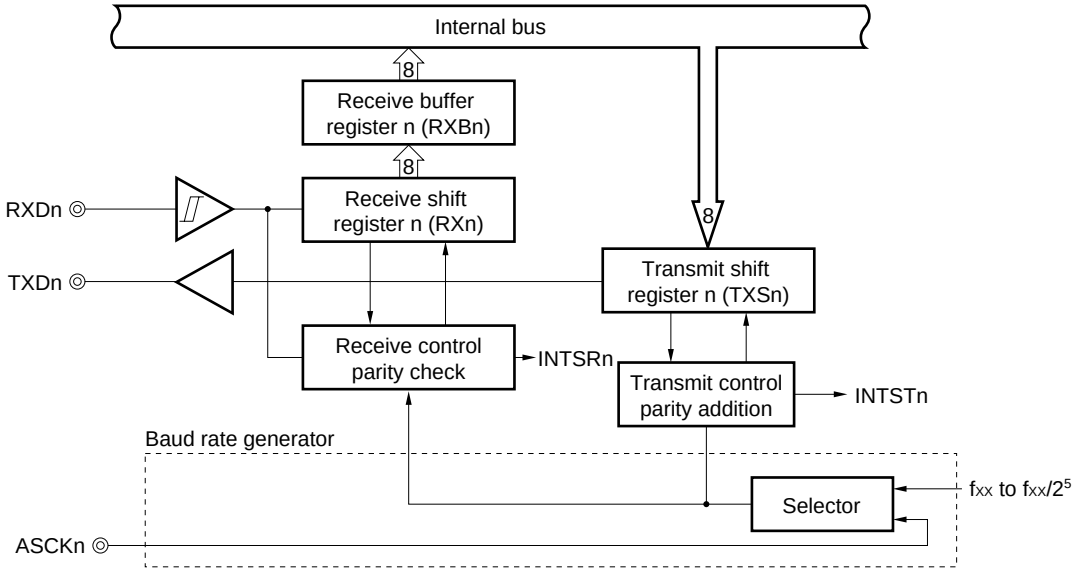
Remark n = 0 to 2

10.3 Asynchronous Serial Interface (UART0 and UART1)

The followings show the characteristics of the asynchronous serial interface (UART0 and UART1).

- Two types of modes
  - Operation stop mode (used when serial transfers are not performed to enable power consumption reduced)
  - Asynchronous serial interface mode
- Full-duplex transmission
- 2-pin configuration
  - TXD0 and TXD1: Transmit data output pins
  - RXD0 and RXD1: Receive data input pins
- 3 types of interrupt sources
  - Receive error interrupt (INTSER0 and INTSER1)
  - Receive end interrupt (INTSR0 and INTSR1)
  - Transmit end interrupt (INTST0 and INTST1)
- Character length: 7 bits/8bits
- Parity function: odd, even, 0, none
- Transmission stop bit: 1 bit/2bits
- On-chip baud rate generator

The following figure shows the configuration of the asynchronous serial interface (UART0 and UART1).



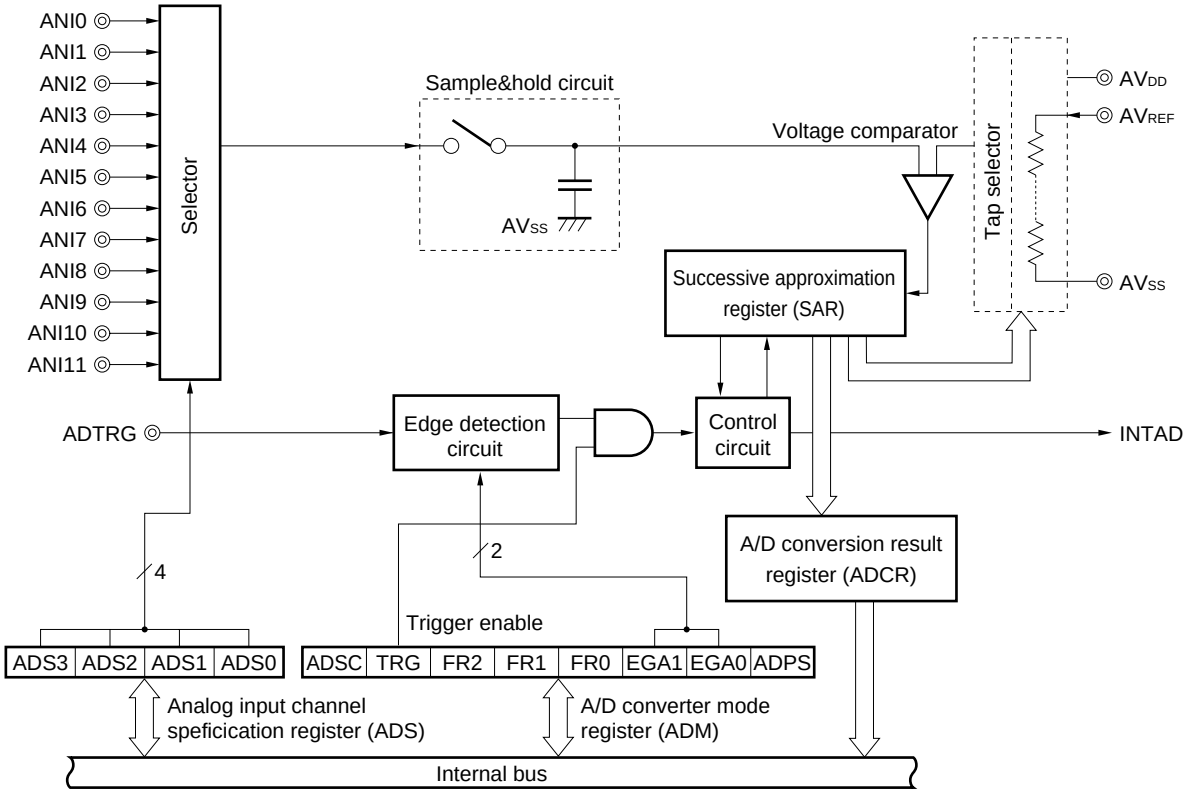
Remark n = 0 or 1

11. A/D CONVERTER

The followings show the characteristics of the A/D converter.

- Analog input: 12 channels
- On-chip 10-bit A/D converter
- On-chip A/D conversion result register (ADCR)
  On-chip A/D conversion result register H (ADCRH) (only higher 8 bits can be read)
- Start of A/D conversion
  - Hardware start: A/D conversion starts by trigger input (ADTRG)
  - Software start: A/D conversion starts by setting A/D converter mode register (ADM)
- Successive approximation method

The following figure shows the configuration of the A/D converter.



12. DMA FUNCTION

The followings show the characteristics of the DMA functions.

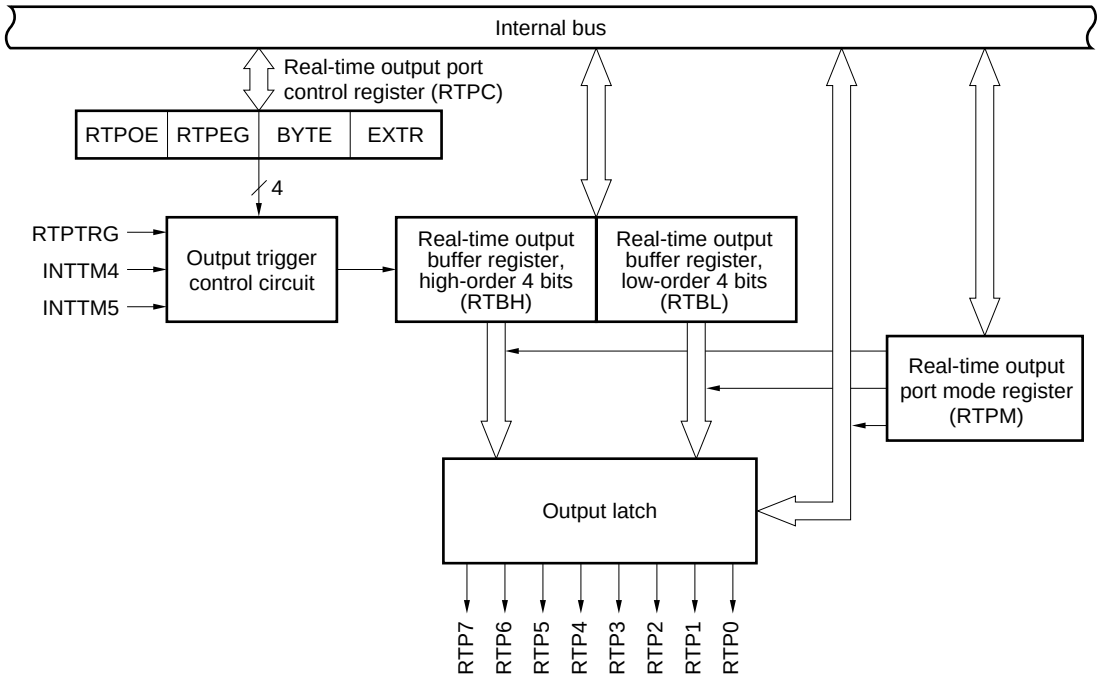
- DMA channel: 3 channels (between internal RAM and on-chip peripheral I/O)
- Data can be transferred in 8-bit/16-bit units
- Maximum number of transfer: 256
- Priority levels of the DMA channels
  DMA0 > DMA1 > DMA2

13. REAL-TIME OUTPUT FUNCTION (RTO)

The followings show the characteristics of the real-time output function.

- Capable of specifying port mode/real-time output port mode in 1-bit units
- Real-time output port operation mode
  4 bits × 2 channels
  8 bits × 1 channel

The following figure shows the configuration of the real-time output function (RTO).



14. PORT FUNCTION

The followings show the characteristics of the port function.

- Number of ports
  Input only port: 13
  I/O port: 72
- Shares pins with other peripheral function I/O
- Input/output can be specified in 1-bit units
- Noise elimination
- Edge detection

15. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, a system reset is performed and the various on-chip hardware devices are reset to their initial state.

When the $\overline{\text{RESET}}$ pin goes from low to high, the reset status is canceled and the CPU resumes program execution. The contents of the various registers should be initialized within the program as necessary.

For the $\overline{\text{RESET}}$ pin, the on-chip noise elimination circuit, which uses analog delay to prevent noise-related malfunction, is provided.

16. INSTRUCTION SET

- How to Read Instruction Set List

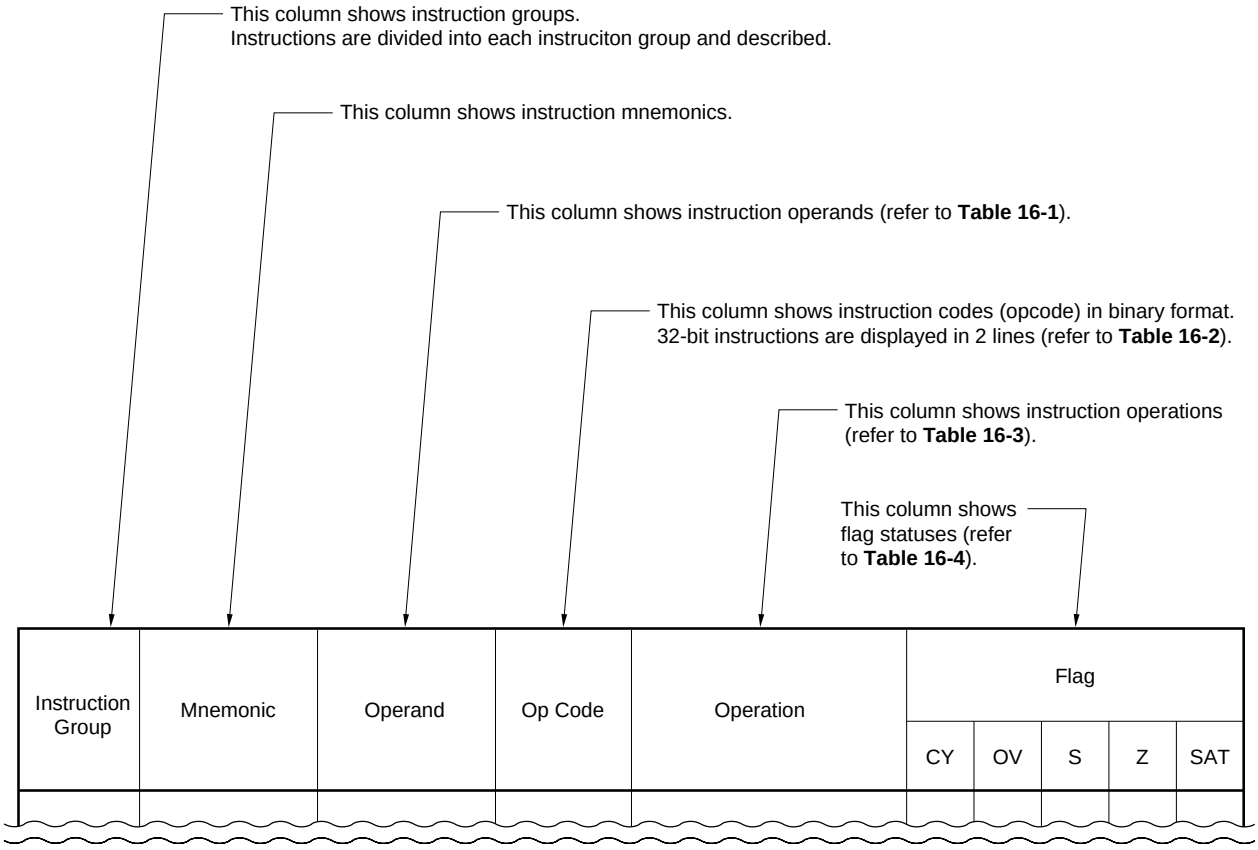


Table 16-1. Symbols in Operand Description

Symbol	Description
reg1	General register (r0 to r31) : Used as source register
reg2	General register (r0 to r31) : Mainly used as destination register
ep	Element pointer (r30)
bit#3	3-bit data for bit number specification
imm×	×-bit immediate data
disp×	×-bit displacement
regID	System register number
vector	5-bit data that specifies trap vector number (00H to 1FH)
cccc	4-bit data that indicates condition code

Table 16-2. Symbols Used for Op Code

Symbol	Description
R	1-bit data of code that specifies reg1 or regID
r	1-bit data of code that specifies reg2
d	1-bit data of displacement
i	1-bit data of immediate data
cccc	4-bit data that indicates condition code
bbb	3-bit data that specifies bit number

Table 16-3. Symbols Used for Operation Description

Symbol	Description
←	Assignment
GR[ ]	General register
SR[ ]	System register
zero-extend (n)	Zero-extends n to word length.
sign-extend (n)	Sign-extends n to word length.
load-memory (a,b)	Reads data of size b from address a.
store-memory (a,b,c)	Writes data b of size c to address a.
load-memory-bit (a,b)	Reads bit b from address a.
store-memory-bit (a,b,c)	Writes c to bit b of address a
saturated (n)	Performs saturated processing of n. (n is 2's complements). Result of calculation of n: If n is n ≥ 7FFFFFFFH as result of calculation, 7FFFFFFFH. If n is n ≤ 80000000H as result of calculation, 80000000H.
result	Reflects result to a flag.
Byte	Byte (8 bits)
Halfword	Half-word (16 bits)
Word	Word (32 bits)
+	Add
–	Subtract
||	Bit concatenation
×	Multiply
÷	Divide
AND	Logical product
OR	Logical sum
XOR	Exclusive logical sum
NOT	Logical negate
logically shift left by	Logical left shift
logically shift right by	Logical right shift
arithmetically shift right by	Arithmetic right shift

Table 16-4. Symbols Used for Flag Operation

Symbol	Description
(blank)	Not affected
0	Cleared to 0
×	Set of cleared according to result
R	Previously saved value is restored

Table 16-5. Condition Codes

Condition Name (cond)	Condition Code (cccc)	Conditional Expression	Description
V	0000	OV = 1	Overflow
NV	1000	OV = 0	No overflow
C/L	0001	CY = 1	Carry Lower (Less than)
NC/NL	1001	CY = 0	No carry No lower (Greater than or equal)
Z/E	0010	Z = 1	Zero Equal
NZ/NE	1010	Z = 0	Not zero Not equal
NH	0011	(CY OR Z) = 1	Not higher (Less than or equal)
H	1011	(CY OR Z) = 0	Higher (Greater than)
N	0100	S = 1	Negative
P	1100	S = 0	Positive
T	0101	–	Always (unconditional)
SA	1101	SAT = 1	Saturated
LT	0110	(S XOR OV) = 1	Less than signed
GE	1110	(S XOR OV) = 0	Greater than or equal signed
LE	0111	((S XOR OV) OR Z) = 1	Less than or equal signed
GT	1111	((S XOR OV) OR Z) = 0	Greater than signed

Instruction Set List (1/4)

Instruction Group	Mnemonic	Operand	Op Code	Operation	Flag				
					CY	OV	S	Z	SAT
Load/Store	SLD.B	disp7 [ep], reg2	rrrrr0110ddddddd	adr ← ep + zero-extend (disp7) GR [reg2] ← sign-extend (Load-memory (adr, Byte))					
	SLD.H	disp8 [ep], reg2	rrrrr1000ddddddd (**Note 1**)	adr ← ep + zero-extend (disp8) GR [reg2] ← sign-extend (Load-memory (adr, Halfword))					
	SLD.W	disp8 [ep], reg2	rrrrr1010ddddddd0 (**Note 2**)	adr ← ep + zero-extend (disp8) GR [reg2] ← Load-memory (adr, Word)					
	LD.B	disp16 [reg1], reg2	rrrrr111000RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) GR [reg2] ← sign-extend (Load-memory (adr, Byte))					
	LD.H	disp16 [reg1], reg2	rrrrr111001RRRRR ddddddddddddddd0 (**Note 3**)	adr ← GR [reg1] + sign-extend (disp16) GR [reg2] ← sign-extend (Load-memory (adr, Halfword))					
	LD.W	disp16 [reg1], reg2	rrrrr111001RRRRR ddddddddddddddd1 (**Note 3**)	adr ← GR [reg1] + sign-extend (disp16) GR [reg2] ← Load-memory (adr, Word))					
	SST.B	reg2, disp7 [ep]	rrrrr0111ddddddd	adr ← ep + zero-extend (disp7) Store-memory (adr, GR [reg2], Byte)					
	SST.H	reg2, disp8 [ep]	rrrrr1001ddddddd (**Note 1**)	adr ← ep + zero-extend (disp8) Store-memory (adr, GR [reg2], Halfword)					
	SST.W	reg2, disp8 [ep]	rrrrr1010ddddddd1 (**Note 2**)	adr ← ep + zero-extend (disp8) Store-memory (adr, GR [reg2], Word)					
	ST.B	reg2, disp16 [reg1]	rrrrr111010RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) Store-memory (adr, GR [reg2], Byte)					
	ST.H	reg2, disp16 [reg1]	rrrrr111011RRRRR ddddddddddddddd0 (**Note 3**)	adr ← GR [reg1] + sign-extend (disp16) Store-memory (adr, GR [reg2], Halfword)					
	ST.W	reg2, disp16 [reg1]	rrrrr111011RRRRR ddddddddddddddd1 (**Note 3**)	adr ← GR [reg1] + sign-extend (disp16) Store-memory (adr, GR [reg2], Word)					
Arithmetic Operation	MOV	reg1, reg2	rrrrr000000RRRRR	GR [reg2] ← GR [reg1]					
	MOV	imm5, reg2	rrrrr010000iiiii	GR [reg2] ← sign-extend (imm5)					
	MOVHI	imm16, reg1, reg2	rrrrr110010RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] + (imm16 || 0^{16})					
	MOVEA	imm16, reg1, reg2	rrrrr110001RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] + sign-extend (imm16)					

Notes 1. dddddddd is the higher 7 bits of disp8.

2. dddddd is the higher 6 bits of disp8.

3. ddddddddddddddd is the higher 15 bits of disp16.

Instruction Set List (2/4)

Instruction Group	Mnemonic	Operand	Op Code	Operation	Flag				
					CY	OV	S	Z	SAT
Arithmetic Operation	ADD	reg1, reg2	rrrrr001110RRRRR	GR [reg2] ← GR [reg2] + GR [reg1]	×	×	×	×	
	ADD	imm5, reg2	rrrrr010010iiiii	GR [reg2] ← GR [reg2] + sign-extend (imm5)	×	×	×	×	
	ADDI	imm16, reg1, reg2	rrrrr110000RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] + sign-extend (imm16)	×	×	×	×	
	SUB	reg1, reg2	rrrrr001101RRRRR	GR [reg2] ← GR [reg2] – GR [reg1]	×	×	×	×	
	SUBR	reg1, reg2	rrrrr001100RRRRR	GR [reg2] ← GR [reg1] – GR [reg2]	×	×	×	×	
	MULH	reg1,reg2	rrrrr000111RRRRR	GR [reg2] ← GR [reg2] Note × GR [reg1] Note (Signed multiplication)					
	MULH	imm5, reg2	rrrrr010111iiiii	GR [reg2] ← GR [reg2] Note × sign-extend (imm5) (Signed multiplication)					
	MULHI	imm16, reg1, reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] Note × imm16 (Signed multiplication)					
	DIVH	reg1, reg2	rrrrr000010RRRRR	GR [reg2] ← GR [reg2] ÷ GR [reg2] Note (Signed division)		×	×	×	
	CMP	reg1, reg2	rrrrr001111RRRRR	result ← GR [reg2] – GR [reg1]	×	×	×	×	
	CMP	imm5, reg2	rrrrr010011iiiii	result ← GR [reg2] – sign-extend (imm5)	×	×	×	×	
	SETF	cccc, reg2	rrrrr1111110cccc 0000000000000000	if conditions are satisfied then GR [reg2] ← 00000001H else GR [reg2] ← 00000000H					
Saturated Operation	SATADD	reg1, reg2	rrrrr000110RRRRR	GR [reg2] ← saturated (GR [reg2] + GR [reg1])	×	×	×	×	×
	SATADD	imm5, reg2	rrrrr010001iiiii	GR [reg2] ← saturated (GR [reg2] + sign-extend (imm5))	×	×	×	×	×
	SATSUB	reg1, reg2	rrrrr000101RRRRR	GR [reg2] ← saturated (GR [reg2] – GR [reg1])	×	×	×	×	×
	SATSUBI	imm16, reg1, reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← saturated (GR [reg1] – sign-extend (imm16))	×	×	×	×	×
	SATSUBR	reg1, reg2	rrrrr000100RRRRR	GR [reg2] ← saturated (GR [reg1] – GR [reg2])	×	×	×	×	×
Logic Operation	TST	reg1, reg2	rrrrr001011RRRRR	result ← GR [reg2] AND GR [reg1]		0	×	×	
	OR	reg1, reg2	rrrrr001000RRRRR	GR [reg2] ← GR [reg2] OR GR [reg1]		0	×	×	
	ORI	imm16, reg1, reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] OR zero-extend (imm16)		0	×	×	
	AND	reg1, reg2	rrrrr001010RRRRR	GR [reg2] ← GR [reg2] AND GR [reg1]		0	×	×	
	ANDI	imm16, reg1, reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] AND zero-extend (imm16)		0	0	×	

Note Only the lower half-word data is valid.

Instruction Set List (3/4)

Instruction Group	Mnemonic	Operand	Op Code	Operation	Flag				
					CY	OV	S	Z	SAT
Logic Operation	XOR	reg1, reg2	rrrrr001001RRRRR	GR [reg2] ← GR [reg2] XOR GR [reg1]		0	×	×	
	XORI	imm16, reg1, reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR [reg2] ← GR [reg1] XOR zero-extend (imm16)		0	×	×	
	NOT	reg1, reg2	rrrrr000001RRRRR	GR [reg2] ← NOT (GR [reg1])		0	×	×	
	SHL	reg1, reg2	rrrrr111111RRRRR 0000000011000000	GR [reg2] ← GR [reg2] logically shift left by GR [reg1])	×	0	×	×	
	SHL	imm5, reg2	rrrrr010110iiiii	GR [reg2] ← GR [reg2] logically shift left by zero-extend (imm5)	×	0	×	×	
	SHR	reg1, reg2	rrrrr1111111cccc 0000000010000000	GR [reg2] ← GR [reg2] logically shift right by GR [reg1]	×	0	×	×	
	SHR	imm5, reg2	rrrrr010100iiiii	GR [reg2] ← GR [reg2] logically shift right by zero-extend (imm5)	×	0	×	×	
	SAR	reg1, reg2	rrrrr111111RRRRR 0000000010100000	GR [reg2] ← GR [reg2] arithmetically shift right by GR [reg1]	×	0	×	×	
	SAR	imm5, reg2	rrrrr010101iiiii	GR [reg2] ← GR [reg2] arithmetically shift right by zero-extend (imm5)	×	0	×	×	
Jump	JMP	[reg1]	00000000011RRRRR	PC ← GR [reg1]					
	JR	disp22	0000011110dddddd dddddddddddddddd0 (**Note 1**)	PC ← PC + sign-extend (disp22)					
	JARL	disp22, reg2	rrrrr11110dddddd dddddddddddddddd0 (**Note 1**)	GR [reg2] ← PC + 4 PC ← PC + sign-extend (disp22)					
	Bcond	disp9	ddddd1011dddcccc (**Note 2**)	if conditions are satisfied then PC ← PC + sign-extend (disp9)					
Bit Manipulate	SET1	bit#3, disp16 [reg1]	00bbb111110RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3) Store memory-bit (adr, bit#3, 1)				×	
	CLR1	bit#3, disp16 [reg1]	10bbb111110RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store memory-bit (adr, bit#3, 0)				×	
	NOT1	bit#3, disp16 [reg1]	01bbb111110RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, Z flag)				×	
	TST1	bit#3, disp16 [reg1]	11bbb111110RRRRR dddddddddddddddd	adr ← GR [reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3))				×	

Notes 1. ddddddddddddddddddddd is the higher 21 bits of dip22.

2. dddddddd is the higher 8 bits of disp9.

Instruction Set List (4/4)

Instruction Group	Mnemonic	Operand	Op Code	Operation		Flag				
						CY	OV	S	Z	SAT
Special	LDSR	reg2, regID	rrrrr111111RRRRR 0000000000100000 (**Note**)	SR [regID] ←GR [reg2]	regID = EIPC, FEPC					
					regID = EIPSW, FEPSW					
					regID = PSW	×	×	×	×	×
	STSR	regID, reg2	rrrrr111111RRRRR 0000000001000000	GR [reg2] ← SR [regID]						
	TRAP	vector	00000111111iiiii 0000000100000000	EIPC ← PC + 4 (Restored PC) EIPSW ← PSW ECR.EICC ← Interrupt code PSW.EP ← 1 PSW.ID ← 1 PC ← 00000040H (vector = 00H to 0FH) 00000050H (vector = 10H to 1FH)						
	RETI		0000011111100000 0000000101000000	if PSW.EP = 1 then PC ← EIPC PSW ← EIPSW else if PSW.NP = 1 then PC ← FEPC PSW ← FEPSW else PC ← EIPC PSW ← EIPSW		R	R	R	R	R
	HALT		0000011111100000 0000000100100000	Stops						
	DI		0000011111100000 0000000101100000	PSW.ID ← 1 (Maskable interrupt disabled)						
	EI		1000011111100000 0000000101100000	PSW.ID ← 0 (Maskable interrupt enabled)						
	NOP		0000000000000000	Uses 1 clock cycle without doing anything						

Note The op code of this instruction uses the field of reg1 through the source register is shown as reg2 in the above table. Therefore, the meaning of register specification for mnemonic description and op code is different from that of the other instructions.

rrr = regID specification

RRRRR = reg2 specification

17. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
	AV_{DD}		–0.5 to +4.6	V
	BV_{DD}		–0.5 to +4.6	V
	V_{SS}		–0.5 to +0.5	V
	AV_{SS}		–0.5 to +0.5	V
	BV_{SS}		–0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 and XT1 pins, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 0.5	V
	V_{I2}	X1, XT1, V_{DD} = 2.7 to 3.6	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 2.7 to 3.6	–0.5 to V_{DD} + 0.5	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect to each other output pins (or I/O pins) of IC products, and do not connect them directly to V_{DD}, V_{CC}, or GND. However, open-drain pins and open-collector pins can be directly connected to each other. Moreover, external circuits that implement a timing that avoids conflict with the output of pins that go into high-impedance can be directly connected.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

OPERATING CONDITIONS

Internal operation clock frequency (ϕ)	Supply voltage (V_{DD}, HV_{DD})	Operating ambient temperature (T_A)
1 MHz ≤ f_{XX} ≤ 13.5 MHz	2.7 to 3.6 V	–40 to +85°C
1 MHz ≤ f_{XX} ≤ 17 MHz	3.0 to 3.6 V	–40 to +85°C
f_{XT} = 32.768 kHz	2.7 to 3.6 V	–40 to +85°C

DC CHARACTERISTICS

(1) Operating Condition (T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	**Note 1**		0.7V_{DD}		V_{DD}	V
	V_{IH3}	**Note 2**		0.75V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1 (P114), XT2		0.75V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than below		0		0.3V_{DD}	V
	V_{IL2}	**Note 1**		0		0.3V_{DD}	V
	V_{IL3}	**Note 2**		0		0.2V_{DD}	V
	V_{IL4}	X1, X2, XT1 (P114), XT2		–0.3		0.2V_{DD}	V
Output voltage, high	V_{OH}	I_{OH} = –3 mA		V_{DD} – 0.6			V
Output voltage, low,	V_{OL}	I_{OL} = 3 mA				0.4	V
Input leak current, high	I_{LIH}	V_I = V_{DD}				5	μA
Input leak current, low	I_{LIL}	V_I = 0 V				–5	μA
Output leak current, high	I_{LOH}	V_O = V_{DD}				5	μA
Output leak current, low	I_{LOL}	V_O = 0 V				–5	μA
Supply current	I_{DD1}	Normal operation	f_{XX} = 13.5 MHz		16	28	mA
	I_{DD2}	HALT mode	f_{XX} = 13.5 MHz		10	18	mA
	I_{DD3}	IDLE mode	f_{XX} = 13.5 MHz		1	9	mA
	I_{DD4}	STOP mode (Subsystem clock stopped)	T_A = –40 to +50°C		1	50	μA
			T_A = –40 to +85°C		1	200	μA
	I_{DD5}	Normal operation	T_A = –40 to +50°C		33	150	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		33	300	μA
	I_{DD6}	HALT mode	T_A = –40 to +50°C		15	95	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		15	245	μA
	I_{DD7}	IDLE mode	T_A = –40 to +50°C		8	74	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		8	224	μA
Pull-up resistance	R_L			10	30	100	kΩ

Notes 1. P70 to P77, P80 to P83, and their alternate-function pins.

2. $\overline{\text{RESET}}$, P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, and their alternate-function pins.

(2) Operating Condition (T_A = –40 to +85°C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Pins other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	**Note 1**		0.7V_{DD}		V_{DD}	V
	V_{IH3}	**Note 2**		0.75V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1 (P114), XT2		0.75V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than below		0		0.3V_{DD}	V
	V_{IL2}	**Note 1**		0		0.3V_{DD}	V
	V_{IL3}	**Note 2**		0		0.2V_{DD}	V
	V_{IL4}	X1, X2, XT1 (P114), XT2		–0.3		0.2V_{DD}	V
Output voltage, high	V_{OH}	I_{OH} = –3 mA		V_{DD} – 0.6			V
Output voltage, low,	V_{OL}	I_{OL} = 3 mA				0.4	V
Input leak current, high	I_{LIH}	V_I = V_{DD}				5	μA
Input leak current, low	I_{LIL}	V_I = 0 V				–5	μA
Output leak current, high	I_{LOH}	V_O = V_{DD}				5	μA
Output leak current, low	I_{LOL}	V_O = 0 V				–5	μA
Supply current	I_{DD1}	Normal operation	f_{XX} = 17 MHz		18	30	mA
	I_{DD2}	HALT mode	f_{XX} = 17 MHz		12	20	mA
	I_{DD3}	IDLE mode	f_{XX} = 17 MHz		1	10	mA
	I_{DD4}	STOP mode (Subsystem clock stopped)	T_A = –40 to +50°C		1	50	μA
			T_A = –40 to +85°C		1	200	μA
	I_{DD5}	Normal operation	T_A = –40 to +50°C		33	150	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		33	300	μA
	I_{DD6}	HALT mode	T_A = –40 to +50°C		15	95	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		15	245	μA
	I_{DD7}	IDLE mode	T_A = –40 to +50°C		8	74	μA
		f_{XT} = 32.768 kHz	T_A = –40 to +85°C		8	224	μA
Pull-up resistance	R_L			10	30	100	kΩ

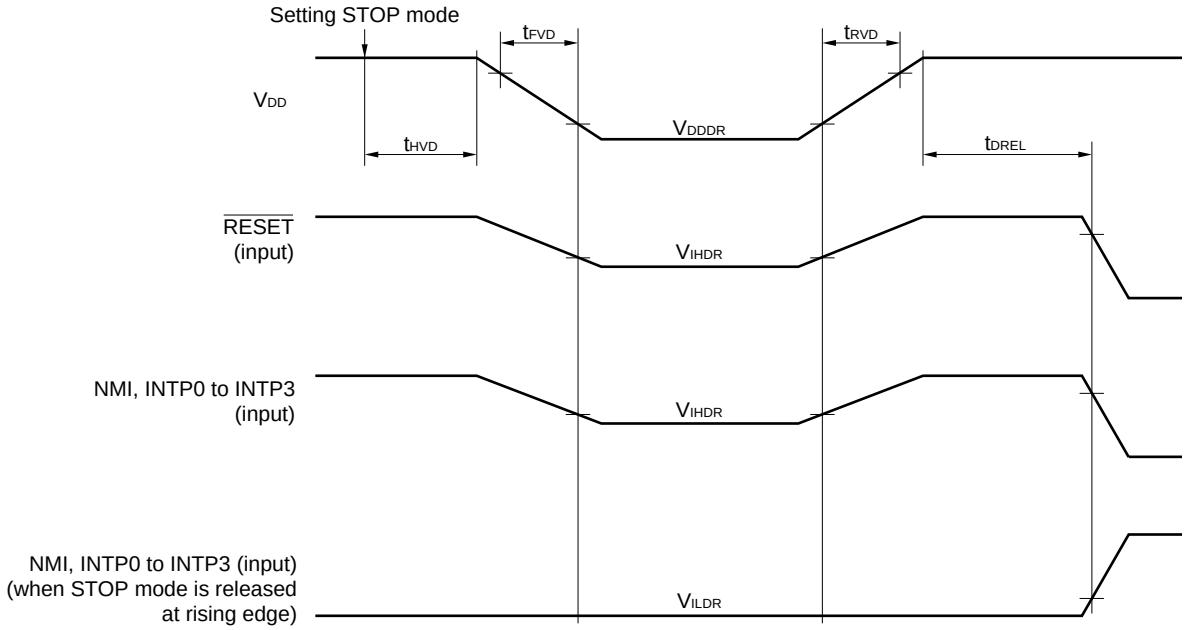
Notes 1. P70 to P77, P80 to P83, and their alternate-function pins.

2. $\overline{\text{RESET}}$, P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, and their alternate-function pins.

DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode		1.5		3.6	V
Data retention current	I_{DDDR}	V_{DDDR} [V]	T_A = 50°C		0.35V_{DDDR}	50	μA
			T_A = 85°C		0.35V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}			0			ms
STOP release signal input time	t_{DREL}			0			ms
Data retention high-level input voltage	V_{IHDR}	All input port		0.9V_{DDDR}		V_{DDDR}	V
Data retention low-level input voltage	V_{ILDR}	All input port		0		0.1V_{DDDR}	V

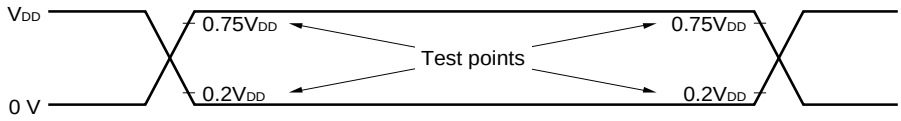
Remark TYP. values are reference values for when T_A = 25°C.



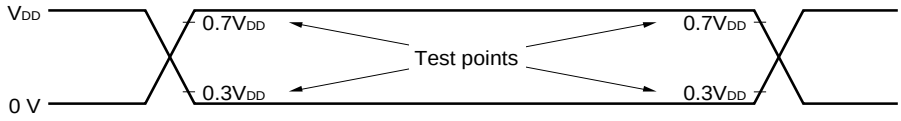
AC CHARACTERISTICS

AC TEST INPUT WAVEFORMS

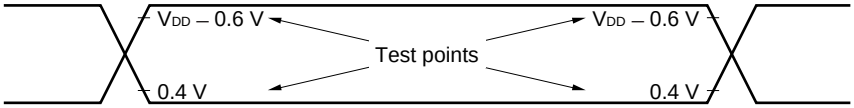
(1) $\overline{\text{RESET}}$, X1, X2, XT1/P114, XT2, P00 to P07, P10, P12, P13, P15, P20, P22, P23, P25 to P27, P30 to P33, P36, P37, and their alternate-function pins



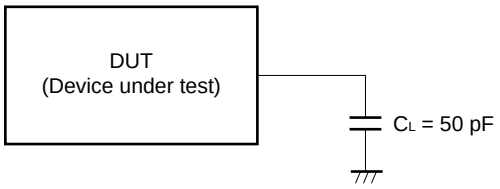
(2) Pins other than (1)



AC TEST OUTPUT TEST POINT



LOAD CONDITIONS



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or some other means.

CLOCK TIMING

(1) Operating Condition (T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		74	1000	ns
XT1 input cycle				28	31	μs
X1 input high-level width	t_{WXH}	<2>		32		ns
XT1 input high-level width				14	15	μs
X1 input low-level width	t_{WXL}	<3>		32		ns
XT1 input low-level width				14	15	μs
X1 input rise time	t_{XR}	<4>			5	ns
X1 input fall time	t_{XF}	<5>			5	ns
CPU operating frequency	ϕ			32 kHz	13.5 MHz	
CLKOUT output cycle	t_{CYK}	<6>		74 ns	31 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.4T – 5		ns
CLKOUT low-level width	t_{WKL}	<8>		0.4T – 5		ns
CLKOUT rise time	t_{KR}	<9>			5	ns
CLKOUT fall time	t_{KF}	<10>			5	ns
X1↓ → CLKOUT delay time	t_{DXK}	<11>		1	30	ns

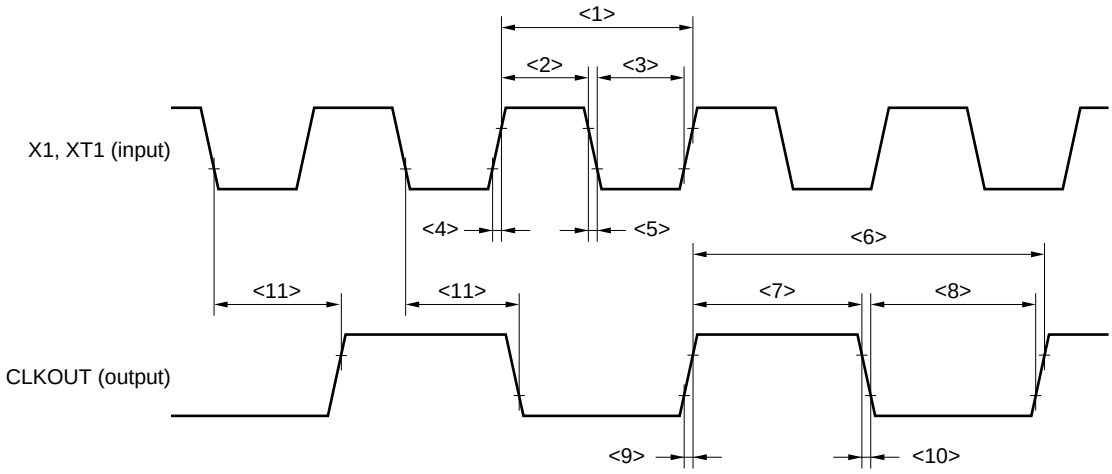
Remark T = t_{CYK}

(2) Operating Condition (T_A = –40 to +85°C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	t_{CYX}	<1>		58	1000	ns
XT1 input cycle				28	31	μs
X1 input high-level width	t_{WXH}	<2>		24		ns
XT1 input high-level width				14	15	μs
X1 input low-level width	t_{WXL}	<3>		24		ns
XT1 input low-level width				14	15	μs
X1 input rise time	t_{XR}	<4>			5	ns
X1 input fall time	t_{XF}	<5>			5	ns
CPU operating frequency	ϕ			32 kHz	17 MHz	
CLKOUT output cycle	t_{CYK}	<6>		58 ns	31 μs	
CLKOUT high-level width	t_{WKH}	<7>		0.4T – 5		ns
CLKOUT low-level width	t_{WKL}	<8>		0.4T – 5		ns
CLKOUT rise time	t_{KR}	<9>			5	ns
CLKOUT fall time	t_{KF}	<10>			5	ns
X1↓ → CLKOUT delay time	t_{DXK}	<11>		1	30	ns

Remark T = t_{CYK}

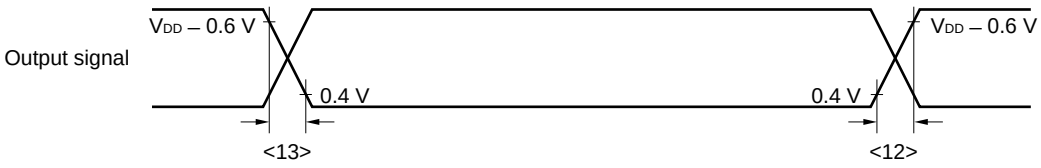
CLOCK TIMING



TIMING OF PINS OTHER THAN X1 AND CLOOUT PINS

(T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	t_{OR}	<12>			15	ns
Output fall time	t_{OF}	<13>			15	ns



BUS TIMING (CLKOUT ASYNCHRONOUS)

(T_A = –40 to +85°C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<14>		0.5T – 15		ns
Address hold time (from ASTB↓)	t_{HSTA}	<15>		0.5T – 15		ns
$\overline{DSTB}$↓ → address float	t_{FDA}	<16>			0	ns
Address → data input setup time	t_{DAID}	<17>			(2 + n)T – 25	ns
$\overline{DSTB}$↓ → data input setup time	t_{DDID}	<18>			(1 + n)T – 25	ns
ASTB↓ → $\overline{DSTB}$↓ delay time	t_{DSTD}	<19>		0.5T – 15		ns
Data input hold time (from $\overline{DSTB}$↓)	t_{HDID}	<20>		0		ns
$\overline{DSTB}$↑ → address output time	t_{DDA}	<21>		(1 + i)T – 15		ns
$\overline{DSTB}$↑ → ASTB↑ delay time	t_{DDST1}	<22>		0.5T – 15		ns
$\overline{DSTB}$↑ → ASTB↓ delay time	t_{DDST2}	<23>		(1.5 + i)T – 15		ns
$\overline{DSTB}$ low-level width	t_{WDL}	<24>		(1 + n)T – 15		ns
ASTB high-level width	t_{WSTH}	<25>		T – 15		ns
$\overline{DSTB}$↓ → data output time	t_{DDOD}	<26>			10	ns
Data output setup time (to $\overline{DSTB}$↑)	t_{SODD}	<27>		(1 + n)T – 20		ns
Data output hold time (from $\overline{DSTB}$↑)	t_{HDOD}	<28>		T – 15		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<29>	n ≥ 1		1.5T – 25	ns
	t_{SAWT2}	<30>	n ≥ 1		(1.5 + n)T – 25	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<31>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<32>	n ≥ 1	(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<33>	n ≥ 1		T – 25	ns
	t_{SSTWT2}	<34>	n ≥ 1		(1 + n)T – 25	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<35>	n ≥ 1	nT		ns
	t_{HSTWT2}	<36>	n ≥ 1	(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<37>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<38>		T – 15		ns
Address float → $\overline{HLDAK}$↓ delay time	t_{DFHA}	<39>		0		ns
$\overline{HLDAK}$↑ → bus output delay time	t_{DHAC}	<40>		0		ns
$\overline{HLDRQ}$↓ → $\overline{HLDAK}$↓ delay time	t_{DHQHA1}	<41>		1.5T	(2n + 7.5)T + 20	ns
$\overline{HLDRQ}$↑ → $\overline{HLDAK}$↑ delay time	t_{DHQHA2}	<42>		0.5T	1.5T + 20	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operation clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
Sampling timing changes when a programmable wait is inserted.

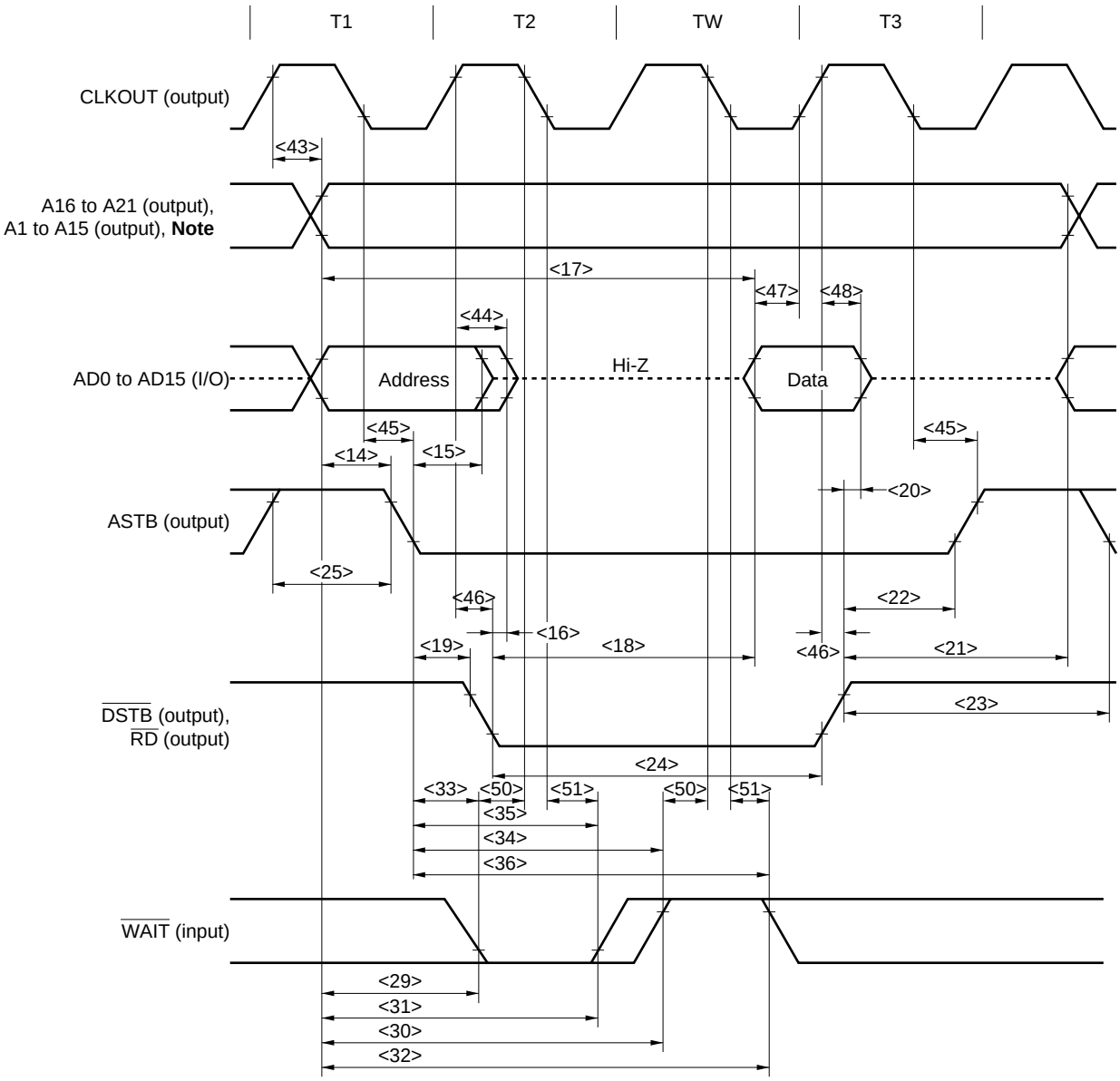
3. i: Number of idle states inserted after the read cycle (0 or 1).

BUS TIMING (CLKOUT SYNCHRONOUS)

(T_A = –40 to +85°C, V_{DD} = BV_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT↑ → address delay time	t_{DKA}	<43>		0	19	ns
CLKOUT↑ → address float delay time	t_{FKA}	<44>		0	22	ns
CLKOUT↓ → ASTB delay time	t_{DKST}	<45>		0	19	ns
CLKOUT↑ → $\overline{\text{DSTB}}$ delay time	t_{DKD}	<46>		0	19	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<47>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<48>		5		ns
CLKOUT↑ → data output delay time	t_{DKOD}	<49>			19	ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	t_{SWTK}	<50>		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	t_{HKWT}	<51>		5		ns
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT↓)	t_{SHQK}	<52>		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↓)	t_{HKHQ}	<53>		5		ns
CLKOUT↑ → $\overline{\text{HLDAK}}$ delay time	t_{DKHA}	<54>			19	ns

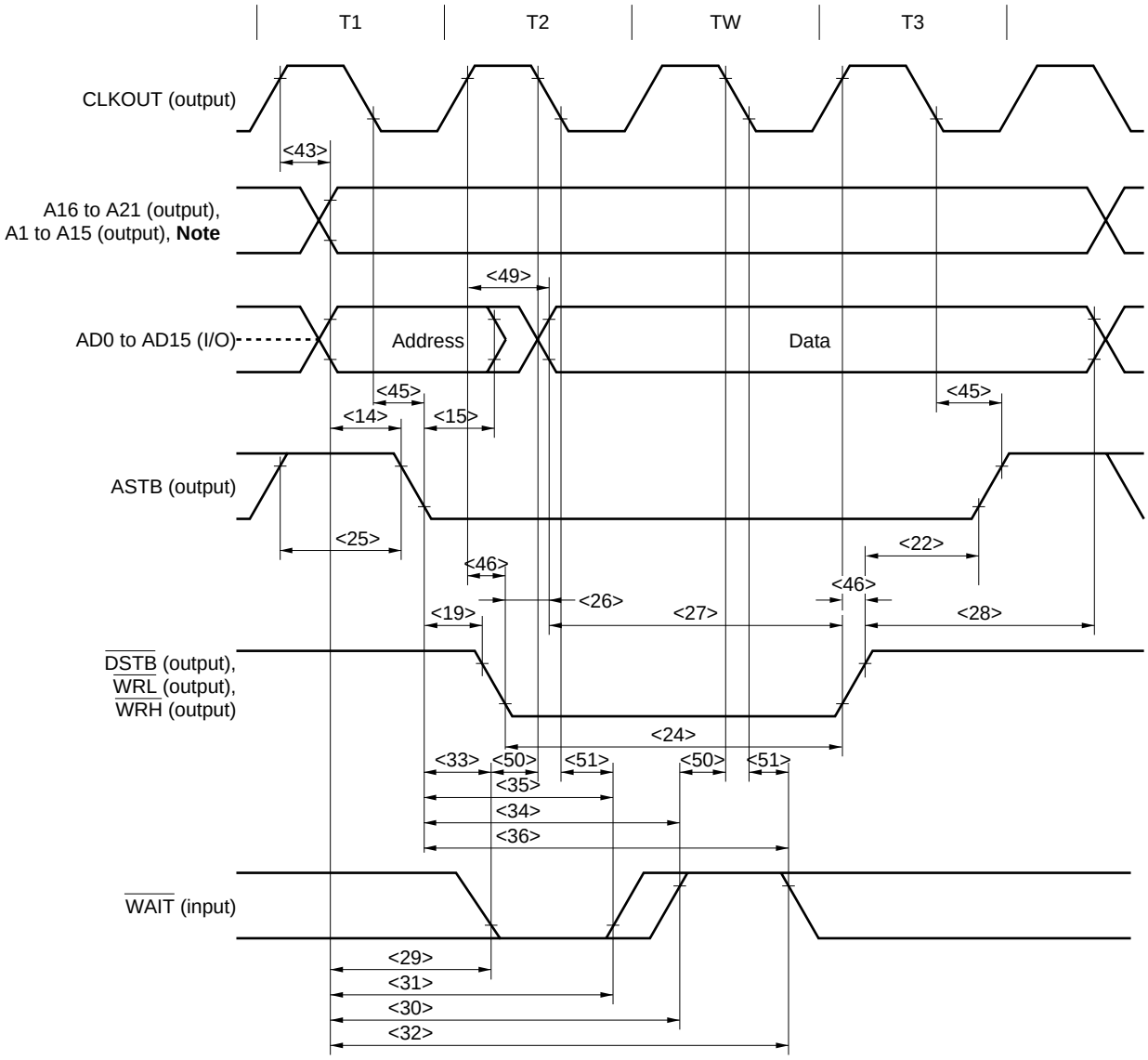
READ CYCLE (CLKOUT SYNCHRONOUS/ASYNCHRONOUS, 1 WAIT)



Note $\overline{\text{R/W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ are high level.

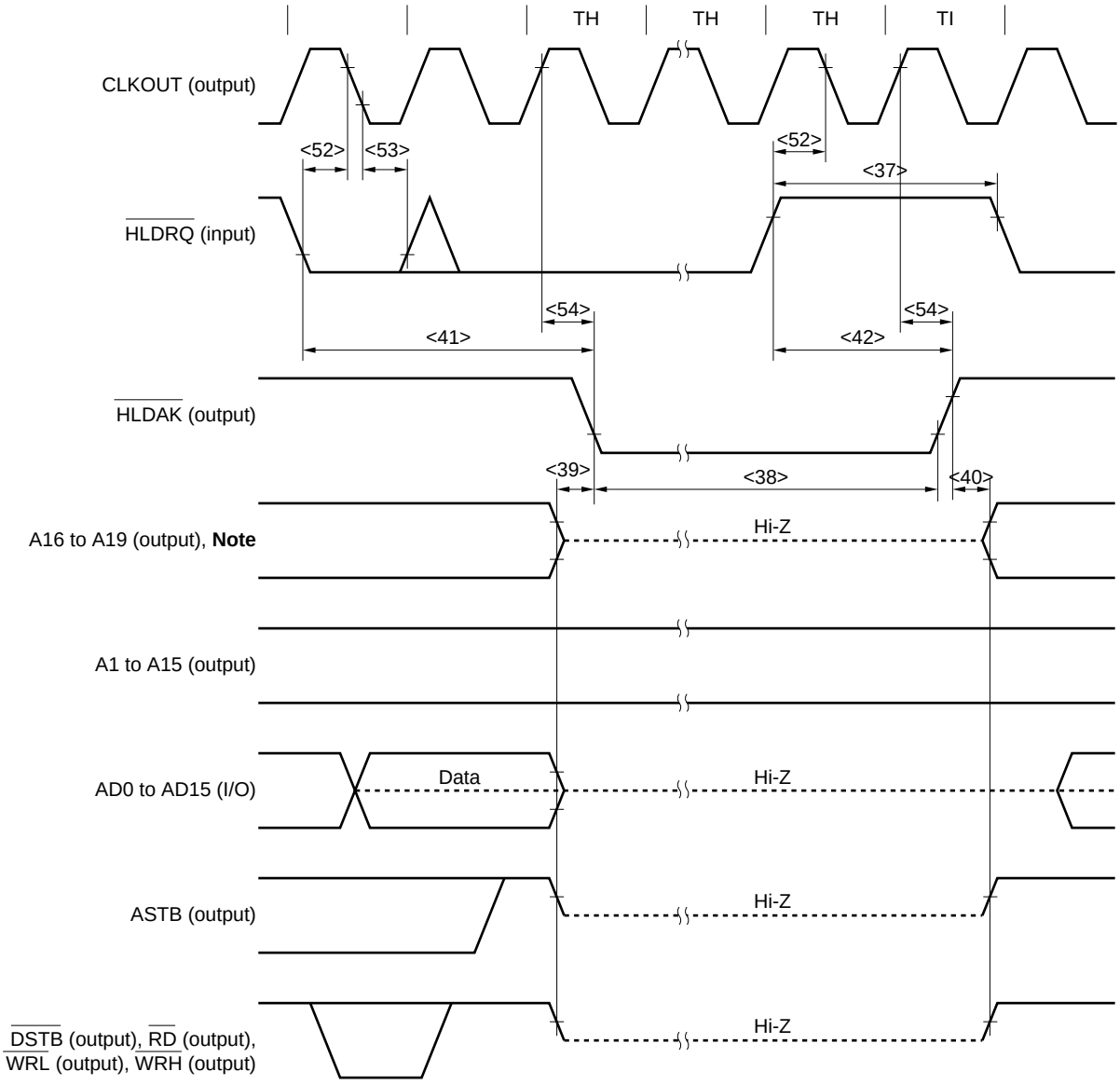
WRITE CYCLE (CLKOUT SYNCHRONOUS/ASYNCHRONOUS, 1 WAIT)



Note $\overline{\text{R/W}}$ (output), $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark $\overline{\text{RD}}$ is high level.

BUS HOLD



Remark R/W (output), UBEN (output), LBEN (output)

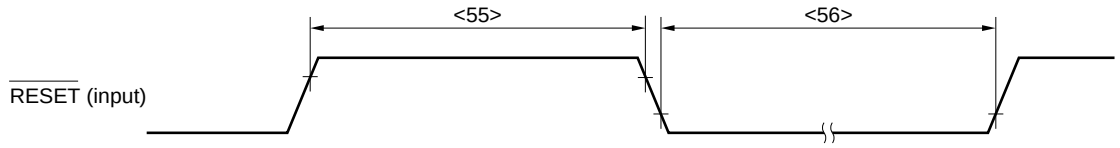
RESET/INTERRUPT TIMING

(T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

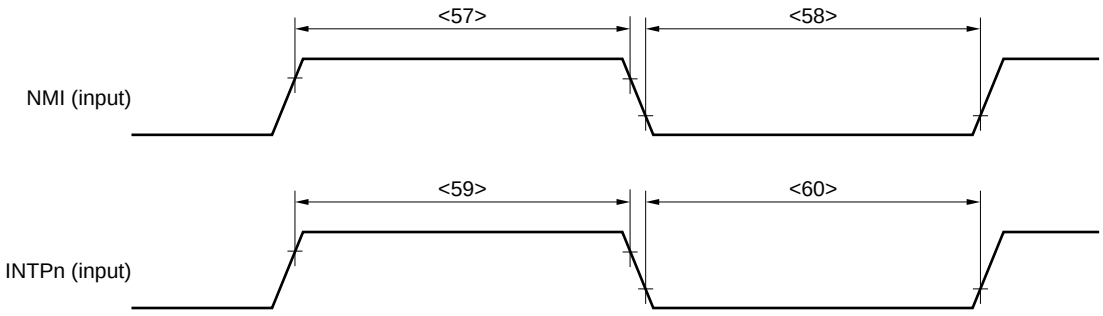
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}	<55>		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL}	<56>		500		ns
NMI high-level width	t_{WNIH}	<57>		500		ns
NMI low-level width	t_{WNIL}	<58>		500		ns
INTPn high-level width	t_{WITH}	<59>	n = 0 to 3	500		ns
			n = 4 to 6	3T + 20		ns
INTPn low-level width	t_{WITL}	<60>	n = 0 to 3	500		ns
			n = 4 to 6	3T + 20		ns

Remark T = 1/f_{XX}

RESET



INTERRUPT



Remark n = 0 to 6

CSI TIMING

(1) Master Mode (T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

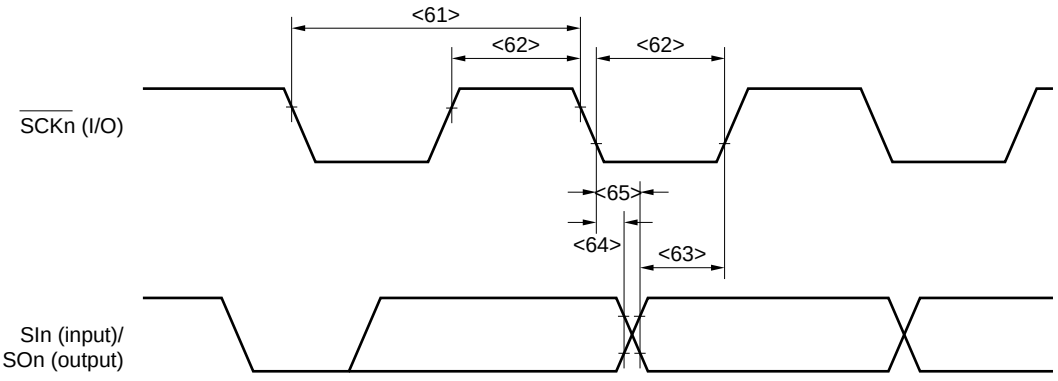
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY1}	<61>		470		ns
$\overline{SCKn}$ high-/low-level width	t_{KH1}, t_{KL1}	<62>		185		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK1}	<63>		50		ns
SIn hold time (from $\overline{SCKn}$↓)	t_{KSI1}	<64>		50		ns
$\overline{SCKn}$↓ → SOn output delay time	t_{KSO1}	<65>			60	ns

Remark n = 0 to 2

(2) Slave Mode (T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle time	t_{KCY2}	<61>		470		ns
$\overline{SCKn}$ high-/low-level width	t_{KH2}, t_{KL2}	<62>		185		ns
SIn setup time (to $\overline{SCKn}$↑)	t_{SIK2}	<63>		50		ns
SIn hold time (from $\overline{SCKn}$↓)	t_{KSI2}	<64>		50		ns
$\overline{SCKn}$↓ → SOn output delay time	t_{KSO2}	<65>			60	ns

Remark n = 0 to 2

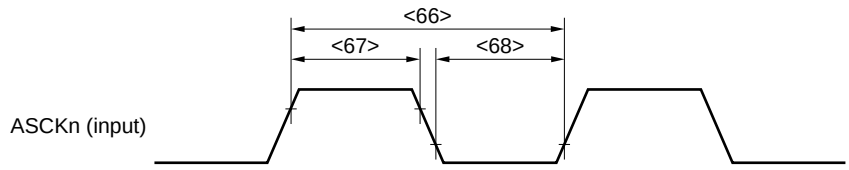


Remark n = 0 to 2

UART TIMING (T_A = –40 to +85°C, V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
ASCKn cycle time	t_{KCY13}	<66>		200		ns
ASCKn high-level width	t_{KH13}	<67>		80		ns
ASCKn low-level width	t_{KL13}	<68>		80		ns

Remark n = 0, 1



Remark n = 0 or 1

A/D CONVERTER

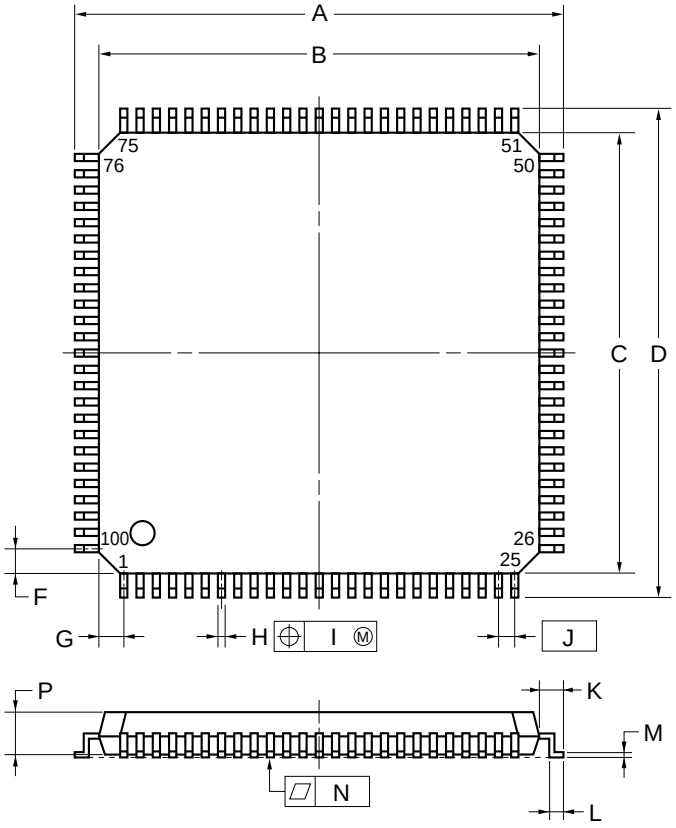
(T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = 0 V, Output Pin Load Capacitance: C_L = 50 pF)

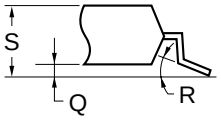
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Overall error [Note]						±8.0	LSB
Linearity error [Note]						±4.0	LSB
Conversion time	t_{CONV}			5			μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{DD}	V
Reference resistance	R_{REF}			10.0	15.5	21.4	kΩ
Power supply current	AI_{DD1}	Operation DC supply				3.0	mA
	AI_{DD2}	when STOP	T_A = –40 to +50°C		1	50	μA
			T_A = –40 to +85°C		1	200	μA

Note Quantization error is excluded.

18. PACKAGE DRAWING

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

19. RECOMMENDED SOLDERING CONDITION

T.B.D

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J98. 11

Related document V850 Family Instruction Table (U10229E)

Reference document Electrical Characteristics for Microcomputer (IEI-601) [Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

V850 Family and V850/SA1 are trademarks of NEC Corporation.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M4 96.5