NEC

MOS INTEGRATED CIRCUIT

μPD30131

VR4131™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30131 (VR4131) is one of the NEC Electronics VR Series™ RISC (Reduced Instruction Set Computer) microprocessors and is a high-performance 64-/32-bit microprocessor employing the MIPS™ RISC architecture.

The VR4131 uses the ultra-low-power-consumption VR4130™ as the CPU core, and has many peripheral functions such as a DMA controller, serial interface, IrDA interface, real-time clock, memory interface, NS16550-compatible serial interface, and 3-wire clocked serial interface. Configured with these functions, the VR4131 is suitable for high-speed battery-driven portable information systems. The external memory bus width can be selected from 32 bits or 16 bits. This processor supports the PCI bus interface conforming to Rev2.1 as the interface for an external device that requires the performance level of a color LCD controller.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

- **VR4131 Hardware User's Manual (U15350E)**
- **VR4100 Series™ Architecture User's Manual (U15509E)**

FEATURES

- Employs 64-bit MIPS architecture
  - Conforms to MIPS III instruction set (deleting FPU, LL, LLD, SC, and SCD instructions)
  - Optimized 6-stage pipeline
- Supports MIPS16 instruction set
- Supports high-speed product-sum operation (MACC) instructions
- Supports five types of operating modes, enabling more effective power-consumption management
- Internal maximum operating frequency: 200 MHz
- On-chip clock generator
- Address space Physical: 32 bits
  Virtual: 40 bits
  Integrates 32 double-entry TLBs
- High-capacity instruction/data separated cache memories
  Instruction: 16 KB
  Data: 16 KB
- Memory controller (ROM, synchronous DRAM (SDRAM), and flash memory supported)
- Supports PCI bus conforming to PCI Rev2.1
- Supports interface with companion chip VRC4173™
- 4-channel DMA controller
- Serial interface (NS16550 compatible)
- On-chip 3-wire clocked serial interface
- IrDA interface for infrared communication
- Debug serial interface
- Power supply voltage:
  $V_{DD}1$ = 1.35 to 1.65 V (internal)
  $V_{DD}3$ = 3.0 to 3.6 V (external)
- Package: 224-pin plastic FBGA

APPLICATIONS

- Battery-driven portable information systems
- Embedded equipment, etc.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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The mark ★ shows major revised points.

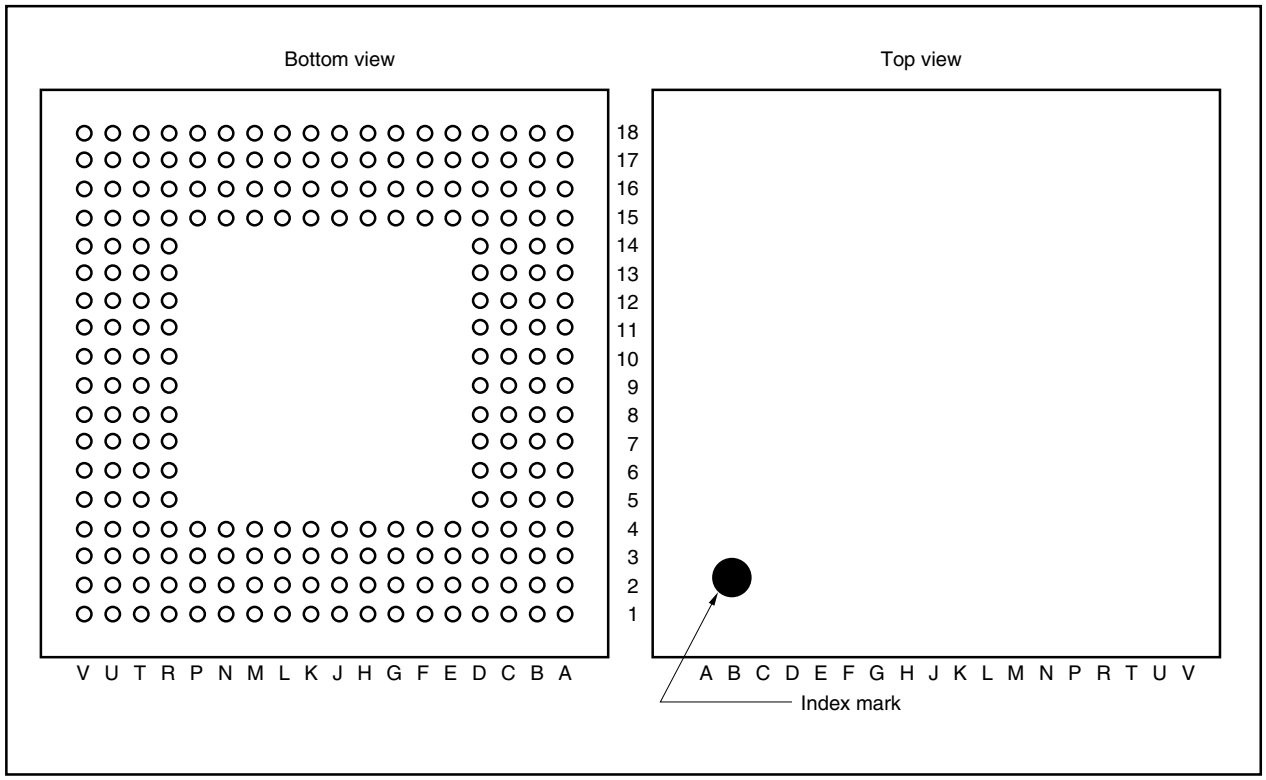
ORDERING INFORMATION

Part Number	Package	Internal Maximum Operating Frequency
μPD30131F1-200-GA2	224-pin plastic FBGA (16 × 16)	200 MHz

PIN CONFIGURATION

Caution The products of revision 2.0 or later are described here. When using the products of revision 1.2 or earlier, contact an NEC Electronics sales representative.

- 224-pin plastic FBGA (16 × 16)
  μPD30131F1-200-GA2



(1/2)

Pin No.	Power Supply[Note]	Pin Name	Pin No.	Power Supply[Note]	Pin Name	Pin No.	Power Supply[Note]	Pin Name
A1	3.3 V	CLKOUT	C14	3.3 V	AD3	H3	3.3 V	ADD13
A2	1.5 V	V_{DD}PD	C15	3.3 V	CBE2	H4	3.3 V	DATA5
A3	1.5 V	V_{DD}P	C16	3.3 V	DEVSEL#	H15	3.3 V	POWER
A4	3.3 V	CLKX1	C17	3.3 V	PAR	H16	3.3 V	GND3
A5	3.3 V	CLKX2	C18	3.3 V	FRAME#	H17	3.3 V	BKTGIO#
A6	3.3 V	PCLK	D1	3.3 V	ADD17	H18	3.3 V	FIRCLK
A7	3.3 V	AD28	D2	3.3 V	ADD21	J1	3.3 V	DATA8
A8	3.3 V	AD23	D3	3.3 V	ADD22	J2	3.3 V	DATA7
A9	3.3 V	AD19	D4	1.5 V	V_{DD}1	J3	3.3 V	ADD11
A10	3.3 V	AD16	D5	3.3 V	GND3	J4	3.3 V	ADD12
A11	3.3 V	AD13	D6	3.3 V	CGND	J15	3.3 V	POWERON
A12	3.3 V	AD12	D7	3.3 V	AD29	J16	3.3 V	MPOWER
A13	3.3 V	AD10	D8	3.3 V	AD24	J17	1.5 V	GND1
A14	3.3 V	AD6	D9	3.3 V	AD20	J18	3.3 V	IRDOUT#/JTDO
A15	3.3 V	AD2	D10	3.3 V	AD15	K1	3.3 V	DATA10
A16	3.3 V	RST#	D11	1.5 V	GND1	K2	3.3 V	DATA9
A17	3.3 V	CBE1	D12	3.3 V	AD8	K3	3.3 V	ADD10
A18	3.3 V	IRDY#	D13	3.3 V	AD4	K4	3.3 V	DATA11
B1	3.3 V	ADD23	D14	3.3 V	AD0	K15	3.3 V	GND3
B2	3.3 V	V_{DD}3	D15	3.3 V	GND3	K16	1.5 V	V_{DD}1
B3	1.5 V	GNDP	D16	3.3 V	GND3	K17	3.3 V	JTDI/RMODE#
B4	3.3 V	CV_{DD}	D17	3.3 V	PERR#	K18	3.3 V	V_{DD}3
B5	3.3 V	RTCX1	D18	3.3 V	STOP#	L1	3.3 V	DATA13
B6	3.3 V	AD30	E1	3.3 V	ADD15	L2	3.3 V	DATA12
B7	3.3 V	AD25	E2	3.3 V	ADD18	L3	3.3 V	GND3
B8	3.3 V	AD22	E3	3.3 V	ADD16	L4	3.3 V	ADD9
B9	3.3 V	AD17	E4	3.3 V	ADD19	L15	3.3 V	RTCRST#
B10	3.3 V	AD14	E15	3.3 V	GND3	L16	3.3 V	RSTSW#
B11	3.3 V	V_{DD}3	E16	3.3 V	GND3	L17	3.3 V	JTCK
B12	3.3 V	AD9	E17	3.3 V	REQ1#	L18	3.3 V	IRDIN
B13	3.3 V	AD5	E18	3.3 V	CLKRUN	M1	3.3 V	DATA15
B14	3.3 V	AD1	F1	3.3 V	GND3	M2	3.3 V	DATA14
B15	3.3 V	CBE3	F2	3.3 V	DATA1	M3	3.3 V	DATA17/GPIO17
B16	3.3 V	CBE0	F3	3.3 V	DATA2	M4	3.3 V	ADD8
B17	3.3 V	V_{DD}3	F4	3.3 V	DATA0	M15	3.3 V	DDIN/GPIO34
B18	3.3 V	TRDY#	F15	3.3 V	REQ0#	M16	3.3 V	LEDOUT#
C1	3.3 V	ADD20	F16	3.3 V	REQ2#	M17	3.3 V	JTMS
C2	3.3 V	ADD24	F17	3.3 V	GNT0#	M18	3.3 V	FIRDIN#/SEL
C3	1.5 V	GNDPD	F18	3.3 V	GNT2#	N1	3.3 V	ADD7
C4	3.3 V	AD27	G1	1.5 V	GND1	N2	3.3 V	DATA16/GPIO16
C5	3.3 V	GND3	G2	3.3 V	ADD14	N3	3.3 V	ADD6
C6	3.3 V	RTCX2	G3	3.3 V	V_{DD}3	N4	3.3 V	DATA18/GPIO18
C7	3.3 V	AD31	G4	3.3 V	DATA3	N15	3.3 V	DRTS#/MIPS16EN/GPIO33
C8	3.3 V	AD26	G15	3.3 V	SERR#	N16	3.3 V	DDOUT/DBUS32/GPIO32
C9	3.3 V	AD21	G16	3.3 V	GNT1#	N17	3.3 V	JTRST#
C10	3.3 V	AD18	G17	3.3 V	BIGENDIAN	N18	3.3 V	HLDRQ#
C11	1.5 V	V_{DD}1	G18	3.3 V	LOCK#	P1	3.3 V	DATA20/GPIO20
C12	3.3 V	AD11	H1	3.3 V	DATA6	P2	3.3 V	DATA19/GPIO19
C13	3.3 V	AD7	H2	3.3 V	DATA4	P3	3.3 V	GND3

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark # indicates active low.

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Pin No.	Power Supply[Note]	Pin Name	Pin No.	Power Supply[Note]	Pin Name	Pin No.	Power Supply[Note]	Pin Name
P4	3.3 V	GND3	T4	3.3 V	DATA27/GPIO27	U12	1.5 V	GND1
P15	3.3 V	RTS#/CLKSEL1	T5	3.3 V	DATA31/GPIO31	U13	3.3 V	SIN
P16	3.3 V	DCTS#/GPIO35	T6	3.3 V	CAS	U14	3.3 V	GPIO3
P17	3.3 V	TxD/CLKSEL2	T7	3.3 V	SWR#	U15	3.3 V	GPIO7
P18	3.3 V	HLDAK#/NWIREEN	T8	3.3 V	CKE0	U16	3.3 V	GPIO8
R1	3.3 V	DATA21/GPIO21	T9	3.3 V	ROMCS0#	U17	3.3 V	$V_{DD}3$
R2	3.3 V	ADD5	T10	3.3 V	IOCS0#	U18	3.3 V	DCD#/GPIO15
R3	3.3 V	$V_{DD}3$	T11	1.5 V	$V_{DD}1$	V1	3.3 V	DATA25/GPIO25
R4	3.3 V	DQM1	T12	3.3 V	GPIO0	V2	3.3 V	DATA26/GPIO26
R5	3.3 V	DATA29/GPIO29	T13	3.3 V	GPIO4	V3	3.3 V	DATA28/GPIO28
R6	3.3 V	WR#	T14	3.3 V	GND3	V4	3.3 V	DATA30/GPIO30
R7	3.3 V	RAS	T15	3.3 V	IORDY	V5	3.3 V	SCLK
R8	3.3 V	DQM3	T16	3.3 V	GPIO10	V6	3.3 V	$V_{DD}3$
R9	3.3 V	CS1#	T17	3.3 V	GPIO13	V7	3.3 V	DQM0
R10	3.3 V	SPOWER	T18	3.3 V	DTR#/CLKSEL0	V8	3.3 V	CKE1
R11	3.3 V	$V_{DD}3$	U1	3.3 V	DATA24/GPIO24	V9	3.3 V	CS2#/ROMCS2#
R12	3.3 V	SOUT	U2	3.3 V	$V_{DD}3$	V10	3.3 V	ROMCS1#
R13	3.3 V	GPIO2	U3	3.3 V	ADD3	V11	3.3 V	GND3
R14	3.3 V	GND3	U4	3.3 V	ADD2	V12	3.3 V	SECLK
R15	3.3 V	BATTINH/BATTINT#	U5	3.3 V	ADD1	V13	3.3 V	GPIO1
R16	3.3 V	DSR#	U6	3.3 V	RD#	V14	3.3 V	GPIO5
R17	3.3 V	CTS#	U7	3.3 V	GND3	V15	3.3 V	GPIO6/SYSDIR
R18	3.3 V	RxD	U8	3.3 V	DQM2	V16	3.3 V	GPIO9
T1	3.3 V	DATA23/GPIO23	U9	3.3 V	CS0#	V17	3.3 V	GPIO11
T2	3.3 V	DATA22/GPIO22	U10	3.3 V	CS3#/ROMCS3#	V18	3.3 V	GPIO12
T3	3.3 V	ADD4	U11	3.3 V	IOCS1#			

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

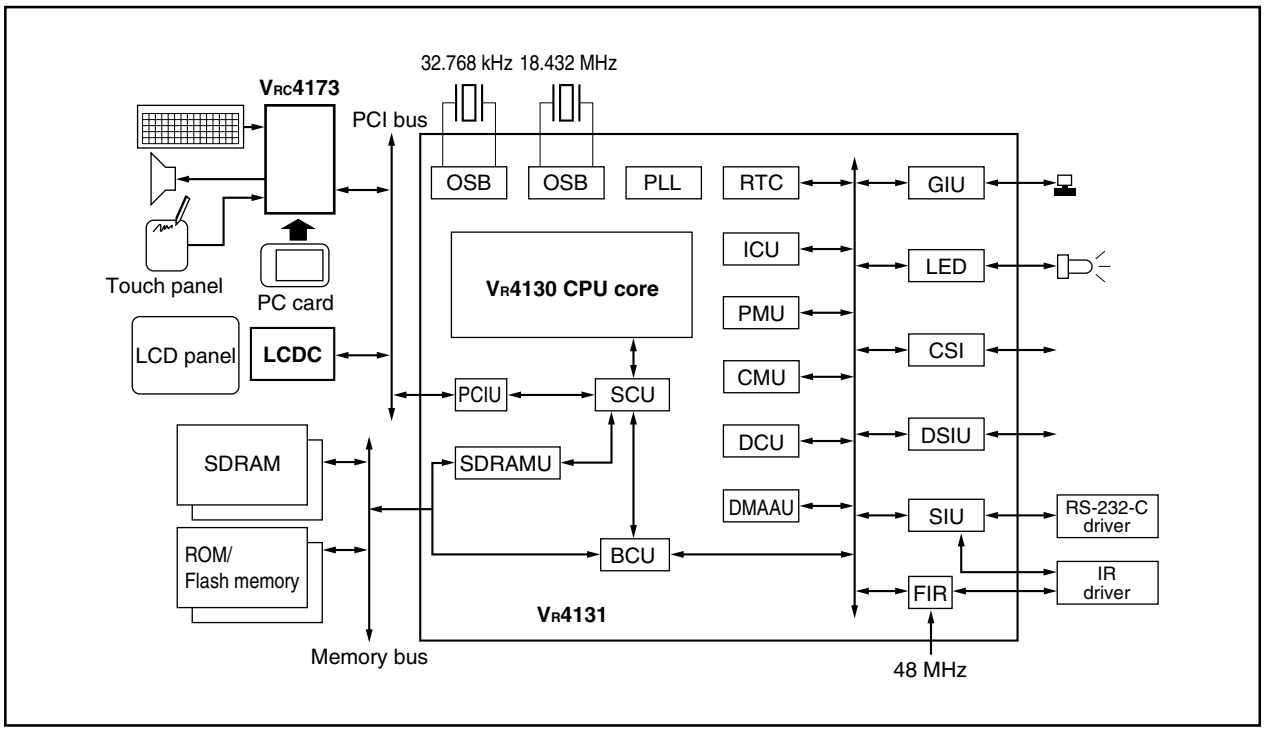
Remark # indicates active low.

PIN IDENTIFICATION

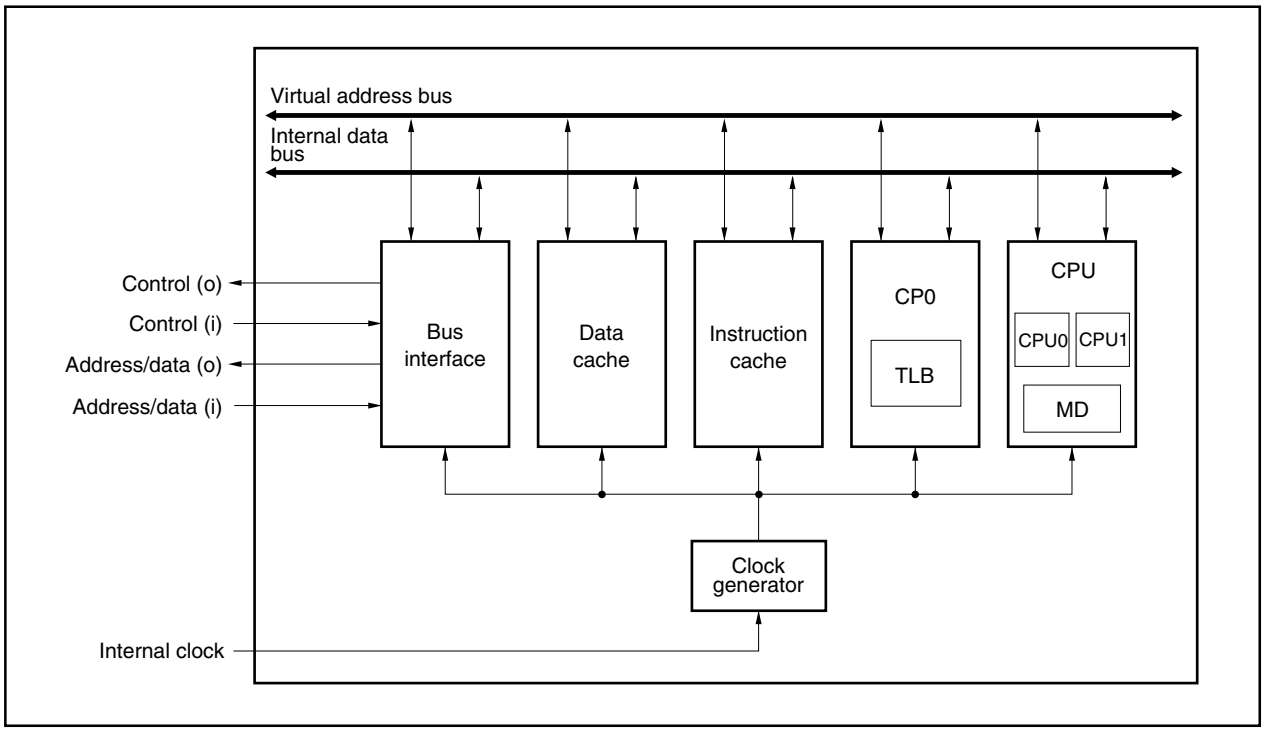
AD(31:0):	Address/data bus	IRDY#:	Initiator ready
ADD(24:1):	Address bus	JTCK:	JTAG clock
BATTINH:	Battery inhibit	JTDI:	JTAG data input
BATTINT#:	Battery interrupt request	JTDO:	JTAG data output
BIGENDIAN:	Big endian	JTMS:	JTAG mode select
BKTGIO#:	Break trigger I/O	JTRST#:	JTAG reset
CAS:	Column address strobe	LEDOUT#:	LED output
CBE(3:0):	Command/byte enable	LOCK#:	Lock
CGND:	GND for oscillator	MIPS16EN:	MIPS16 enable
CKE(1:0):	Clock enable	MPOWER:	Main power
CLKSEL(2:0):	Clock select	NWIREEN:	N-wire enable
CLKOUT:	Clock output	PAR:	Parity
CLKRUN:	Clock run	PCLK:	PCI clock
CLKX1:	Clock X1	PERR#:	Parity error
CLKX2:	Clock X2	POWER:	Power switch
CS(3:0)#:	Chip select	POWERON:	Power on state
CTS#:	Clear to send	RAS:	Row address strobe
CV_{DD}:	V_{DD} for oscillator	RD#:	Read
DATA(31:0):	Data bus	REQ(2:0)#:	Request
DBUS32:	Data bus 32	RMODE#:	Reset mode
DCD#:	Data carrier detect	ROMCS(3:0)#:	ROM chip select
DCTS#:	Debug serial clear to send	RST#:	Reset
DDIN:	Debug serial data input	RSTSW#:	Reset switch
DDOUT:	Debug serial data output	RTCRST#:	Real-time clock reset
DEVSEL#:	Device select	RTCX1:	Real-time clock X1
DQM(3:0):	Data input/output	RTCX2:	Real-time clock X2
DRTS#:	Debug serial request to send	RTS#:	Request to send
DSR#:	Data set ready	RxD:	Receive data
DTR#:	Data terminal ready	SCLK:	SDRAM clock
FIRCLK:	FIR clock	SECLK:	Clocked serial clock
FIRDIN#:	FIR data input	SEL:	IrDA module select
FRAME#:	Cycle frame	SERR#:	System error
GND1, GND3:	Ground	SIN:	Clocked serial input
GNDP, GNDPD:	GND for PLL	SOUT:	Clocked serial output
GNT(2:0)#:	Grant	SPOWER:	SDRAM power control
GPIO(13:0):	General purpose I/O	STOP#:	Target assert stop
GPIO(35:15):	General purpose I/O	SWR#:	SDRAM write
HLDAK#:	Hold acknowledge	SYSDIR:	System bus buffer direction
HLDRQ#:	Hold request	TRDY#:	Target ready
IOCS(1:0)#:	I/O chip select	TxD:	Transmit data
IORDY:	I/O ready	$V_{DD}1$, $V_{DD}3$:	Power supply voltage
IRDIN:	IrDA data input	$V_{DD}P$, $V_{DD}PD$:	V_{DD} for PLL
IRDOUT#:	IrDA data output	WR#:	Write

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Caution The products of revision 2.0 or later are described here. When using the products of revision 1.2 or earlier, contact an NEC Electronics sales representative.

Remark # indicates active low.

1.1 Pin Functions

(1) Memory interface signals (1/2)

Signal	I/O	Function
SCLK	Output	Operation clock for SDRAM
ADD(24:1)	Output	Higher 24 bits of the 25-bit address bus These signals are used to specify addresses for the VR4131, SDRAM, ROM, and I/O space.
DATA(15:0)	I/O	16-bit data bus These signals are used to transfer data between the VR4131 and the SDRAM, ROM, or I/O space.
DATA(31:16)/ GPIO(31:16)	I/O	The function differs depending on the DBUS32 pin setting. • **When DBUS32 = 1** These signals function as the higher 16 bits of the 32-bit data bus. They are used to transfer data between the VR4131 and the DRAM or ROM. • **When DBUS32 = 0** These signals function as general-purpose I/O ports.
CKE(1:0)	Output	Clock enable signals for SDRAM CKE(1:0) supports the following banks. SDRAM bank / CKE(1:0) / 32-bit data bus / 16-bit data bus Bank 3 / CKE1 / CS3#/ROMCS3# / DQM3 Bank 2 / CKE0 / CS2#/ROMCS2# / DQM2 Bank 1 / CKE1 / CS1# / CS1# Bank 0 / CKE0 / CS0# / CS0#
DQM3	Output	The function differs depending on the setting of the DBUS32 pin and the connected device. • **When DBUS32 = 1 and** SDRAM is accessed: This is the byte enable signal for DATA(31:24) of the 32-bit data bus. A 32-bit external I/O device is accessed: This is the byte enable signal for DATA(31:24) of the 32-bit data bus. • **When DBUS32 = 0 and** SDRAM is accessed: This is the CS signal for SDRAM. This signal becomes active when a command is issued for the SDRAM connected to the highest address.
DQM2	Output	The function differs depending on the setting of the DBUS32 pin and the connected device. • **When DBUS32 = 1 and** SDRAM is accessed: This is the byte enable signal for DATA(23:16) of the 32-bit data bus. A 32-bit external I/O device is accessed: This is the byte enable signal for DATA(23:16) of the 32-bit data bus. • **When DBUS32 = 0 and** SDRAM is accessed: This is the CS signal for SDRAM. This signal becomes active when a command is issued for the SDRAM connected to the second highest address.

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Signal	I/O	Function
DQM1	Output	The function differs depending on the connected device. When SDRAM is accessed: This is the byte enable signal for DATA(15:8). When a 32-bit external I/O device is accessed: This is the byte enable signal for DATA(15:8). When a 16-bit external I/O device is accessed (little endian): This is the ADD0 signal of the address bus. When a 16-bit external I/O device is accessed (big endian): This is the high-byte enable signal of the I/O bus.
DQM0	Output	The function differs depending on the connected device. When SDRAM is accessed: This is the byte enable signal for DATA(7:0). When a 32-bit external I/O device is accessed: This is the byte enable signal for DATA(7:0). When a 16-bit external I/O device is accessed (little endian): This is the high-byte enable signal of the I/O bus. When a 16-bit external I/O device is accessed (big endian): This is the ADD0 signal of the address bus.
CS(1:0)#	Output	Chip select signal for SDRAM
RAS	Output	RAS signal for SDRAM
CAS	Output	CAS signal for SDRAM
SYSDIR/GPIO6	I/O	Direction signal for SDRAM If not used as the SYSDIR signal, this signal can be used as a GPIO pin.
SPOWER	Output	Power supply control signal for SDRAM
RD#	Output	This signal becomes active when a read access is performed for data from the I/O space and ROM.
WR#	Output	This signal becomes active when writing data to the I/O space.
SWR#	Output	This signal becomes active when writing data to SDRAM.
ROMCS(1:0)#	Output	Chip select signals for ROM
CS(3:2)#/ ROMCS(3:2)#	Output	Chip select signals for an expansion SDRAM or expansion ROM • **When using expansion SDRAM** These signals function as CS(3:2)#. • **When using expansion ROM** These signals function as ROMCS(3:2)#.
HLDRQ#	Input	Bus mastership request signal for system bus and DRAM sent from the external bus master
HLDAK#/NWIREEN	Output	Bus mastership enable signal for system bus and DRAM sent to the external bus master This signal is used as the NWIREEN signal during RTC reset.

(2) I/O device interface signals

Signal	I/O	Function
IOCS(1:0)#	Output	Device chip select signals These signals become active when the VR4131 accesses the I/O device using the ADD bus or DATA bus.
IORDY	Input	Device ready signal Make this signal active in a state in which the I/O device can be accessed from the VR4131.

(3) Clock interface signals

Signal	I/O	Function
RTCX1	Input	This is the 32.768 kHz oscillator's input pin. It is connected to one side of a crystal resonator.
RTCX2	Output	This is the 32.768 kHz oscillator's output pin. It is connected to one side of a crystal resonator.
CLKX1	Input	This is the 18.432 MHz oscillator's input pin. It is connected to one side of a crystal resonator.
CLKX2	Output	This is the 18.432 MHz oscillator's output pin. It is connected to one side of a crystal resonator.
FIRCLK	Input	This is the 48 MHz clock input pin. This signal inputs a clock when FIR is used.
CLKOUT	Output	This is the clock output to supply an external device. A 9.216 MHz clock is output in the non-Hibernate mode. The clock output stops at low level during Hibernate mode.

(4) Battery monitor interface signals

Signal	I/O	Function
BATTINH/ BATTINT#	Input	The function differs depending on the setting of the MPOWER pin. • **When MPOWER = 0** BATTINH function This signal enables/disables activation at power-on. 1: Activation enabled 0: Activation disabled • **When MPOWER = 1** BATTINT# function This is an interrupt signal that is output when the remaining power is low during normal operation. An external circuit checks the remaining battery power. Activate the signal at this pin if voltage sufficient for operation cannot be supplied.

(5) Initialization interface signals

Signal	I/O	Function
MPOWER	Output	This signal indicates that the VR4131 is operating. This signal is inactive in Hibernate mode.
POWERON	Output	This signal indicates that the VR4131 is ready to operate. It becomes active when a power-on factor is detected and becomes inactive when the BATTINH/BATTINT# signal check operation is completed.
POWER	Input	This is the VR4131 activation signal.
RSTSW#	Input	This is the VR4131 reset signal.
RTCRST#	Input	This signal resets the RTC. When power is first supplied to a device, an external circuit must assert the signal at this pin for about 2 s.

(6) RS-232-C interface signals

Signal	I/O	Function
RxD	Input	This is a receive data signal. It is used when the RS-232-C controller sends serial data to the VR4131.
CTS#	Input	This is a transmit enable signal. Assert this signal when the RS-232-C controller is ready to receive transmission of serial data.
DCD#/GPIO15	Input	This is a carrier detection signal. Assert this signal when valid serial data is being received. It is also used as a power-on factor for the VR4131. When this pin is not used for the DCD# signal, this pin can be used as an interrupt detection input for the GIU.
DSR#	Input	This is the data set ready signal. Assert this signal when the RS-232-C controller is ready to transfer serial data between the controller and the VR4131.
TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0	I/O	The function differs depending on the operating status. • **During normal operation (output)** Signals used for serial communication TxD signal: This is a transmit data signal. It is used when the VR4131 sends serial data to the RS-232-C controller. RTS# signal: This is a transmit request signal. This signal is asserted when the VR4131 is ready to receive serial data from the RS-232-C controller. DTR# signal: This is a terminal equipment ready signal. This signal is asserted when the VR4131 is ready to transmit or receive serial data. • **During RTC reset (input)** Signals (CLKSEL(2:0)) used to set the CPU core operation frequency, BUSCLK frequency, and internal bus clock frequency. These signals are sampled when the RTCRST# signal changes from low level to high level. For the relationship between the CLKSEL pin setting and each clock frequency, see **Table 1-1 Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value)**.

Table 1-1. Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value)

CLKSEL(2:0)	PClock (MHz)	VTClock (MHz)	TClock (MHz)	MasterOut (MHz)
111	RFU	RFU	RFU	RFU
110	199.1	33.2	16.6	4.15
101	181.0	30.2	15.1	3.77
100	165.9	33.2	16.6	4.15
011	153.1	30.6	15.3	3.83
010	132.7	33.2	16.6	4.15
001	99.5	33.2	16.6	4.15
000	RFU	RFU	RFU	RFU

Remark RFU: Reserved for Future Use

(7) Debug serial interface signals

Signal	I/O	Function
DDIN/GPIO34	I/O	Debug serial data input signal. This signal can be used as a general-purpose output port when not being used as the DDIN signal.
DCTS#/GPIO35	I/O	Transmit enable signal. Assert this signal when the RS-232-C controller can receive the serial data transmission. This signal can be used as a general-purpose output port when not being used as the DCTS# signal.
DDOUT/ DBUS32/GPIO32	I/O	The function differs depending on the operating status. • **During normal operation (output)** DDOUT: This signal functions as the debug serial transmit data signal. • **During RTC reset (input)** DBUS32: This signal functions as the data bus width switching signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Data bus is used with 32-bit width 0: Data bus is used with 16-bit width This signal can be used as a general-purpose output port when not being used as the DDOUT or DBUS32 signal.
DRTS#/ MIPS16EN/ GPIO33	I/O	The function differs depending on the operating status. • **During normal operation (output)** DRTS#: This signal functions as the debug serial transmit request signal. • **During RTC reset (input)** MIPS16EN: This signal functions as the MIPS16 instruction enable signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: MIPS16 instructions enabled 0: MIPS16 instructions disabled This signal can be used as a general-purpose output port when not being used as the DRTS# or MIPS16EN signal.

(8) IrDA interface signals

Signal	I/O	Function
IRDIN	Input	This is an IrDA serial data input signal. It is used when the serial data is transferred from the IrDA controller to the VR4131. Both FIR and SIR can be used. If the IrDA controller used is a Hewlett Packard Company product, however, this signal should be used only for SIR.
FIRDIN#/SEL	I/O	The function differs according to the IrDA controller to be used. • **Hewlett Packard controller or SHARP Semiconductor controller** FIRDIN#: It is an FIR receive data input signal. • **TEMIC Semiconductor controller** SEL: It is a signal output for the FIR/SIR switching.
IRDOUT#/JTDO	Output	This is the IrDA serial data output signal. It is used when the serial data is transferred from the VR4131 to the IrDA controller. This signal can be used as a JTAG serial data output signal when JTAG is used.

(9) Clocked serial signals

Signal	I/O	Function
SIN	Input	Clocked serial input signal
SOUT	Output	Clocked serial output signal
SECLK	Output	Synchronous clock output for the clocked serial interface

(10) General-purpose I/O signals

Signal	I/O	Function
GPIO(3:0)	I/O	Maskable activation factor input signals. These signals can be used as general-purpose I/O ports after activation.
GPIO(5:4)	I/O	General-purpose I/O ports.
SYSDIR/GPIO6	I/O	Refer to **(1) Memory interface signals**.
GPIO(8:7)	I/O	General-purpose I/O ports.
GPIO(12:9)	I/O	Maskable activation factor input signals. These signals can be used as general-purpose I/O ports after activation.
GPIO13	I/O	General-purpose I/O port. This signal is recommended to be used as a V_{RC}4173 interrupt.
DCD#/GPIO15	Input	Refer to **(6) RS-232-C interface signals**.
GPIO(31:16)/ DATA(31:16)	I/O	Refer to **(1) Memory interface signals**.
DDOUT/ DBUS32/ GPIO32	I/O	Refer to **(7) Debug serial interface signals**.
DRTS#/ MIPS16EN/ GPIO33	I/O	Refer to **(7) Debug serial interface signals**.
DDIN/GPIO34	I/O	Refer to **(7) Debug serial interface signals**.
DCTS#/GPIO35	I/O	Refer to **(7) Debug serial interface signals**.

(11) LED interface signal

Signal	I/O	Function
LEDOUT#	Output	This is an output signal for lighting LEDs in normal operation mode. This pin has to be pulled up regardless of whether the LED function is being used; otherwise the internal cache does not work correctly.

(12) PCI Like bus interface signals

Signal	I/O	Function
AD(31:0)	I/O	This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output.
CBE(3:0)	I/O	These are the bus-command/byte-enable signals. In the address phase, bus commands are output, and in the data phase, they operate as the byte-enable signals.
DEVSEL#	I/O	This signal is asserted when the target is accessed and continues being asserted until the completion of the transaction.
FRAME#	I/O	This signal is asserted when the initiator starts the transaction. It also remains asserted throughout burst transfer.
REQ(2:0)#	Input	These signals are asserted when the master sends a request to the VR4131 for the bus mastership.
GNT(2:0)#	Output	These signals are asserted when the VR4131 grants bus mastership to the device making the request with the REQ# signal.
IRDY#	I/O	This signal is asserted when the initiator is in the data transfer enabled state.
LOCK#	I/O	This signal indicates a resource lock.
PAR	I/O	This signal outputs a low level if the number of “1” bits from the 36 AD(31:0) and CBE(3:0) signals is even, and a high level if the number is odd.
PERR#	I/O	This signal is asserted when a parity error occurs following a parity check by the data-read initiator in the read cycle or the data-write target in the write cycle.
SERR#	I/O	This signal is asserted when a fatal error for the system occurs.
STOP#	I/O	This signal is asserted when the target requires the initiator to abort the transaction.
TRDY#	I/O	This signal is asserted when the target is in the transfer-enabled state.
PCLK	Output	This is the PCI bus reference clock.
CLKRUN	I/O	This signal controls the clock for power management.
RST#	Output	This is the PCI bus reset signal.

(13) Debug interface signals

Signal	I/O	Function
JTCK	Input	This is the clock input for JTAG.
JTMS	Input	This is the JTAG mode setting input signal.
JTDI/RMODE#	Input	This is the RMODE#/JTDI alternate function pin. When JTRST# is active, it functions as RMODE#, and when JTRST# is inactive, it functions as JTDI. If a debugging tool is not connected externally, pull up to high level. • **RMODE#: Input** When JTRST# is active, this becomes the reset mode pin. The debug reset initial value is determined according to the level of this signal. Debug reset resets the processor with two kinds of resets: a debug cold reset and debug soft reset. These two resets function in the same way as a cold reset input and a soft reset input from the target system. 0: The debug reset is valid; the CPU core is reset. 1: The debug reset is invalid; the CPU core is not reset. • **JTDI: Input** When JTRST# is inactive this becomes the JTAG data input signal.
JTRST#	Input	This is the JTAG reset signal.
BKTGIO#	I/O	• **BKTGIO#: In the input setting** When JTRST# is inactive and BKTGIO# is in the input setting, BKTGIO# becomes the event trigger/break request input pin. When the event trigger input is valid, if BKTGIO# is made low level, the normal mode user program is aborted, and the processor is forcibly changed to debug mode. If BKTGIO# becomes low level in debug mode, the break request is held pending until the processor returns to normal mode. 0: A break is requested and the processor is forcibly changed to debug mode. 1: The current status of the processor is maintained. • **BKTGIO#: In the output setting** When JTRST# is inactive and BKTGIO# is in the output setting, BKTGIO# becomes the event trigger/break output pin. While the processor is operating in normal mode, if an event is detected upon a match with either of the conditions of the hardware breakpoints (instruction address breakpoint or data access breakpoint), a low level (1 pulse) is output from BKTGIO# as an event trigger, and report of the event detection is sent to the external debugging tool. All the events detected after the last event trigger has been output are sent as one event trigger. If the processor mode is changed to debug mode, the low-level output continues, and none of the as unreported events are sent. 0: Detects a hardware breakpoint. The processor is in debug mode. 1: The processor is in normal mode.
HLDAK#/NWIREEN	I/O	The function differs depending on the operating status. • **During RTC reset (input)** NWIREEN: This is the HALTimer shutdown function control signal and N-Wire use enable signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: HALTimer shutdown function disabled (HALTimer shutdown is not executed even if HALTimer is not cleared), N-Wire can be used. 0: HALTimer shutdown function enabled (if HALTimer is not cleared, shutdown is executed 4 seconds after power-on), N-Wire cannot be used. • **When the HLDEN bit of the BCUCNTREG1 register is 1** HLDAK#: The signal that gives the mastership of the system bus and DRAM bus to the external bus master.
IRDOUT#/JTDO	Output	• **When N-Wire cannot be used** IRDOUT#: This is the IrDA serial data output signal. • **When N-Wire can be used** JTDO: This is the JTAG data output signal.

★

(14) Dedicated V_{DD} and GND signals

Signal	Power Supply[Note]	Function
V_{DD}P	1.5 V	Dedicated V_{DD} for the PLL analog unit
GNDP	1.5 V	Dedicated GND for the PLL analog unit
V_{DD}PD	1.5 V	Dedicated V_{DD} for the PLL digital unit. Its function is identical to V_{DD}1.
GNDPD	1.5 V	Dedicated GND for the PLL digital unit. Its function is identical to GND1.
CV_{DD}	3.3 V	Dedicated V_{DD} for the oscillator
CGND	3.3 V	Dedicated GND for the oscillator
V_{DD}1	1.5 V	Normal 1.5 V V_{DD}
GND1	1.5 V	GND for normal 1.5 V system
V_{DD}3	3.3 V	Normal 3.3 V V_{DD}
GND3	3.3 V	GND for normal 3.3 V system

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark The V_R4131 has two power supplies, but there are no restrictions on the order of supply voltage application.

(15) Other signal

Signal	I/O	Function
BIGENDIAN	Input	This signal selects big endian. 1: Big endian (pull up[Note]) 0: Little endian (pull down[Note])

Note When pulling up, the pin must be connected to V_{DD}3 via a resistor. When pulling down, the pin may be directly connected to GND3.

1.2 Pin Status in Specific States

(1/4)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
AD(31:0)	0	0	0	Hold	**Note 1**
ADD(24:1)	0	0	0	**Note 2**	Hi-Z
BATTINH/BATTINT#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
BIGENDIAN	Hi-Z	0	0	0	Hold
BKTGIO#	**Note 3**	**Note 4**	**Note 3**	Hold	Hold
CAS	0	0	0	**Note 2**	Hi-Z
CBE(3:0)	0	0	0	Hold	**Note 1**
CKE(1:0)	0	0	0	**Note 2**	Hi-Z
CLKOUT	0	0	CLK	CLK	CLK
CLKRUN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
CS(1:0)#	Hi-Z	1	1	**Note 2**	Hi-Z
CS2#/ROMCS2#	Hi-Z	**Note 5**	1	**Note 2**	**Note 6**
CS3#/ROMCS3#	Hi-Z	**Note 7**	1	**Note 2**	**Note 8**
CTS#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DATA(15:0)	0	0	0	**Note 2**	Hi-Z

Notes 1. Normal operation

2. Maintains the previous status.
For the pin status during the bus hold period, however, refer to the During Bus Hold column.

3. The value differs depending on debugger control. It is either 1 or high impedance.

4. The value differs depending on debugger control. It is either 0 or high impedance.

5. Depends on the status of the BCUCNTREG3 register's EXT_ROMCS0 bit and the DBUS32 pin.
When the EXT_ROMCS0 bit is 0 and the DBUS32 pin = 1: High level
If a combination other than above: High impedance

6. Depends on the status of the BCUCNTREG3 register's EXT_ROMCS0 bit and the DBUS32 pin.
When the EXT_ROMCS0 bit is 0 and the DBUS32 pin = 1: High impedance
If a combination other than above: High level

7. Depends on the status of the BCUCNTREG3 register's EXT_ROMCS1 bit and the DBUS32 pin.
When the EXT_ROMCS1 bit is 0 and DBUS32 = 1: High level
If a combination other than above: High impedance

8. Depends on the status of the BCUCNTREG3 register's EXT_ROMCS1 bit and the DBUS32 pin.
When the EXT_ROMCS1 bit is 0 and DBUS32 = 1: High impedance
If a combination other than above: High level

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

(2/4)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
DATA(31:16)/GPIO(31:16)	**Note 1**	**Note 1**	**Note 1**	**Note 2**	**Note 3**
DCD#/GPIO15	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DCTS#/GPIO35	Hi-Z	**Note 4**	**Note 4**	Hold	Hold
DDIN/GPIO34	Hi-Z	**Note 5**	**Note 5**	Hold	Hold
DDOUT/DBUS32/GPIO32	Hi-Z	**Note 6**	**Note 6**	Hold	Hold
DEVSEL#	Hi-Z	Hi-Z	Hi-Z	Hold	**Note 7**
DQM(3:0)	Hi-Z	0	0	**Note 2**	Hi-Z
DRTS#/MIPS16EN/GPIO33	Hi-Z	**Note 8**	**Note 8**	Hold	Hold
DSR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DTR#/CLKSEL0	Hi-Z	1	1	Hold	Hold
FIRCLK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
FIRDIN#/SEL	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
FRAME#	Hi-Z	Hi-Z	Hi-Z	Hold	**Note 7**

Notes 1. When the DBUS32 bit is 1: Low level
When the DBUS32 bit is 0: High impedance

2. Maintains the previous status.
For the pin status during the bus hold period, however, refer to the During Bus Hold column.

3. When the DBUS32 bit is 1: High impedance
When the DBUS32 bit is 0: Maintains the previous status

4. Depends on the status of the GIUPODATEN register's PIOEN35 bit.
When the PIOEN35 bit is 0: High impedance
When the PIOEN35 bit is 1: Maintains the status of the preceding Fullspeed mode

5. Depends on the status of the GIUPODATEN register's PIOEN34 bit.
When the PIOEN34 bit is 0: High impedance
When the PIOEN34 bit is 1: Maintains the status of the preceding Fullspeed mode

6. Depends on the status of the GIUPODATEN register's PIOEN32 bit.
When the PIOEN32 bit is 0: High level
When the PIOEN32 bit is 1: Maintains the status of the preceding Fullspeed mode

7. Normal operation

8. Depends on the status of the GIUPODATEN register's PIOEN33 bit.
When the PIOEN33 bit is 0: High level
When the PIOEN33 bit is 1: Maintains the status of the preceding Fullspeed mode

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

(3/4)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
GNT(2:0)#	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPIO(5:0)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPIO6/SYSDIR	0	**Note 1**	**Note 1**	**Note 2**	**Note 3**
GPIO(13:7)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
★ HLDAK#/NWIREEN	Hi-Z	0	0	Hold	0
HLDRQ#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IOCS(1:0)#	Hi-Z	Hi-Z	1	1	1
IORDY	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDOUT#/JTDO	0	0	0	0	0
IRDY#	Hi-Z	Hi-Z	Hi-Z	Hold	**Note 4**
JTCK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTDI/RMODE#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTMS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTRST#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
LEDOUT#	Hi-Z	1	1	1	**Note 4**
LOCK#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	**Note 4**
MPOWER	0	0	1	1	1
PAR	0	0	**Note 5**	Hold	**Note 4**
PCLK	0	0	0	Hold	**Note 4**
PERR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	**Note 4**
POWER	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
POWERON	0	0	0	0	0
RAS	0	0	0	**Note 2**	Hi-Z
RD#	Hi-Z	Hi-Z	1	**Note 2**	Hi-Z

Notes 1. Depends on the setting of the BCUCNTREG3 register's SYSDIR_EN bit.
When the SYSDIR_EN bit is 1: Low level
When the SYSDIR_EN bit is 0: High impedance

2. Maintains the previous status.
For the pin status during the bus hold period, however, refer to the During Bus Hold column.

3. Depends on the setting of the BCUCNTREG3 register's SYSDIR_EN bit.
When the SYSDIR_EN bit is 1: High impedance
When the SYSDIR_EN bit is 0: Maintains the previous status

4. Normal operation

5. Undefined. Drive either a low or high level.

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

(4/4)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
REQ(2:0)#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
ROMCS(1:0)#	Hi-Z	Hi-Z	1	1	1
RST#	0	0	0	Hold	**Note 1**
RSTSW#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
RTCRST#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
RTS#/CLKSEL1	Hi-Z	1	1	1	Hold
RxD	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SCLK	0	0	**Note 2**	**Note 3**	Hi-Z
SECLK	0	0	1	Hold	Hold
SERR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	**Note 4**
SIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SOUT	0	0	0	1	1
SPOWER	0	1	1	1	1
STOP#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	**Note 4**
SWR#	Hi-Z	0	0	**Note 3**	Hi-Z
TRDY#	Hi-Z	Hi-Z	Hi-Z	Hold	**Note 4**
TxD/CLKSEL2	Hi-Z	1	1	1	Hold
WR#	Hi-Z	Hi-Z	1	**Note 3**	Hi-Z

Notes 1. Maintains the previous status.

2. Outputs clock.

3. Maintains the previous status.
For the pin status during the bus hold period, however, refer to the During Bus Hold column.

4. Normal operation

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

1.3 Pin Handling and I/O Circuit Types

(1/2)

Pin Name	Pin Handling	Recommended Connection of Unused Pins	Drive Capability	I/O Circuit Type
AD(31:0)	–	Leave open	–	A
ADD(24:1)	–	–	**Note 1**	A
BATTINH/BATTINT#	–	–	–	B
BIGENDIAN	**Note 2**	Connect to V_{DD} or GND via a resistor or directly	–	A
BKTGIO#	–	Leave open	–	A
CAS	–	–	–	A
CBE(3:0)	–	Leave open	–	A
CKE(1:0)	–	–	120 pF	A
CLKOUT	–	Leave open	–	A
CLKRUN	Pull up	Connect to V_{DD} via a resistor	–	A
CS(1:0)#	–	–	120 pF	A
CS2#/ROMCS2#	–	Leave open	120 pF	A
CS3#/ROMCS3#	–	Leave open	120 pF	A
CTS#	–	Connect to V_{DD} or GND	–	A
DATA(15:0)	–	–	120 pF	A
DATA(31:16)/GPIO(31:16)	–	Connect to V_{DD} or GND via a resistor	120 pF	A
DCD#/GPIO15	–	Connect to V_{DD} via a resistor	–	B
DCTS#/GPIO35	–	Connect to V_{DD} or GND via a resistor	–	A
DDIN/GPIO34	–	Connect to V_{DD} or GND via a resistor	–	A
DDOUT/DBUS32/GPIO32	Pull up/pull down	–	–	A
DEVSEL#	Pull up	Connect to V_{DD} via a resistor	–	A
DQM(3:0)	–	–	120 pF	A
DRTS#/MIPS16EN/GPIO33	Pull up/pull down	–	–	A
DSR#	–	Connect to V_{DD} or GND	–	A
DTR#/CLKSEL0	Pull up/pull down	–	–	A
FIRCLK	–	Connect to V_{DD} via a resistor	–	A
FIRDIN#/SEL	–	Connect to V_{DD} or GND via a resistor	–	A
FRAME#	Pull up	Connect to V_{DD} via a resistor	–	A
GNT(2:0)#	–	Leave open	–	A
GPIO(5:0)	–	Connect to V_{DD} or GND via a resistor	–	B
GPIO6/SYSDIR	–	Leave open	–	B
GPIO(13:7)	–	Connect to V_{DD} or GND via a resistor	–	B
HLDAK#/NWIREEN	Pull down	Connect to GND via a resistor	–	A
HLDRQ#	Pull up	Leave open	–	A
IOCS(1:0)#	–	Leave open	–	A

Notes 1. The drive capability of ADD(4:1) is 120 pF and that of the other signals is 40 pF.

2. Pull the pin up or down. When pulling up, the pin must be connected to $V_{DD}3$ via a resistor. When pulling down, the pin may be directly connected to GND3.

Remarks 1. External handling is not required for the pins with no special directions in the Pin Handling column (–).

2. The pins with no special directions in the Recommended Connection of Unused Pins column are the pins that are always used.

(2/2)

Pin Name	Pin Handling	Recommended Connection of Unused Pins	Drive Capability	I/O Circuit Type
IORDY	–	Connect to V_{DD} or GND via a resistor	–	A
IRDIN	–	Connect to V_{DD} or GND via a resistor	–	A
IRDOUT#/JTDO	–	Leave open	–	A
IRDY#	Pull up	Connect to V_{DD} via a resistor	–	A
JTCK	Pull up	Connect to V_{DD} or GND	–	B
JTDI/RMODE#	Pull up	Connect to V_{DD} via a resistor	–	A
JTMS	Pull up	Connect to V_{DD} or GND	–	A
JTRST#	–	Leave open	–	A
LEDOUT#	Pull up[Note]	Connect to V_{DD} via a resistor[Note]	–	A
LOCK#	Pull up	Connect to V_{DD} via a resistor	–	A
MPOWER	–	–	–	A
PAR	–	Leave open	–	A
PCLK	–	Leave open	–	A
PERR#	Pull up	Connect to V_{DD} via a resistor	–	A
POWER	–	–	–	B
POWERON	–	–	–	A
RAS	–	–	–	A
RD#	–	–	–	A
REQ(2:0)#	–	Connect to V_{DD}	–	A
ROMCS(1:0)#	–	Leave open	120 pF	A
RST#	–	Leave open	–	A
RSTSW#	–	–	–	B
RTCRST#	–	–	–	B
RTS#/CLKSEL1	Pull up/pull down	–	–	A
RxD	–	Connect to V_{DD} or GND	–	A
SCLK	–	–	120 pF	A
SECLK	–	Leave open	–	A
SERR#	Pull up	Connect to V_{DD} via a resistor	–	A
SIN	–	Connect to V_{DD} or GND	–	A
SOUT	–	Leave open	–	A
SPOWER	–	–	–	A
STOP#	Pull up	Connect to V_{DD} via a resistor	–	A
SWR#	–	–	–	A
TRDY#	Pull up	Connect to V_{DD} via a resistor	–	A
TxD/CLKSEL2	Pull up/pull down	–	–	A
WR#	–	Leave open	–	A

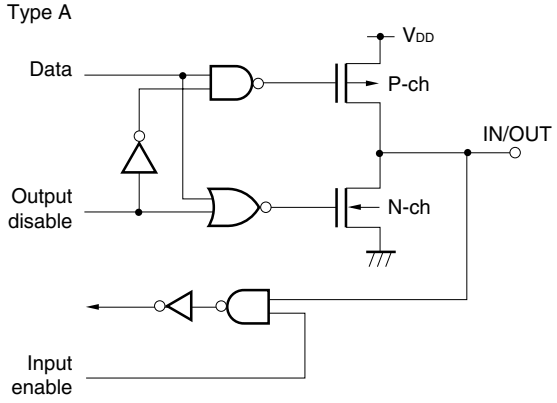
Note LEDOUT# pin has to be pulled up regardless of whether the LED function is being used.

Remarks 1. External handling is not required for the pins with no special directions in the Pin Handling column (–).

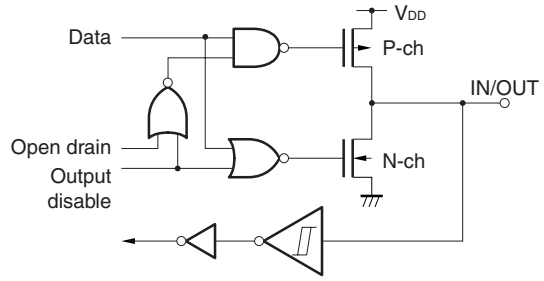
2. The pins with no special directions in the Recommended Connection of Unused Pins column are the pins that are always used.

1.4 Pin I/O Circuits

Type A



Type B



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD1}	Applies to V_{DD}P, V_{DD}PD, and V_{DD}1 pins	−0.5 to +1.8	V
	V_{DD3}	Applies to CV_{DD} and V_{DD}3 pins	−0.5 to +4.0	V
Input voltage	V_I	$V_{DD3} \geq 3.7$ V	−0.5 to +4.0	V
		$V_{DD3} < 3.7$ V	−0.5 to V_{DD3} + 0.3	V
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be −1.5 V if the input pulse is less than 10 ns.

Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD1}	Applies to V_{DD}P, V_{DD}PD, and V_{DD}1 pins	1.35	1.65	V
	V_{DD3}	Applies to CV_{DD} and V_{DD}3 pins	3.0	3.6	V
Ambient temperature	T_A		−40	+85	°C
Oscillation start voltage[Note 1]	V_{DDS}			3.0	V
Oscillation hold voltage[Note 2]	V_{DDH1}			2.5	V
Oscillation hold voltage[Note 3]	V_{DDH2}			3.0	V

Notes 1. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

2. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V.		10	pF
I/O capacitance	C_{IO}			10	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD1} = 1.35 to 1.65 V, V_{DD3} = 3.0 to 3.6 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2 mA	0.8V_{DD3}			V
Output voltage, low	V_{OL1}	I_{OL} = 2 mA			0.4	V
Clock input voltage, high[Note 1]	V_{IH1}		0.8V_{DD3}		V_{DD3} + 0.3	V
Clock input voltage, low[Note 1]	V_{IL1}		–0.3		0.3V_{DD3}	V
		Pulse under 10 ns[Note 2]	–1.5		0.3V_{DD3}	V
Input voltage, high[Note 3]	V_{IH2}		2.0		V_{DD3} + 0.3	V
Input voltage, low[Note 3]	V_{IL2}		–0.3		0.3V_{DD3}	V
		Pulse under 10 ns[Note 2]	–1.5		0.3V_{DD3}	V
Input voltage, high[Note 4]	V_{IH3}		0.85V_{DD3}		V_{DD3} + 0.3	V
Input voltage, low[Note 4]	V_{IL3}		–0.3		0.6	V
		Pulse under 10 ns[Note 2]	–1.5		0.3V_{DD3}	V
Hysteresis voltage[Notes 4, 5]	V_H			0.17V_{DD3}		V
Input leakage current	I_{LI}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V			±5	μA
Output leakage current	I_{LO}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V			±5	μA

Notes 1. Applies to FIRCLK pin.

2. Precision tests have not been performed. Only guaranteed as design characteristics.

3. Except RTCX1, CLKX1, FIRCLK, POWER, RSTSW#, RTCRST#, DCD#/GPIO15, GPIO(13:0), and BATTINH/BATTINT# pins.

4. Applies to POWER, RSTSW#, RTCRST#, DCD#/GPIO15, GPIO(13:0), and BATTINH/BATTINT# pins.

5. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

(2/2)

Parameter	Symbol	Condition	MIN.	TYP.[Note 1]	MAX.	Unit
Supply current	I_{DD1}[Note 2]	In Fullspeed mode		145	240	mA
		In Standby mode		48	97	mA
		In Suspend mode		7	20	mA
		In Exsuspend mode		0.8	10	mA
		In Hibernate mode, V_{DD1} = 0.0 V, when LED unit is off.		0	0	μA
	I_{DD3}[Note 3]	In Fullspeed mode		30	60	mA
		In Standby mode		15	45	mA
		In Suspend mode		3.5	10.5	mA
		In Exsuspend mode		3.5	10.5	mA
		In Hibernate mode, when LED unit is off.		200	500	μA

Notes 1. Unless otherwise specified, these are reference values at T_A = 25°C, V_{DD1} = 1.5 V, V_{DD3} = 3.3 V.

2. Total current flowing to the V_{DD}P, V_{DD}PD, and V_{DD}1 pins.

3. Total current flowing to the CV_{DD} and V_{DD}3 pins.

Remarks 1. In the Fullspeed mode, the maximum values of I_{DD1} and I_{DD3} are not generated at the same time.

2. A current over the TYP. value may flow depending on the usage conditions, so consider the MAX. value of the supply current when designing the power supplies.

3. I_{DD1} in the Fullspeed mode is in proportion to the CPU core frequency (f_{PCYC}). Therefore, the TYP. value of I_{DD1} becomes as follows depending on the CPU core frequency.

Supply current (I_{DD1}) = 145 × f_{PCYC}/199.1 (mA)

Data Retention Characteristics (T_A = 25°C)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data retention voltage[Note]	V_{DDDR3}	Hibernate mode	2.5	3.6	V
Data retention input voltage, high	V_{IHDR}	Applies to RTCRST# pin	$0.9V_{DDDR3}$		V

Note The data retention voltage is the voltage at which the operation of the ElapsedTime counter and the data retention of the registers of the following peripheral units are guaranteed, and is not applied to the internal data of the CPU core. It is applied to the 3.3 V power supply (CV_{DD}, $V_{DD}3$).

BCU: BCUCNTREG3

PMU: PMUCNTREG(15:8), PMUCNT2REG, PMUWAITREG, PMUTCLKDIVREG, PMUINTRCLKDIVREG

RTC: ETIMELREG, ETIMEMREG, ETIMEHREG, ECMPLREG, ECMPMREG, ECMPHREG, RTCL1LREG, RTCL1HREG, RTCL1CNTLREG, RTCL1CNTHREG, RTCL2LREG, RTCL2HREG, RTCL2CNTLREG, RTCL2CNTHREG, RTCINTREG(2:0)

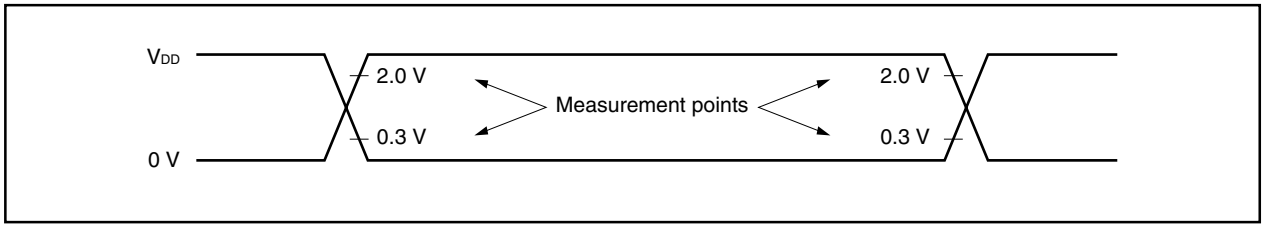
GIU: GIUPODATL, GIUPODATEN

LED: LEDHTSREG, LEDLTSREG, LEDCNTREG

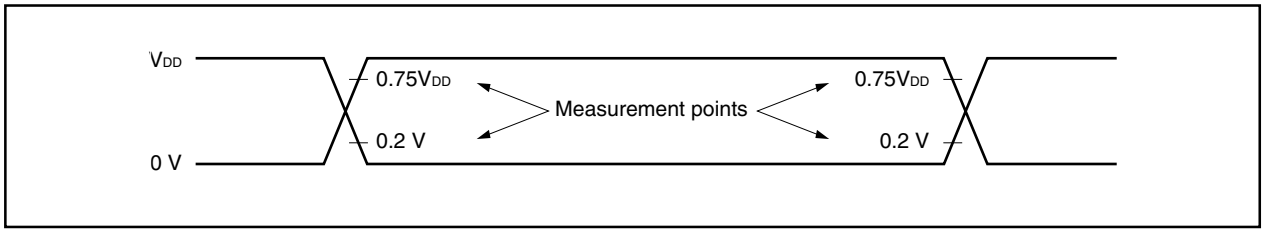
AC Characteristics (T_A = –40 to +85°C)

AC test input waveform

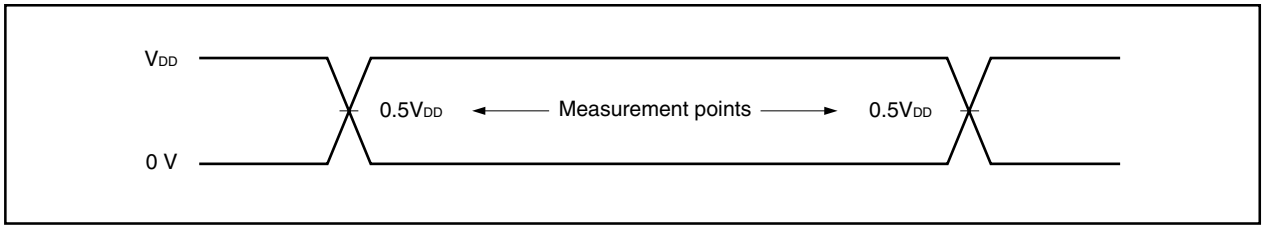
(a) DATA(15:0), DATA(31:16)/GPIO(31:16), IORDY, RxD, CTS#, DSR#, TxD/CLKSEL2, FIRCLK, RTS#/CLKSEL1, DTR#/CLKSEL0, IRDIN, FIRDIN#/SEL, DDIN/GPIO34, DCTS#/GPIO35, DDOUT/DBUS32/GPIO32, AD(31:0), CBE(3:0), DEVSEL#, FRAME#, REQ(2:0)#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, CLKRUN, DRTS#/MIPS16EN/GPIO33, SIN, HLDRQ#, JTDI/RMODE#, BKTGIO#, HLDAK#/NWIREEN



(b) BATTINH/BATTINT#, DCD#/GPIO15, GPIO(13:7), SYSDIR/GPIO6, GPIO(5:0), POWER, RSTSW#, RTCRST#, JTCK, JTMS, JTRST#, BIGENDIAN

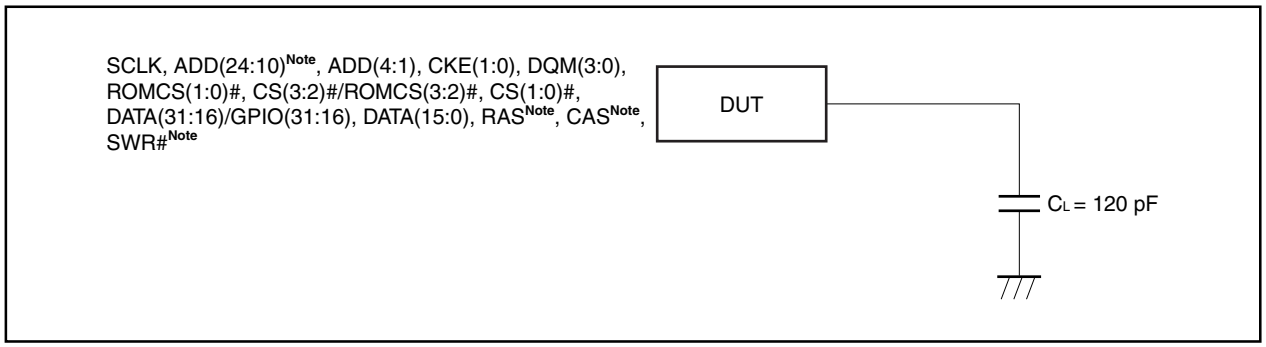


AC test output measurement points



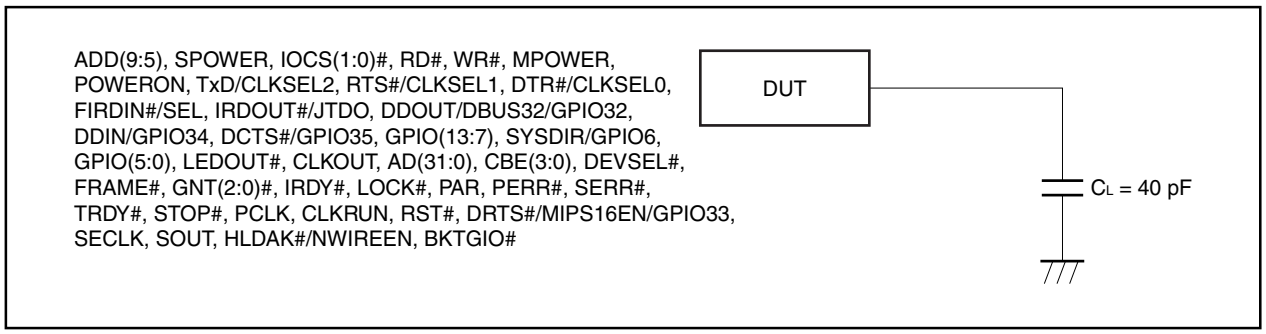
Load conditions

(a) SCLK, ADD(24:10)[Note], ADD(4:1), CKE(1:0), DQM(3:0), ROMCS(1:0)#, CS(3:2)#/ROMCS(3:2)#, CS(1:0)#, DATA(31:16)/GPIO(31:16), DATA(15:0), RAS[Note], CAS[Note], SWR#[Note]



Note The ADD(24:10), RAS, CAS, and SWR# pins are low-drive-capacity pins. These pins are measurement using 120 pF, but designing with an external load of 40 pF or lower is recommended.

(b) ADD(9:5), SPOWER, IOCS(1:0)#, RD#, WR#, MPOWER, POWERON, TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0, FIRDIN#/SEL, IRDOUT#/JTDO, DDOUT/DBUS32/GPIO32, DDIN/GPIO34, DCTS#/GPIO35, GPIO(13:7), SYSDIR/GPIO6, GPIO(5:0), LEDOUT#, CLKOUT, AD(31:0), CBE(3:0), DEVSEL#, FRAME#, GNT(2:0)#, IRDY#, LOCK#, PAR, PERR#, SERR#, TRDY#, STOP#, PCLK, CLKRUN, RST#, DRTS#/MIPS16EN/GPIO33, SECLK, SOUT, HLDAK#/NWIREEN, BKTGIO#



(1) Clock parameters

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FIRCLK clock frequency[Note 1]	$f_{FIRCYC1}$	In FIR 4 Mbps	47.99520	48	48.00480	MHz
	$f_{FIRCYC2}$	In FIR 1.152/0.576 Mbps	47.93800	48	48.02976	MHz
FIRCLK clock duty[Note 1]	$t_{FIRDUTY}$		10		90	%
SCLK high-level width[Note 2]	t_{CH}		3.5			ns
SCLK low-level width[Note 2]	t_{CL}		3.5			ns
SCLK jitter[Note 3]	t_{Jitter}				3.5	%
CPU core operating frequency	f_{PCYC}	CLKSEL(2:0) = 111[Note 4]		RFU		MHz
		CLKSEL(2:0) = 110		199.1		MHz
		CLKSEL(2:0) = 101		180.9		MHz
		CLKSEL(2:0) = 100		165.8		MHz
		CLKSEL(2:0) = 011		153.1		MHz
		CLKSEL(2:0) = 010		132.7		MHz
		CLKSEL(2:0) = 001		99.5		MHz
		CLKSEL(2:0) = 000[Note 4]		RFU		MHz

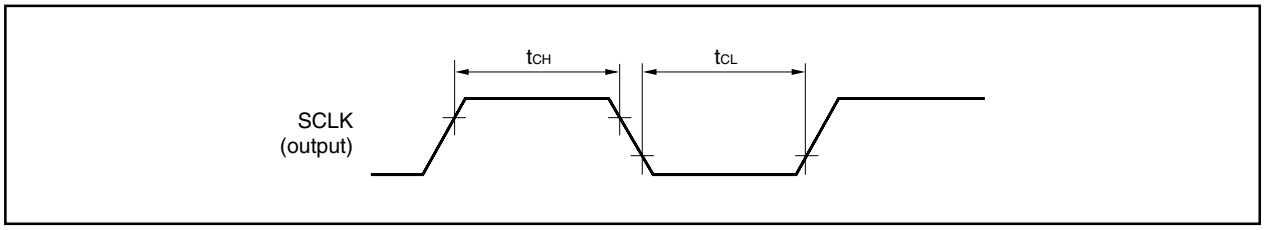
Notes 1. Applies to the FIRCLK pin.

2. Applies to the SCLK pin.

3. Precision tests have not been performed. Only guaranteed as design characteristics.

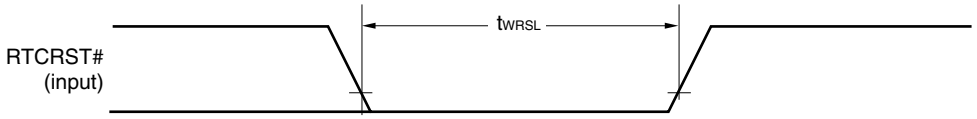
4. Do not set CLKSEL(2:0) = 111, 000.

Remark CLKSEL(2:0): Value set to the TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins after reset



(2) Reset parameters

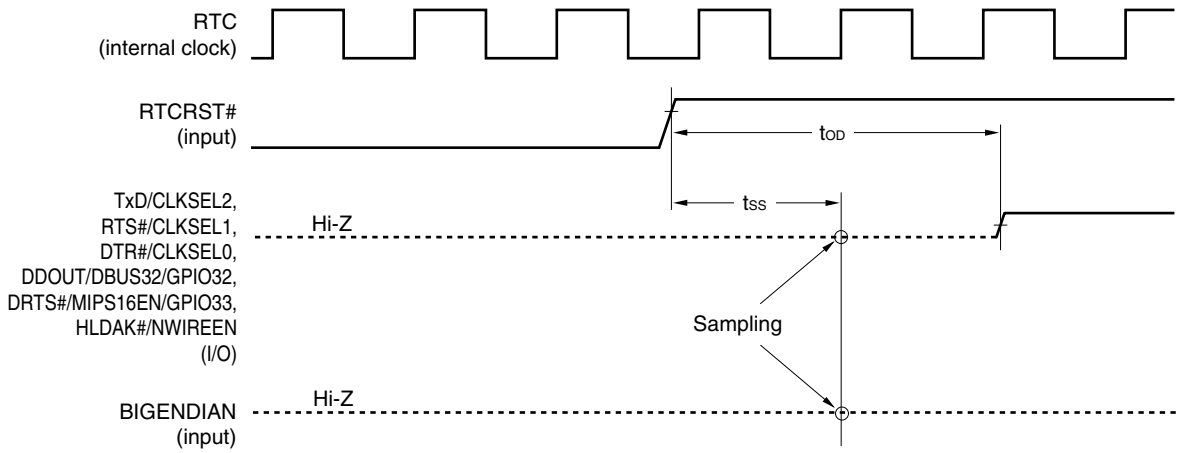
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	Applies to RTCRST# pin	305		μs



Remark For the RTCRST# characteristics at power application, refer to **VR4131 Hardware User's Manual**.

(3) Initialization parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RTCRST# ↑)	t_{SS}			61.04	μs
Output delay time (from RTCRST# ↑)	t_{OD}		61.04		μs



Remark Set the input data level by using a pull-up or pull-down resistor with high resistance.

(4) GPIO interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width[Note 1]	t_{INP1}	**Note 2**	326 × N		ns
GPIO input rise time	t_{GPINR1}	**Note 3**		200	ns
	t_{GPINR2}	**Note 4**		10	ns
GPIO input fall time	t_{GPINF1}	**Note 3**		200	ns
	t_{GPINF2}	**Note 4**		10	ns
Output level width	t_{OUTP}	**Note 5**	30		ns

Notes 1. The N value is set using the IDIV(1:0) bits of the PMUINTRCLKDIVREG register.

IDIV(1:0)	N
11	RFU
10	4
01	8
00	2

2. Applies to the GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), DCD#/GPIO15, and DATA(31:16)/GPIO(31:16) pins.

3. Applies to the GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), and DCD#/GPIO15 pins.

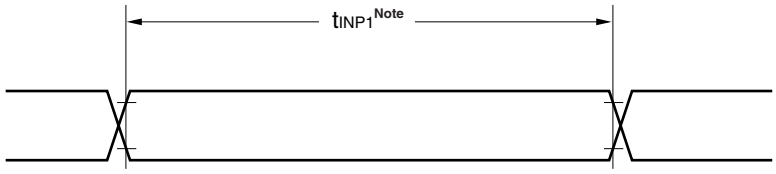
4. Applies to the DATA(31:16)/GPIO(31:16) pins.

5. Applies to the GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), DATA(31:16)/GPIO(31:16), DDOUT/DBUS32/GPIO32, DRTS#/MIPS16EN/GPIO33, DDIN/GPIO34, and DCTS#/GPIO35 pins.

Caution These parameters apply when the SYSDIR/GPIO6, DATA(31:16)/GPIO(31:16), DDOUT/DBUS32/GPIO32, DRTS#/MIPS16EN/GPIO33, DDIN/GPIO34, or DCTS#/GPIO35 pin is used as a GPIO signal.

(4) GPIO interface parameters (2/2)

(a) Input level width

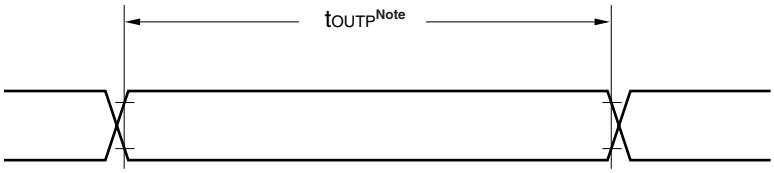


Note GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), DCD#/GPIO15, DATA(31:16)/GPIO(31:16) pins

(b) GPIO input rise/fall time

Notes 1. GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), DCD#/GPIO15 pins
2. DATA(31:16)/GPIO(31:16) pins

(c) Output level width



Note GPIO(5:0), SYSDIR/GPIO6, GPIO(13:7), DATA(31:16)/GPIO(31:16), DDOUT/DBUS32/GPIO32, DRTS#/MIPS16EN/GPIO33, DDIN/GPIO34, DCTS#/GPIO35 pins

(5) Normal ROM parameters (1/2)

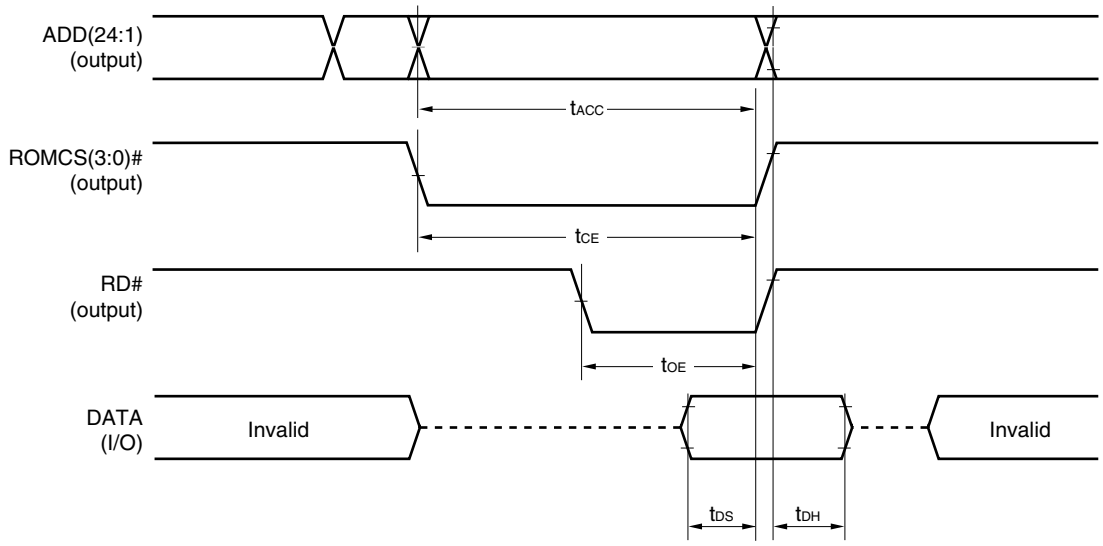
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}		T × N – 19		ns
Data access time (from ROMCS(3:0)# ↓)[Note]	t_{CE}		T × N – 19		ns
Data access time (from RD# ↓)[Note]	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

Note The value of N is set by using the rom2_wait(3:0) bits of the ROMSPEEDREG register.
The value of T is set by using the CLKSEL(2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register.

rom2_wait(3:0)	N	rom2_wait(3:0)	N
1111	18	0111	10
1110	17	0110	9
1101	16	0101	8
1100	15	0100	7
1011	14	0011	6
1010	13	0010	5
1001	12	0001	4
1000	11	0000	3

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	RFU	RFU	10.0	15.1	20.1	25.1	30.1	RFU
101	RFU	RFU	11.1	16.6	22.1	27.6	33.2	RFU
100	RFU	RFU	12.1	18.1	24.1	30.1	36.2	RFU
011	RFU	RFU	13.1	19.6	26.1	32.7	RFU	RFU
010	RFU	RFU	15.1	22.6	30.1	37.7	RFU	RFU
001	10.0	RFU	20.1	30.1	RFU	RFU	RFU	RFU
000	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

(5) Normal ROM parameters (2/2)



Remark The broken lines indicate high impedance.

(6) Page ROM parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC1}		T × N – 19		ns
	t_{ACC2}		T × M – 8		ns
Data access time (from ROMCS(3:0)# ↓)[Note]	t_{CE}		T × N – 19		ns
Data access time (from RD# ↓)[Note]	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns

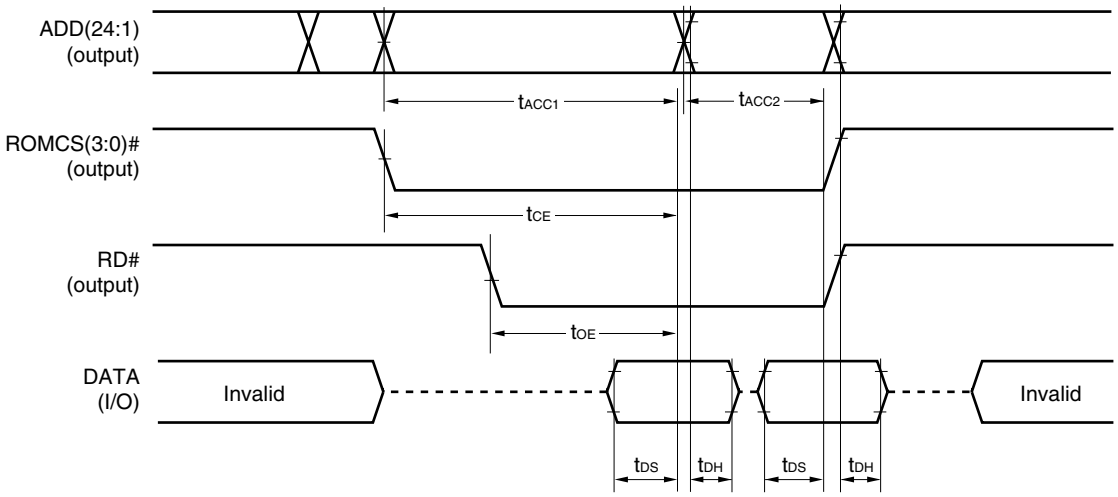
Note The value of N is set by using the rom2_wait(3:0) bits of the ROMSPEEDREG register.
The value of M is set by using the rom4_wait(1:0) bits of the ROMSPEEDREG register.
The value of T is set by using the CLKSEL(2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register.

rom2_wait(3:0)	N	rom2_wait(3:0)	N
1111	18	0111	10
1110	17	0110	9
1101	16	0101	8
1100	15	0100	7
1011	14	0011	6
1010	13	0010	5
1001	12	0001	4
1000	11	0000	3

rom4_wait(1:0)	M
11	5
10	4
01	3
00	2

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	RFU	RFU	10.0	15.1	20.1	25.1	30.1	RFU
101	RFU	RFU	11.1	16.6	22.1	27.6	33.2	RFU
100	RFU	RFU	12.1	18.1	24.1	30.1	36.2	RFU
011	RFU	RFU	13.1	19.6	26.1	32.7	RFU	RFU
010	RFU	RFU	15.1	22.6	30.1	37.7	RFU	RFU
001	10.0	RFU	20.1	30.1	RFU	RFU	RFU	RFU
000	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

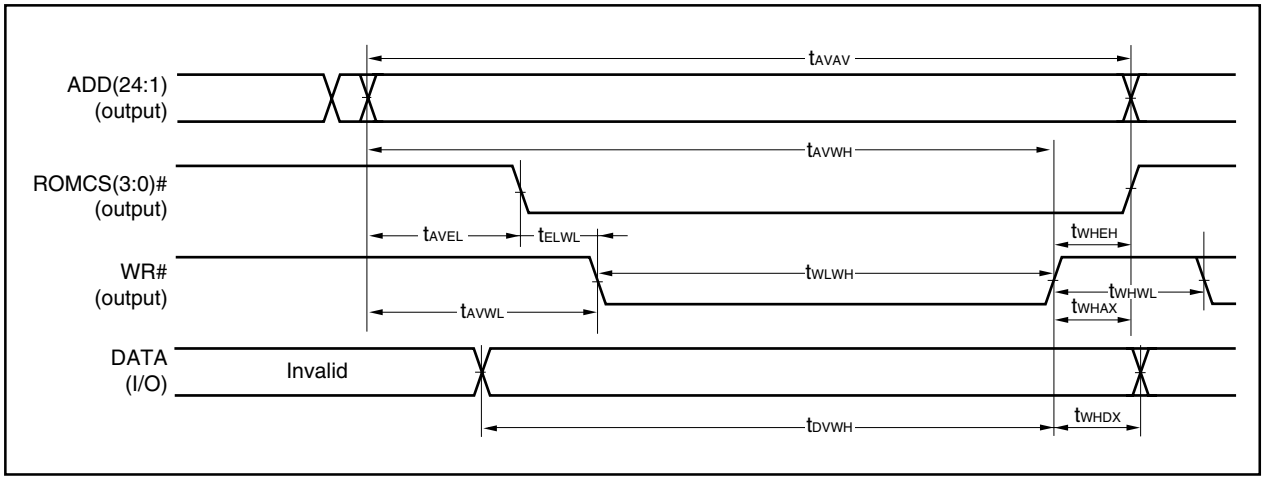
(6) Page ROM parameters (2/2)



Remark The broken lines indicate high impedance.

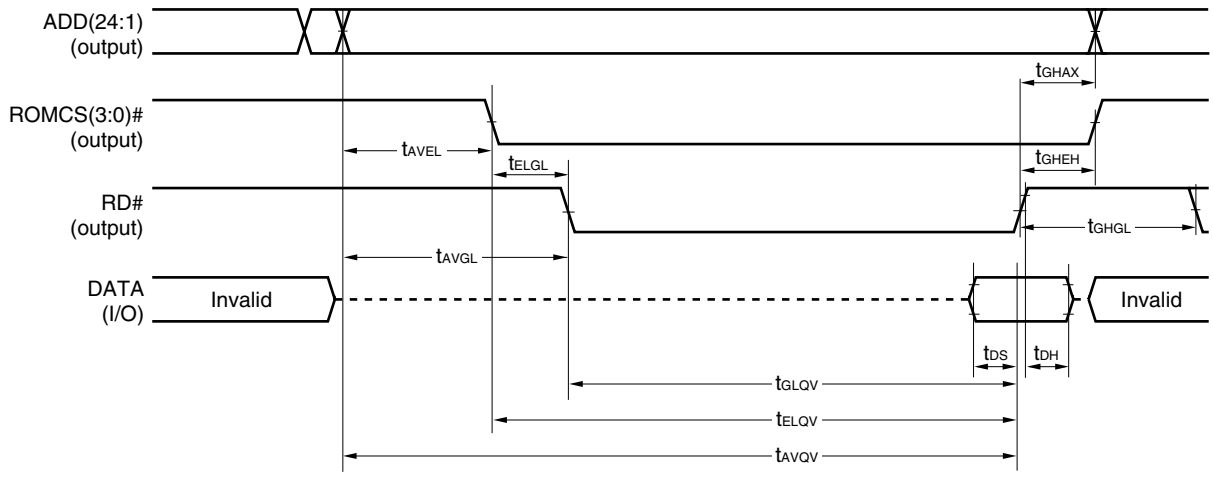
(7) Flash memory mode write parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write cycle time	t_{AVAV}		150		ns
Address setup time (to WR# ↑)	t_{AVWH}		75		ns
Address setup time (to ROMCS(3:0)# ↓)	t_{AVEL}		0		ns
ROMCS(3:0)# setup time (to WR# ↓)	t_{ELWL}		10		ns
WR# low-level width	t_{WLWH}		75		ns
ROMCS(3:0)# hold time (from WR# ↑)	t_{WHEH}		10		ns
Address hold time (from WR# ↑)	t_{WHAX}		10		ns
WR# high-level width	t_{WHWL}		75		ns
Address setup time (to WR# ↓)	t_{AVWL}		25		ns
Data output setup time (to WR# ↑)	t_{DVWH}		75		ns
Data output hold time (from WR# ↑)	t_{WHDX}		10		ns



(8) Flash memory mode read parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time from address	t_{AVQV}		180		ns
Data output delay time from ROMCS(3:0)#	t_{ELQV}		180		ns
Address setup time (to ROMCS(3:0)# ↓)	t_{AVEL}		0		ns
Data output delay time from RD# ↓	t_{GLQV}		80		ns
Address setup time (to RD# ↓)	t_{AVGL}		0		ns
ROMCS(3:0)# hold time (from RD# ↑)	t_{GHEH}		10		ns
Address hold time (from RD# ↑)	t_{GHAX}		10		ns
RD# high-level width	t_{GHGL}		75		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		5		ns
ROMCS(3:0)# setup time (to RD# ↓)	t_{ELGL}		10		ns



Remark The broken lines indicate high impedance.

(9) I/O (LCD) interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)[Notes 1, 2]	t_{AS}		T × K – 15		ns
Address hold time (from command signal ↑)[Notes 1, 2]	t_{AH}		T × N – 15		ns
Command signal recovery time[Notes 1, 2]	t_{RY}		T × (N + 1) – 15		ns
IORDY sampling start time[Note 2]	t_{CLR}		T × L – 15		ns
Command signal delay time from IORDY ↑[Notes 1, 2]	t_{RHCH}		T × M – 15	T × (M + 2) + 15	ns
IORDY hold time (from command signal ↑)[Note 1]	t_{RYZ}		0		ns
Data output setup time (to command signal ↓)[Notes 1, 2]	t_{DSTC}		T × (K – 1) – 15		ns
Data output setup time (to command signal ↑)[Notes 1, 2]	t_{DVCH}		T×(K+L+M–1)–15		ns
Data output hold time (from command signal ↑)[Notes 1, 2]	t_{CHDV}		T × N		ns
Data input setup time (to command signal ↑)[Note 1]	t_{DS}		0		ns
Data input hold time (from command signal ↑)[Note 1]	t_{DH}		5		ns

Notes 1. With the V_R4131, the RD# and WR# signals are called the command signals for the LCD interface.

2. The values of K, L, M, and N are set by using the ion_1_wait(3:0) bits, ion_2_wait(3:0) bits, ion_3_wait(3:0) bits, and ion_5_wait(1:0) bits, respectively, of the IOnSPEEDREG register. The value of T is set by using the CLKSEL(2:0) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register (n = 0, 1).

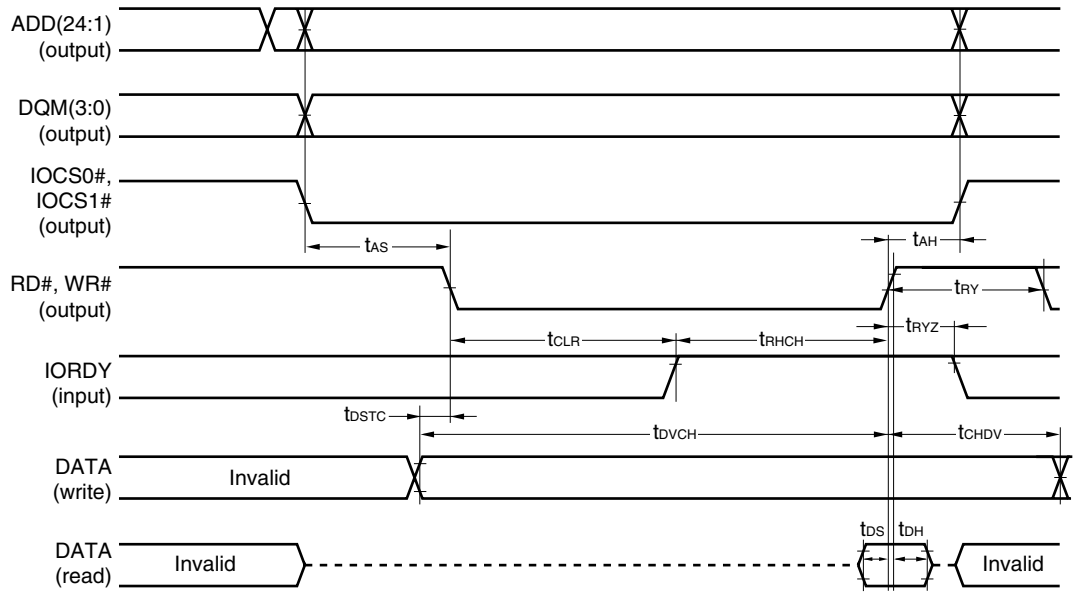
ion_1_wait(3:0) ion_2_wait(3:0) ion_3_wait(3:0)	K (ion_1_wait(3:0))	L (ion_2_wait(3:0))	M (ion_3_wait(3:0))
1111	16	14	18
1110	15	13	17
1101	14	12	16
1100	13	11	15
1011	12	10	14
1010	11	9	13
1001	10	8	12
1000	9	7	11
0111	8	6	10
0110	7	5	9
0101	6	4	8
0100	5	3	7
0011	4	2	6
0010	3	1	5
0001	2	0	4
0000	1	–1	3

ion_5_wait(1:0)	N
11	4
10	3
01	2
00	1

Remark n = 0, 1

(9) I/O (LCD) interface parameters (2/2)

CLKSEL(2:0) \ VTDIV(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	RFU	RFU	10.0	15.1	20.1	25.1	30.1	RFU
101	RFU	RFU	11.1	16.6	22.1	27.6	33.2	RFU
100	RFU	RFU	12.1	18.1	24.1	30.1	36.2	RFU
011	RFU	RFU	13.1	19.6	26.1	32.7	RFU	RFU
010	RFU	RFU	15.1	22.6	30.1	37.7	RFU	RFU
001	10.0	RFU	20.1	30.1	RFU	RFU	RFU	RFU
000	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU



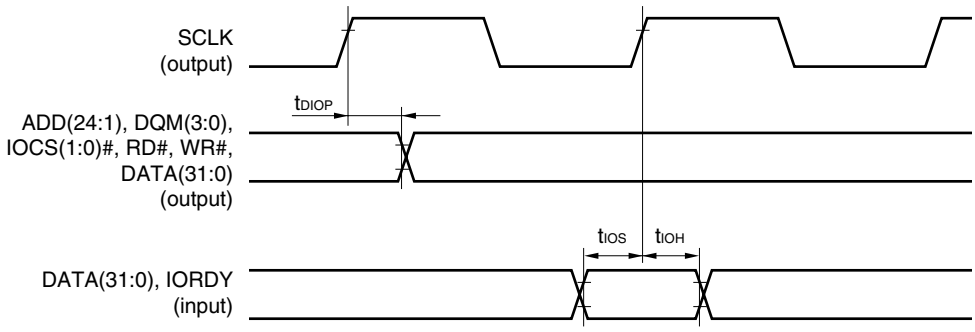
Remark The broken lines indicate high impedance.

(10) IOCS interface parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output delay time (from SCLK ↑)Note 1	t_{DIOP}		1.1	11.7	ns
Data input setup time (to SCLK ↑)Note 2	t_{IOS}		6.2		ns
Data input hold time (from SCLK ↑)Note 2	t_{IOH}		2.9		ns

Notes 1. Applies to the ADD(24:1), DQM(3:0), IOCS(1:0), RD#, WR#, and DATA(31:0) pins.

2. Applies to the IORDY and DATA(31:0) pins.

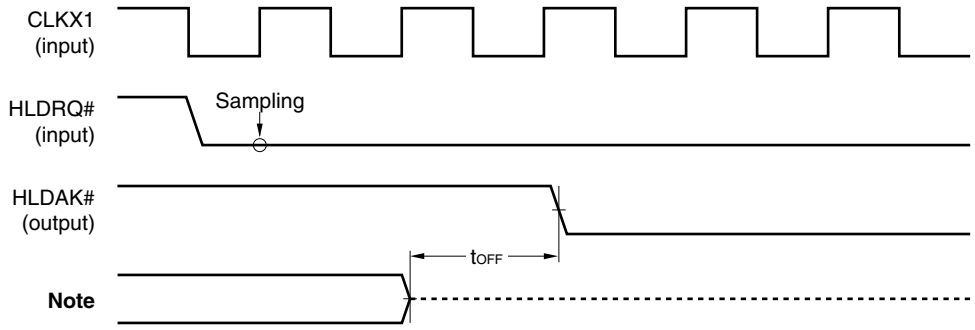


(11) Bus hold parameters (1/3)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
HLDRQ# input pulse width[Note]	t_{HP}	In Fullspeed/Standby/Suspend mode	271		ns
Data floating delay time	t_{OFF}	In Fullspeed/Standby/Suspend mode	0		ns
Data valid delay time	t_{ON}	In Fullspeed/Standby/Suspend mode	0		ns

Note When the VR4131 receives an input signal of less than 271 ns, the bus hold operation may malfunction. Change the signal input to the HLDRQ# pin to one with a pulse width of 271 ns or more.

(a) Starting bus hold



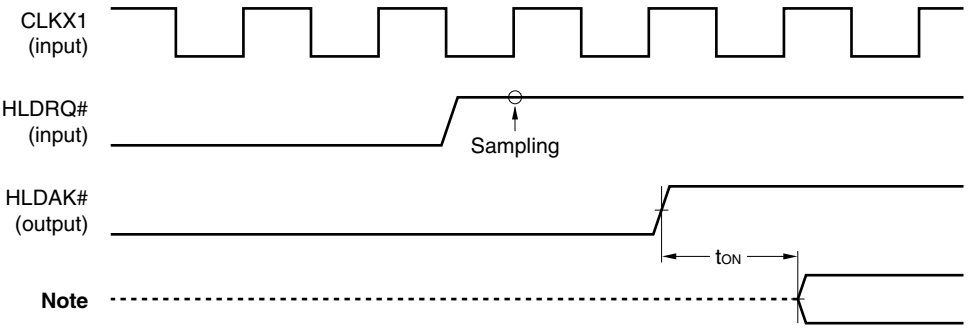
Note Applies to the following pins.

- ADD(24:1), DATA(15:0), CKE(1:0), DQM(3:0), CS(1:0)#, RAS, CAS, SCLK, RD#, WR#, and SWR# pins
- SYSDIR/GPIO6 pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA(31:16)/GPIO(31:16) pins in 32-bit data bus mode
- CS(3:2)#/ROMCS(3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode

Remark The broken lines indicate high impedance.

(11) Bus hold parameters (2/3)

(b) Releasing bus hold (HLDRQ#)



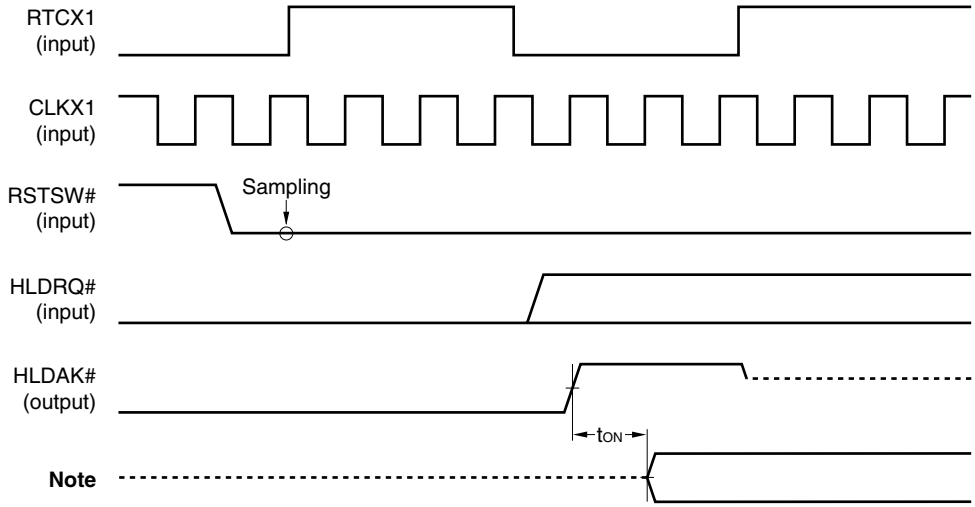
Note Applies to the following pins.

- ADD(24:1), DATA(15:0), CKE(1:0), DQM(3:0), CS(1:0)#, RAS, CAS, SCLK, RD#, WR#, and SWR# pins
- SYSDIR/GPIO6 pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA(31:16)/GPIO(31:16) pins in 32-bit data bus mode
- CS(3:2)#/ROMCS(3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode

Remark The broken lines indicate high impedance.

(11) Bus hold parameters (3/3)

(c) Releasing bus hold (RSTSW#)



Note Applies to the following pins.

- ADD(24:1), DATA(15:0), CKE(1:0), DQM(3:0), CS(1:0)#, RAS, CAS, SCLK, RD#, WR#, and SWR# pins
- SYSDIR/GPIO6 pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA(31:16)/GPIO(31:16) pins in 32-bit data bus mode
- CS(3:2)#/ROMCS(3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode

Remark The broken lines indicate high impedance.

(12) Serial interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
TxD output pulse width[Note]	t_{TXD}		N – 0.1	N + 0.1	μs
RxD input pulse width[Note]	t_{RXD}		(9/16) × N		μs
IRDOUT# high-level output pulse width[Note]	t_{IRDOUT}		(3/16) × N – 0.1	(3/16) × N + 0.1	μs
IRDIN input pulse width	t_{IRDIN}		1		μs

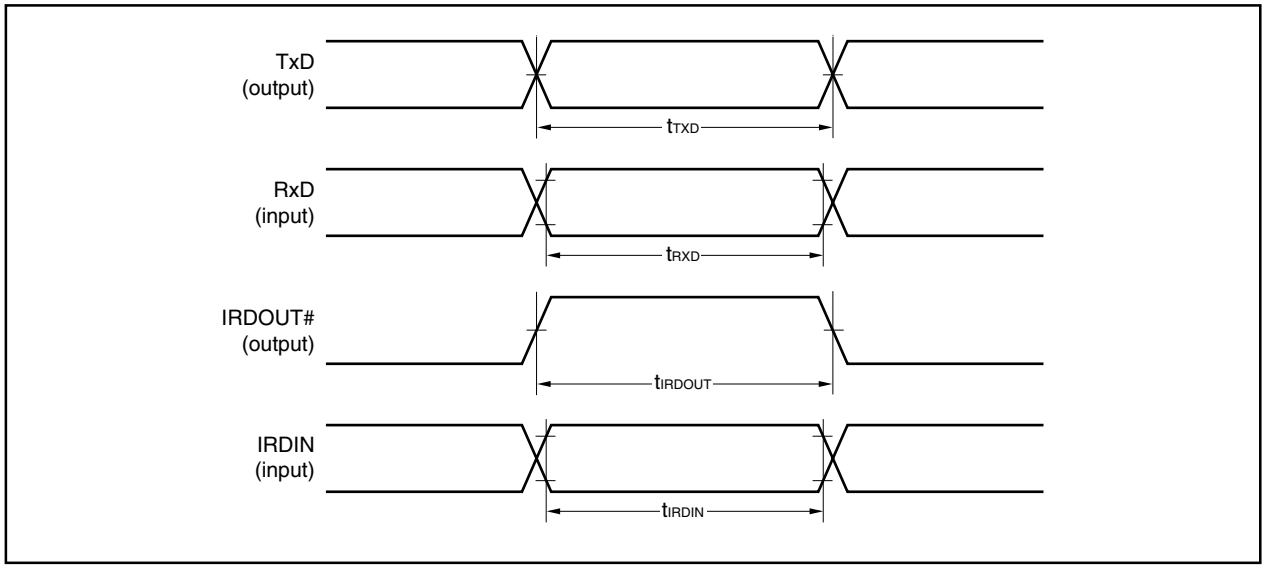
Note N indicates the data transfer cycle per bit, which is determined by the divisor of the baud rate generator that is set with the SIUDLL and SIUDLM registers.

★

Baud Rate (bps)	Divisor (SIUDLM, SIUDLL Registers)	N (μs)
50	23,040	20,000.00
75	15,360	13,333.33
110	10,473	9,090.91
134.5	8,565	7,434.94
150	7,680	6,666.67
300	3,840	3,333.33
600	1,920	1,666.67
1,200	960	833.33
1,800	640	555.56
2,000	576	500.00
2,400	480	416.67
3,600	320	277.78
4,800	240	208.33
7,200	160	138.89
9,600	120	104.17
19,200	60	52.08
38,400	30	26.04
57,600	20	17.36
115,200	10	8.68

Remark Baud rate = (18.432 MHz/16)/(value set in the SIUDLM and SIUDLL registers)

(12) Serial interface parameters (2/2)



(13) Debug serial interface parameters

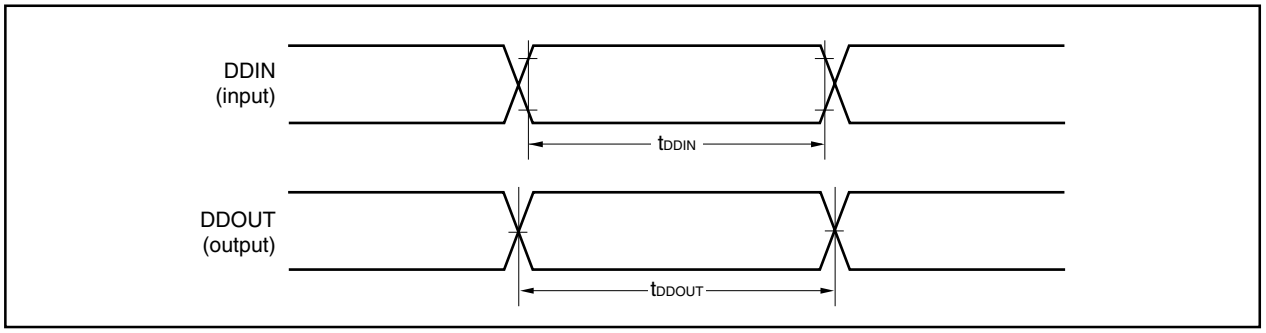
Parameter	Symbol	Condition	MIN.	MAX.	Unit
DDOUT output pulse width[Note]	t_{DDOUT}		N – 0.1	N + 0.1	μs
DDIN input pulse width[Note]	t_{DDIN}		(9/16) × N		μs

Note N indicates the data transfer cycle per bit, which is determined by the divisor of the baud rate generator that is set with the DSIUDLL and DSIUDLM registers.

★

Baud Rate (bps)	Divisor (DSIUDLM, DSIUDLL Registers)	N (μs)
50	23,040	20,000.00
75	15,360	13,333.33
110	10,473	9,090.91
134.5	8,565	7,434.94
150	7,680	6,666.67
300	3,840	3,333.33
600	1,920	1,666.67
1,200	960	833.33
1,800	640	555.56
2,000	576	500.00
2,400	480	416.67
3,600	320	277.78
4,800	240	208.33
7,200	160	138.89
9,600	120	104.17
19,200	60	52.08
38,400	30	26.04
57,600	20	17.36
115,200	10	8.68

Remark Baud rate = (18.432 MHz/16)/(value set in the DSIUDLM and DSIUDLL registers)



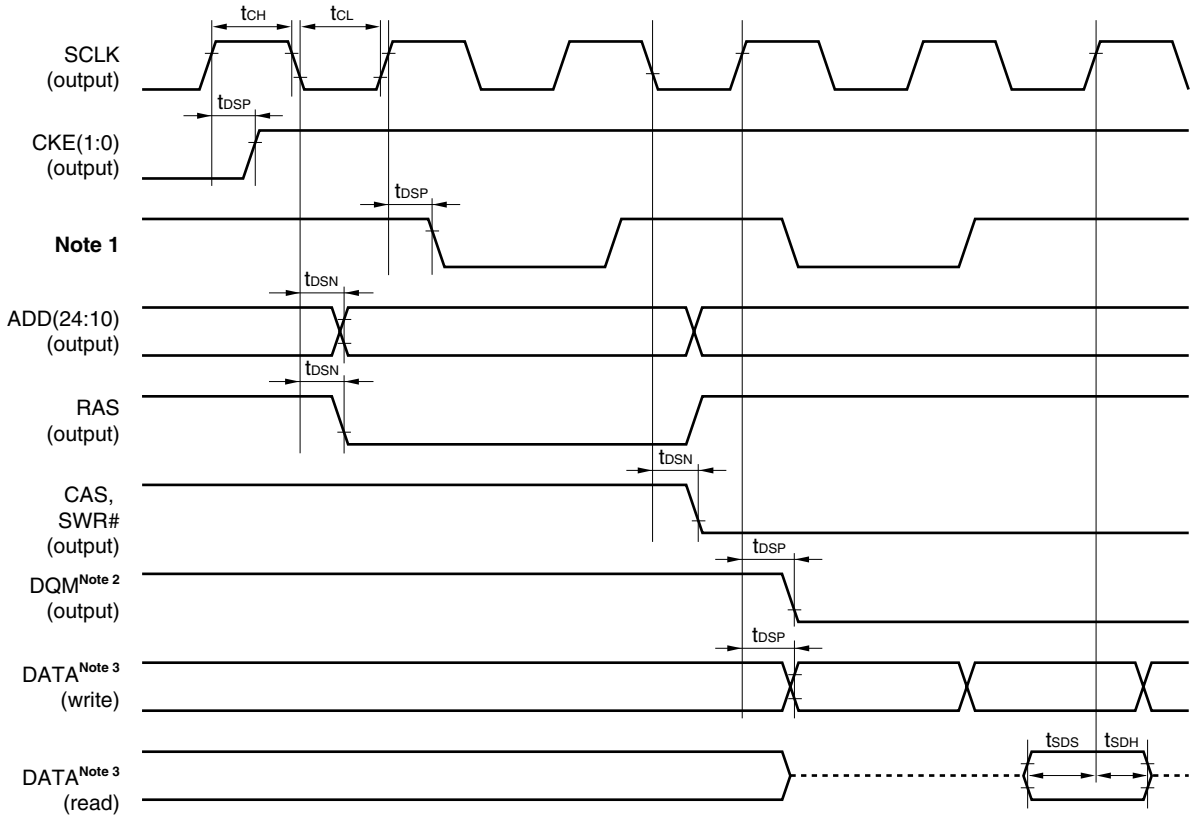
(14) SDRAM interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCLK jitter[Note]	t_{Jitter}			3.5	%
SCLK high-level width	t_{CH}		3.5		ns
SCLK low-level width	t_{CL}		3.5		ns
Output delay time (from SCLK ↑)	t_{DSP}		1.1	7.1	ns
Output delay time (from SCLK ↓)	t_{DSN}		–3.7	11.9	ns
Data input setup time	t_{SDS}		1.6		ns
Data input hold time	t_{SDH}		2.9		ns

Note Precision tests have not been performed. Only guaranteed as design characteristics.

Remark The maximum frequency of SCLK is 100 MHz.

(14) SDRAM interface parameters (2/2)



Notes 1. The pins to which this signal applies differ depending on the state of the DBUS32 pin and the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register.

When DBUS32 = 0: CS(1:0)#, DQM(3:2)

When DBUS32 = 1 and EXT_ROMCS(1:0) = 11: CS(1:0)#

When DBUS32 = 1 and EXT_ROMCS(1:0) = 10: CS(1:0)#, CS2#/ROMCS2#

When DBUS32 = 1 and EXT_ROMCS(1:0) = 00: CS(1:0)#, CS(3:2)#/ROMCS(3:2)#

2. The pins to which this signal applies differ depending on the state of the DBUS32 pin.

When DBUS32 = 0: DQM (1:0)

When DBUS32 = 1: DQM (3:0)

3. The pins to which this signal applies differ depending on the state of the DBUS32 pin.

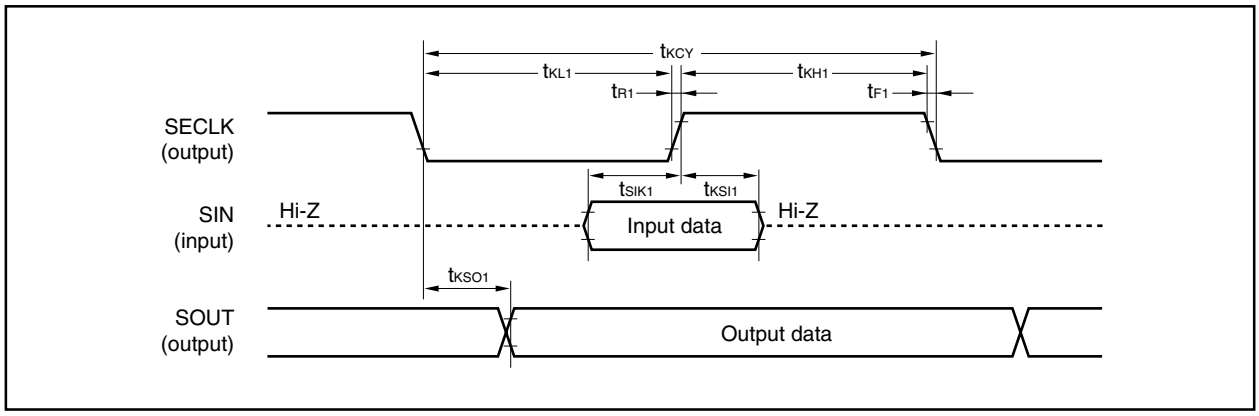
When DBUS32 = 0: DATA(15:0)

When DBUS32 = 1: DATA(15:0), DATA(31:16)/GPIO(31:16)

Remark The broken lines indicate high impedance.

(15) CSI (clocked serial interface) parameters

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating frequency					9.216	MHz
SECLK clock cycle time	t_{KCY}		108			ns
SECLK high-level width	t_{KH1}		$t_{KCY}/2 - 10$			ns
SECLK low-level width	t_{KL1}		$t_{KCY}/2 - 10$			ns
SECLK rise time	t_{R1}				10	ns
SECLK fall time	t_{F1}				10	ns
SIN input setup time (to SECLK ↑)	t_{SIK1}		30			ns
SIN input hold time (from SECLK ↑)	t_{KSI1}		20			ns
SOUT output delay time (from SECLK ↓)	t_{KSO1}				20	ns



(16) PCI like bus interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
PCLK clock cycle[Notes 1, 2]	t_{CLK}		T × P		ns
PCLK high-level width[Notes 1, 2]	t_{CLKH}		(T × P/2) – 4		ns
PCLK low-level width[Notes 1, 2]	t_{CLKL}		(T × P/2) – 4		ns
Output valid delay time (from PCLK ↑)[Note 3]	t_{VAL}		2	12	ns
Delay time from floating to valid (from PCLK ↑)[Note 4]	t_{ON}		2		ns
Output floating delay time (from PCLK ↑)[Note 4]	t_{OFF}			28	ns
Data input setup time[Note 5]	t_{SU}		7		ns
Data input hold time[Note 5]	t_{DH}		0		ns

Notes 1. Applies to the PCLK pin.

2. The value of P is set by using the SEL_CLK(1:0) bits of the PCICLKSELREG register, and the value of T is set by using the CLKSEL(2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register.

SEL_CLK(1:0)	P
11	3
10	1
01	4
00	2

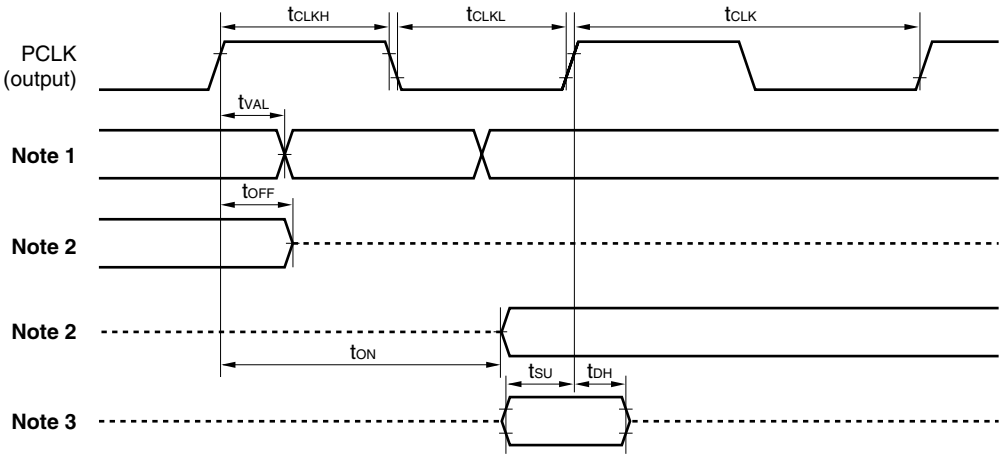
VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	RFU	RFU	10.0	15.1	20.1	25.1	30.1	RFU
101	RFU	RFU	11.1	16.6	22.1	27.6	33.2	RFU
100	RFU	RFU	12.1	18.1	24.1	30.1	36.2	RFU
011	RFU	RFU	13.1	19.6	26.1	32.7	RFU	RFU
010	RFU	RFU	15.1	22.6	30.1	37.7	RFU	RFU
001	10.0	RFU	20.1	30.1	RFU	RFU	RFU	RFU
000	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

3. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, GNT(2:0)#, and RST# pins.

4. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, and TRDY# pins.

5. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, and REQ(2:0)# pins.

(16) PCI like bus interface parameters (2/2)



Notes 1. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, GNT(2:0)#, and RST# pins.

2. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, and TRDY# pins.

3. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, and REQ(2:0)# pins.

Remark The broken lines indicate high impedance.

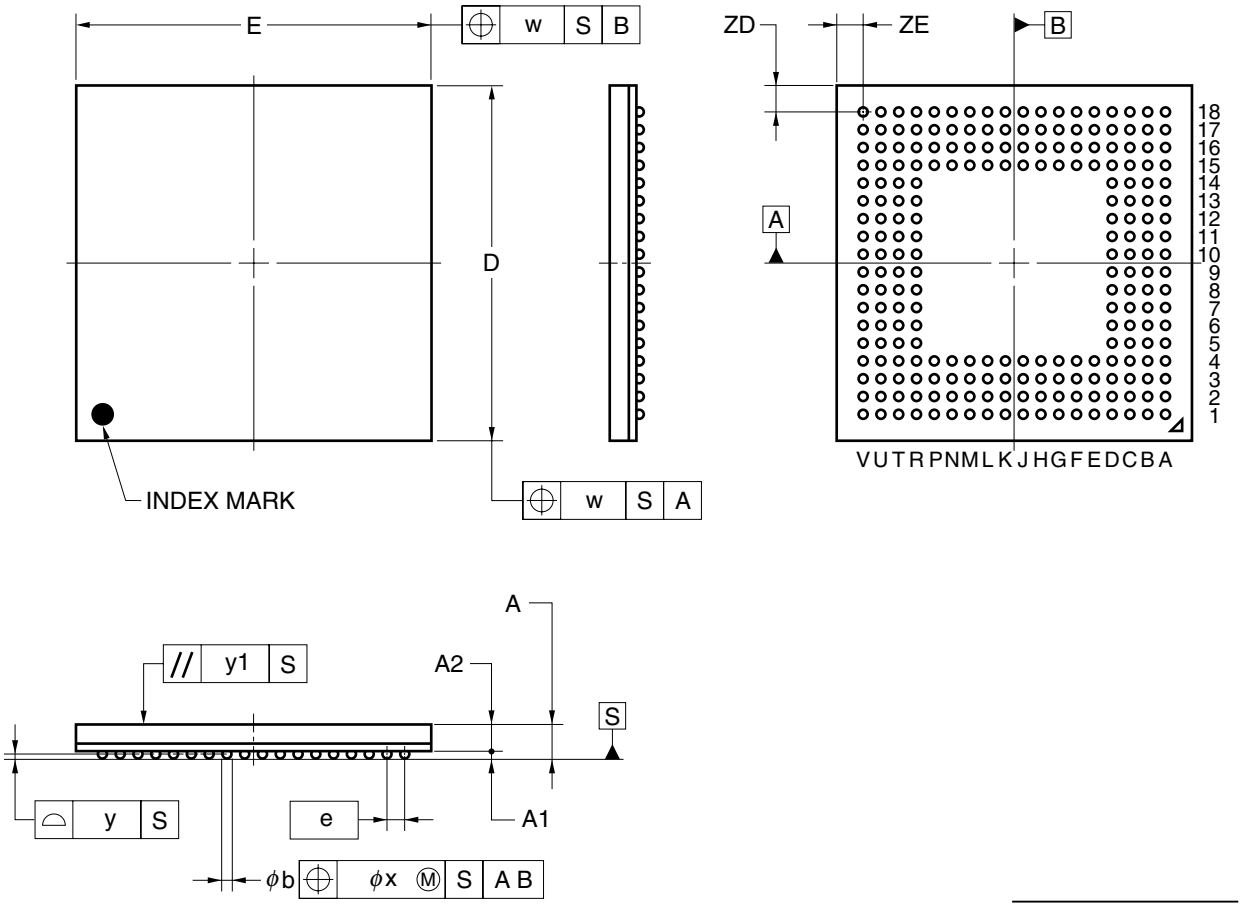
Load Coefficient (Delay Time per Load Capacitance)

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

Caution Precision tests have not been performed. Only guaranteed as design characteristics.

3. PACKAGE DRAWING

224-PIN PLASTIC FBGA (16x16)



ITEM	MILLIMETERS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P224F1-80-GA2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD30131 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30131F1-200-GA2: 224-pin plastic FBGA (16 × 16)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times max., Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 to 72 hours.)	IR35-203-2

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related documents VRC4173 User's Manual (U14579E)
μPD31173 (VRC4173) Data Sheet (U15338E)

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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