NEC

MOS INTEGRATED CIRCUIT

μPD178F124

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178F124 is a flash memory model of the μPD178023 and 178024, and is provided with a flash memory to/from which data can be written/erased with the microcontroller mounted on a printed circuit board.

For the detailed functional description, refer to the following User's Manuals:

μPD178024, 178124 Subseries User's Manual : U13915E
78K/0 Series User's Manual - Instruction : U12326E

FEATURES

- Serial interface (I^2C bus and UART mode)
- Hardware for PLL frequency synthesizer
- Pin-compatible with mask ROM models (except V_{PP} pin)
- Flash memory: 32K bytes[Note]
- Internal high-speed RAM: 1024 bytes
- Operable at same supply voltage as mask ROM models : V_{DD} = 4.5 to 5.5 V (during CPU and PLL operations)
  : V_{DD} = 3.5 to 5.5 V (during CPU operation)

Note The capacities of the flash memory can be changed using the memory size select register (IMS).

Remark For the differences between the flash memory model and mask ROM models, refer to **1. DIFFERENCES BETWEEN μPD178F124 AND MASK ROM MODELS**.

The electrical specifications (such as supply current) in the μPD178F124 differ from those of the mask ROM models. Confirm these differences before mass-producing any application set.

APPLICATION FIELD

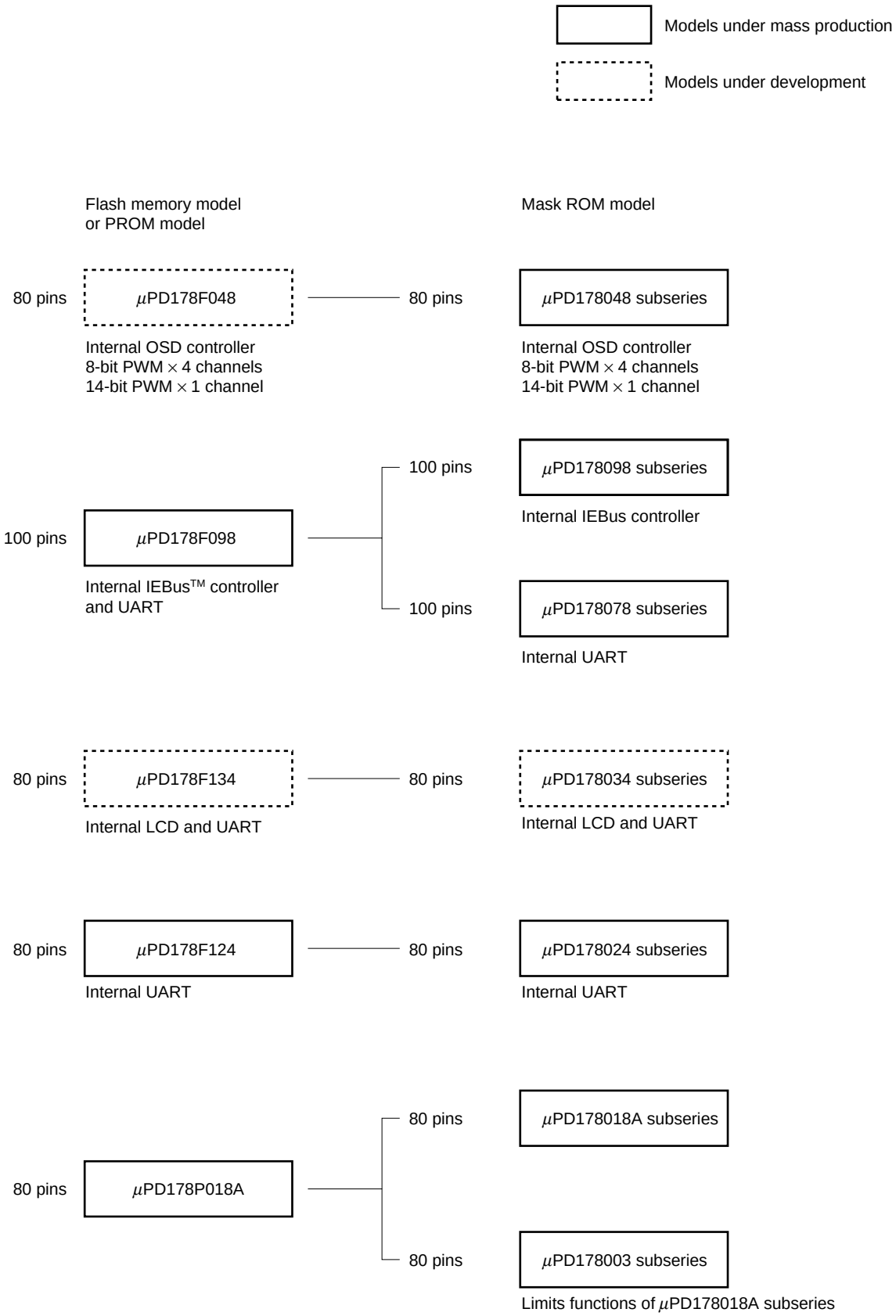
Car stereos

ORDERING INFORMATION

Part Number	Package
μPD178124GF-3B9	80-pin plastic QFP (14 × 20)
μPD178124GC-8BT	80-pin plastic QFP (14 × 14)

Document No. U14933EJ1V0DS00 (1st edition)
Date Published August 2000 N CP(K)
Printed in Japan

DEVELOPMENT OF 8-BIT DTS SERIES



FUNCTIONAL OUTLINE

(1/2)

Item		μPD178F124
Internal	Flash memory	32 Kbytes
	High-speed RAM	1024 bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.45 μs/0.89 μs/1.78 μs/3.56 μs/7.11 μs (with crystal resonator of f_X = 4.5 MHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.
I/O port		Total : 62 pins • CMOS I/O : 53 pins • CMOS input : 6 pins • N-ch open-drain output : 3 pins
A/D converter		8-bit resolution × 6 channels (V_{DD} = 3.5 to 5.5 V)
Serial interface		• I^2C bus mode[Note] : 1 channel • 3-wire mode : 1 channel • UART mode : 1 channel
Timer		• Basic timer (timer carry FF (10 Hz)) : 1 channel • 8-bit timer/event counter : 2 channels • Watchdog timer : 1 channel
Buzzer output		1 channel (1 kHz, 1.5 kHz, 3 kHz, 4 kHz)
Vectored interrupt source	Maskable	Internal : 11 External: 5
	Non-maskable	Internal: 1
	Software	1
PLL frequency synthesizer	Division mode	2 types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOL and VCOH pins)
	Reference frequency	Seven types selectable in software (1, 3, 9, 10, 12.5, 25, 50 kHz)
	Charge pump	Error out output: 2 pins
	Phase comparator	Unlock detectable in software

Note When the I^2C bus mode is used (including when the mode is implemented in software without using the peripheral hardware), consult NEC when ordering a mask.

(2/2)

Item	μPD178F124
Frequency counter	Frequency measurement • AMIFC pin: For 450-kHz counting • FMIFC pin: For 450-kHz/10.7-MHz counting

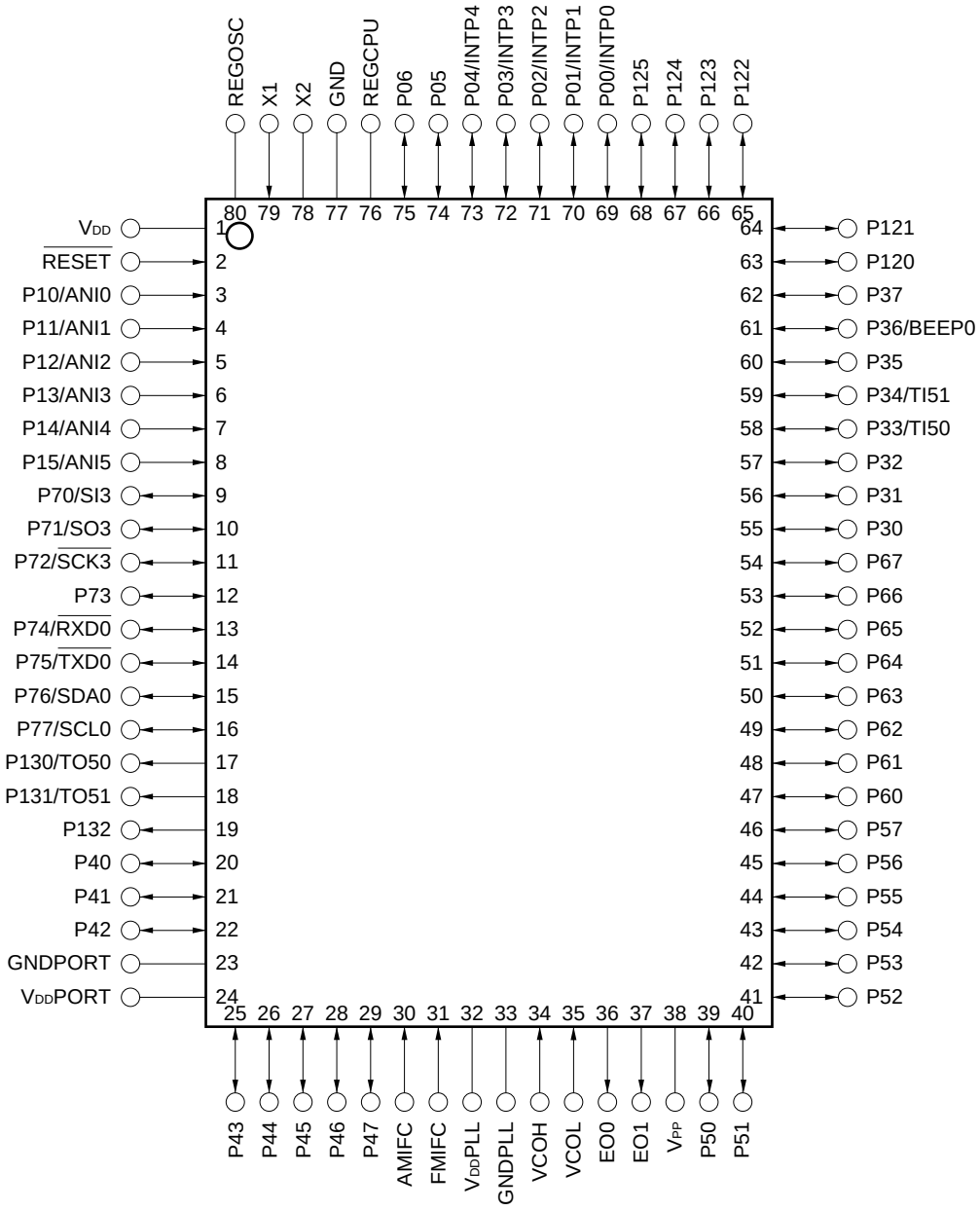
Reset	• Reset by $\overline{\text{RESET}}$ pin
	• Internal reset by watchdog timer
	• Reset by power-ON clear circuit
	  • Detection of less than 4.5 V[Note] (Reset does not occur, however.)
	  • Detection of less than 3.5 V[Note] (during CPU operation)
	  • Detection of less than 2.3 V[Note] (in STOP mode)

Supply voltage	• V_{DD} = 4.5 to 5.5 V (during CPU, PLL operation) • V_{DD} = 3.5 to 5.5 V (during CPU operation)
Package	• 80-pin plastic QFP (14 × 20) • 80-pin plastic QFP (14 × 14)

Note These voltages are the maximum values. In practice, the chip may be reset at voltages lower than these.

PIN CONFIGURATION (Top View)

- **80-pin plastic QFP (14 × 20)**
  μPD178F124GF-3B9



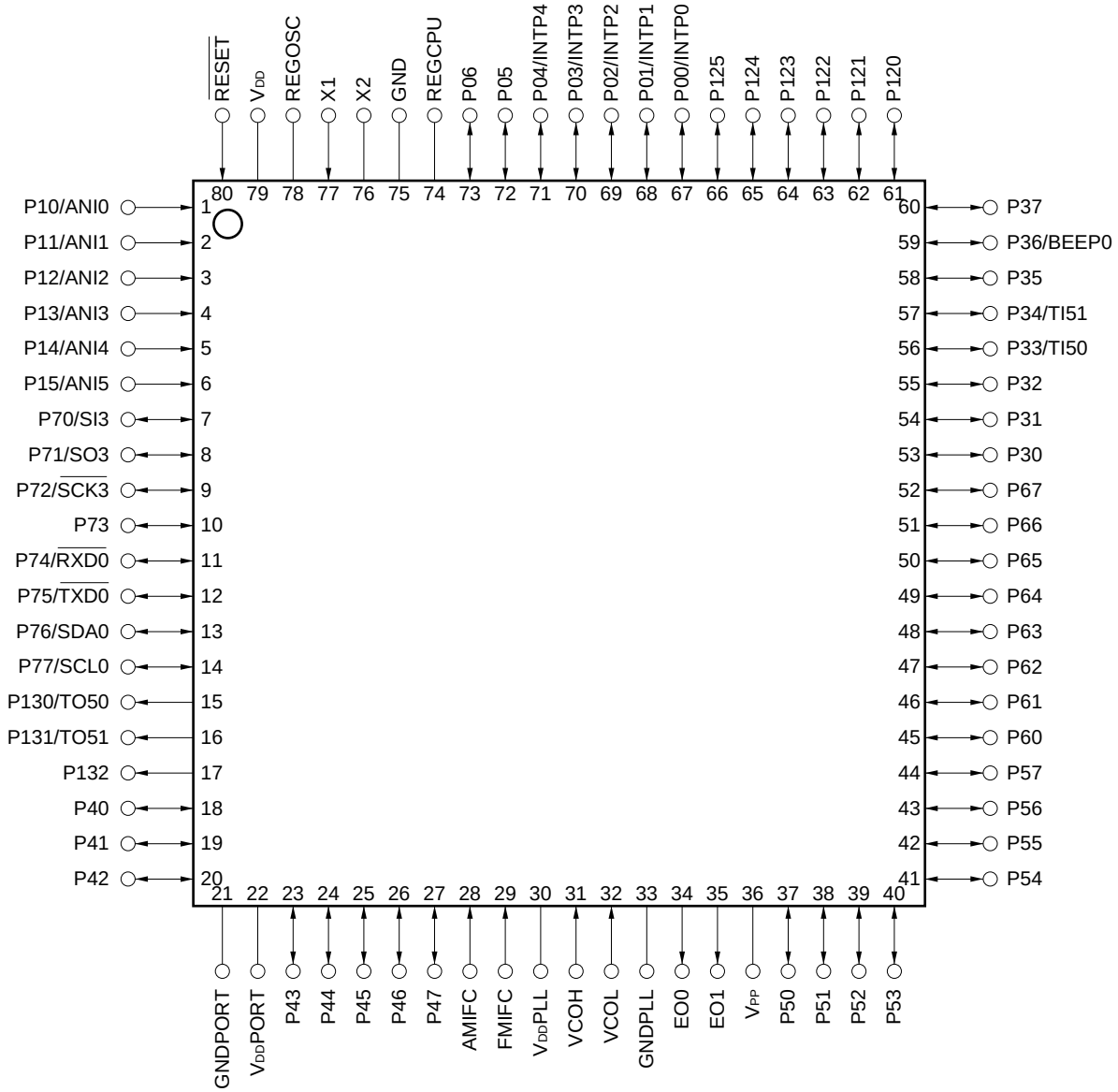
Cautions 1. Directly connect the V_{PP} to GND in normal operating mode.

2. Keep the voltage at V_{DD}PORT and V_{DD}PLL at the same voltage as V_{DD}.

3. Keep the voltage at GNDPORT and GNDPLL at the same voltage as GND.

4. Connect each of the REGOSC and REGCPU pins to GND via 0.1-μF capacitor.

- **80-pin plastic QFP (14 × 14)**
  μPD178F124GC-8BT



Cautions 1. Directly connect the V_{PP} to GND in normal operating mode.

2. Keep the voltage at V_{DD}PORT and V_{DD}PLL at the same voltage as V_{DD}.

3. Keep the voltage at GNDPORT and GNDPLL at the same voltage as GND.

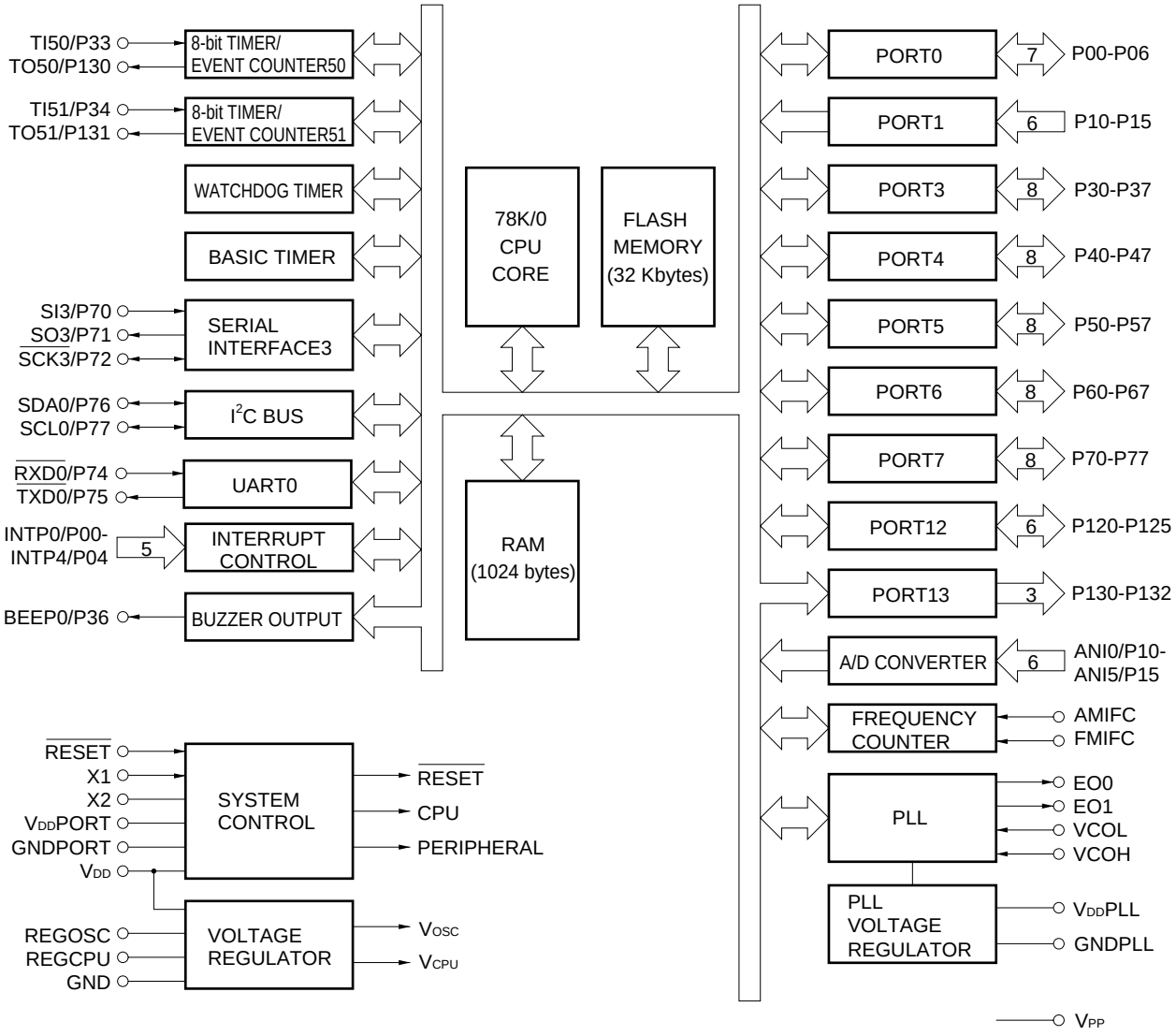
4. Connect each of the REGOSC and REGCPU pins to GND via 0.1-μF capacitor.

PIN NAME

AMIFC : AM intermediate frequency counter input
ANI0-ANI5 : A/D converter input
BEEP0 : Buzzer output
EO0, EO1 : Error out output
FMIFC : FM intermediate frequency counter input
GND : Ground
GNDPLL : PLL ground
GNDPORT : Port ground
INTP0-INTP4 : Interrupt input
P00-P06 : Port 0
P10-P15 : Port 1
P30-P37 : Port 3
P40-P47 : Port 4
P50-P57 : Port 5
P60-P67 : Port 6
P70-P77 : Port 7
P120-P125 : Port 12
P130-P132 : Port 13

REGCPU : Regulator for CPU power supply
REGOSC : Regulator for oscillator
$\overline{\text{RESET}}$: Reset input
$\overline{\text{RXD0}}$: Serial (UART0) data input
$\overline{\text{SCK3}}$: Serial (SIO3) clock input/output
SCL0 : Serial (IIC0) clock input/output
SDA0 : Serial (IIC0) data input/output
SI3 : Serial (SIO3) data input
SO3 : Serial (SIO3) data output
TI50, TI51 : 8-bit timer clock input
TO50, TO51 : 8-bit timer output
$\overline{\text{TXD0}}$: Serial (UART0) data output
VCOL, VCOH : Local oscillation input
V_{DD} : Power supply
V_{DD}PLL : PLL power supply
V_{DD}PORT : Port power supply
V_{PP} : Programming power supply
X1, X2 : Crystal resonator

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD178F124 AND MASK ROM MODELS

The μPD178F124 is provided with a flash memory to/from which data can be rewritten/erased with the device mounted on a printed circuit board. The differences between the flash memory model (μPD178F124) and mask ROM models (μPD178023 and 178024) are shown in Table 1-1.

Table 1-1. Differences between μPD178F124 and Mask ROM Models

Item		μPD178F124	μPD178023, 178024
Internal memory	ROM structure	Flash memory	Mask ROM
	ROM capacity	32K bytes	μPD178023 : 24K bytes μPD178024 : 32K bytes
Internal ROM capacity selected by memory size select register (IMS)		Equivalent to mask ROM model	μPD178023 : C6H μPD178024 : C8H
IC pin		Not provided	Provided
V_{PP} pin		Provided	Not provided
Electrical specifications, recommended soldering conditions		See the relevant data sheet.	

2. PIN FUNCTION LIST

2.1 Port Pins

Pin Name	I/O	Function	At Reset	Shared by:
P00-P04	I/O	Port 0. 7-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	INTP0-INTP4
P05, P06				—
P10-P15	Input	Port 1. 6-bit input port.	Input	ANI0-ANI5
P30-P32	I/O	Port 3. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P33				TI50
P34				TI51
P35				—
P36				BEEP0
P37				—
P40-47	I/O	Port 4. 8-bit I/O port. Can be set in input or output mode in 1-bit units. Internal pull-up resistors can be specified in software. Interrupt function by key input is provided.	Input	—
P50-P57	I/O	Port 5. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P60-P67	I/O	Port 6. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P70	I/O	Port 7. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	SI3
P71				SO3
P72				$\overline{\text{SCK3}}$
P73				—
P74				$\overline{\text{RXD0}}$
P75				$\overline{\text{TXD0}}$
P76				SDA0
P77				SCL0
P120-P125	I/O	Port 12. 6-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P130	Output	Port 13. 3-bit output port. N-ch open-drain output port (12 V withstand)	Low-level output	TO50
P131				TO51
P132				—

2.2 Pins Other Than Port Pins

Pin Name	I/O	Function		At Reset	Shared by:
INTP0-INTP4	Input	External maskable interrupt input whose valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.		Input	P00-P04
SI3	Input	Serial data input to serial interface.		Input	P70
SO3	Output	Serial data output from serial interface.		Input	P71
SDA0	I/O	Serial data input/output to/from serial interface.	N-ch open drain I/O	Input	P76
$\overline{SCK3}$	I/O	Serial clock input/output to/from serial interface.		Input	P72
SCL0			N-ch open drain I/O		P77
$\overline{RXD0}$	Input	Serial data input to asynchronous serial interface (UART0).		Input	P74
$\overline{TXD0}$	Output	Serial data output from asynchronous serial interface (UART0).			P75
TI50	Input	External count clock input to 8-bit timer (TM50).		Input	P33
TI51		External count clock input to 8-bit timer (TM51).			P34
TO50	Output	8-bit timer (TM50) output.		Low-level output	P130
TO51		8-bit timer (TM51) output.			P131
BEEP0	Output	Buzzer output.		Input	P36
ANI0-ANI5	Input	Analog input to A/D converter.		Input	P10-P15
EO0, EO1	Output	Error out output from charge pump of PLL frequency synthesizer.		–	–
VCOL	Input	Inputs local oscillation frequency of PLL (in HF and MF modes).		–	–
VCOH		Inputs local oscillation frequency of PLL (in VHF mode).			
AMIFC	Input	Input to AM intermediate frequency counter.		Input	–
FMIFC		Input to FM or AM intermediate frequency counter.			
$\overline{RESET}$	Input	System reset input.		–	–
X1	Input	Connection of crystal resonator for system clock oscillation.		–	–
X2	–			–	–
REGOSC	–	Regulator for oscillator. Connect this pin to GND via 0.1-μF capacitor.		–	–
REGCPU	–	Regulator for CPU power supply. Connect this pin to GND via 0.1-μF capacitor.		–	–
V_{DD}	–	Positive power supply.		–	–
GND	–	Ground.		–	–
V_{DD}PORT	–	Port power supply.		–	–
GNDPORT	–	Port ground.		–	–
V_{DD}PLL**Note**	–	PLL positive power supply.		–	–
GNDPLL**Note**	–	PLL ground.		–	–
V_{PP}	–	Setting flash memory programming mode. Applying high voltage for program write/verify. Connect directly to GND or GNDPORT in normal operation mode.		–	–

Note Connect a capacitor of about 1000 pF between the V_{DD}PLL and GNDPLL pins.

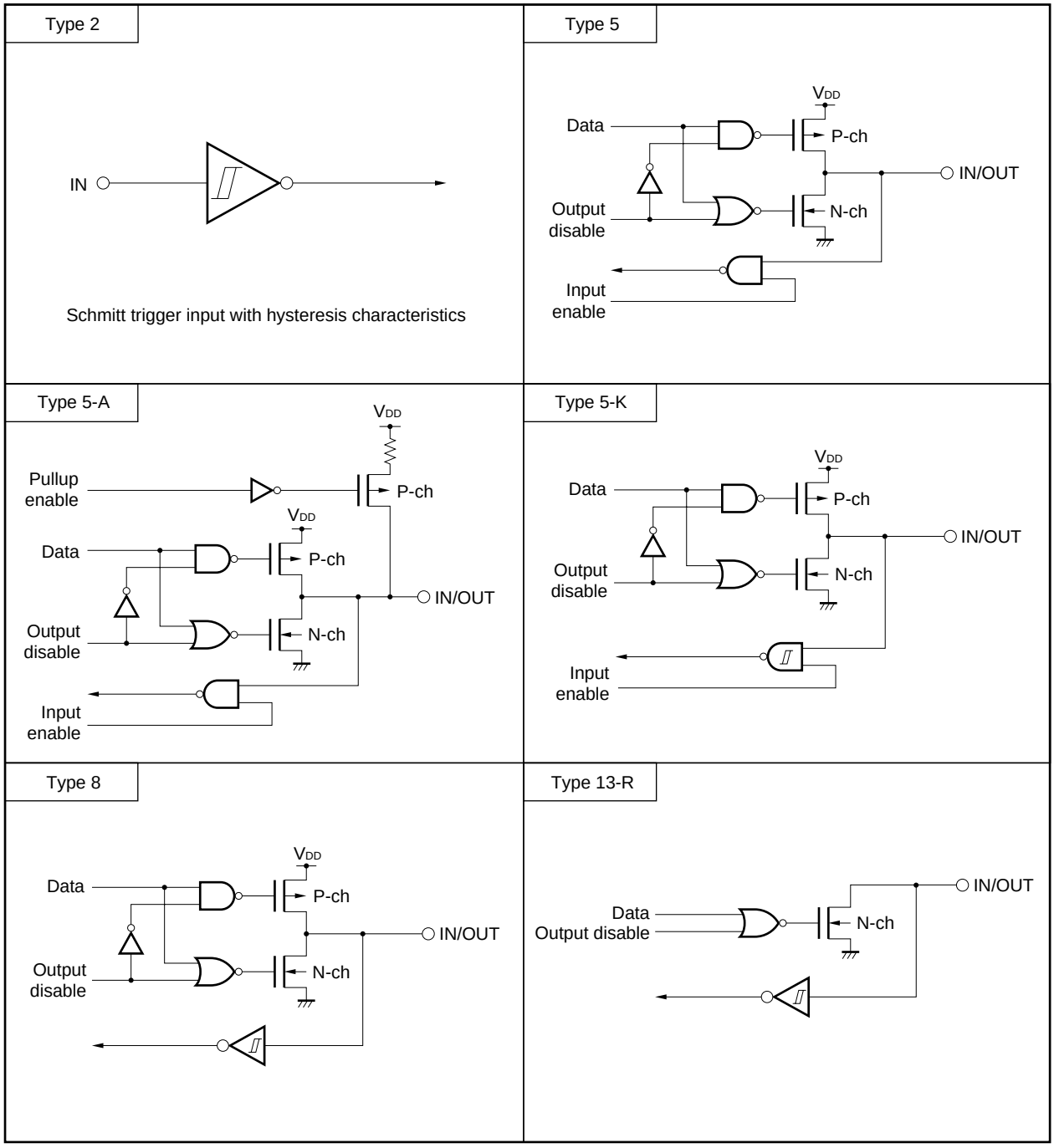
2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the types of the I/O circuits of the respective pins and the recommended connections of the pins when they are not used. For the configuration of the I/O circuit of each pin, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin

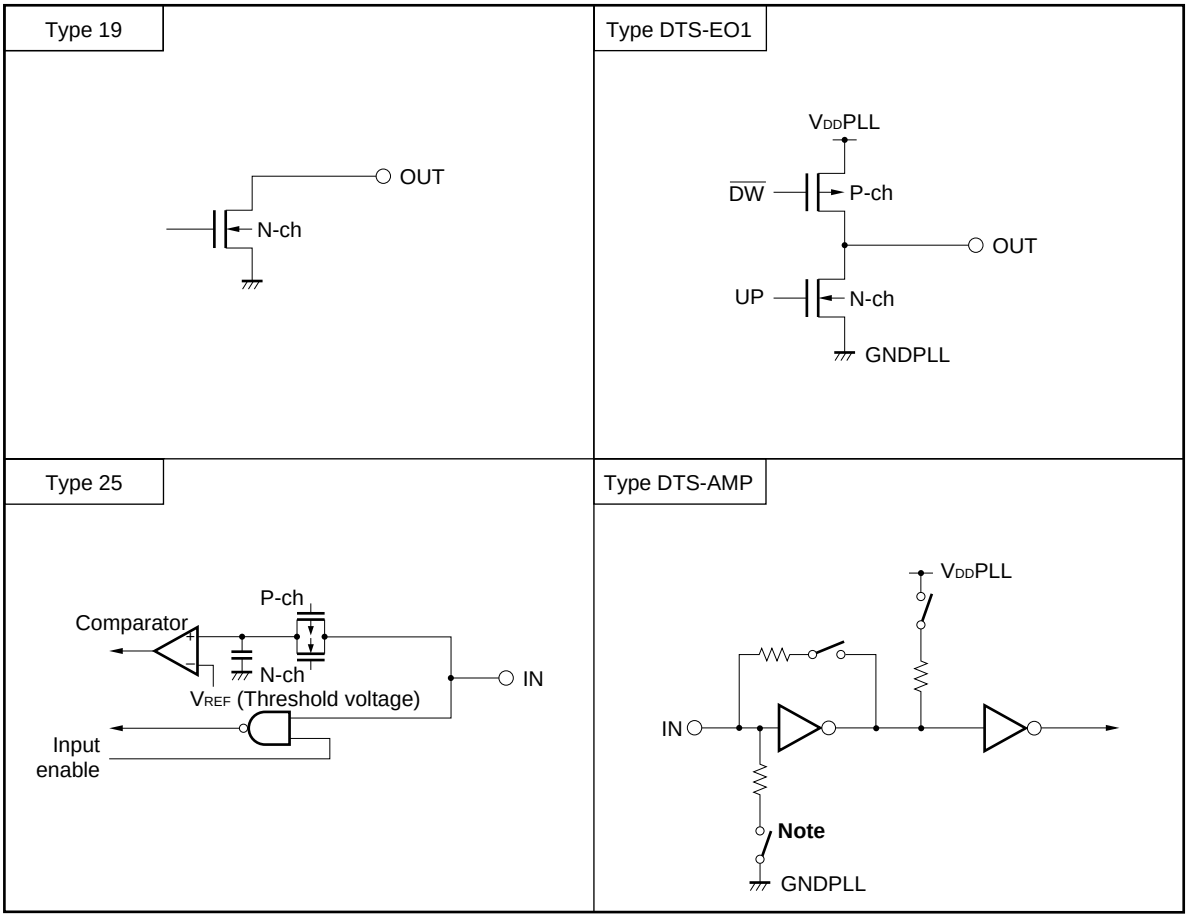
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P00/INTP0-P04/INTP4	8	I/O	Set these pins in general-purpose input mode in software, and connect each of them to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P05, P06			
P10/ANI0-P15/ANI5	25	Input	Connect each of them to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P30-P32	5	I/O	Set these pins in general-purpose input mode in software, and output low-level signal. Leave unconnected.
P33/TI50	5-K		
P34/TI51			
P35	5		
P36/BEEP0			
P37			
P40-P47	5-A		Set these pins in general-purpose input mode in software, and connect each of them to GND or GNDPORT via resistor.
P50-P57	5		Set these pins in general-purpose input mode in software, and connect each of them to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P60-P67	5		Set these pins in general-purpose input mode in software, and output low-level signal. Leave unconnected.
P70/SI3	5-K		Set these pins in general-purpose input mode in software, and connect each of them to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P71/SO3	5		
P72/$\overline{SCK3}$	5-K		
P73	5		
P74/$\overline{RXD0}$	5-K		
P75/$\overline{TXD0}$	5		
P76/SDA0	13-R		
P77/SCL0			
P120-P125	5		
P130/TO50	19	Output	Set these pins to low-level output in software and leave unconnected.
P131/TO51			
P132			
EO0, EO1	DTS-EO1	Output	Leave unconnected.
VCOL, VCOH	DTS-AMP	Input	Disable PLL in software and select pull-down.
AMIFC, FMIFC			Set these pins in general-purpose input port mode in software and connect each of them to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
REGOSC, REGCPU	–	–	Connect these pins to GND via 0.1-μF capacitor.
$\overline{RESET}$	2	Input	–
V_{DD}PLL	–	–	Connect this pin to V_{DD}.
GNDPLL			Directly connect these pins to GND or GNDPORT.
V_{PP}			

Figure 2-1. I/O Circuits of Respective Pins (1/2)



Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

Figure 2-1. I/O Circuits of Respective Pins (2/2)



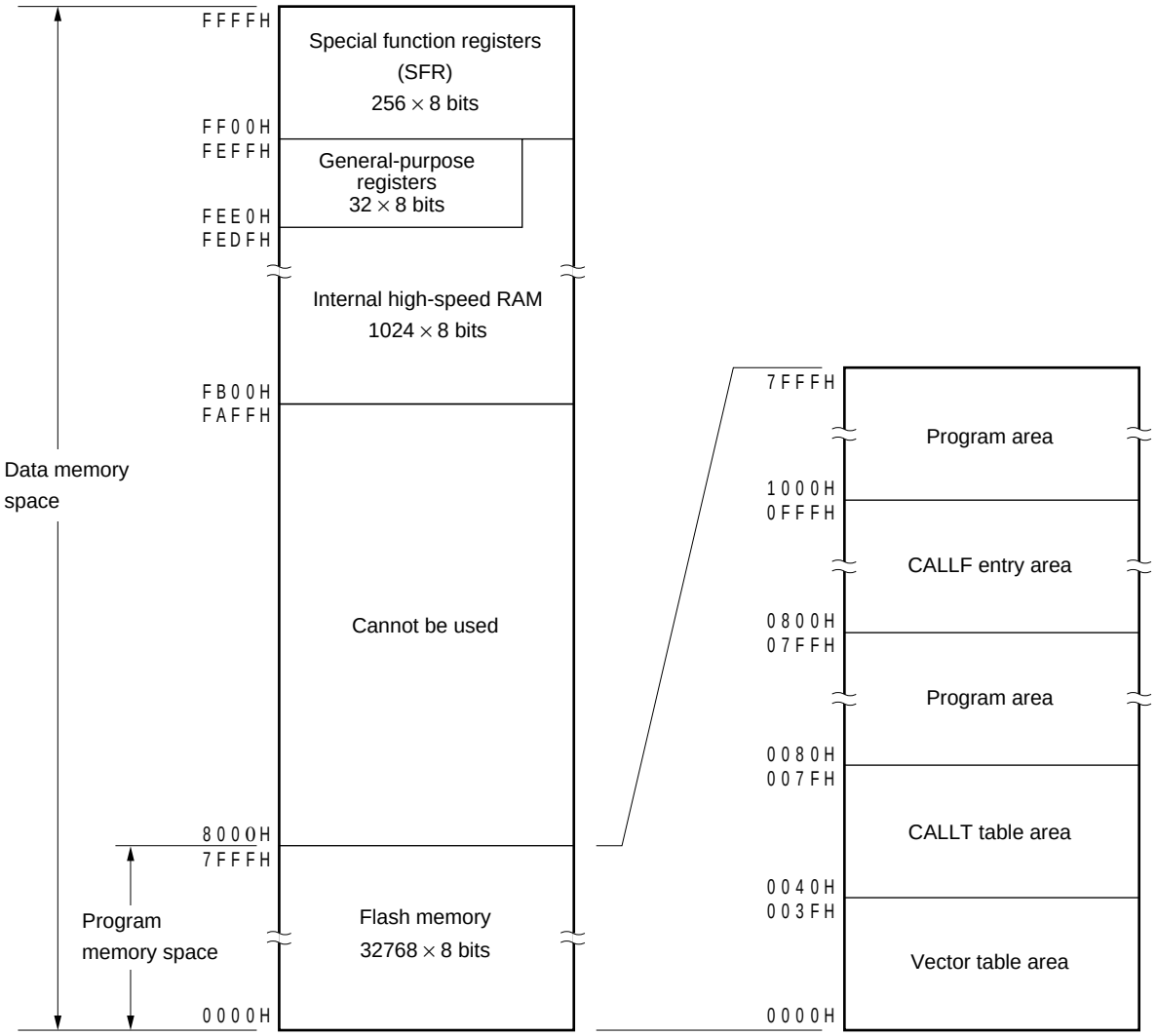
Note This switch is selectable in software only for the VCOL and VCOH pins.

Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

3. MEMORY SPACE

Figure 3-1 shows the memory map of the μPD178F124.

Figure 3-1. Memory Map



3.1 Memory Size Select Register (IMS)

The memory size select register (IMS) sets the internal memory capacity.

When the target mask ROM model is the μPD178023, μPD178024, set this register to C6H, C8H respectively.

Use an 8-bit memory manipulation instruction to set the IMS.

This register is set to CFH at reset.

Caution Be sure to set the IMS to C6H or C8H as the program initial setting. The IMS set value changes to CFH when reset. Therefore, set C6H or C8H again after reset.

Figure 3-2. Format of Memory Size Select Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selects Internal High-speed RAM Capacity
1	1	0	1024 bytes
Others			Setting prohibited

RAM3	RAM2	RAM1	RAM0	Selects Flash Memory Capacity
0	1	1	0	24K bytes
1	0	0	0	32K bytes
Others				Setting prohibited

Table 3-1 indicates the setting of IMS to perform the same memory mapping as that of a mask ROM model.

Table 3-1. Set Value of Memory Size Select Register (IMS)

Targeted Model	Set Value of IMS
μPD178023	C6H
μPD178024	C8H

3.2 Internal Extension RAM Size Select Register (IXS)

The internal extension RAM size select register (IXS) sets the internal extension RAM capacity.

When the target mask ROM model is the μPD178023, μPD178024, use this register with the initial value (0CH).

Use an 8-bit memory manipulation instruction to set the IXS.

This register is set to 0CH at reset.

Caution Do not assign a value other than that the initial value.

Figure 3-3. Format of Internal Extension RAM Size Select Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects Internal Extension RAM Capacity
0	1	1	0	0	0 byte
Others					Setting prohibited

Table 3-2 indicates the setting of IXS to perform the same memory mapping as that of a mask ROM model.

Table 3-2. Set Value of Internal Extension RAM Size Select Register

Targeted Model	Set Value of IXS
μPD178023, 178024	0CH

4. INTERRUPT FUNCTION

The μPD178F124 has the following three types and 17 sources of interrupts:

- Non-maskable : 1[Note]
- Maskable : 16[Note]
- Software : 1

Note Two types of watchdog interrupt sources (INTWDT), non-maskable and maskable, are available, and either of them can be selected.

Table 4-1. Interrupt Sources

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTKY	Detection of key input of port 4	Internal	0010H	(B)
	7	INTIIC0	End of transfer by serial interface IIC0		0012H	
	8	INTBTM0	Generation of basic timer match signal		0014H	
	9	INTAD3	End of conversion by A/D converter		0016H	
	10	–	–	–	0018H[Note 3]	–
	11	INTCSI3	End of transfer by serial interface SIO3	Internal	001AH	(B)
	12	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		001CH	
	13	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		001EH	
	14	INTSER0	Reception error of serial interface UART0		0020H	
	15	INTSR0	End of reception by serial interface UART0		0022H	
	16	INTST0	End of transmission by serial interface UART0		0024H	
Software	–	BRK	Execution of BRK instruction	–	003EH	(D)

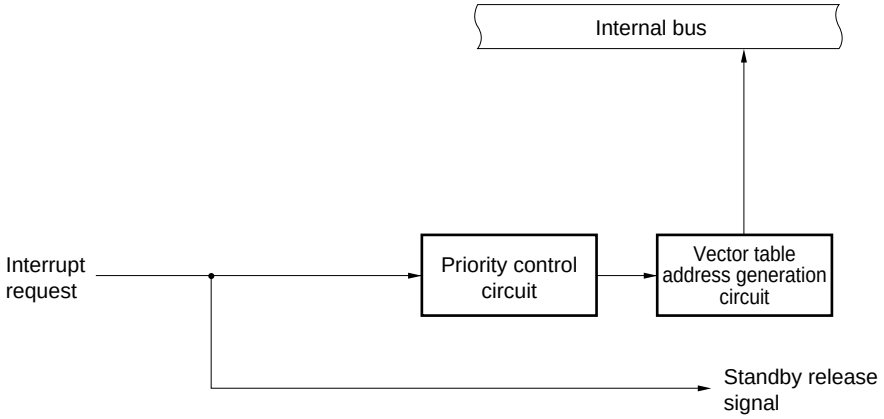
Notes 1. If two or more maskable interrupts occur at the same time, they are acknowledged or kept pending according to their default priorities. The default priority 0 is the highest, while 16 is the lowest.

2. (A) to (D) under the heading Basic Configuration Type corresponds to (A) to (D) in Figure 4-1.

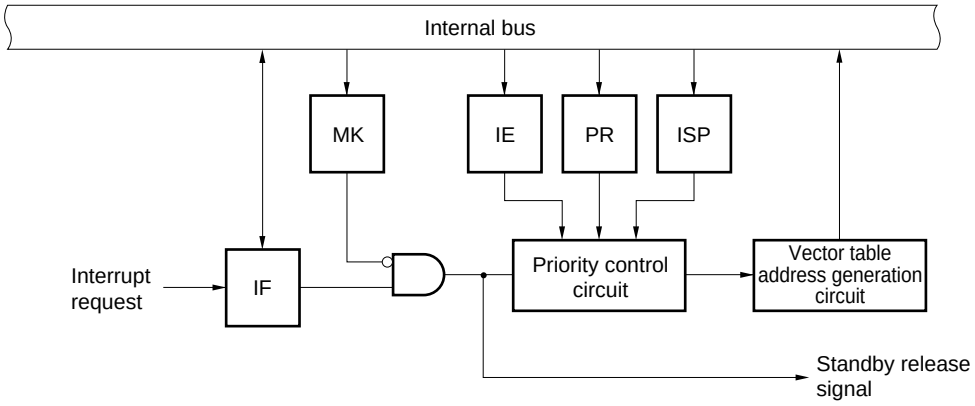
3. There are no interrupt sources corresponding to vector addresses 0018H.

Figure 4-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

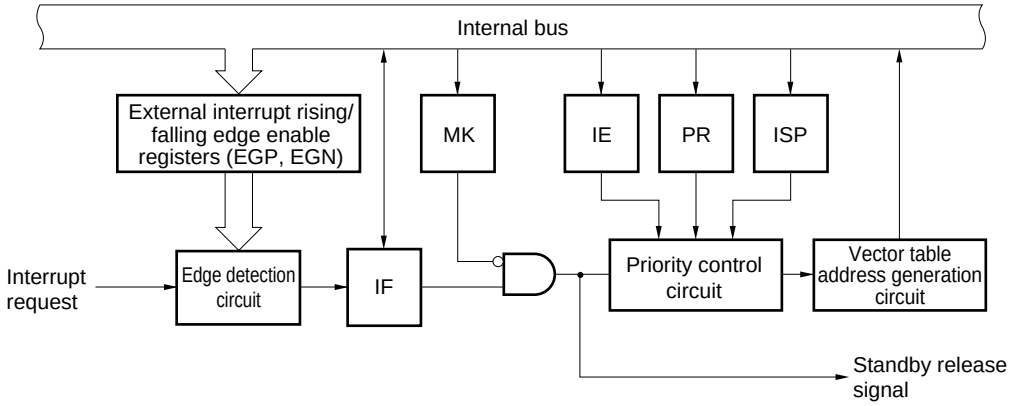
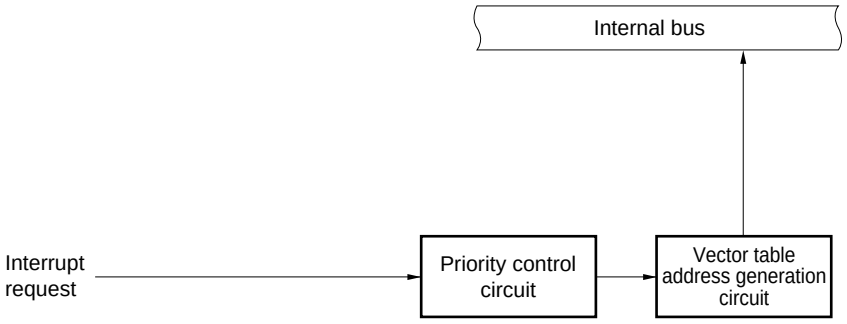


Figure 4-1. Basic Configuration of Interrupt Function (2/2)

(D) Software interrupt



Remark IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

5. FLASH MEMORY PROGRAMMING

The program memory provided in the μPD178F124 is flash memory.

The flash memory can be written on-board, i.e., with the μPD178F124 mounted on the target system.

To do so, connect a dedicated flash writer (Flashpro III (Part number FL-PR3, PG-FP3)) to the host machine and target system.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

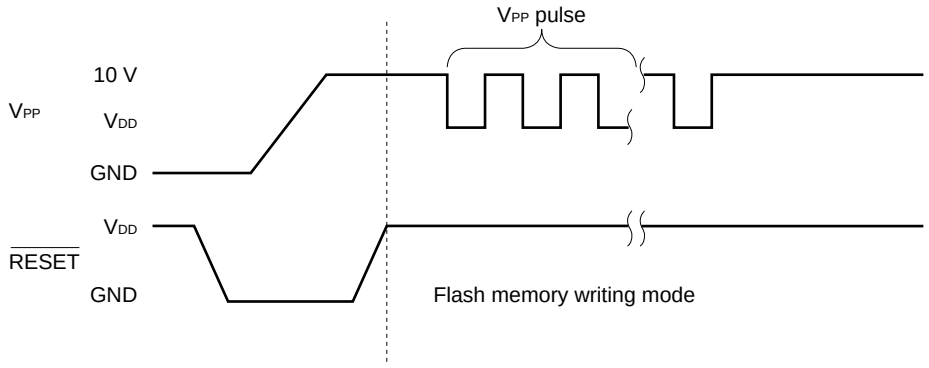
The flash memory is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 5-1. To select a communication mode, the format shown in Figure 5-1 is used. Each communication mode is selected depending on the number of V_{PP} pulses shown in Table 5-1.

Table 5-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O (SIO3)	1	SI3/P70 SO3/P71 $\overline{SCK3}$/P72	0
UART0	1	$\overline{RXD0}$/P74 $\overline{TXD0}$/P75	8

Caution Be sure to select a communication mode by the number of V_{PP} pulses shown in Table 6-1.

Figure 5-1. Communication Mode Selection Format



5.2 Flash Memory Programming Function

An operation such as writing the flash memory is performed when a command or data is transmitted/received in the selected communication mode. The major flash memory programming functions are listed in Table 5-2.

Table 5-2. Major Flash Memory Programming Functions

Function	Description
Batch erase	Erases all memory contents.
Batch blank check	Checks erased status of entire memory.
Data write	Writes data to flash memory starting from write start address and based on number of data (bytes) to be written).
Batch verify	Compares all contents of memory with input data.

5.3 Connecting Flashpro III

Connection with Flashpro III differs depending on the communication mode (3-wire serial I/O or UART0). Figures 5-2 and 5-3 show the connection in the respective modes.

Figure 5-2. Connection of Flashpro III in 3-Wire Serial I/O Mode

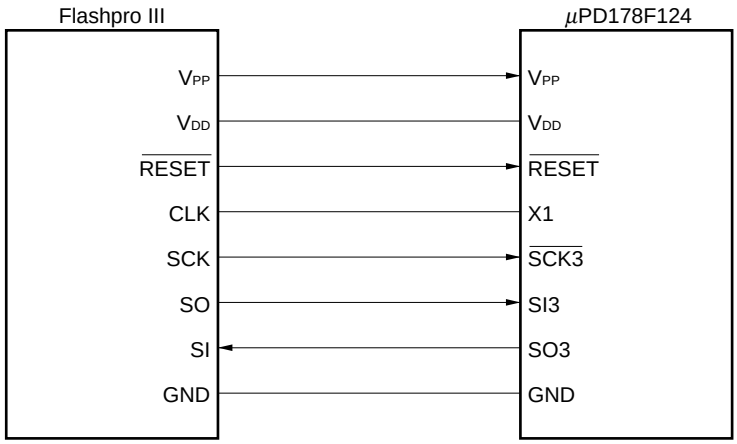
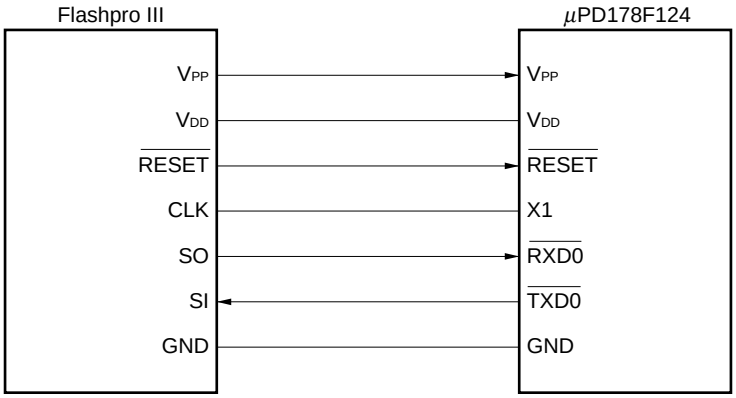


Figure 5-3. Connection of Flashpro III in UART0 Mode



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.0	V
	V_{DD}PORT			–0.3 to V_{DD} + 0.3 Note 1	V
	V_{DD}PLL			–0.3 to V_{DD} + 0.3 Note 1	V
	V_{PP}			–0.3 to +10.5	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Excluding P130 to P132		–0.3 to V_{DD} + 0.3	V
Output breakdown voltage	V_{BDS}	P130-P132	N-ch open drain	16	V
Analog input voltage	V_{AN}	P10-P15	Analog input pin	–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin		–8	mA
		Total of P00-P06, P30-P37, P54-P57, P60-P67, and P120-P125		–15	mA
		Total of P40-P47, P50-P53, and P70-P77		–15	mA
Low-level output current	I_{OL} Note 2	1 pin	Peak value	16	mA
			r.m.s	8	mA
		Total of P00-P06, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P120-P125, and P130-P132	Peak value	30	mA
			r.m.s	15	mA
Operating temperature	T_A	During normal operation		–40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			–55 to +125	°C

Notes 1. Keep the voltage at V_{DD}PORT and V_{DD}PLL same as that at the V_{DD} pin.

2. Calculate the r.m.s as follows: [r.m.s] = [Peak value] x $\sqrt{\text{Duty}}$

Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Be sure to use the product with these ratings never being exceeded.

Remark Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

Recommended Supply Voltage Ranges (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	When CPU is operating and PLL is stopped	3.5	5.0	5.5	V
Data retention voltage	V_{DDR}	When crystal oscillation stops	2.3		5.5	V
Output breakdown voltage	V_{BDS}	P130-P132 (N-ch open drain)			15	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V) (1/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P10-P15, P30-P32, P35-P37, P40-P47, P50-P57, P60-P67, P71, P73, P120-P125		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P06, P33, P34, P70, P72, P74-P75, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P76, P77 (N-ch open-drain I/O)	4.5 V ≤ V_{DD} ≤ 5.5 V	0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P10-P15, P30-P32, P35-P37, P40-P47, P50-P57, P60-P67, P71, P73, P120-P125		0		0.3 V_{DD}	V
	V_{IL2}	P00-P06, P33, P34, P70, P72, P74-P75, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P76, P77 (N-ch open-drain I/O)	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
High-level output voltage	V_{OH1}	P00-P06, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P120-P125	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OH} = –3 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OL1}	P00-P06, P30-P37, P40-47, P50-57, P60-P67, P70-P75, P120-P125	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1 mA			1.0	V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OL} = 100 μA			0.5	V
	V_{OL2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA			1.0	
	V_{OL3}	P76, P77 (N-ch open-drain I/O)	4.5 V ≤ V_{DD} ≤ 5.5 V I_{OL} = 3 mA			0.4	V
			4.5 V ≤ V_{DD} ≤ 5.5 V I_{OL} = 6 mA			0.6	V
High-level input leakage current	I_{LH}	P00-P06, P10-P15, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P120-P125, $\overline{\text{RESET}}$	V_{IN} = V_{DD}			3	μA

Remark Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V) (2/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Low-level input leakage current	I_{LIL}	P00-P06, P10-P15, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P120-P125, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
Output off leakage current	I_{LOH1}	P130-P132	V_{OUT} = 15 V			–3	μA
	I_{LOL1}	P130-P132	V_{OUT} = 0 V			3	μA
	I_{LOH2}	P76, P77 (at N-ch open drain I/O)	V_{OUT} = V_{DD}			–3	μA
	I_{LOL2}	P76, P77 (at N-ch open drain I/O)	V_{OUT} = 0 V			3	μA
	I_{LOH3}	EO0, EO1	V_{OUT} = V_{DD}			–3	μA
	I_{LOL3}	EO0, EO1	V_{OUT} = 0 V			3	μA
Supply current[Note]	I_{DD1}	When CPU is operating and PLL is stopped. Sine wave input to X1 pin At f_X = 4.5 MHz V_{IN} = V_{DD}			5.0	18	mA
	I_{DD2}	In HALT mode with PLL stopped. Sine wave input to X1 pin At f_X = 4.5 MHz V_{IN} = V_{DD}			0.3	0.8	mA
Data retention voltage	V_{DDR1}	When crystal resonator is oscillating		3.5		5.5	V
	V_{DDR2}	When crystal oscillation is stopped	Power-failure detection function	2.2			V
	V_{DDR3}		Data memory retained	2.0			V
Data retention current	I_{DDR1}	When crystal oscillation is stopped	T_A = 25°C, V_{DD} = 5 V		2.0	4.0	μA
	I_{DDR2}				2.0	20	μA

Note Excluding AV_{DD} current and V_{DD}PLL current.

Remarks 1. f_X: System clock oscillation frequency

2. Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

Reference Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD3}	When CPU and PLL are operating. Sine wave input to VCOH pin At f_{IN} = 160 MHz V_{IN} = 0.15 V_{P-P}		5		mA

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	f_X = 4.5 MHz	0.44		7.11	μs
TI50, TI51 input frequency	f_{TI5}				2	MHz
TI50, TI51 input high-/low-level widths	t_{TIH5} t_{TIL5}		200			ns
Interrupt input high-/low-level widths	t_{INTH} t_{INTL}	INTP0-INTP4	1			μs
$\overline{\text{RESET}}$ pin low-level width	t_{RSL}		10			μs

(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface (IIC0)

I^2C bus mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	–	0.6	–	μs
SCL0 clock low-level width		t_{LOW}	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	–	–	–	μs
	I^2C bus		0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
SDA0 and SCL0 signal rise time		t_R	–	1000	20+0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	–	300	20+0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike restrained by input filter		t_{SP}	–	–	0	50	ns
Each bus line capacitative load		Cb	–	400	–	400	pF

Notes 1. The first clock pulse is generated at the start condition after this period.

2. The device needs to internally supply a hold time of at least 300 ns for the SDA0 signal to fill the undefined area at the falling edge of the SCL0 ($V_{IHmin.}$ of the SCL0 signal).

3. Unless the device extends the low hold time (t_{LOW}) of the SCL0 signal, it is necessary to fill only the maximum data hold time ($t_{HD:DAT}$).

4. The high-speed mode I^2C bus can be used in the standard mode I^2C bus system. In this case, satisfy the following conditions:

- When the device does not extend the low hold time of the SCL0 signal
  $t_{SU:DAT} \geq 250$ ns
- When the device extends the low hold time of the SCL0 signal
  Send the next data bit to the SDA line before releasing the SCL0 line ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns : in the standard mode I^2C bus specification)

5. Cb: Total capacitance of one bus line (unit: pF)

(b) Serial interface (SIO3)

(i) 3-wire serial I/O mode ($\overline{SCK3}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK1}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI1}		400			ns
$\overline{SCK3}\downarrow\rightarrow$ SO3 output delay time	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{SCK3}$ and SO3 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK3}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH2}, t_{KL2}		400			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK2}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI2}		400			ns
$\overline{SCK3}\downarrow\rightarrow$ SO3 output delay time	t_{KSO2}	C = 100 pF **Note**			300	ns
$\overline{SCK3}$ at rising or falling edge time	t_{R2}, t_{F2}				1000	ns

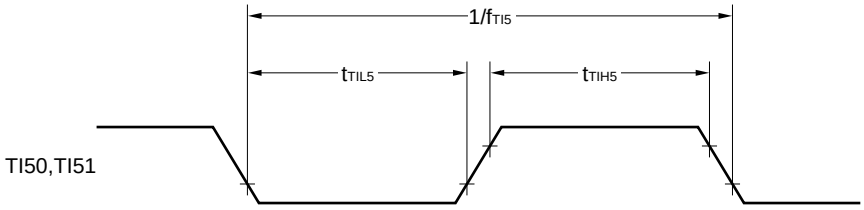
Note C is the load capacitance of SO3 output line.

(d) Serial interface (UART0: Dedicated baud rate generator output)

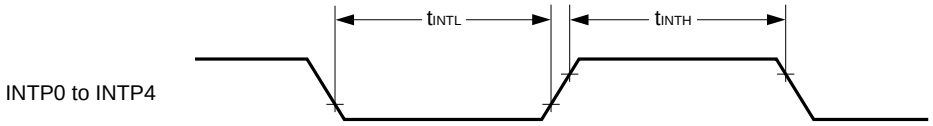
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38400	bps

AC Timing Test Point (Excluding X1 Input)

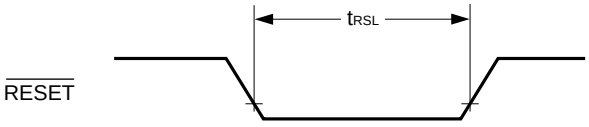
TI Timing



Interrupt Input Timing

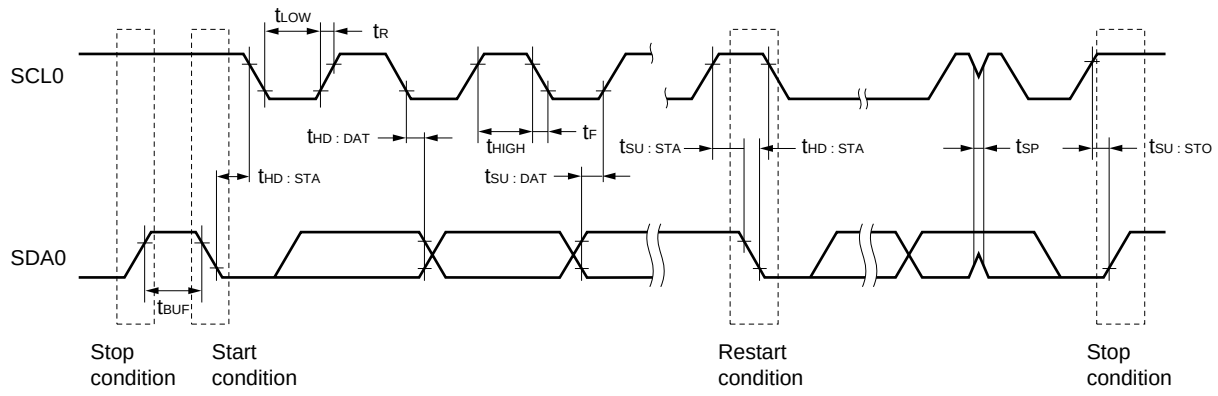


$\overline{\text{RESET}}$ Input Timing

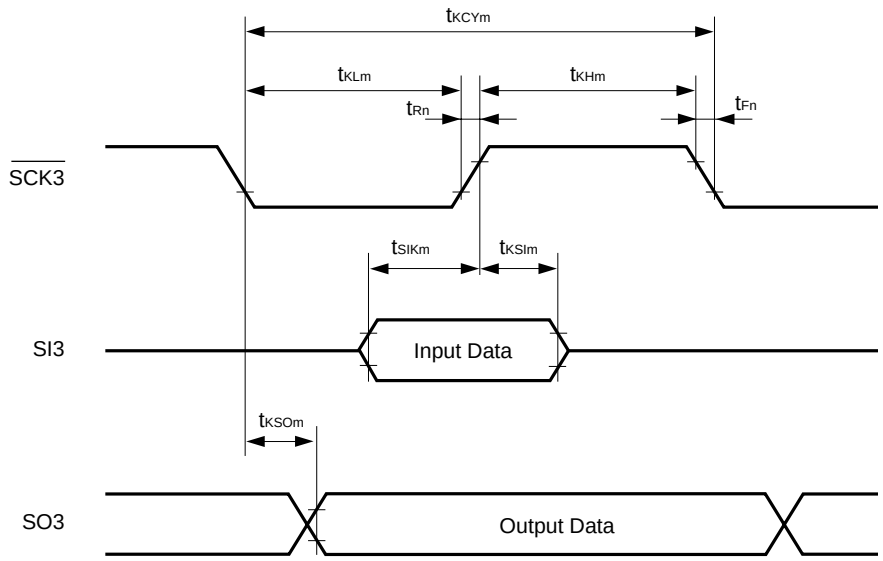


Serial Transfer Timing

I²C bus mode:



3-wire serial I/O mode:



Remark m = 1, 2
n = 2

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total conversion error[Note]		V_{DD} = 4.5 ~ 5.5 V			±1.0	%
					±1.4	%
Conversion time	t_{CONV}		21.3		64.0	μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Note Excluding quantization error (±1/2LSB)

PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin, MF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.5		3.0	MHz
	f_{IN2}	VCOL pin, HF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		40	MHz
	f_{IN3}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	60		130	MHz
	f_{IN4}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.3 V_{P-P}	40		160	MHz

IFC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN5}	AMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz
	f_{IN6}	FMIFC pin, FMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		11	MHz
	f_{IN7}	FMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz

Flash Memory Programming Characteristics (V_{DD} = 3.5 to 5.5 V, T_A = 10 to 40°C)

(1) Write/delete characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin)**Note**	I_{DDW}	When $V_{PP} = V_{PP1}$, f_X = 4.5 MHz			20	mA
Write current (V_{PP} pin)**Note**	I_{PPW}	When $V_{PP} = V_{PP1}$, f_X = 4.5 MHz			20	mA
Delete current (V_{DD} pin)**Note**	I_{DDE}	When $V_{PP} = V_{PP1}$, f_X = 4.5 MHz			20	mA
Delete current (V_{PP} pin)**Note**	I_{PPE}	When $V_{PP} = V_{PP1}$			100	mA
Unit delete time	t_{ER}		0.5	1	1	s
Total delete time	t_{ERA}				20	s
Number of overwrite	C_{WRT}	Delete and write are counted as one cycle			20	times
V_{PP} power supply voltage	V_{PP0}	In normal mode	0		0.2 V_{DD}	V
	V_{PP1}	At flash memory programming	9.7	10.0	10.3	V

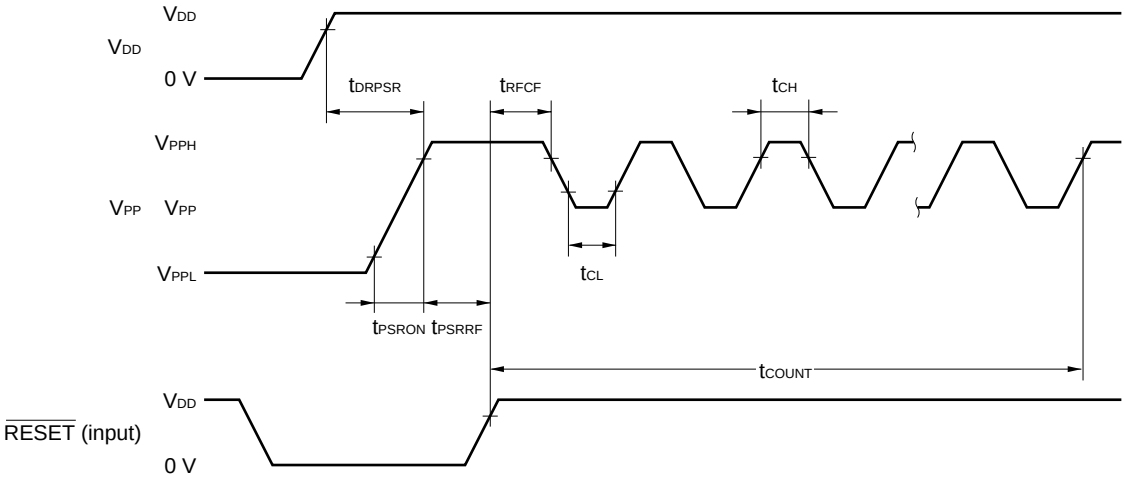
Note AV_{DD} current and Port current (current flowing to internal pull-up resistor) are not included.

Remark f_X: System clock oscillation frequency

(2) Serial write operation characteristics

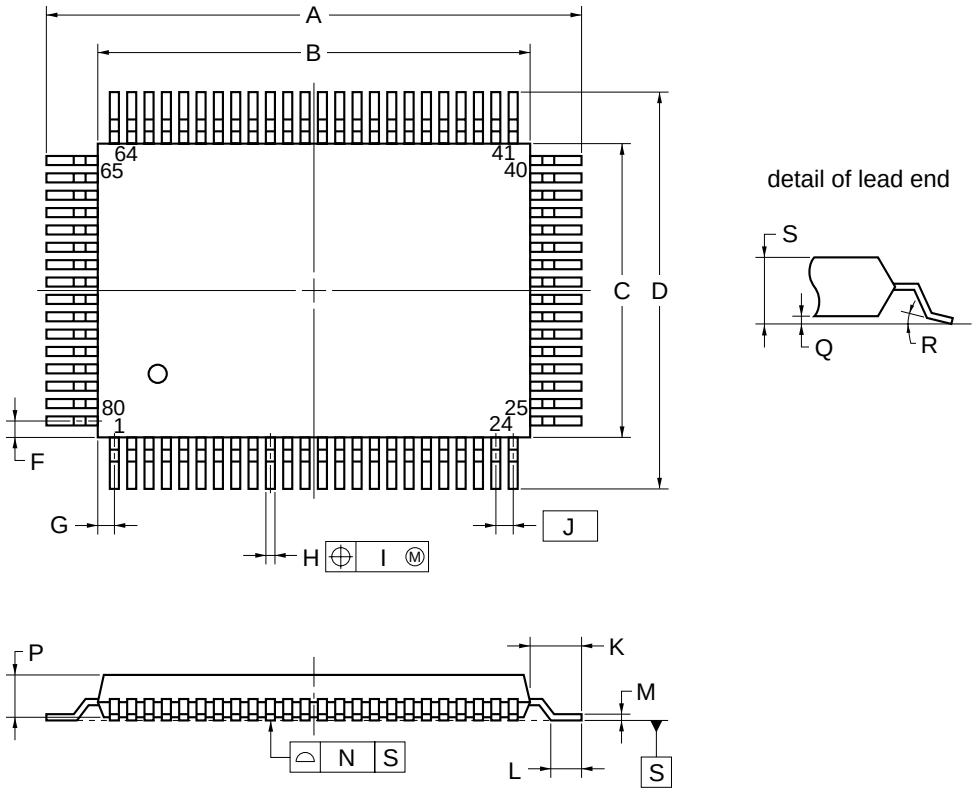
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} setup time	t_{PSRON}	V_{PP} high voltage	1.0			μs
V_{PP}↑ setup time from V_{DD}↑	t_{DRPSR}	V_{PP} high voltage	1.0			μs
$\overline{RESET}$↑ setup time from V_{PP}↑	t_{PSRRF}	V_{PP} high voltage	1.0			μs
V_{PP} count start time from $\overline{RESET}$↑	t_{RFCF}		1.0			μs
Count execution time	t_{COUNT}				2.0	ms
V_{PP} counter high-level width	t_{CH}		8.0			μs
V_{PP} counter low-level width	t_{CL}		8.0			μs
V_{PP} counter noise elimination width	t_{NFW}			40		ns

Flash Write Mode Setting Timing



7. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x20)



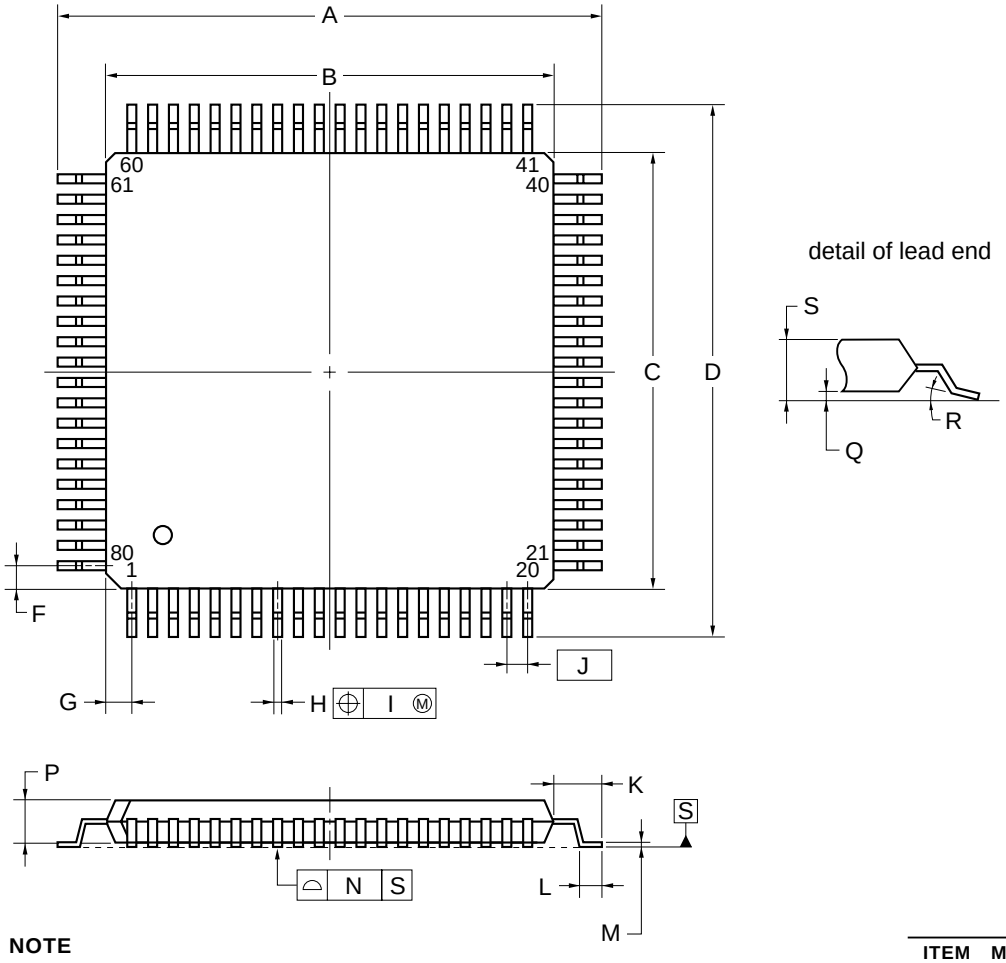
NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	0.8
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P80GF-80-3B9-5

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

8. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Table 8-1. Soldering Conditions for Surface-Mount Type

μPD178F124GF-3B9: 80-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec max. (210°C min.), Number of times: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec max. (200°C min.), Number of times: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec max., Number of times: 1, Preheating temperature: 120°C max., (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec max (per device side)	–

Caution Do not use two or more soldering methods in combination (except partial heating).

μPD178F124GC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec max. (210°C min.), Number of times: 2 max.	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec max. (200°C min.), Number of times: 2 max.	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec max., Number of times: 1, Preheating temperature: 120°C max., (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec max (per device side)	–

Caution Do not use two or more soldering methods in combination (except partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD178F124.

(1) Language processor software

RA78K0[Notes 1, 2, 3]	Assembler package common to 78K/0 series
CC78K0[Notes 1, 2, 3]	C compiler package common to 78K/0 series
DF178124[Notes 1, 2, 3]	Device file for μPD178024 subseries
CC78K0-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0 series

(2) Flash memory writing tools

Fashpro III (Part number: FL-PR3[Note 4], PG-FP3)	Dedicated flash writer
FA-80GF[Note 4]	Flash memory writing adapter
FA-80GC-8BT[Note 4]	

(3) Debugging tools

- **When in-circuit emulator IE-78K0-NS is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board for enhancing and expanding the IE-78K0-NS function
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series (except notebook-type PC) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when a notebook-type PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when a IBM PC/AT™ compatible machine is used (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-178134-NS-EM1	Emulation board for emulating the μPD178024 subseries
NP-80GF[Note 4]	Emulation probe for 80-pin plastic QFP (GF-3B9 type)
EV-9200G-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GF-3B9 type)
NP-80GC[Note 4]	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-8BT type)
SM78K0[Notes 1, 2]	System simulator common to 78K/0 series
ID78K0-NS[Notes 1, 2]	Integrated debugger common to 78K/0 series
DF178124[Notes 1, 2, 3]	Device file for μPD178024 subseries

Notes 1. PC-9800 series (Japanese Windows™) based

2. IBM PC/AT compatible machine (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEW-OS™) based

4. Products of Naito Densei Machida Mfg. Co., Ltd. (Tel: 044-822-3813).

Remark Use the RA78K0, CC78K0, and SM78K0 in combination with the DF178124.

- **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 series
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series (except notebook-type PC) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when a IBM PC/AT compatible machine is used (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-178134-NS-EM1	Emulation board for emulating the μPD178024 subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-178134-NS-EM1 on IE-78001-R-A.
EP-78130GF-R	Emulation probe for 80-pin plastic QFP (GF-3B9 type)
EV-9200G-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GF-3B9 type)
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Socket to be mounted on the board of the target system for 80-pin plastic QFP (GC-8BT type)
SM78K0 Notes 1, 2	System simulator common to 78K/0 series
ID78K0 Notes 1, 2	Integrated debugger common to 78K/0 series
DF178124 Notes 1, 2, 3	Device file for μPD178024 subseries

Real-time OS

RX78K0 Notes 1, 2, 3	Real-time OS for 78K/0 series
MX78K0 Notes 1, 2, 3	OS for 78K/0 series

Notes 1. PC-9800 series (Japanese Windows) based

2. IBM PC/AT compatible machine (Japanese/English windows) based

3. HP9000 series 700 (HP-UX) based, SPARCstation (SunOS, Solaris) based, NEWS (NEW-OS) based

Remark Use SM78K0 in combination with the DF178124.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device Documents

Title		Document No.	
		Japanese	English
μPD178023, 178024 Data Sheet		U14126J	U14126E
μPD178F124 Data Sheet		U14933J	This document
μPD178024, 178124 Subseries User's Manual		U13915J	U13915E
78K/0 Series User's Manual—Instruction		U12326J	U12326E
78K/0 Series Application Note	Basics (I)	U12704J	U12704E
78K/0, 78K/0S Series Flash Memory Write Application Note		U14458J	U14458E

Development Tool Documents (User's Manual)

Title		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
PG-FP3 Flash Memory Programmer		U13502J	U13502E
IE-78001-R-A In-circuit Emulator		U14142J	To be prepared
IE-78K0-NS In-circuit Emulator		U13731J	U13731E
IE-178134-NS-EM1 Emulation Board		To be prepared	To be prepared
EP-78230 Emulation Probe		EEU-985	EEU-1515
EP-78130 Emulation Probe		–	EEU-1470
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	–
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
ID78K0-NS Integrated Debugger Windows Based	Operation	U14379J	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 Windows Based	Operation	U14910J	To be prepared

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

Related Documents for Embedded Software (User's Manual)

Title		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Fundamental	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257J	U12257E

Other Documents

Title	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Guides on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality/Reliability Handbook	C12769J	—
Microcomputer Product Series Guide	U11416J	—

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[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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