NEC

MOS INTEGRATED CIRCUIT

μPD178096A,178098A

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178096A and 178098A are 8-bit single-chip CMOS microcontrollers containing hardware for digital tuning systems.

These microcontrollers employ a 78K/0 Series architecture CPU and allow easy access to internal memories at high speed and easy control of peripheral hardware units. The high-speed 78K/0 Series instructions are ideal for system control.

As peripheral hardware, a prescaler, PLL frequency synthesizer, and frequency counter for digital tuning systems are provided, as well as many I/O ports, timers, A/D converter, serial interface, and a power-ON clear circuit. In addition, the μPD178096A and 178098A have an IEBus™ controller.

Moreover, a flash memory model, the μPD178F098, that operates in the same supply voltage range as the mask ROM models, and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD178078, 178098 Subseries User's Manual: U12790E
78K/0 Series User's Manual - Instructions: U12326E

FEATURES

● High-capacity ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory		
		Internal High-Speed RAM	Internal Buffer RAM	Internal Expansion RAM
μPD178096A	48 KB	1024 bytes	32 bytes	1024 bytes
μPD178098A	60 KB			2048 bytes

● Instruction cycle:
0.32 μs (with crystal resonator of fx = 6.3 MHz)

● Many internal hardware units
General-purpose I/O ports, A/D converter, serial interface, IEBus controller, timers, frequency counter, power-ON clear circuit

● Hardware for PLL frequency synthesizer
dual modulus prescaler, programmable divider, phase comparator, charge pump

● Vectored interrupt sources: 21

● Supply voltage:
V_{DD} = 4.5 to 5.5 V (during PLL and CPU operations)
V_{DD} = 3.5 to 5.5 V (during CPU operation)

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APPLICATION FIELD

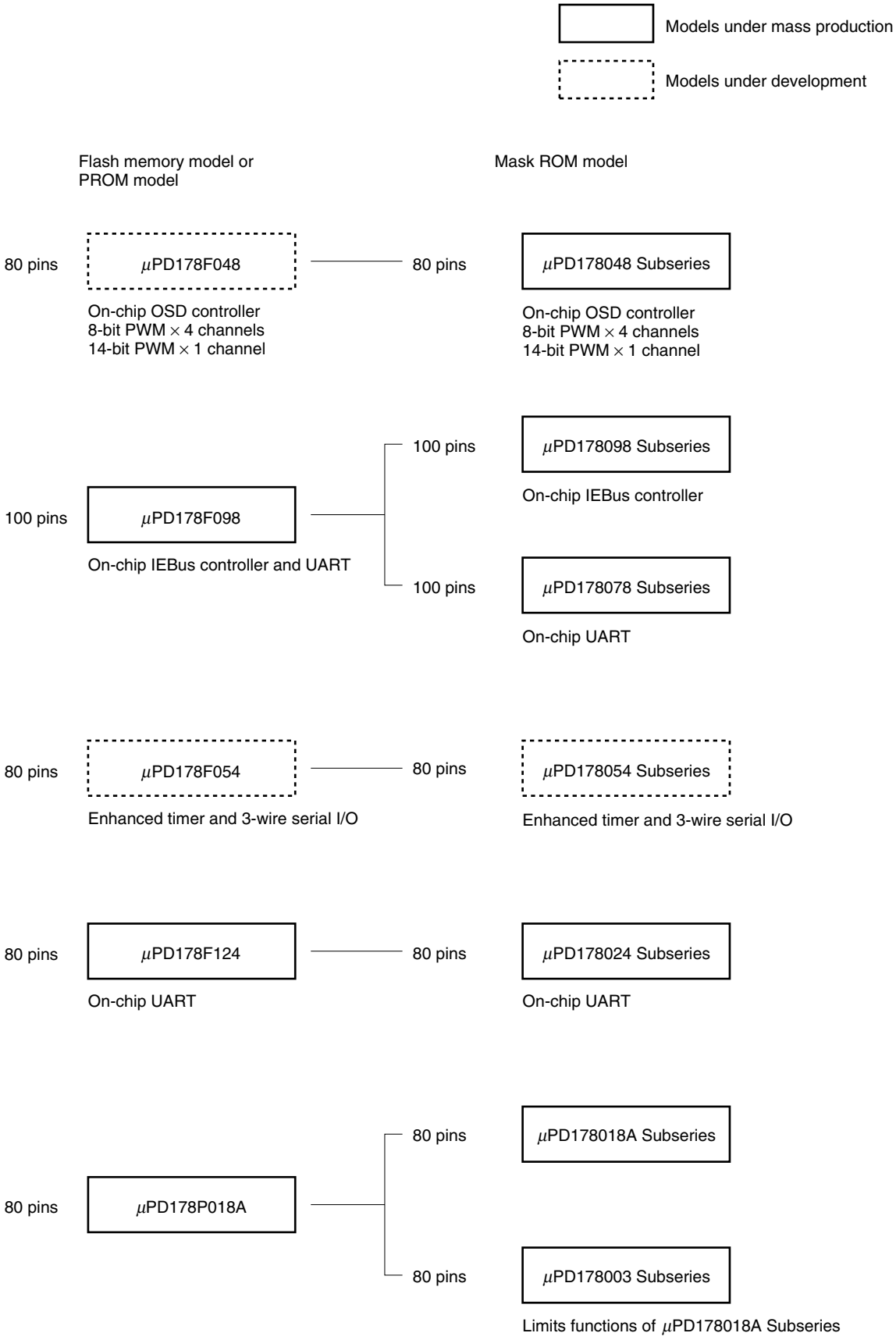
Car stereos

ORDERING INFORMATION

Part Number	Package
μPD178096AGF-×××-3BA	100-pin plastic QFP (14 × 20)
μPD178098AGF-×××-3BA	100-pin plastic QFP (14 × 20)

Remark ××× indicates ROM code suffix, which is E×× when the I^2C bus is used.

8-BIT DTS SERIES LINEUP



OVERVIEW OF FUNCTIONS

(1/2)

Item		μPD178096A	μPD178098A
Internal memory	ROM	48 KB	60 KB
	High-speed RAM	1024 bytes	
	Buffer RAM	32 bytes	
	Expansion RAM	1024 bytes	2048 bytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		• 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.08 μs (with crystal resonator of fx = 6.3 MHz) • 0.44 μs/0.89 μs/1.78 μs/3.56 μs/7.11 μs (with crystal resonator of fx = 4.5 MHz)**Note 1**	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 80 pins • CMOS input: 8 pins • CMOS I/O: 64 pins • N-ch open-drain output: 8 pins	
A/D converter		8-bit resolution × 8 channels	
Serial interface		• 3-wire/SBI/2-wire/I²C bus**Note 2** mode selectable: 1 channel • 3-wire mode: 1 channel • 3-wire mode (with automatic transmit/receive function of up to 32 bytes): 1 channel	
IEBus controller		Provided	
Timer		• Basic timer (timer carry FF (10 Hz)): 1 channel • 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watchdog timer: 1 channel	
Buzzer output		BEEP0 pin: 1 kHz, 1.5 kHz, 3 kHz, 4 kHz	
		BUZ pin: 0.77 kHz, 1.54 kHz, 3.08 kHz, 6.15 kHz (with crystal resonator of fx = 6.3 MHz)	

Notes 1. When using the IEBus controller, the 4.5 MHz crystal resonator cannot be used. Be sure to use the 6.3 MHz crystal resonator.

2. When the I²C bus mode is used (including when the mode is implemented in software without using the peripheral hardware), consult NEC when ordering a mask.

(2/2)

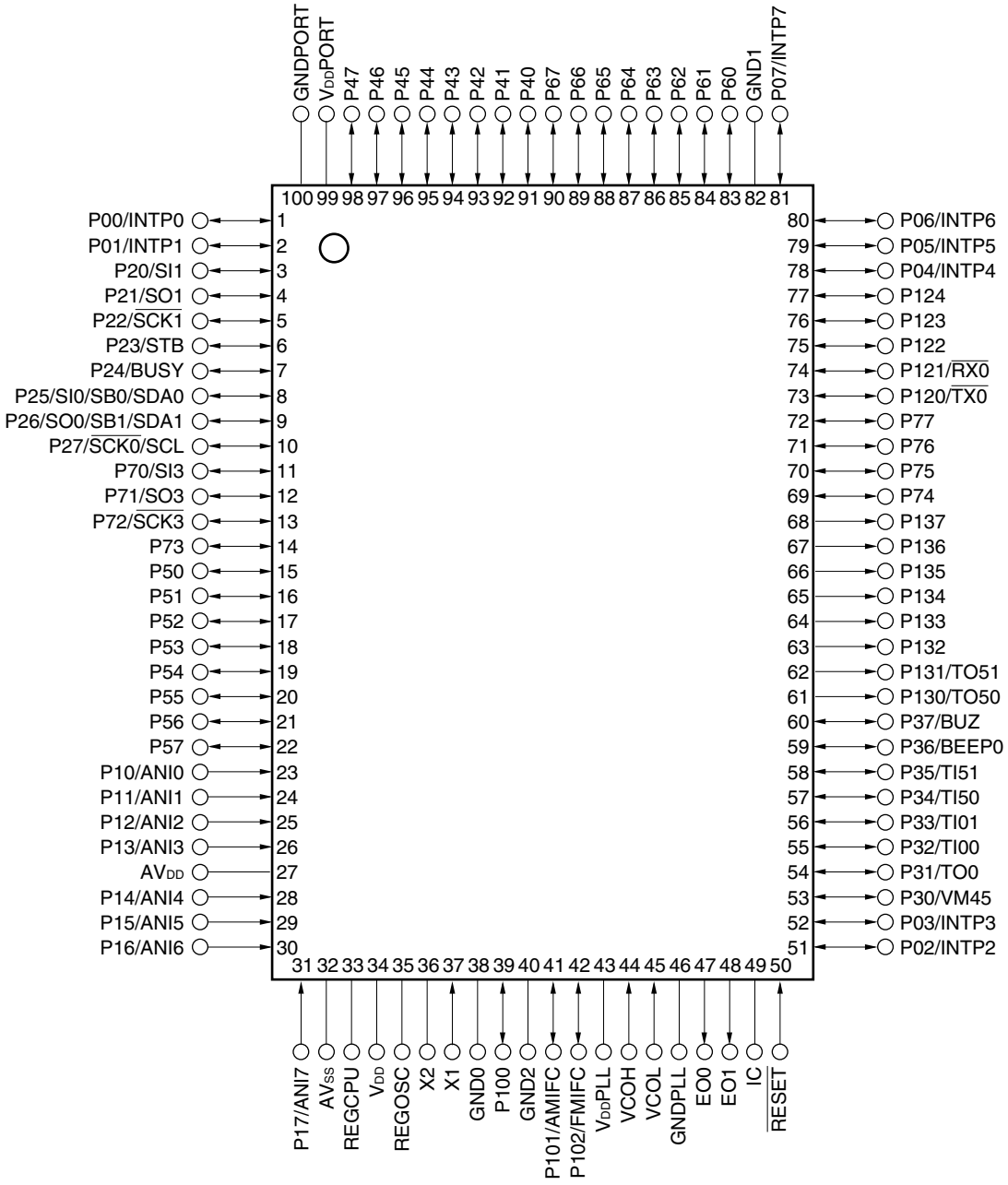
Item		μPD178096A	μPD178098A
Vectored interrupt sources	Maskable	Internal: 12 External: 8	
	Non-maskable	Internal: 1	
	Software	1	
PLL frequency synthesizer	Division mode	2 types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOL and VCOH pins)	
	Reference frequency	Seven types selectable in software (1, 3, 9, 10, 12.5, 25, 50 kHz)	
	Charge pump	Error out output: 2 pins	
	Phase comparator	Unlock detectable in software	
Frequency counter		Frequency measurement • AMIFC pin: For 450 kHz counting • FMIFC pin: For 450 kHz/10.7 MHz counting	
Standby function		• HALT mode • STOP mode	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit • Detection of less than 4.5 V[Note] (Reset does not occur, however.) • Detection of less than 3.5 V[Note] (during CPU operation) • Detection of less than 2.3 V[Note] (in STOP mode)	
Supply voltage		• V_{DD} = 4.5 to 5.5 V (during CPU, PLL operation) • V_{DD} = 3.5 to 5.5 V (during CPU operation)	
Package		100-pin plastic QFP (14 × 20)	

Note These voltages are the maximum values. In practice, the chip may be reset at voltages lower than these.

PIN CONFIGURATION (Top View)

• 100-pin plastic QFP (14 × 20)

μPD178096AGF-×××-3BA, 178098AGF-×××-3BA



Cautions 1. Connect the IC (Internally Connect) pin directly to GND0, GND1, or GND2.

2. Keep the voltage at AV_{DD}, V_{DD}PORT, and V_{DD}PLL pins same as that at the V_{DD} pin.

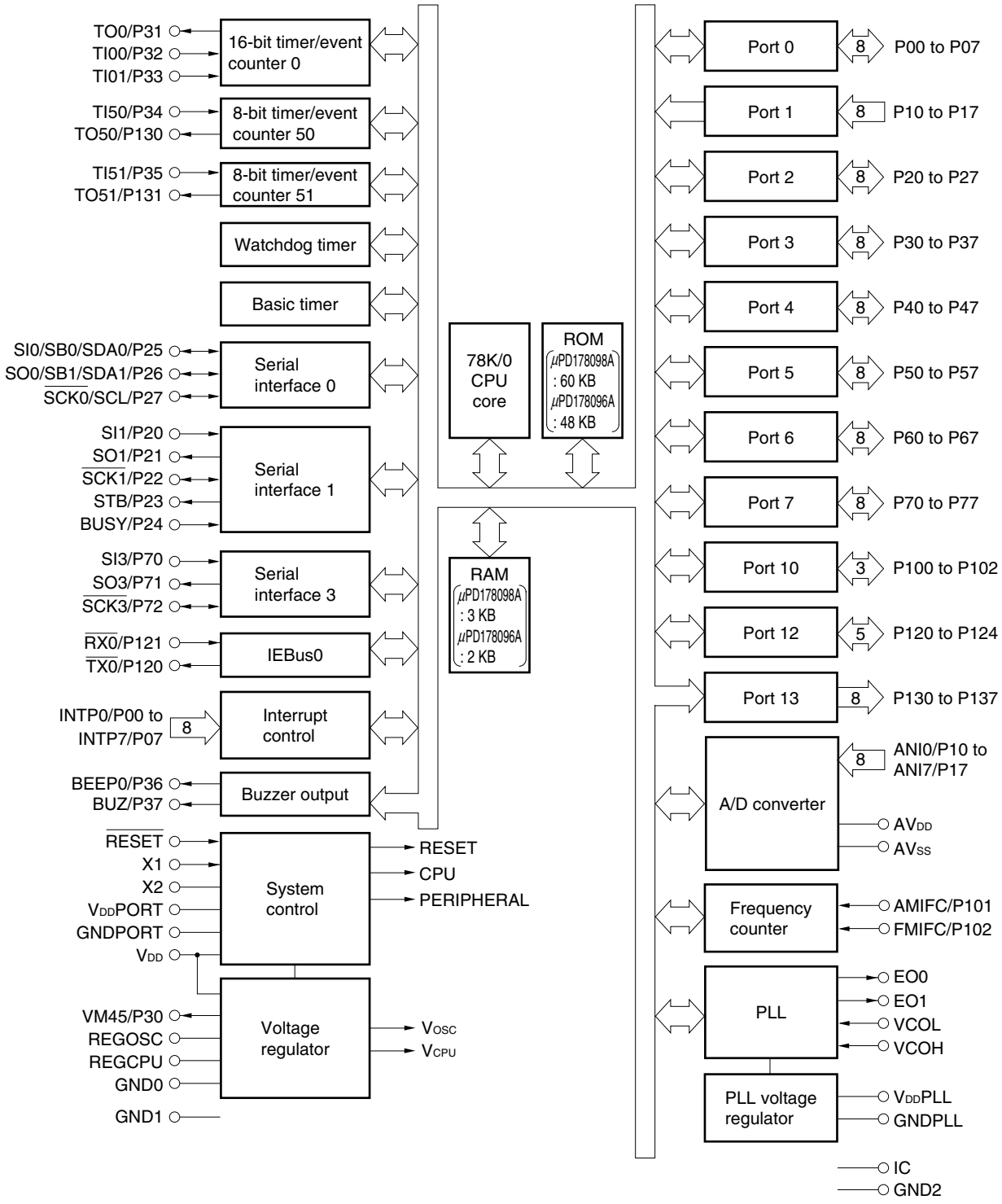
3. Keep the voltage at AV_{SS}, GNDPORT, and GNDPLL pins same as that at GND0, GND1, or GND2.

4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1 μF capacitor.

Pin Name

AMIFC:	AM intermediate frequency counter input	P130 to P137:	Port 13
		REGCPU:	Regulator for CPU power supply
ANI0 to ANI7:	A/D converter input	REGOSC:	Regulator for oscillation circuit
AV_{DD}:	A/D converter power supply	$\overline{RESET}$:	Reset input
AV_{SS}:	A/D converter ground	$\overline{RX0}$:	IEBus serial data input
BUSY:	Busy output	SB0, SB1:	Serial data bus input/output
BEEP0, BUZ:	Buzzer output	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK3}$:	Serial clock input/output
EO0, EO1:	Error out output	SCL:	Serial clock input/output
FMIFC:	FM intermediate frequency counter input	SDA0, SDA1:	Serial data input/output
		SI0, SI1, SI3:	Serial data input
GNDPLL:	PLL ground	SO0, SO1, SO3:	Serial data output
GND0 to GND2:	Ground	STB:	Strobe output
IC:	Internally connected	TI00, TI01:	16-bit timer capture trigger input
INTP0 to INTP7:	Interrupt input	TI50, TI51:	8-bit timer clock input
P00 to P07:	Port 0	TO0:	16-bit timer output
P10 to P17:	Port 1	TO50, TO51:	8-bit timer output
P20 to P27:	Port 2	$\overline{TX0}$:	IEBus serial data output
P30 to P37:	Port 3	VCOL, VCOH:	Local oscillation input
P40 to P47:	Port 4	V_{DD}PORT:	Port power supply
P50 to P57:	Port 5	V_{DD}PLL:	PLL power supply
P60 to P67:	Port 6	V_{DD}:	Power supply
P70 to P77:	Port 7	VM45:	V_{DD} = 4.5 V monitor output
P100 to P102:	Port 10	X1, X2:	Crystal resonator
P120 to P124:	Port 12		

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	Input	INTP0 to INTP7
P10 to P17	Input	Port 1 8-bit input port	Input	ANI0 to ANI7
P20	I/O	Port 2	Input	SI1
P21		8-bit I/O port		SO1
P22		Input/output can be specified in 1-bit units.		$\overline{\text{SCK1}}$
P23				STB
P24				BUSY
P25				SI0/SB0/SDA0
P26				SO0/SB1/SDA1
P27				$\overline{\text{SCK0}}$/SCL
P30	I/O	Port 3	Input	VM45
P31		8-bit I/O port		TO0
P32		Input/output can be specified in 1-bit units.		TI00
P33				TI01
P34				TI50
P35				TI51
P36				BEEP0
P37				BUZ
P40 to 47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	Input	–
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	Input	–
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units.	Input	–
P70	I/O	Port 7	Input	SI3
P71		8-bit I/O port		SO3
P72		Input/output can be specified in 1-bit units.		$\overline{\text{SCK3}}$
P73				–
P74				–
P75				–
P76, P77				–

1.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P100	I/O	Port 10	Input	–
P101		3-bit I/O port		AMIFC
P102		Input/output can be specified in 1-bit units.		FMIFC
P120	I/O	Port 12	Input	$\overline{TX0}$
P121		5-bit I/O port		$\overline{RX0}$
P122 to P124		Input/output can be specified in 1-bit units.		–
P130	Output	Port 13	Low-level output	TO50
P131		8-bit output port		TO51
P132 to P137		N-ch open-drain output port (15 V withstand)		–

1.2 Non-Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
INTP0 to INTP7	Input	External maskable interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.		Input	P00 to P07
SI0	Input	Serial interface serial data input		Input	P25/SB0/SDA0
SI1					P20
SI3					P70
SO0	Output	Serial interface serial data output		Input	P26/SB1/SDA1
SO1					P21
SO3					P71
SB0	I/O	Serial interface serial data input/output	N-ch open drain I/O	Input	P25/SI0/SDA0
SB1					P26/SO0/SDA1
SDA0					P25/SI0/SB0
SDA1					P26/SO0/SB1
$\overline{SCK0}$	I/O	Serial interface serial clock input/output		Input	P27/SCL
$\overline{SCK1}$					P22
$\overline{SCK3}$					P72
SCL			N-ch open drain I/O		P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output		Input	P23
BUSY	Input	Serial interface automatic transmit busy input		Input	P24
VW45	Output	V_{DD} = 4.5 V monitor output		Input	P30
TI00	Input	External count clock input to 16-bit timer/event counter 0		Input	P32
TI01					P33
TI50	Input	External count clock input to 8-bit timer/event counter 50		Input	P34
TI51		External count clock input to 8-bit timer/event counter 51			P35

1.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TO0	Output	16-bit timer/event counter 0 output	Input	P31
TO50		8-bit timer/event counter 50 output	Low-level output	P130
TO51		8-bit timer/event counter 51 output		P131
BEEP0	Output	Buzzer output	Input	P36
BUZ				P37
ANI0 to ANI7	Input	Analog input to A/D converter	Input	P10 to P17
EO0, EO1	Output	Error out output from charge pump of PLL frequency synthesizer	–	–
VCOL	Input	Inputs local oscillation frequency of PLL (in HF and MF modes)	–	–
VCOH	Input	Inputs local oscillation frequency of PLL (in VHF mode)	–	–
AMIFC	Input	Input to AM intermediate frequency counter	Input	P101
FMIFC	Input	Input to FM intermediate frequency or AM intermediate frequency counter	Input	P102
$\overline{TX0}$	Output	IEBus controller data output	Input	P120
$\overline{RX0}$	Input	IEBus controller data input	Input	P121
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connection of crystal resonator for system clock oscillation	–	–
X2	–		–	–
REGOSC	–	Regulator for oscillation circuit. Connect this pin to GND via 0.1 μF capacitor	–	–
REGCPU	–	Regulator for CPU power supply. Connect this pin to GND via 0.1 μF capacitor	–	–
V_{DD}	–	Positive power supply	–	–
GND0 to GND2	–	Ground	–	–
V_{DD}PORT	–	Port power supply	–	–
GNDPORT	–	Port ground	–	–
AV_{DD}	–	A/D converter positive power supply. Keep voltage at this pin same as that at V_{DD}	–	–
AV_{SS}	–	A/D converter ground. Keep voltage at this pin same as that at GND0 through GND2	–	–
V_{DD}PLL**Note**	–	PLL positive power supply	–	–
GNDPLL**Note**	–	PLL ground	–	–
IC	–	Internally connected. Directly connect this pin to GND0, GND1, or GND2	–	–

Note Connect a capacitor of about 1000 pF between the V_{DD}PLL and GNDPLL pins.

1.3 Pin I/O Circuits and Recommended Connections of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, refer to **Figure 3-1**.

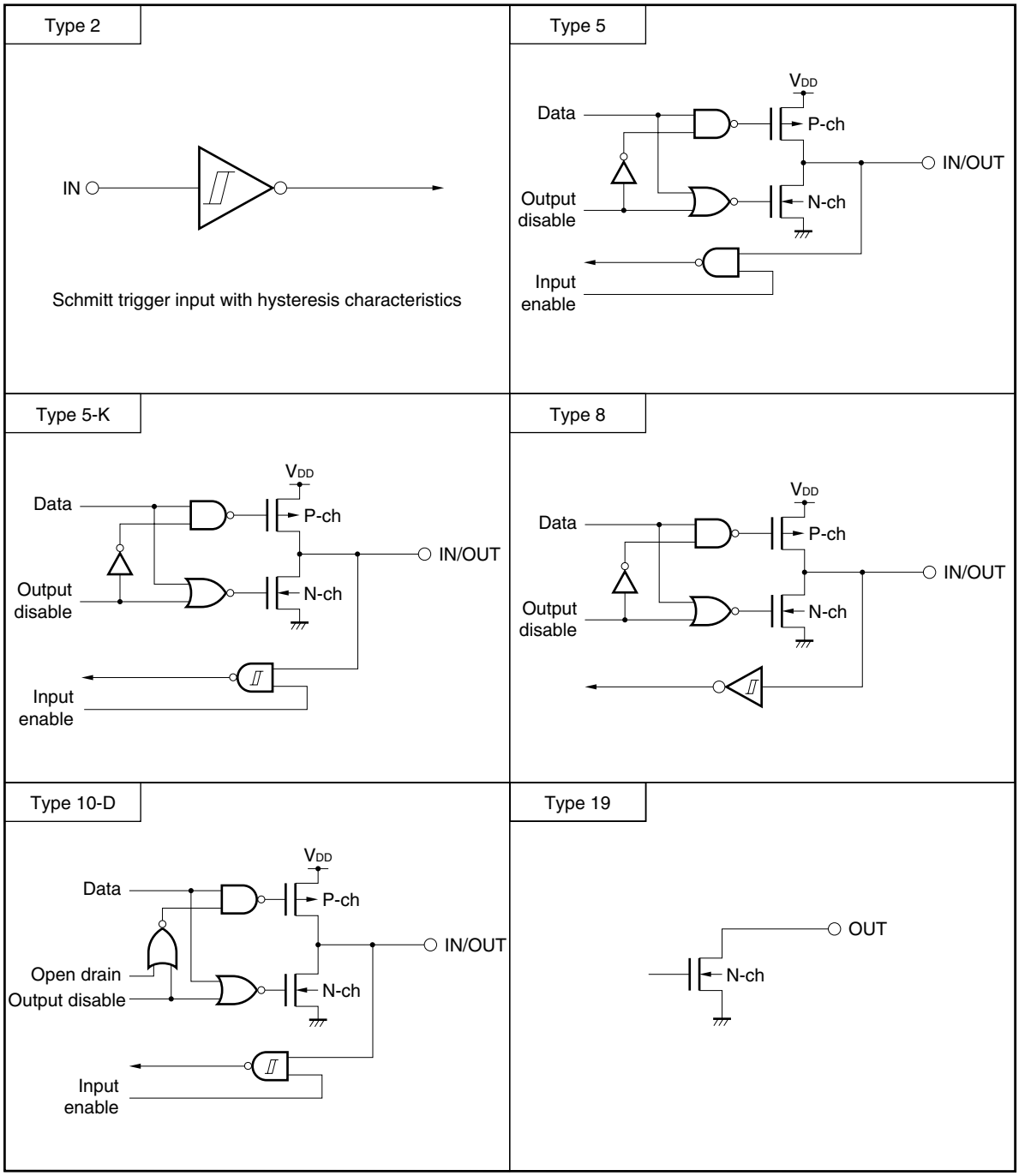
Table 1-1. Types of I/O Circuit (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P00/INTP0 to P07/INTP7	8	I/O	Input: Independently connect to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT via a resistor. Output: Leave open.
P10/ANI0 to P17/ANI7	25	Input	Connect to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT.
P20/SI1	5-K	I/O	Input: Independently connect to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT via a resistor. Output: Leave open.
P21/SO1	5		
P22/$\overline{\text{SCK1}}$	5-K		
P23/STB	5		
P24/BUSY	5-K		
P25/SI0/SB0/SDA0	10-D		
P26/SO0/SB1/SDA1			
P27/$\overline{\text{SCK0}}$/SCL			
P30/VM45	5		
P31/TO0			
P32/TI00	5-K		
P33/TI01			
P34/TI50			
P35/TI51			
P36/BEEP0	5		
P37/BUZ			
P40 to P47			
P50 to P57			
P60 to P67			
P70/SI3	5-K		
P71/SO3	5		
P72/$\overline{\text{SCK3}}$	5-K		
P73	5		
P74	5-K		
P75	5		
P76, P77			
P100			
P101/AMIFC			
P102/FMIFC			
P120/$\overline{\text{TX0}}$			
P121/$\overline{\text{RX0}}$	5-K		
P122 to P124	5		

Table 1-1. Types of I/O Circuit (2/2)

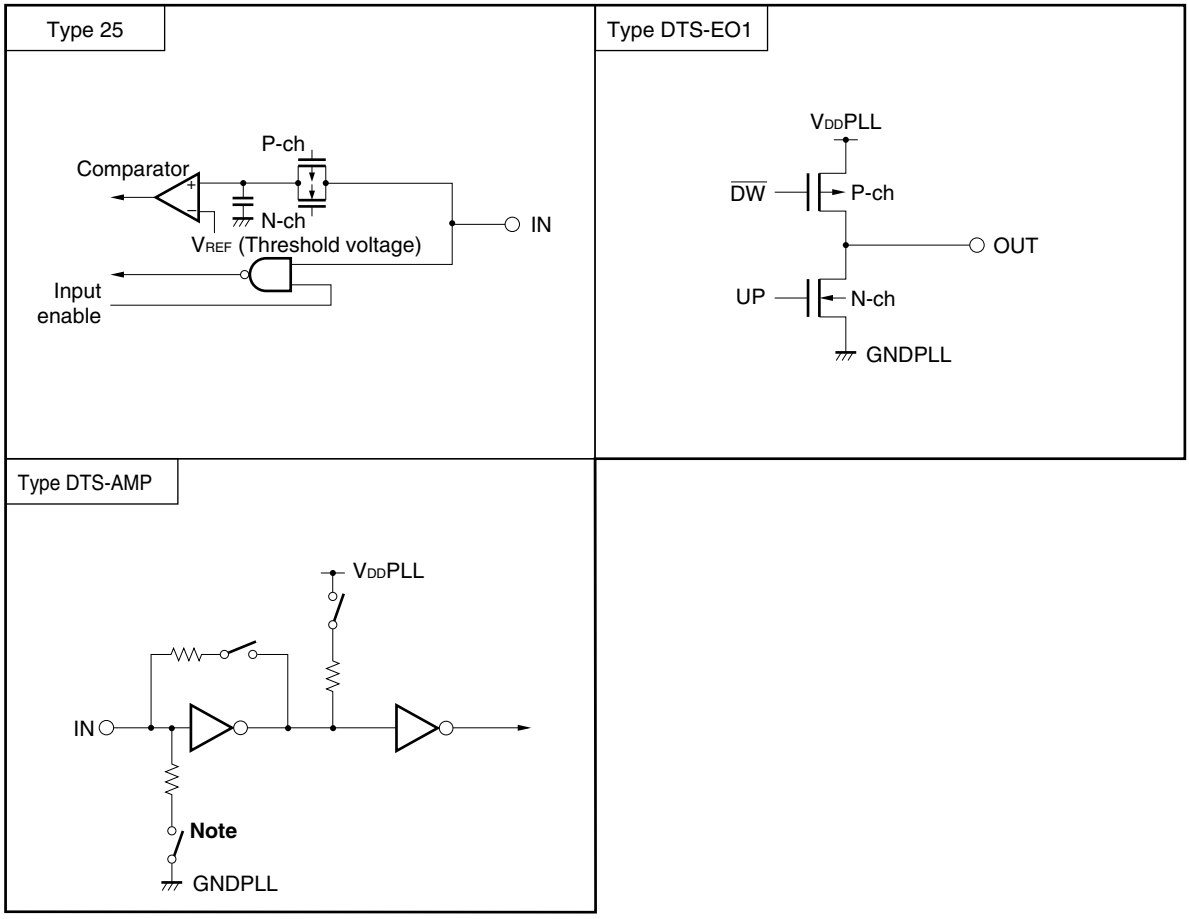
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P130/TO50	19	Output	Leave open.
P131/TO51			
P132 to P137			
EO0	DTS-EO1		
EO1			
VCOL, VCOH	DTS-AMP2	Input	Disable PLL in software and select pull-down.
REGOSC, REGCPU	–	–	Connect to GND0, GND1, or GND2 via 0.1 μF capacitor.
$\overline{\text{RESET}}$	2	Input	–
AV_{DD}	–	–	Connect to V_{DD} or V_{DD}PORT.
AV_{SS}			Connect directly to GND0 to GND2, or GNDPORT.
IC			

Figure 1-1. Pin I/O Circuits (1/2)



Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

Figure 1-1. Pin I/O Circuits (2/2)



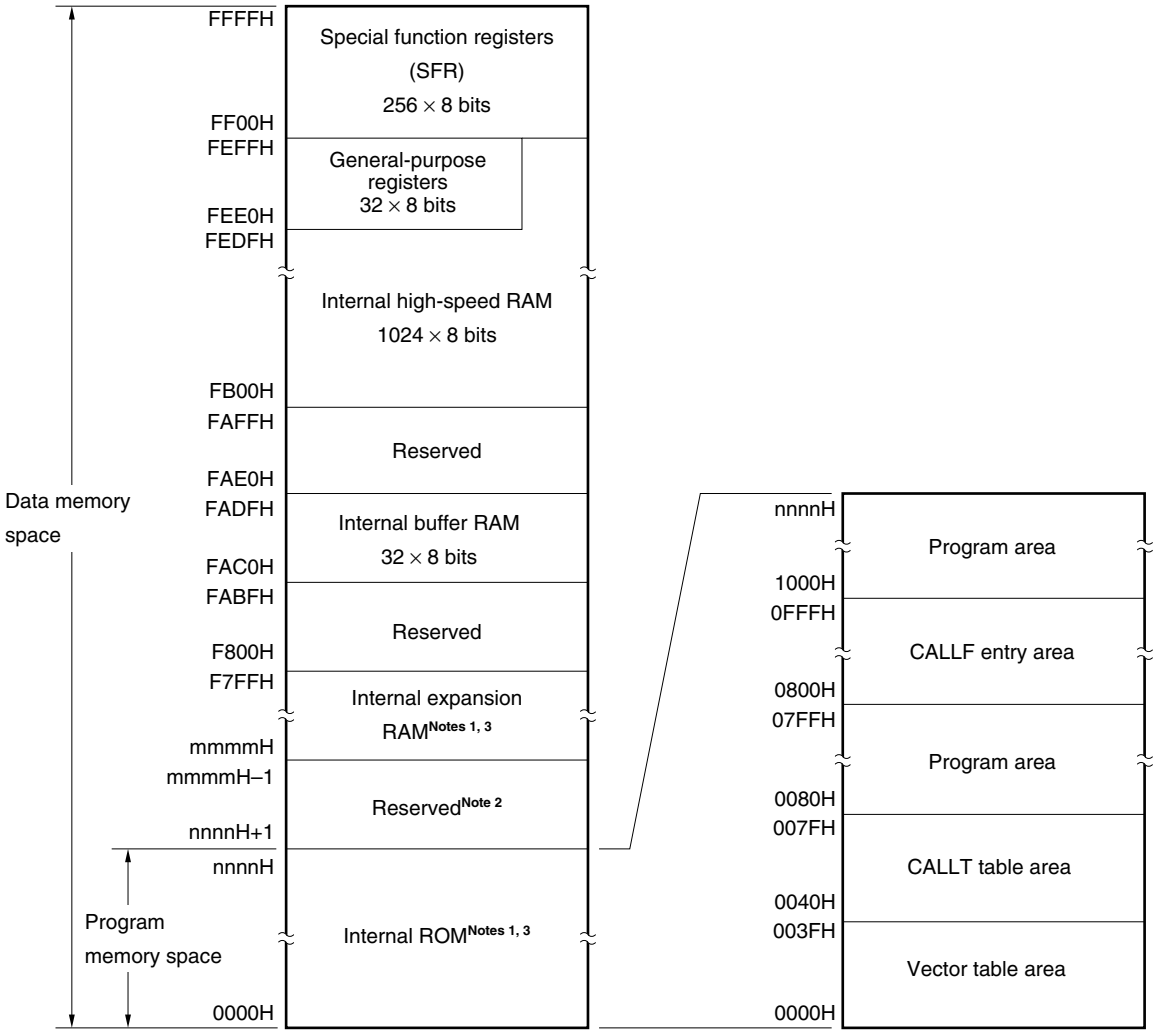
Note This switch is selectable in software only for the VCOL and VCOH pins.

Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

2. MEMORY SPACE

Figure 2-1 shows the memory map of the μPD178096A and 178098A.

Figure 2-1. Memory Map



Notes 1. The internal ROM and internal expansion RAM capacities vary depending on the model (refer to the table below).

Part Number	Internal ROM Last Address nnnnH	Internal Expansion RAM First Address mmmmH
μPD178096A	BFFFH	F400H
μPD178098A	EFFFH	F000H

2. The μPD178098A does not have this reserved area.

Notes 3. The initial values of the memory size switching register (IMS) and internal expansion RAM size switching register (IXS) are CFH and 0CH, respectively. The following values must be set to the registers of each model.

Part Number	IMS	IXS
μPD178096A	CCH	0AH
μPD178098A	CFH	08H

2.1 Memory Size Switching Register (IMS)

IMS is used to select the capacity of the internal memory.

Set CCH to this register of the μPD178096A. Set CFH to the IMS of the μPD178098A.

Use an 8-bit memory manipulation instruction to set IMS.

IMS is set to CFH after reset.

Figure 2-2. Format of Memory Size Switching Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selection of internal high-speed RAM capacity
1	1	0	1024 bytes
Other than above			Setting prohibited

RAM3	RAM2	RAM1	RAM0	Selection of internal ROM capacity
1	1	0	0	48 KB
1	1	1	1	60 KB
Other than above				Setting prohibited

2.2 Internal Expansion RAM Size Switching Register (IXS)

IXS is used to select the capacity of the internal expansion RAM.

Set 0AH of this register of the μPD178096A. Set 08H of the IXS of the μPD178098A.

Use an 8-bit memory manipulation instruction to set IXS.

IXS is set to 0CH after reset.

Figure 2-3. Format of Internal Expansion RAM Size Switching Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of internal expansion RAM capacity
0	1	0	0	0	2048 bytes
0	1	0	1	0	1024 bytes
Other than above					Setting prohibited

3. PERIPHERAL HARDWARE FUNCTION FEATURES

3.1 Ports

The following three types of I/O ports are available:

• CMOS input (port 1):	8 pins
• CMOS I/O (ports 0, 2 to 7, 10, and 12):	64 pins
• N-ch open-drain output (port 13):	8 pins
Total:	80 pins

Table 3-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units.
Port 1	P10 to P17	Input-only port.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units.
Port 3	P30 to P37	I/O port. Input/output can be specified in 1-bit units.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units.
Port 6	P60 to P67	I/O port. Input/output can be specified in 1-bit units.
Port 7	P70 to P77	I/O port. Input/output can be specified in 1-bit units.
Port 10	P100 to P102	I/O port. Input/output can be specified in 1-bit units.
Port 12	P120 to P124	I/O port. Input/output can be specified in 1-bit units.
Port 13	P130 to P137	N-ch open-drain output port.

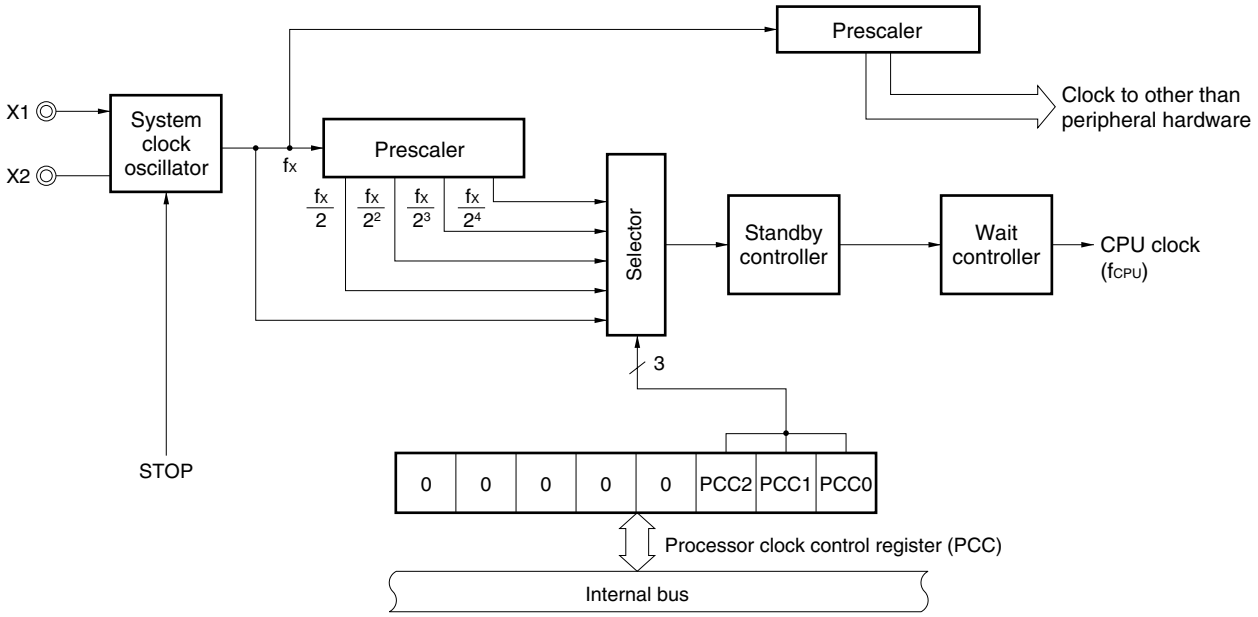
3.2 Clock Generator

The instruction execution time can be changed as follows:

- 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.08 μs (system clock: 6.3 MHz crystal resonator)
- 0.44 μs/0.89 μs/1.78 μs/3.56 μs/7.11 μs (system clock: 4.5 MHz crystal resonator)[Note]

Note When using the IEBus controller, the 4.5 MHz crystal resonator cannot be used. Be sure to use the 6.3 MHz crystal resonator.

Figure 3-1. Block Diagram of Clock Generator

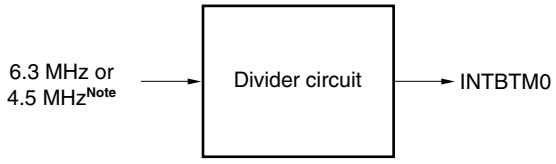


3.3 Timers

Five timer channels are provided.

- Basic timer: 1 channel
- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watchdog timer: 1 channel

Figure 3-2. Block Diagram of Basic Timer



Note When using the IEBus controller, the 4.5 MHz crystal resonator cannot be used. Be sure to use the 6.3 MHz crystal resonator.

Figure 3-3. Block Diagram of 16-Bit Timer/Event Counter 0

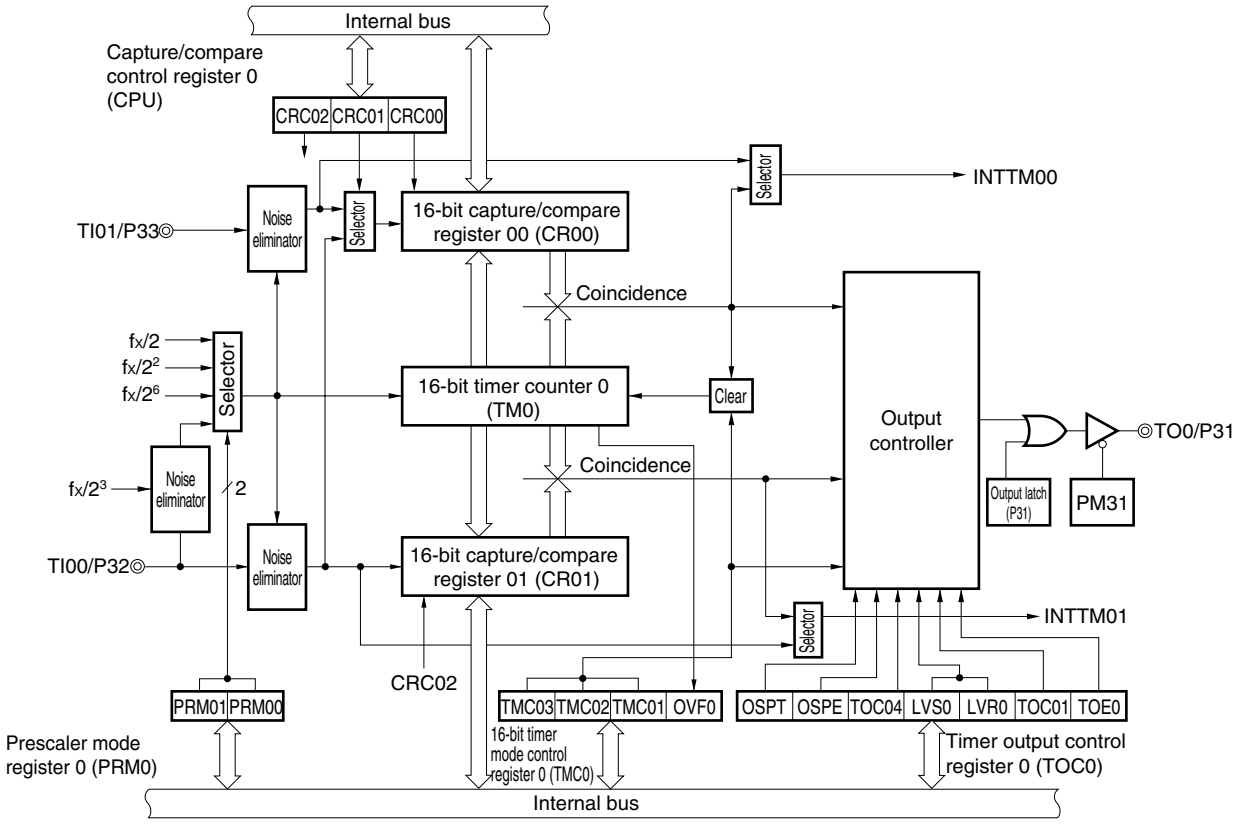


Figure 3-4. Block Diagram of 8-Bit Timer/Event Counter 50

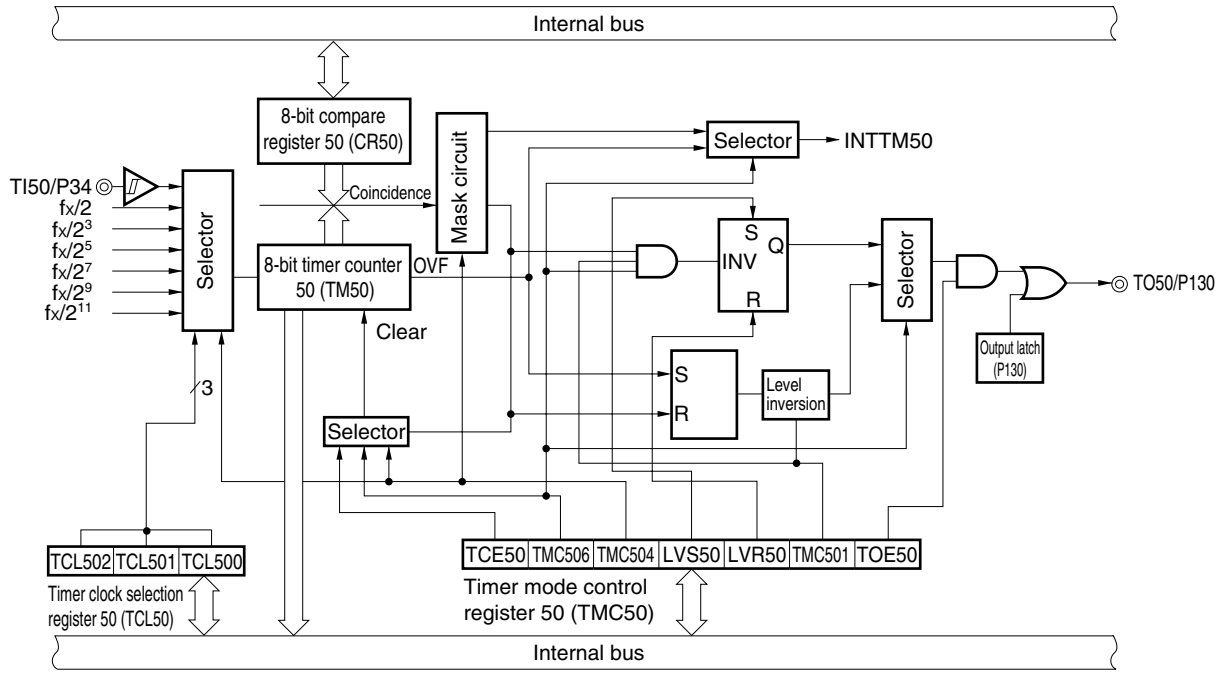


Figure 3-5. Block Diagram of 8-Bit Timer/Event Counter 51

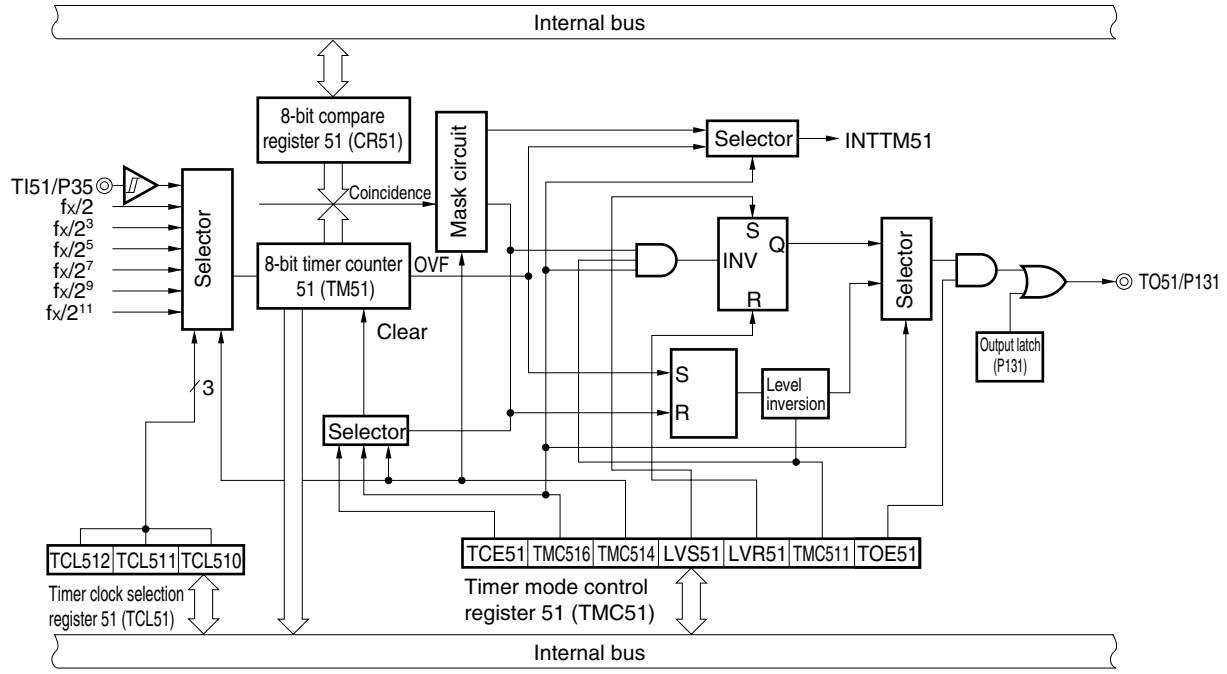
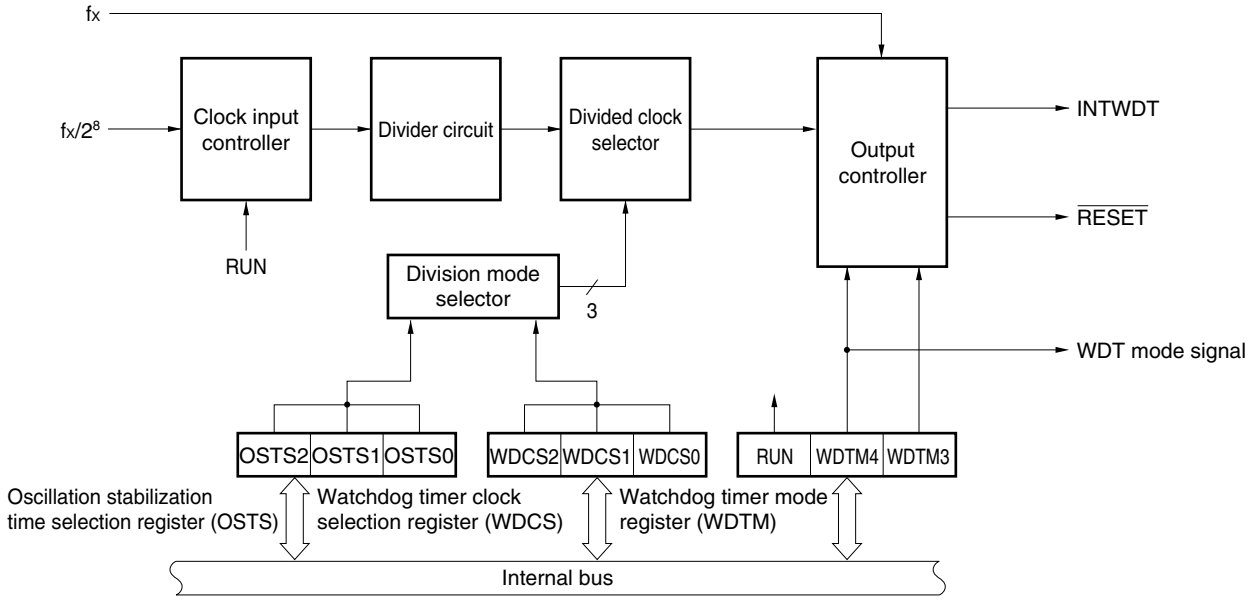


Figure 3-6. Block Diagram of Watchdog Timer



3.4 Buzzer Output Controller

Two types of buzzer output controllers are provided.

- BEEP0 ... 1 kHz/1.5 kHz/3 kHz/4 kHz
- BUZ ... 0.77 kHz/1.54 kHz/3.08 kHz/6.15 kHz (system clock: 6.3 MHz crystal resonator)

Figure 3-7. Block Diagram of Buzzer Output Controller (BEEP0)

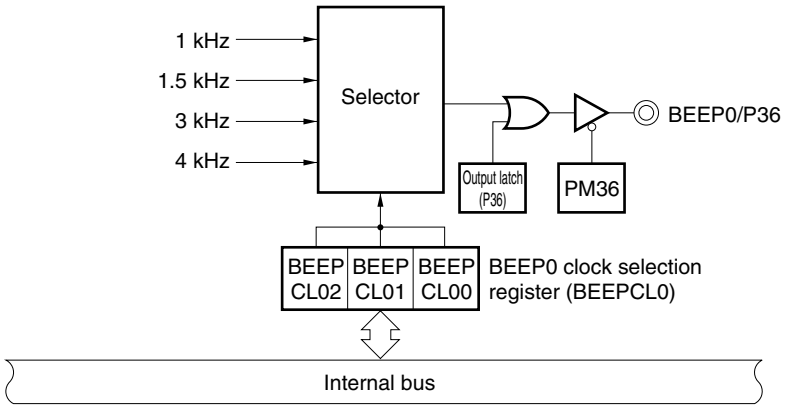
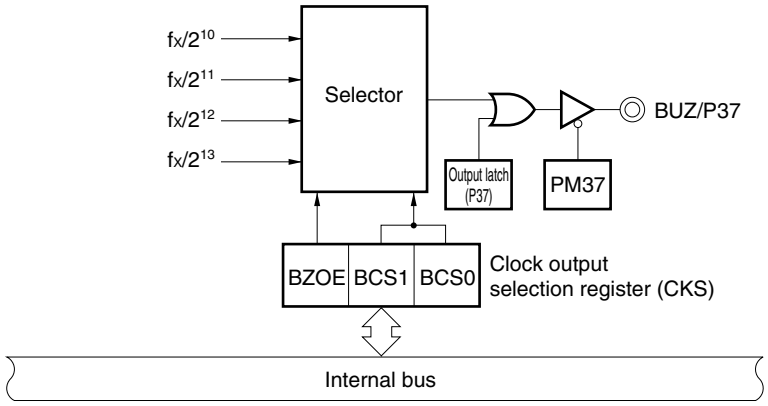


Figure 3-8. Block Diagram of Buzzer Output Controller (BUZ)

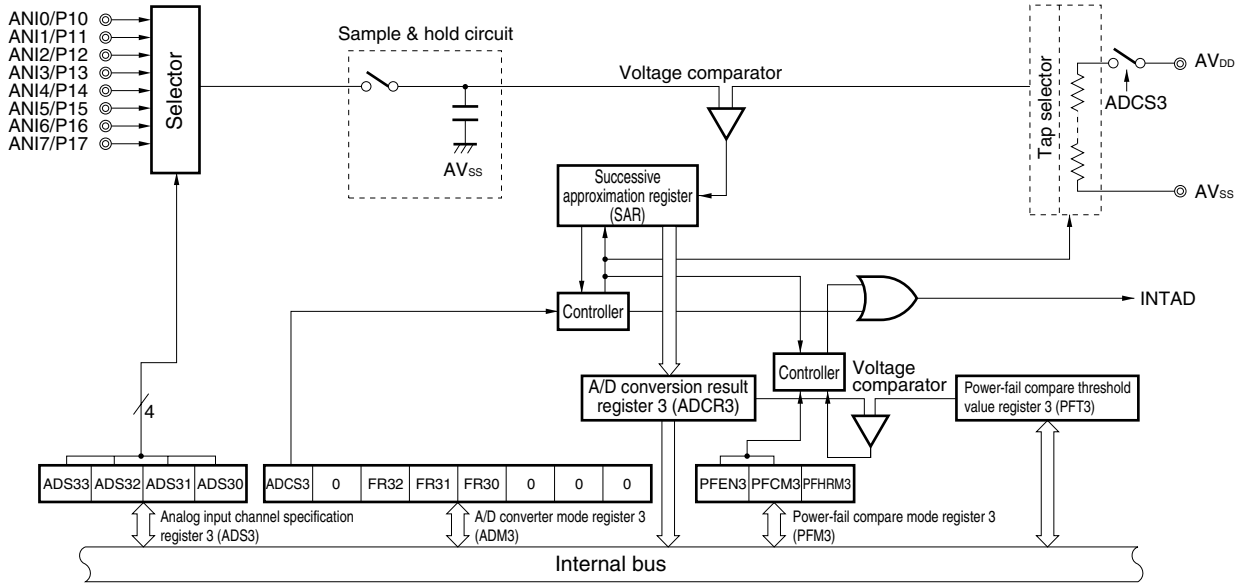


Remark fx: System clock frequency

3.5 A/D Converter

An A/D converter with a resolution of 8 bits × 8 channels is provided.

Figure 3-9. Block Diagram of A/D Converter



3.6 Serial Interface

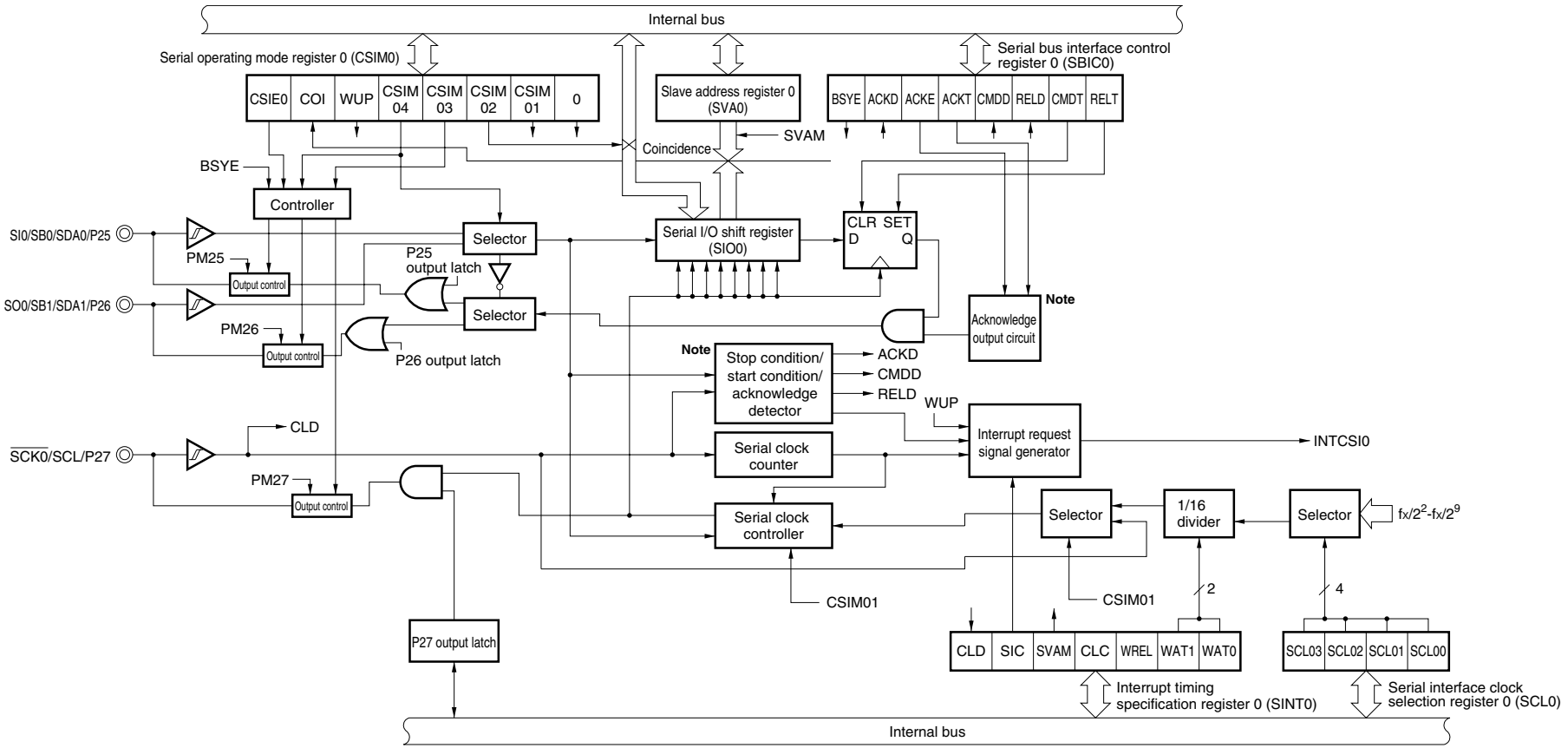
The μPD178096A and 178098A have three channels.

- Serial interface 0
- Serial interface 1
- Serial interface 3

Table 3-2. Types and Functions of Serial Interfaces

Function	Serial Interface 0	Serial Interface 1	Serial Interface 3
3-wire serial I/O mode	○ (MSB/LSB first selectable)	○ (MSB/LSB first selectable)	○ (MSB first)
3-wire serial I/O mode with automatic transmit/receive function	–	○ (MSB/LSB first selectable)	–
SBI (serial bus interface) mode	○ (MSB first)	–	–
2-wire serial I/O mode	○ (MSB first)	–	–
I^2C bus mode	○ (MSB first)	–	–

Figure 3-10. Block Diagram of Serial Interface 0



Note Example in I^2C bus mode operation.

Remark Output control performs selection between CMOS output and N-ch open drain output.

Figure 3-11. Block Diagram of Serial Interface 1

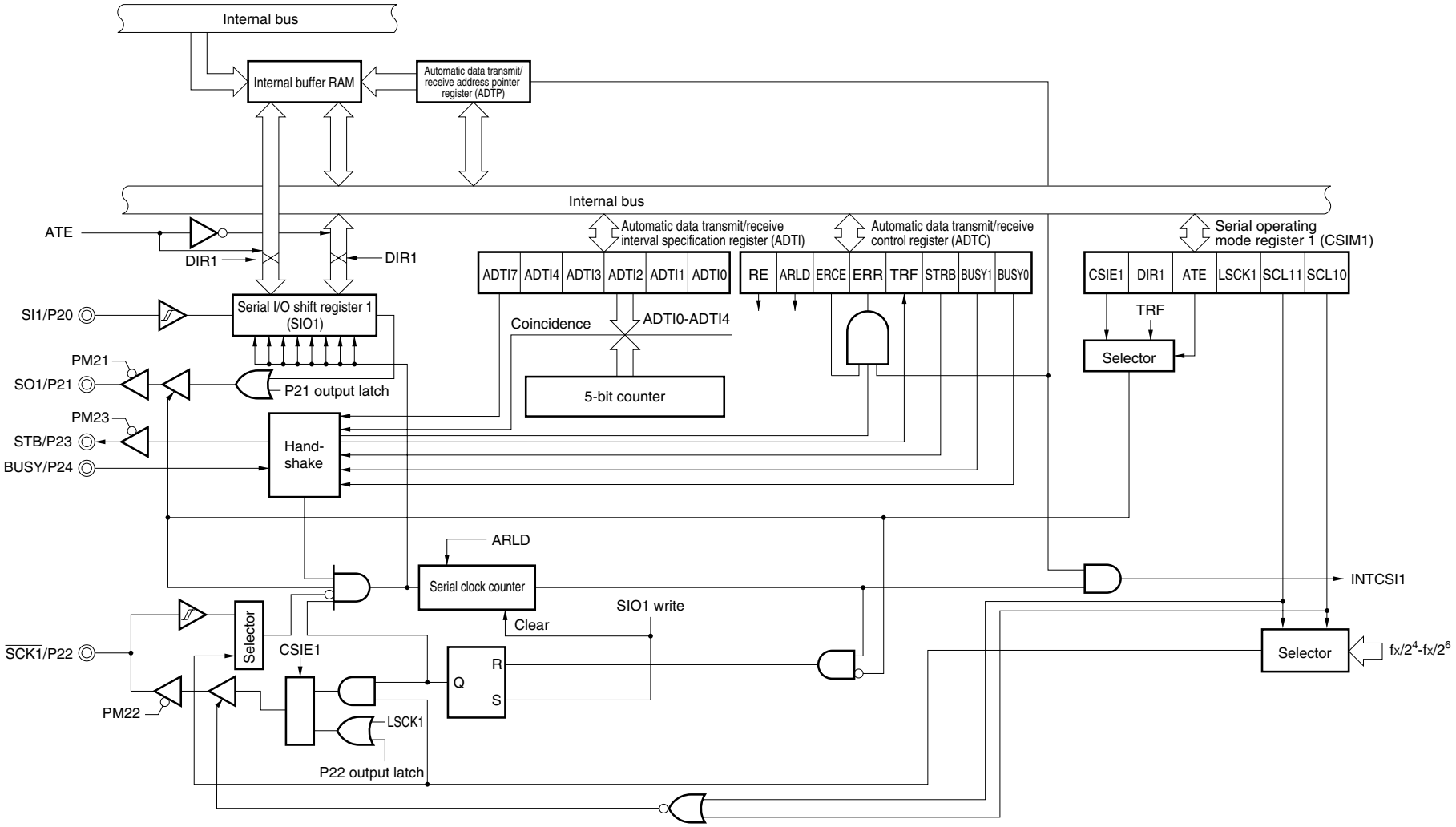
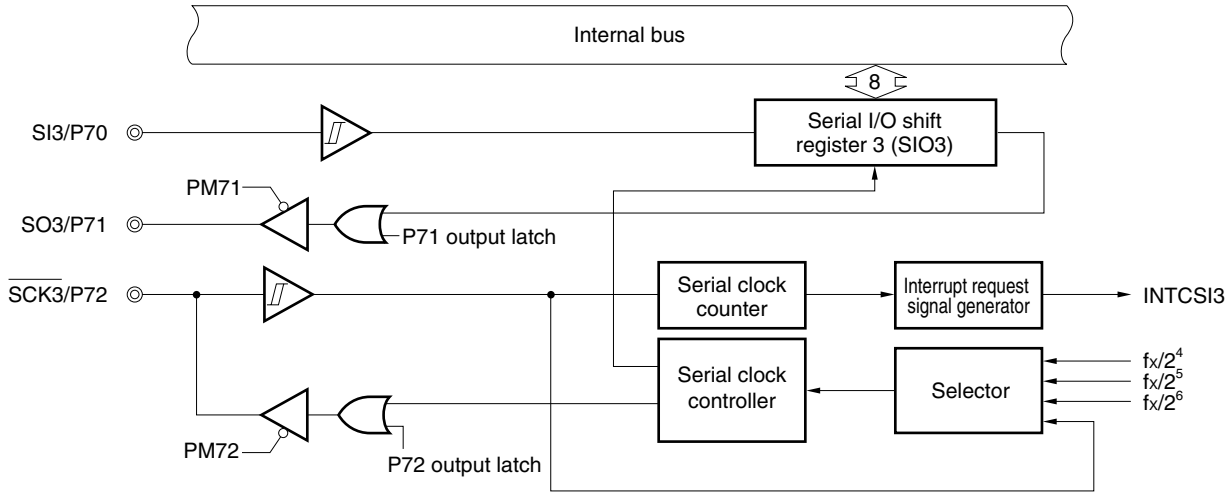


Figure 3-12. Block Diagram of Serial Interface 3



3.7 IEBus Controller

The μPD178096A and 178098A have an IEBus controller. The functions of this IEBus controller are limited as compared with the existing IEBus interface functions of the μPD78098 Subseries.

Table 3-3 compares the interfaces of the μPD78098 Subseries and μPD178098A Subseries.

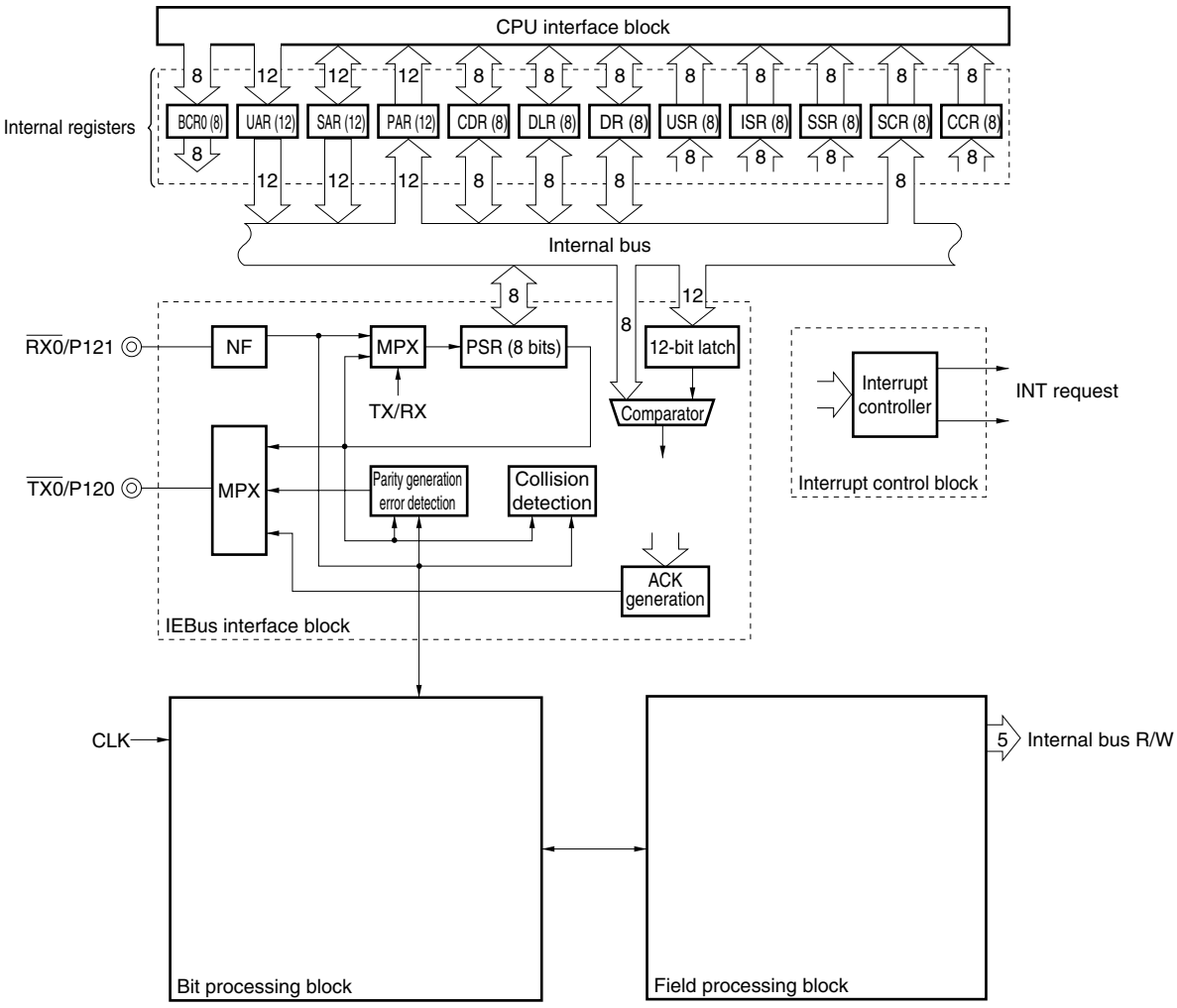
Table 3-3. Comparison of IEBus Interface (Between μPD78098 Subseries and μPD178098A Subseries)

Item	μPD78098 Subseries IEBus	μPD178098A Subseries IEBus
Communication mode	Modes 0, 1, and 2	Fixed to mode 1
Internal system clock	f_X = 6.0 (6.29) MHz	f_X = 6.3 MHz[Note]
Internal buffer size	Transmit buffer: 33 bytes (FIFO) Receive buffer: 40 bytes (FIFO) Up to 4 frames can be received.	Transmit buffer: 1 byte Receive buffer: 1 byte
CPU processing	Communication start processing (data setting) Setting and management of each communication status Writing data to transmit buffer Reading data from receive buffer	Communication start processing (data setting) Setting and management of each communication status Writing data per 1 byte Reading data per 1 byte Management of transmission such as slave status Management of multiple frames, re-master request processing
Hardware processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic answering of ACK/NACK Automatic data re-transmission processing Automatic re-master processing Transmission processing such as automatic slave status Multiple frame reception processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic answering of ACK/NACK Automatic data re-transmission processing

Note The IEBus controller of the μPD178098A Subseries operates at f_X = 6.3 MHz, and not at f_X = 4.5 MHz.

Remark f_X: System clock frequency

Figure 3-13. Block Diagram of IEBus Controller



The IEBus mainly consists of the following six internal blocks:

- CPU interface block
- Interrupt control block
- Internal registers
- Bit processing block
- Field processing block
- IEBus interface block

<CPU interface block>
This block interfaces between the CPU (78K/0) and IEBus.

<Interrupt control block>
This block passes interrupt request signals from the IEBus to the CPU.

<Internal registers>
These are control registers that are used to control the IEBus and settings of each field.

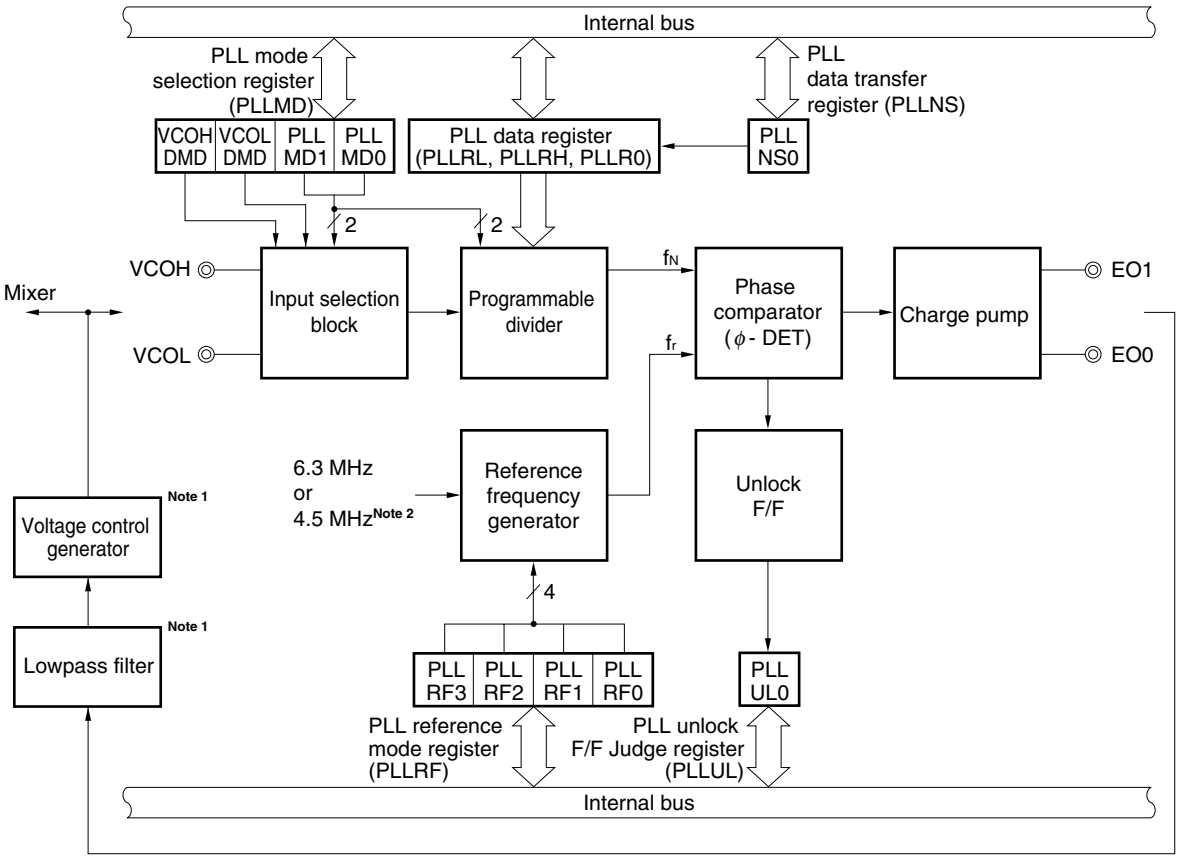
<Bit processing block>
This block generates and disassembles bit timing, and mainly consists of a bit sequence ROM, 8-bit preset timer, and decision unit.

<Field processing block>
This block generates each field in a communication frame and mainly consists of a field sequence ROM, 4-bit down counter, and decision unit.

<IEBus interface block>
This is the interface block for an external driver/receiver, and mainly consists of a noise filter, shift register, collision detector, parity detector, parity generator, and ACK/NACK generator.

3.8 PLL Frequency Synthesizer

Figure 3-14. Block Diagram of PLL Frequency Synthesizer

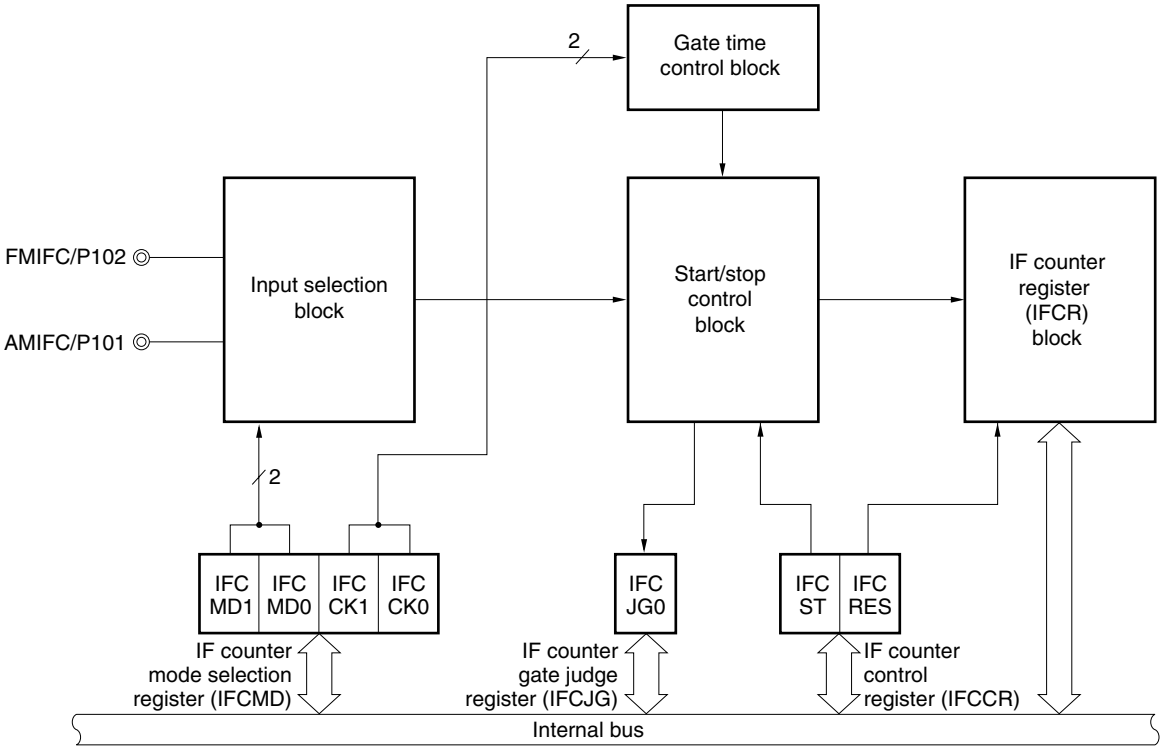


Notes 1. These are external circuits.

2. When the IEBus controller is used, the 4.5 MHz crystal resonator cannot be used. Be sure to use the 6.3 MHz crystal resonator.

3.9 Frequency Counter

Figure 3-15. Block Diagram of Frequency Counter



4. INTERRUPT FUNCTION

A total of 21 interrupt sources are provided, divided into the following three types.

- Non-maskable: 1[Note]
- Maskable: 20[Note]
- Software: 1

Note Two types of watchdog interrupt sources (INTWDT), non-maskable and maskable, are available, and either of them can be selected.

Table 4-1. Interrupt Sources (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTCSI0	End of transfer by serial interface 0	Internal	0016H	(B)
	10	INTCSI1	End of transfer by serial interface 1		0018H	
	11	INTCSI3	End of transfer by serial interface 3		001AH	
	12	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		001CH	
	13	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		001EH	
	14	–	–	–	**Note 3**	–
	15	–	–		**Note 3**	
	16	–	–		**Note 3**	
	17	INTBTM0	Generation of coincidence signal of basic timer	Internal	0026H	(B)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 22 is the lowest order.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 4-1.

3. There are no interrupt sources corresponding to vector addresses 0020H, 0022H, and 0024H.

Table 4-1. Interrupt Sources (2/2)

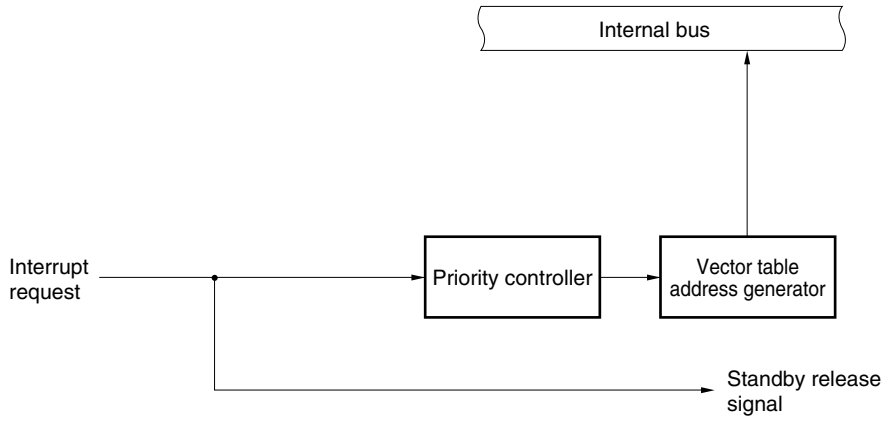
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	18	INTTM00	Generation of signal indicating coincidence between 16-bit timer counter 0 (TM0) and capture/compare register 00 (CR00) (when CR00 is used as compare register)	Internal	0028H	(B)
			Detection of input edge of TI00/P32 pin (when CR00 is used as capture register)	External		(D)
	19	INTTM01	Generation of signal indicating coincidence between 16-bit timer counter 0 (TM0) and capture/compare register 01 (CR01) (when CR01 is used as compare register)	Internal	002AH	(B)
			Detection of input edge of TI01/P33 pin (when CR01 is used as capture register)	External		(D)
	20	INTIE1	IEBus0 data access request	Internal	002CH	(B)
	21	INTIE2	IEBus0 communication error and start/end of communication		002EH	
	22	INTAD	End of conversion by A/D converter AD1		0030H	(B)
Software	–	BRK	Execution of BRK instruction	–	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 22 is the lowest order.

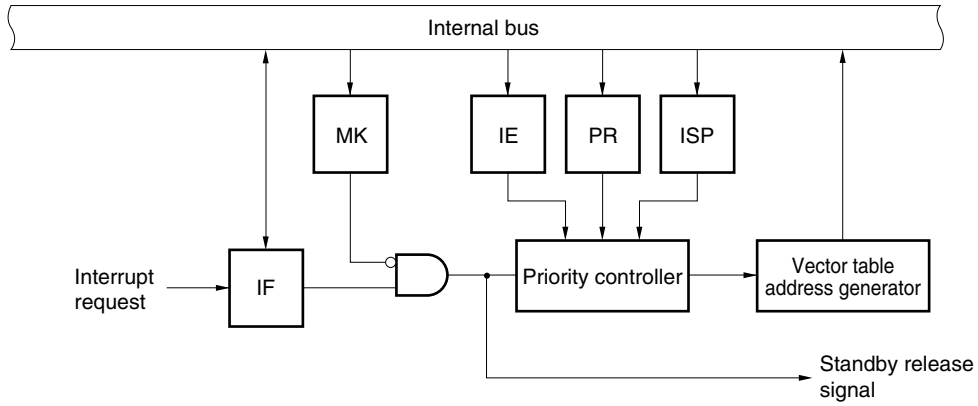
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 4-1.

Figure 4-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP7)

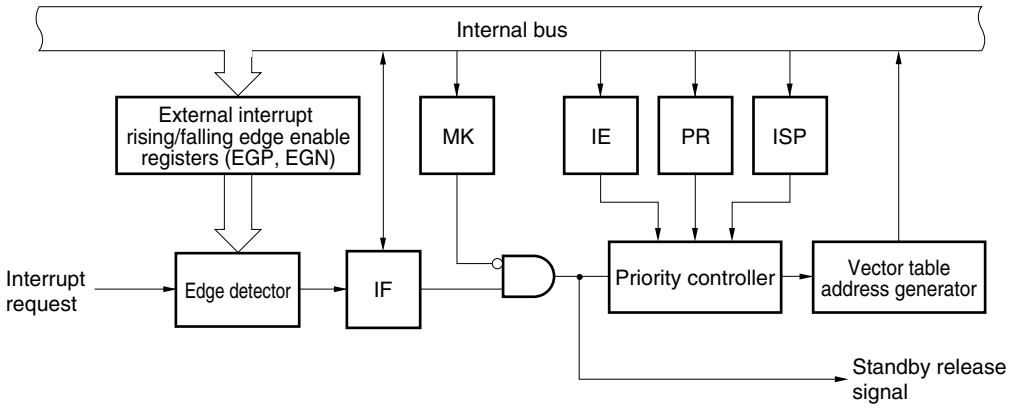
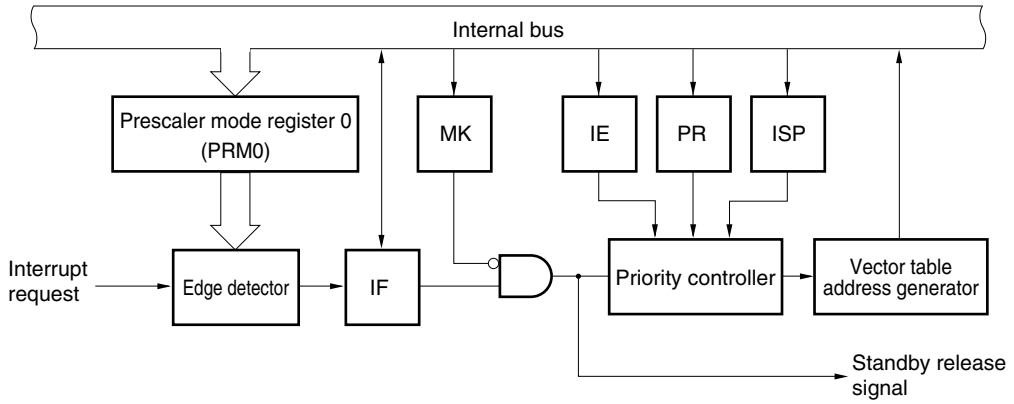
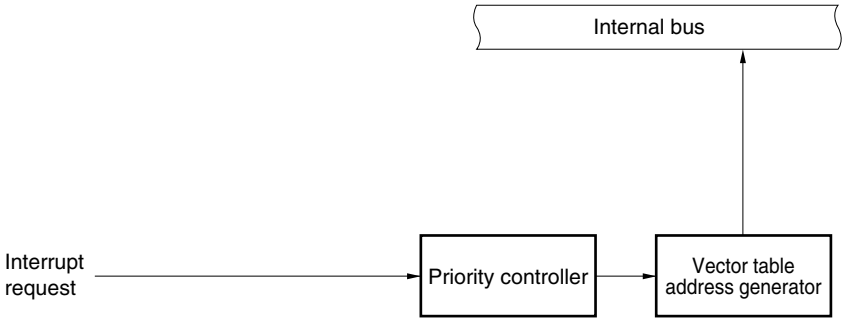


Figure 4-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupts (INTTM00, INTTM01)



(E) Software interrupt



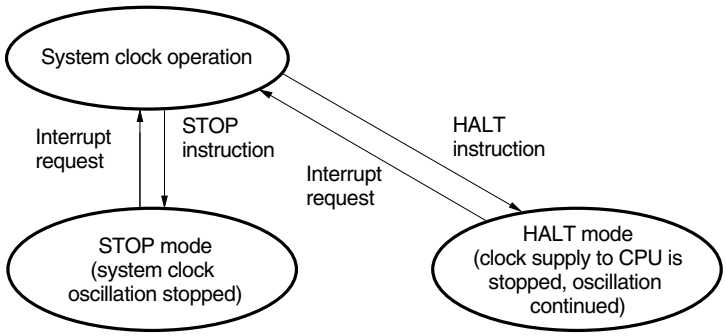
Remark IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

5. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode: The CPU operating clock is stopped.
  The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode: The system clock oscillation is stopped. All operations by the system clock are stopped and current consumption can be considerably reduced.

Figure 5-1. Standby Function



6. RESET FUNCTION

There are the following three reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer inadvertent program loop time detection
- Internal reset by Power-ON Clear (POC).

7. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +6.0	V
	V_{DD}PORT				–0.3 to V_{DD} + 0.3 Note 1	V
	AV_{DD}				–0.3 to V_{DD} + 0.3 Note 1	V
	V_{DD}PLL				–0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_I				–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Excluding P130 to P137			–0.3 to V_{DD} + 0.3	V
Output breakdown voltage	V_{BDS}	P130 to P137	N-ch open drain		16	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	1 pin			–8	mA
		Total for P00, P01, P20 to P27, P50 to P57, and P70 to P73			–15	mA
		Total for P02 to P07, P30 to P37, P40 to P47, P60 to P67, P74 to P77, and P120 to P124			–15	mA
		Total for P100 to P102			–10	mA
Output current, low	I_{OL} Note 2	1 pin		Peak value	16	mA
				rms	8	mA
		Total for P00, P01, P20 to P27, P50 to P57, and P70 to P73		Peak value	30	mA
				rms	15	mA
		Total for P02 to P07, P30 to P37, P40 to P47, P60 to P67, P74 to P77, P120 to P124, and P130 to P137		Peak value	30	mA
				rms	15	mA
		Total for P100 to P102		Peak value	20	mA
				rms	10	mA
Operating temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–55 to +125	°C

Notes 1. Keep the voltage at V_{DD}PORT, AV_{DD}, and V_{DD}PLL same as that at the V_{DD} pin.

2. The rms value should be calculated as follows: [rms] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate function pins are the same as those of port pins.

Recommended Supply Voltage Ranges (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	When CPU is operating and PLL is stopped	3.5	5.0	5.5	V
Data retention voltage	V_{DDR}	When crystal oscillation stops	2.3		5.5	V
Output breakdown voltage	V_{BDS}	P130 to P137 (N-ch open drain)			15	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30, P31, P36, P37, P40 to P47, P50 to P57, P60 to P67, P71, P73, P75 to P77, P100 to P102, P120, P122 to P124		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P07, P20, P22, P24 to P27, P32 to P35, P70, P72, P74, P121, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30, P31, P36, P37, P40 to P47, P50 to P57, P60 to P67, P71, P73, P75 to P77, P100 to P102, P120, P122 to P124		0		0.3V_{DD}	V
	V_{IL2}	P00 to P07, P20, P22, P24 to P27, P32 to P35, P70, P72, P74, P121, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
Output voltage, high	V_{OH1}	P00 to P07, P20 to P24, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P100 to P102, P120 to P124	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OH} = –3 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P100 to P102, P120 to P124, P130 to P137	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1 mA			1.0	V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OL} = 100 μA			0.5	V
	V_{OL2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA			1.0	V
Input leakage current, high	I_{LIH}	P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P100 to P102, P120 to P124, $\overline{\text{RESET}}$	V_I = V_{DD}			3	μA

Remark Unless specified otherwise, the characteristics of alternate function pins are the same as those of port pins.

DC Characteristics (T_A = −40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, low	I_{LIL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P100 to P102, P120 to P124, $\overline{\text{RESET}}$	V_I = 0 V			–3	μA
Output off leakage current	I_{LOH1}	P130 to P137	V_O = 15 V			–3	μA
	I_{LOL1}	P130 to P137	V_O = 0 V			3	μA
	I_{LOH2}	P25 to P27 (at N-ch open drain I/O)	V_O = V_{DD}			–3	μA
	I_{LOL2}	P25 to P27 (at N-ch open drain I/O)	V_O = 0 V			3	μA
	I_{LOH3}	EO0, EO1	V_O = V_{DD}			–3	μA
	I_{LOL3}	EO0, EO1	V_O = 0 V			3	μA
Supply current[Note]	I_{DD1}	When CPU is operating and PLL is stopped. Sine wave input to X1 pin V_I = V_{DD} fx = 6.3 MHz			4.0	20	mA
	I_{DD2}	In HALT mode with PLL stopped. Sine wave input to X1 pin V_I = V_{DD} fx = 6.3 MHz			0.3	1.0	mA
Data retention voltage	V_{DDR1}	When crystal resonator is oscillating		3.5		5.5	V
	V_{DDR2}	When crystal oscillation is stopped	Power-failure detection function	2.2			V
	V_{DDR3}		Data memory retained	2.0			V
Data retention current	I_{DDR1}	When crystal oscillation is stopped	T_A = 25°C, V_{DD} = 5 V		2.0	4.0	μA
	I_{DDR2}				2.0	20	μA

Note Excluding AV_{DD} current and V_{DD}PLL current.

Remarks 1. fx: System clock oscillation frequency

2. Unless specified otherwise, the characteristics of alternate function pins are the same as those of port pins.

Reference Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD5}	When CPU and PLL are operating. Sine wave input to VCOH pin At f_{IN} = 160 MHz, V_{IN} = 0.15V_{P-P}		5		mA

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	At f_X = 6.3 MHz	0.32		5.08	μs
		At f_X = 4.5 MHz[Note 1]	0.44		7.11	μs
TI00, TI01 input high-/low-level widths	t_{TIH0}, t_{TIL0}		4/fsam[Note 2]			s
TI50, TI51 input frequency	f_{TI5}				2	MHz
TI50, TI51 input high-/low-level widths	t_{TIH5}, t_{TIL5}		200			ns
Interrupt input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0 to INTP7	1			μs
$\overline{\text{RESET}}$ pin low-level width	t_{RSL}		10			μs

Notes 1. When the IEBus controller is used, the 4.5 MHz crystal resonator cannot be used. Be sure to use the 6.3 MHz crystal resonator.

2. f_{sam} = f_X/2, f_X/4, f_X/64 selectable by bits 0 and 1 (PRM00 and PRM01) of prescaler mode register 0 (PRM0). However, f_{sam} = f_X/8 when the valid edge of TI00 is selected as the count clock.

(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2 - 50$			ns
			$t_{KCY1}/2 - 100$			ns
SI0 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK0}\downarrow$ to SO0 output	t_{KSO1}	C = 100 pF Note			300	ns

Note C is the load capacitance of the $\overline{SCK0}$ and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI0 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK0}\downarrow$ to SO0 output	t_{KSO2}	C = 100 pF Note			300	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO3}	R = 1 kΩ C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output lines.

(iv) SBI mode ($\overline{SCK0}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 5.5 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
Delay time from $\overline{SCK0}$↓ to SB0, SB1 output	t_{KSO4}	R = 1 kΩ C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}	C = 100 pF Note		$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI5}			600			ns
Delay time from $\overline{SCK0}\downarrow$ to SB0, SB1 output	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI6}			$t_{KCY6}/2$			ns
Delay time from $\overline{SCK0}\downarrow$ to SB0, SB1 output	t_{KSO6}	R = 1 kΩ	V_{DD} = 4.5 to 5.5 V	0		300	ns
		C = 100 pF Note		0		500	ns
$\overline{SCK0}$ rise/fall time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(vii) I²C Bus mode (SCL ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 kΩ		10			μs
SCL high-level width	t_{KH7}	C = 100 pF Note		t_{KCY7} – 160			ns
SCL low-level width	t_{KL7}			t_{KCY7} – 50			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO7}		V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0 and SDA1 output lines.

(viii) I²C Bus mode (SCL ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
Delay time from SCL↓ to SDA0, SDA1 output	t_{KSO8}	R = 1 kΩ	V_{DD} = 4.5 to 5.5 V	0		300	ns
		C = 100 pF Note		0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL rise/fall time	t_{R8}, t_{F8}					1000	ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) Serial interface 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}		$t_{KCY9}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO9}	C = 100 pF Note			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO10}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}				1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY11}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH11}, t_{KL11}		$t_{KCY11}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK11}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI11}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO11}	C = 100 pF Note			300	ns
STB$\uparrow$ from $\overline{SCK1}\uparrow$	t_{SBD}		$t_{KCY11}/2 - 100$		$t_{KCY11}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY11}/2 - 30$		$t_{KCY11}/2 + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}		100			ns
$\overline{SCK1}\downarrow$ from busy inactive	t_{SPS}		200			ns

Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH12}, t_{KL12}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK12}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI12}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO12}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise/fall time	t_{R12}, t_{F12}				1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial interface 3

(i) 3-wire serial I/O mode ($\overline{SCK3}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY13}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH13}, t_{KL13}		$t_{KCY13}/2 - 50$			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK13}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI13}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO13}	C = 100 pF Note			300	ns

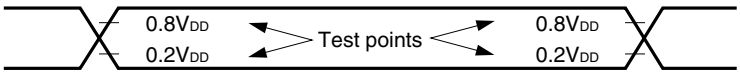
Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK3}$ ... External clock input)

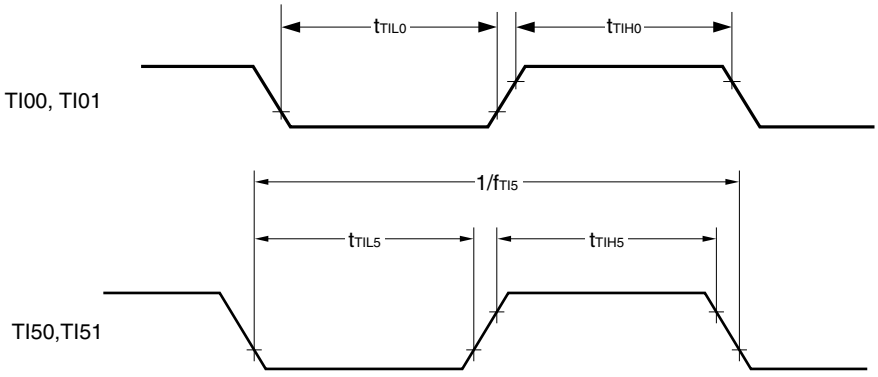
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY14}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH14}, t_{KL14}		400			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK14}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI14}		400			ns
Delay time from $\overline{SCK3}\downarrow$ to SO3 output	t_{KSO14}	C = 100 pF Note			300	ns
$\overline{SCK3}$ rise/fall time	t_{R14}, t_{F14}				1000	ns

Note C is the load capacitance of the SO3 output line.

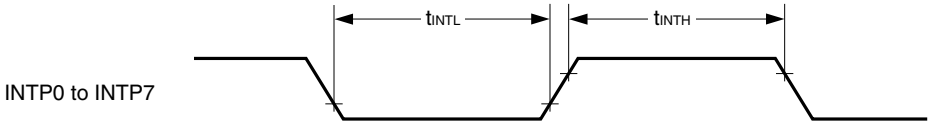
AC Timing Test Points (excluding X1 input)



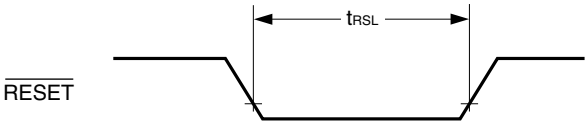
TI Timing



Interrupt Input Timing

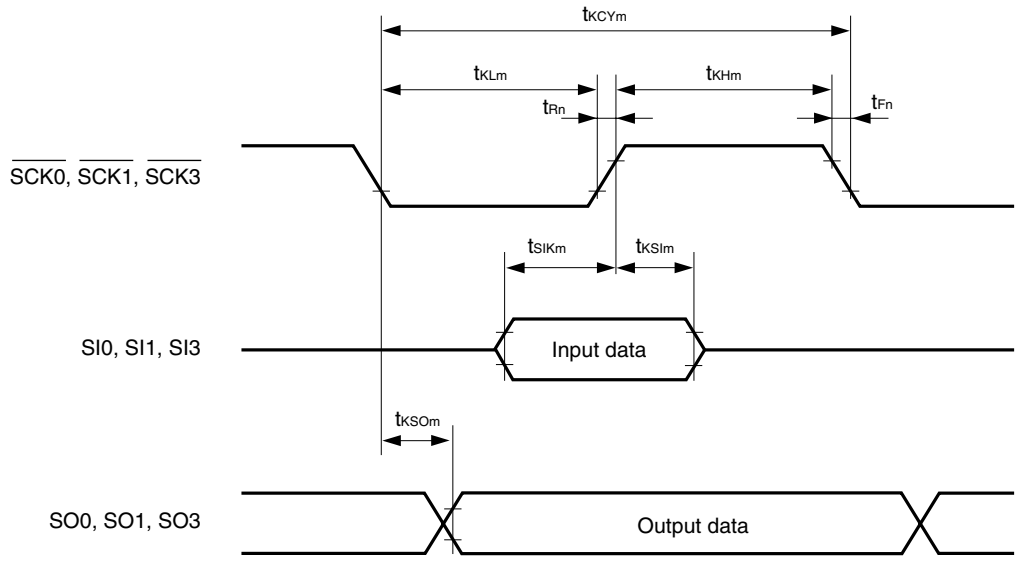


$\overline{\text{RESET}}$ Input Timing



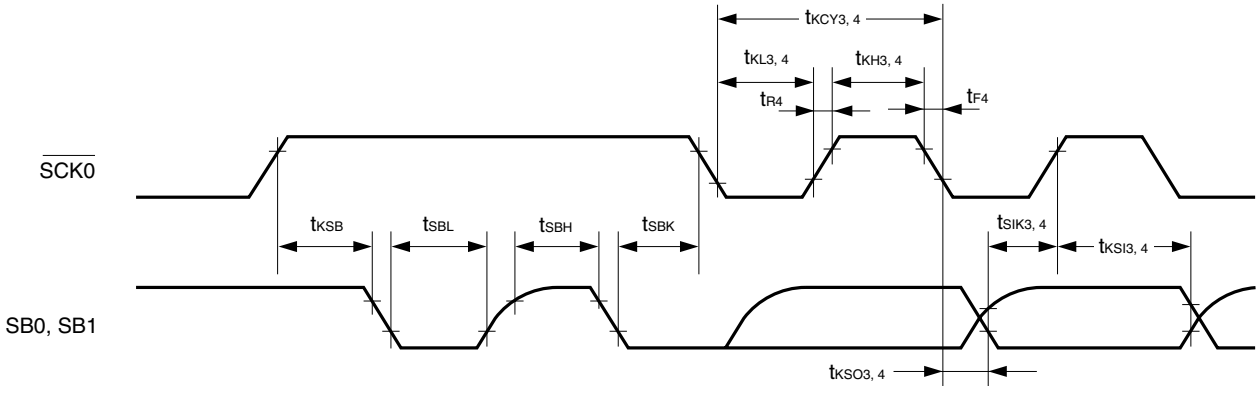
Serial Transfer Timing

3-wire serial I/O mode:

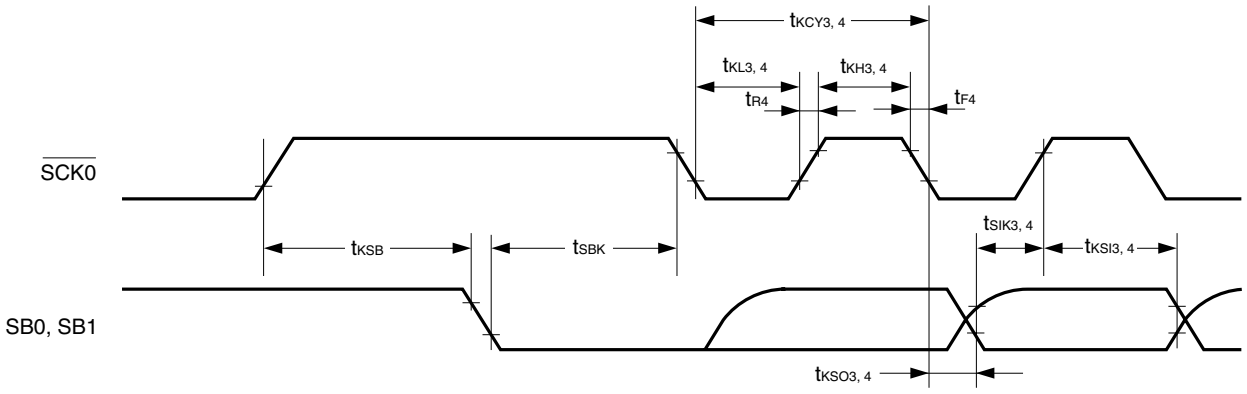


Remark m = 1, 2, 9, 10, 13, 14
n = 2, 10, 14

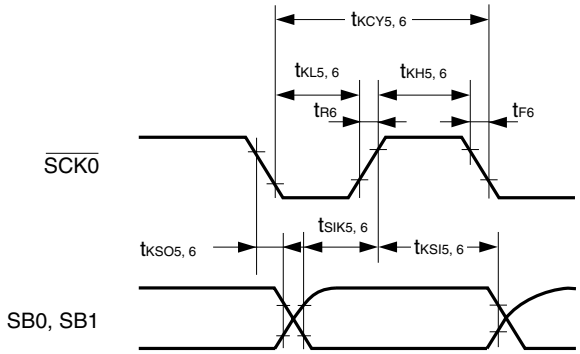
SBI mode (bus release signal transfer):



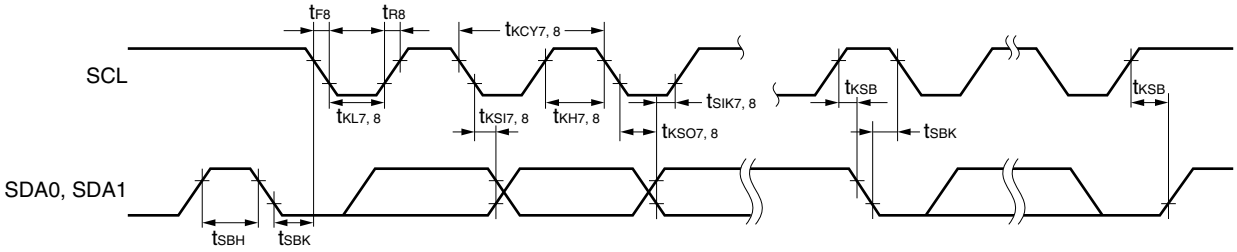
SBI mode (command signal transfer):



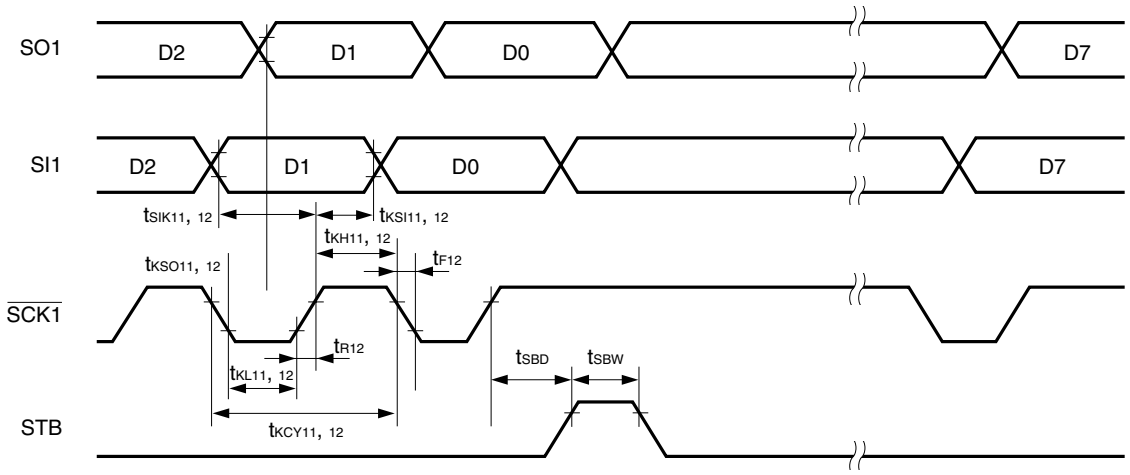
2-wire serial I/O mode:



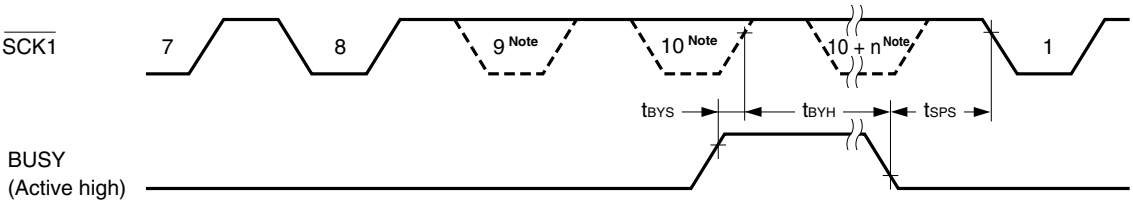
I²C bus mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_S	Fixed to mode 1		6.3 Note		MHz

Note Although the system clock frequency is 6.0 MHz in the IEBus standard, in these products, normal operation is guaranteed at 6.3 MHz.

Remark 6.0 MHz and 6.3 MHz cannot both be used as the IEBus system clock frequency.

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall conversion error[Notes 1, 2]		V_{DD} = 4.5 to 5.5 V			±1.0	%FSR
					±1.4	%FSR
Conversion time	t_{CONV}		15.2		45.7	μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. It is indicated as a ratio to the full-scale value.

PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin, MF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.5		3.0	MHz
	f_{IN2}	VCOL pin, HF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		40	MHz
	f_{IN3}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	60		130	MHz
	f_{IN4}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.3 V_{P-P}	40		160	MHz

Remark The above values are the result of NEC's evaluation of the device. If the device is likely to be affected by noise in your application, it is recommended to use the device at a voltage higher than the above values.

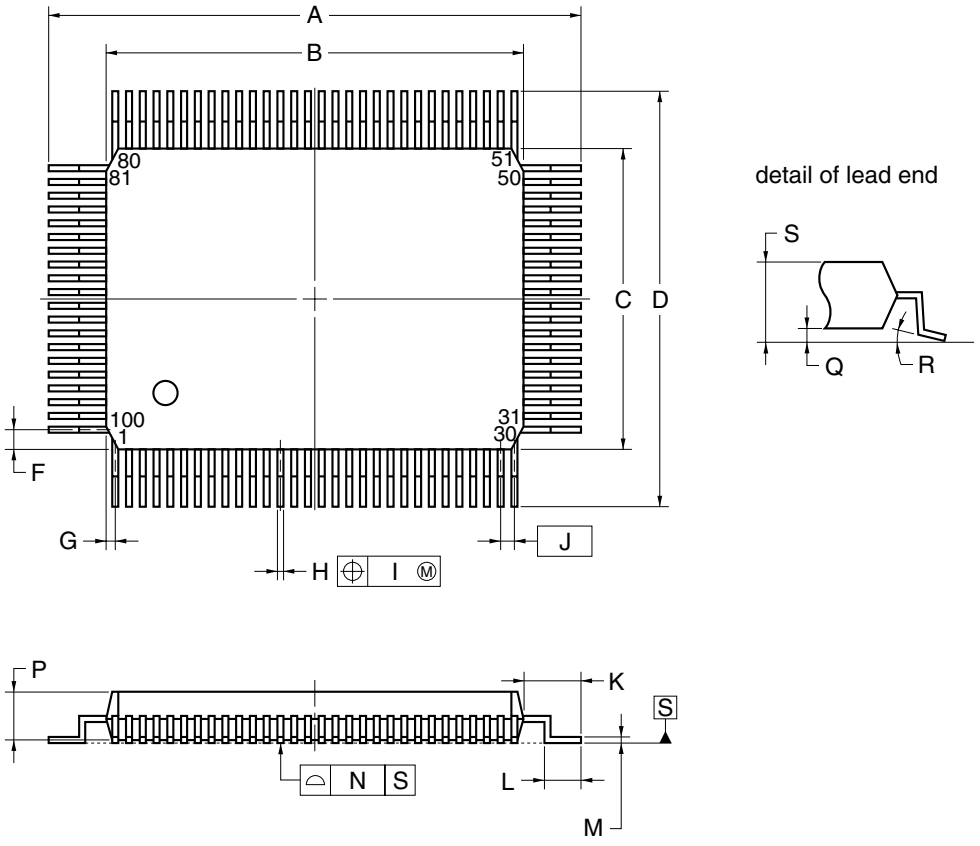
IFC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN5}	AMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz
	f_{IN6}	FMIFC pin, FMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		11	MHz
	f_{IN7}	FMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz

Remark The above values are the result of NEC's evaluation of the device. If the device is likely to be affected by noise in your application, it is recommended to use the device at a voltage higher than the above values.

9. PACKAGE DRAWING

100-PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

10. RECOMMENDED SOLDERING CONDITIONS

The μPD178096A and 178098A should be soldered and mounted under the following recommended conditions. For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.
For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions

μPD178096AGF-×××-3BA: 100-pin plastic QFP (14 × 20)

μPD178098AGF-×××-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec max. (at 210°C or higher), Count: 3 times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec max. (at 200°C or higher), Count: 3 times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec max., Count: 1, Preheating temperature: 120°C max., (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD178098A Subseries.

Language processor software

RA78K0[Notes 1, 2, 3]	Assembler package common to 78K/0 Series
CC78K0[Notes 1, 2, 3]	C compiler package common to 78K/0 Series
DF178098[Notes 1, 2, 3]	Device file for μPD178098A Subseries
CC78K0-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0 Series

Flash memory writing tools

Flashpro III (Part number: FL-PR3[Note 4], PG-FL3)	Dedicated flash programmer
FA-100GF-3BA[Note 4]	Flash programmer adapter

Debugging tools

- **When in-circuit emulator IE-78K0-NS is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board for enhancing and expanding the IE-78K0-NS function
IE-70000-98-IF-C	Interface adapter necessary when PC-9800 series (except notebook PC) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when a notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when IBM PC/AT™ compatible machine is used as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-178098-NS-EM1	Emulation board to emulate μPD178098A Subseries
NP-100GF[Note 4]	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K0[Notes 1, 2]	System simulator common to 78K/0 Series
ID78K0-NS[Notes 1, 2]	Integrated debugger common to 78K/0 Series
DF178098[Notes 1, 2, 3]	Device file for μPD178098A Subseries

Notes 1. PC-9800 series (Japanese Windows™) based
2. IBM PC/AT compatible machine (Japanese/English Windows) based
3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based
4. Products of Naito Densei Machida Mfg. Co., Ltd. (Tel: +81-44-822-3813).

Remark Use the RA78K0, CC78K0, and SM78K0 in combination with the DF178098.

• **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter necessary when PC-9800 series (except notebook PC) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter necessary when IBM PC/AT compatible machine is used as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when EWS is used as host machine
IE-178098-NS-EM1	Emulation board to emulate μPD178098A Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-178098-NS-EM1 on IE-78001-R-A
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K0 Notes 1, 2	System simulator common to 78K/0 Series
ID78K0 Notes 1, 2	Integrated debugger common to 78K/0 Series
DF178098 Notes 1, 2, 3	Device file for μPD178098A Subseries

Real-time OS

RX78K0 Notes 1, 2, 3	Real-time OS for 78K/0 series
MX78K0 Notes 1, 2, 3	OS for 78K/0 series

Notes 1. PC-9800 series (Japanese Windows) based
2. IBM PC/AT compatible machine (Japanese/English Windows) based
3. HP9000 series 700 (HP-UX) based, SPARCstation (SunOS, Solaris) based, NEWS (NEWS-OS) based

Remark Use the SM78K0 in combination with the DF178098.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Device

Document Name		Document No.
μPD178096A, 178098A Data Sheet		This document
μPD178F098 Data Sheet		U12920E
μPD178078, 178098 Subseries User's Manual		U12790E
78K/0 Series User's Manual - Instructions		U12326E
78K/0 Series Application Note	Basics (I)	U12704E

Documents Related to Development Tools (User's Manual)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
IE-78001-R-A		To be prepared
IE-78K0-NS		U13731E
IE-178098-NS-EM1		U14013E
EP-78064		EEU-1469
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.
78K/0 Series Real-time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Guides on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
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- Network requirements

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Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Tel: 01908-691-133
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Tel: 040-2445845
Fax: 040-2444580

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Fax: 01-3067-5899

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Madrid Office
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Tel: 091-504-2787
Fax: 091-504-2860

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Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

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