NEC

MOS INTEGRATED CIRCUIT

μPD178002, 178003

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD178002 and 178003 are 8-bit single-chip CMOS microcontrollers that incorporate hardware for digital tuning systems.

The CPU uses the 78K/0 architecture, which makes it easy to implement high-speed access to internal memory and control of peripheral hardware. Also, the instructions used are the high-speed 78K/0 instructions, suitable for system control.

The peripheral hardware includes an input/output port, 8-bit timer, A/D converter, serial interface, power-on-clear circuits, as well as a pre-scaler for digital tuning, a PLL frequency synthesizer, and a frequency counter.

The μPD178P018A, one-time PROM or EPROM versions that can be operated in the same supply voltage range as for the mask ROM versions, and various development tools, are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD178003 Subseries User's Manual: U13033E
78K/0 Series User's Manual — Instructions: U12326E

FEATURES

- Program memory (ROM) capacity
  μPD178002: 16 Kbytes
  μPD178003: 24 Kbytes
- Data memory (RAM) capacity: 512 bytes
- Instruction cycle: 0.44 μs (4.5 MHz crystal resonator used)
- Selected peripheral hardware of the μPD178018A Subseries
  General-purpose I/O ports, A/D converter, serial interface, timer, frequency counter, power-on-clear circuits.
- On-chip hardware for a PLL frequency synthesizer.
  Dual modulus pre-scaler, programmable divider, phase comparator, charge pump.
- Vector interrupt sources: 8
- Supply Voltage: V_{DD} = 4.5 to 5.5 V (during PLL operation)
  V_{DD} = 3.5 to 5.5 V (during CPU operation, when the system clock is f_X/2 or lower)
  V_{DD} = 4.5 to 5.5 V (during CPU operation, when the system clock is f_X)

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The mark ★ shows major revised points.

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APPLICATIONS

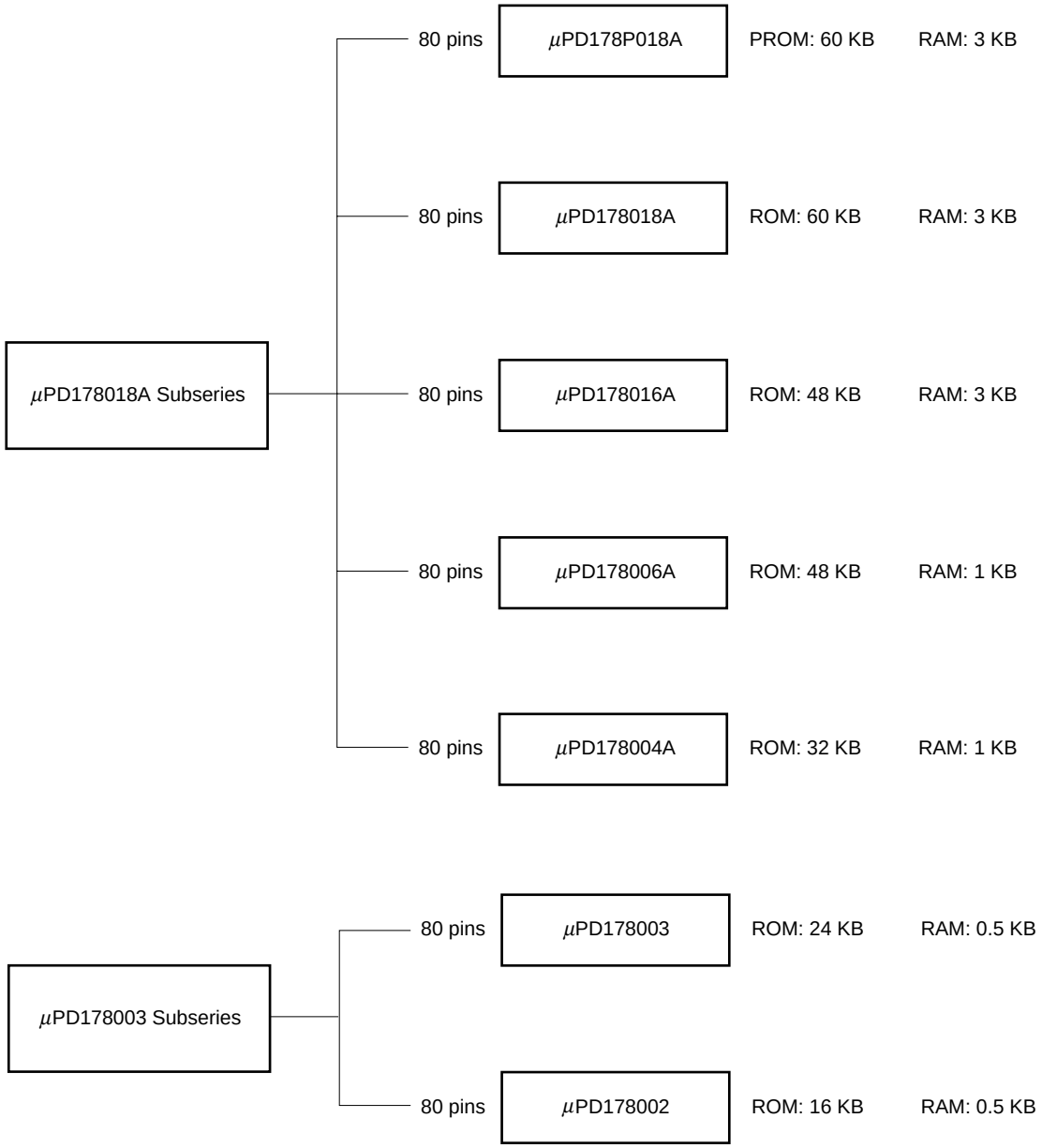
Car stereo, home stereo systems.

ORDERING INFORMATION

Part Number	Package
μPD178002GC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)
μPD178003GC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)

Remark ××× indicates ROM code suffix.

μPD178003 AND μPD178018A SUBSERIES LINEUP



OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD178002	μPD178003
Internal memory	ROM (ROM configuration)	16 Kbytes (mask ROM)	24 Kbytes (mask ROM)
	High-speed RAM	512 bytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (with 4.5 MHz crystal resonator used)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O port		Total: 62 CMOS input: 1 CMOS I/O: 54 N-ch open-drain I/O: 4 N-ch open-drain output: 3	
★ A/D converter		8-bit resolution × 3 channels	
Serial interface		• 3-wire serial I/O mode: 1 channel	
Timer		• Basic timer (timer carry FF (10 Hz)): 1 channel • 8-bit timer/event counter: 2 channels	
Buzzer (BEEP) output		1.5 kHz, 3 kHz, 6 kHz	
Vectored interrupt sources	Maskable	Internal: 5, external: 2	
	Software	1	
Test input		Internal: 1	
PLL frequency synthesizer	Division mode	Two types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOH and VCOL pins)	
	Reference frequency	7 types selectable by program (1, 3, 5, 9, 10, 25, 50 kHz)	
	Charge pump	Error out output: 2	
	Phase comparator	Unlock detectable by program	
Frequency counter		• Frequency measurement • AMIFC pin: for 450 kHz count • FMIFC pin: for 450 kHz/10.7 MHz count	
Standby function		• HALT mode • STOP mode	

Reset		• Reset by $\overline{\text{RESET}}$ pin
		• Reset by power-on clear circuit (3-value detection)
		  • Detection of less than 4.5 V**Note** (CPU clock: f_X)
		  • Detection of less than 3.5 V**Note** (CPU clock: f_X/2 or less and on power application)
		  • Detection of less than 2.5 V**Note** (in STOP mode)	

Supply voltage		• V_{DD} = 4.5 to 5.5 V (with PLL operating) • V_{DD} = 3.5 to 5.5 V (with CPU operating, CPU clock: f_X/2 or less) • V_{DD} = 4.5 to 5.5 V (with CPU operating, CPU clock: f_X)	
Package		• 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)	
One-time PROM		μPD178P018A	

Note These voltage values are maximum values. The reset is actually executed at a voltage lower than these values.

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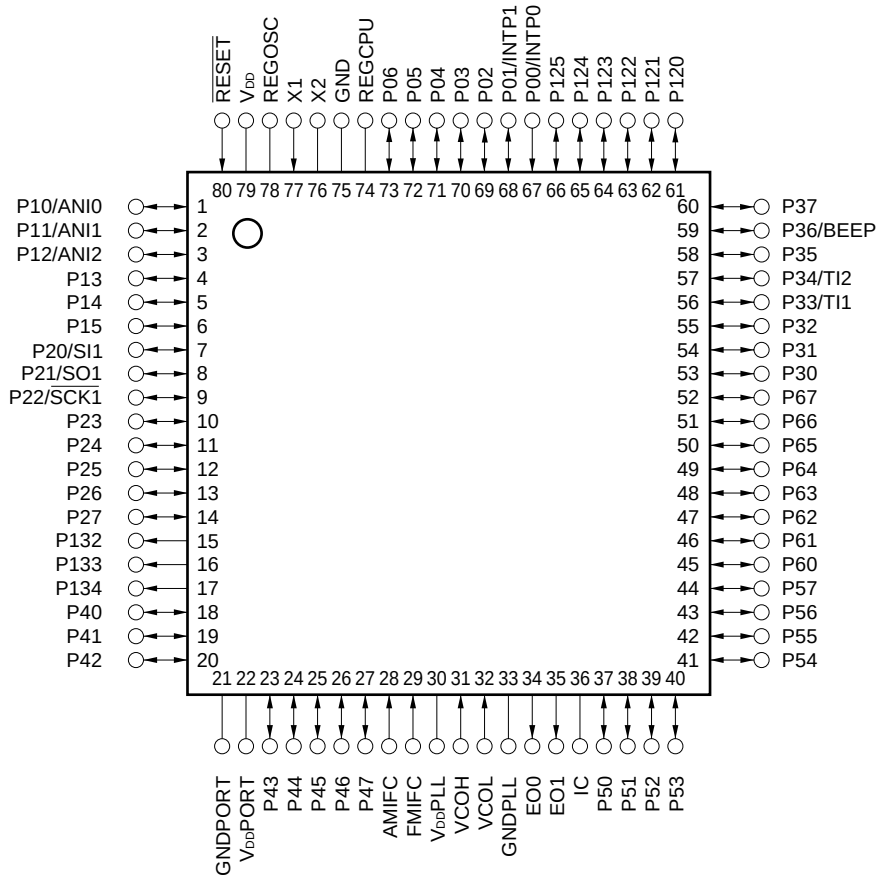
1. PIN CONFIGURATION (TOP VIEW)

- **80-PIN PLASTIC QFP (14 × 14 mm, 0.65 mm pitch)**
  μPD178002GC-×××-3B9
  μPD178003GC-×××-3B9



★ ★ ★

Cautions 1. Connect the IC (Internally Connected) pin directly to GND.

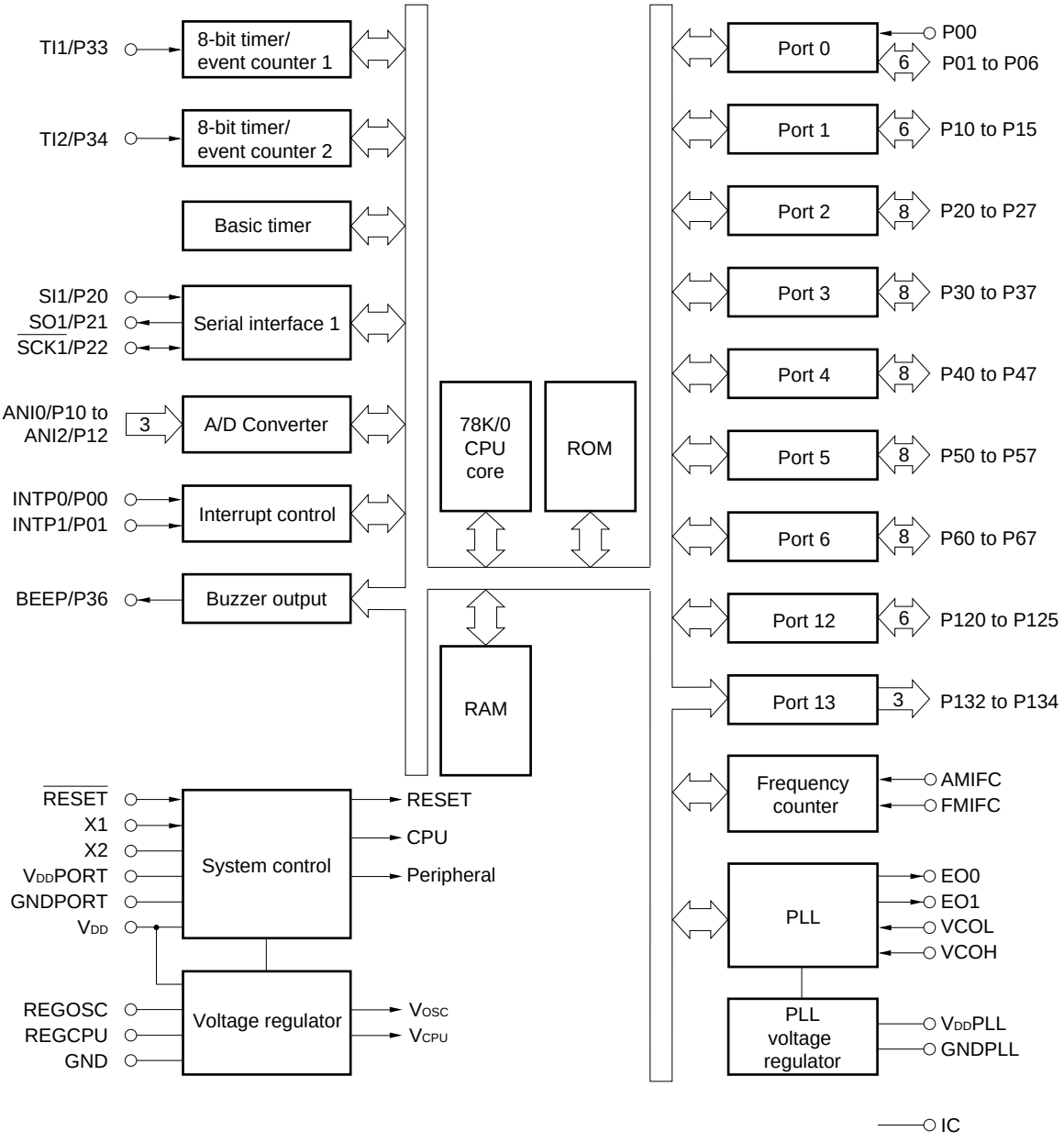
2. Connect V_{DD}PORT and V_{DD}PLL pins to V_{DD}.

3. Connect the GNDPORT and GNDPLL pins to GND.

4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1 μF capacitor.

AMIFC:	AM Intermediate Frequency Counter Input	P60 to P67:	Port 6
★ ANI0 to ANI2:	A/D Converter Input	P120 to P125:	Port 12
BEEP:	Buzzer Output	P132 to P134:	Port 13
EO0, EO1:	Error Out Output	REGCPU :	Regulator for CPU Power Supply
FMIFC:	FM Intermediate Frequency Counter Input	REGOSC :	Regulator for Oscillator
GND:	Ground	$\overline{\text{RESET}}$:	Reset Input
GNDPLL:	PLL Ground	$\overline{\text{SCK1}}$:	Serial Clock Input/Output
GNDPORT:	Port Ground	SI1:	Serial Data Input
IC:	Internally Connected	SO1:	Serial Data Output
INTP0, INTP1:	Interrupt Inputs	TI1, TI2:	Timer Clock Input
P00 to P06:	Port 0	VCOL, VCOH:	Local Oscillator Input
P10 to P15:	Port 1	V_{DD}:	Power Supply
P20 to P27:	Port 2	V_{DD}PLL:	PLL Power Supply
P30 to P37:	Port 3	V_{DD}PORT:	Port Power Supply
P40 to P47:	Port 4	X1, X2:	Crystal Resonator Connection
P50 to P57:	Port 5		

2. BLOCK DIAGRAM



Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 7-bit input/output port	Input only	Input	INTP0
P01	I/O		Input/output mode can be specified in 1-bit units.	Input	INTP1
P02 to P06					—
P10 to P12	I/O	Port 1 6-bit input/output port Input/output mode can be specified in 1-bit units.		Input	ANI0 to ANI2
★ P13 to P15					—
P20	I/O	Port 2 8-bit input/output port Input/output mode can be specified in 1-bit units.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23 to P27					—
P30 to P32	I/O	Port 3 8-bit input/output port Input/output mode can be specified in 1-bit units.		Input	—
P33					TI1
P34					TI2
P35					—
P36					BEEP
P37					—
P40 to P47	I/O	Port 4 8-bit input/output port Input/output mode can be specified in 8-bit units. The test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5 8-bit input/output port Input/output mode can be specified in 1-bit units.		Input	—
P60 to P63	I/O	Port 6 8-bit input/output port Input/output mode can be specified in 1-bit units.	Middle voltage N-ch open-drain input/output port LEDs can be driven directly.	Input	—
P64 to P67					
P120 to P125	I/O	Port 12 6-bit input/output port Input/output mode can be specified in 1-bit units.		Input	—
P132 to P134	Output	Port 13 3-bit output port N-ch open-drain output port.		—	—

3.2 Non-port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0, INTP1	Input	External maskable interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00, P01
SI1	Input	Serial interface serial data input	Input	P20
SO1	Output	Serial interface serial data output	Input	P21
$\overline{SCK1}$	I/O	Serial interface serial clock input/output	Input	P22
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P33
TI2		External count clock input to 8-bit timer (TM2)		P34
BEEP	Output	Buzzer output	Input	P36
ANI0 to ANI5	Input	A/D converter analog input	Input	P10 to P15
EO0, EO1	Output	Error out output from charge pump of the PLL frequency synthesizer	—	—
VCOL	Input	Inputs PLL local band frequency (In HF, MF mode)	—	—
VCOH	Input	Inputs PLL local band frequency (In VHF mode)	—	—
AMIFC	Input	Inputs AM intermediate frequency counter	—	—
FMIFC	Input	Inputs FM intermediate frequency or AM intermediate frequency counter	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for system clock oscillation	—	—
X2	—		—	—
REGOSC	—	Oscillation regulator. Connect to GND via a 0.1 μF capacitor.	—	—
REGCPU	—	CPU power supply regulator. Connect to GND via a 0.1 μF capacitor.	—	—
V_{DD}	—	Positive power supply	—	—
GND	—	Ground	—	—
V_{DD}PORT	—	Positive power supply for port block	—	—
GNDPORT	—	Ground for port block	—	—
V_{DD}PLL[Note]	—	Positive power supply for PLL	—	—
GNDPLL[Note]	—	Ground for PLL	—	—
IC	—	Internally connected. Connect directly to GND or GNDPORT.	—	—

Note Connect a capacitor of about 1000pF between the V_{DD}PLL pin and GNDPLL pin.

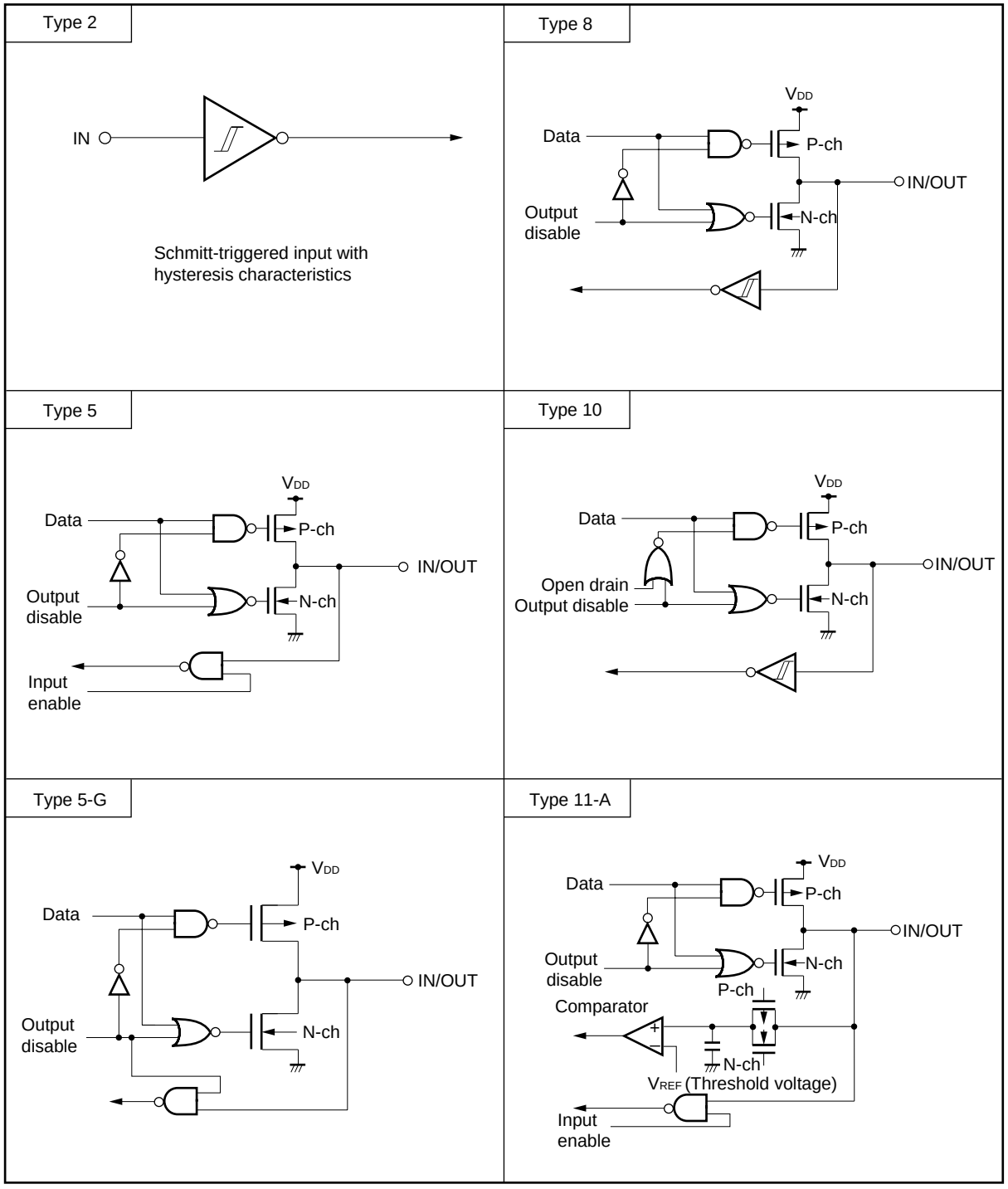
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	2	Input	Connect to GND or GNDPORT.
P01/INTP1, P02 to P06	8	I/O	Set in general-purpose input port mode by software and independently connect to V_{DD}, V_{DD}PORT, GND, or GNDPORT via a resistor.
P10/ANI0 to P12/ANI2	11-A		
★ P13 to P15	5		
P20/SI1	8		
P21/SO1	5		
P22/$\overline{\text{SCK1}}$	8		
P23	5		
P24	8		
P25 to P27	10		
P30 to P32	5		
P33/TI1, P34/TI2	8		
P35 P36/BEEP P37	5		
P40 to P47	5-G		
P50 to P57	5		
★ P60 to P63	13-G		
P64 to P67	5		
P120 to P125			
P132 to P134	19	Output	Set to low-level output by software and leave open.
EO0, EO1	DTS-EO1		Leave open.
VCOL, VCOH	DTS-AMP	Input	Set to pin disabled status by software and leave open.
AMIFC, FMIFC			
IC	—	—	Connect directly to GND or GNDPORT.

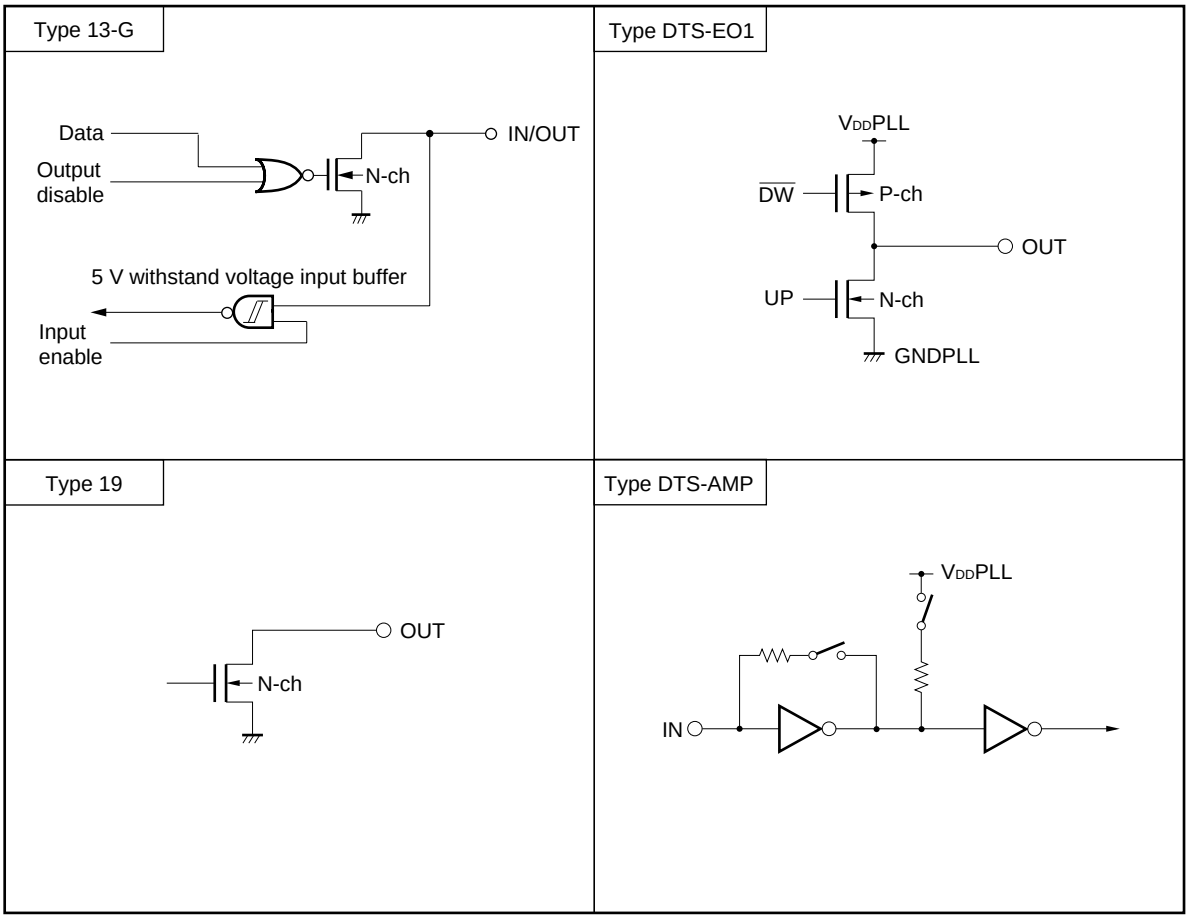
Figure 3-1. Pin Input/Output Circuits (1/2)



Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

Figure 3-1. Pin Input/Output Circuits (2/2)

★

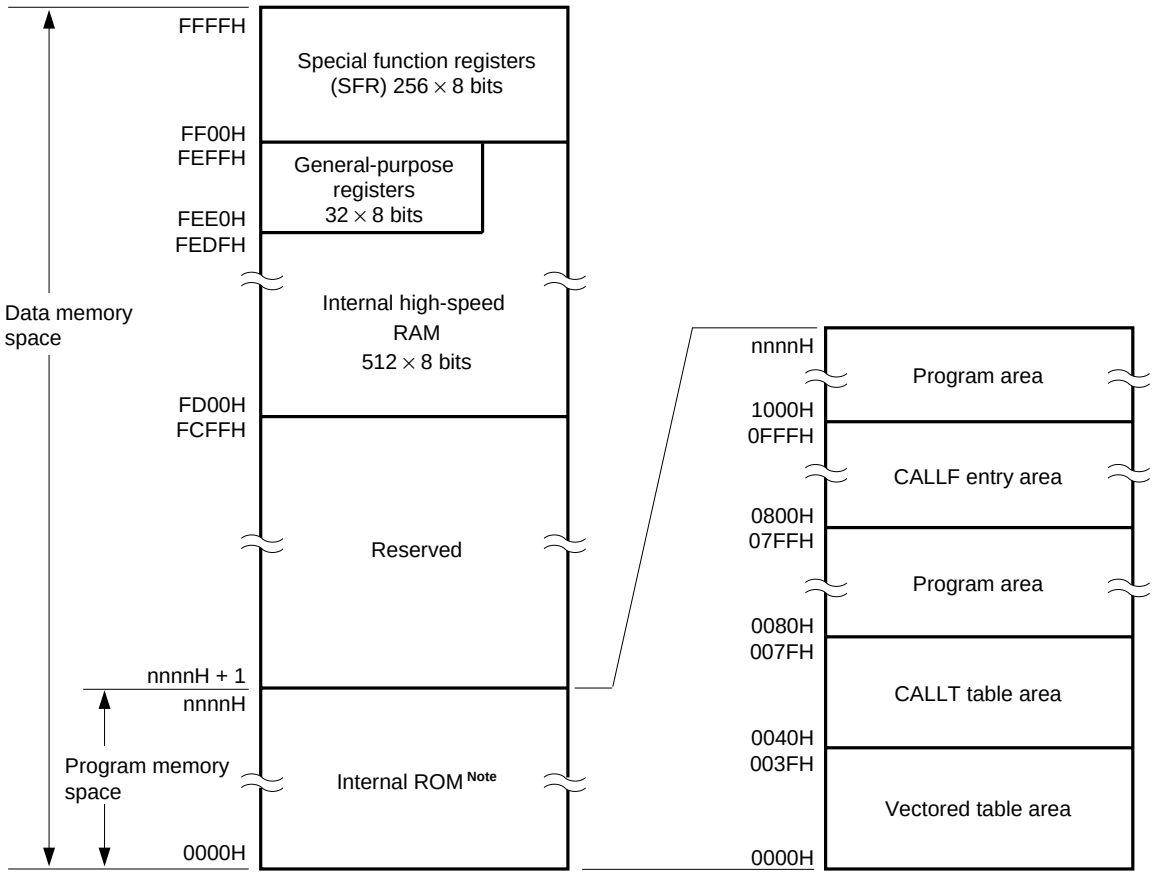


Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

4. MEMORY SPACE

Figure 4-1 shows the μPD178002 and 178003 memory map.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD178002	3FFFH
μPD178003	5FFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following four types of I/O ports are available.

- CMOS input (P00): 1
- CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 12): 54
- N-ch open-drain input/output (P60 to P63): 4
- N-ch open-drain output (Port 13): 3

Total: 62

Table 5-1. Port Functions

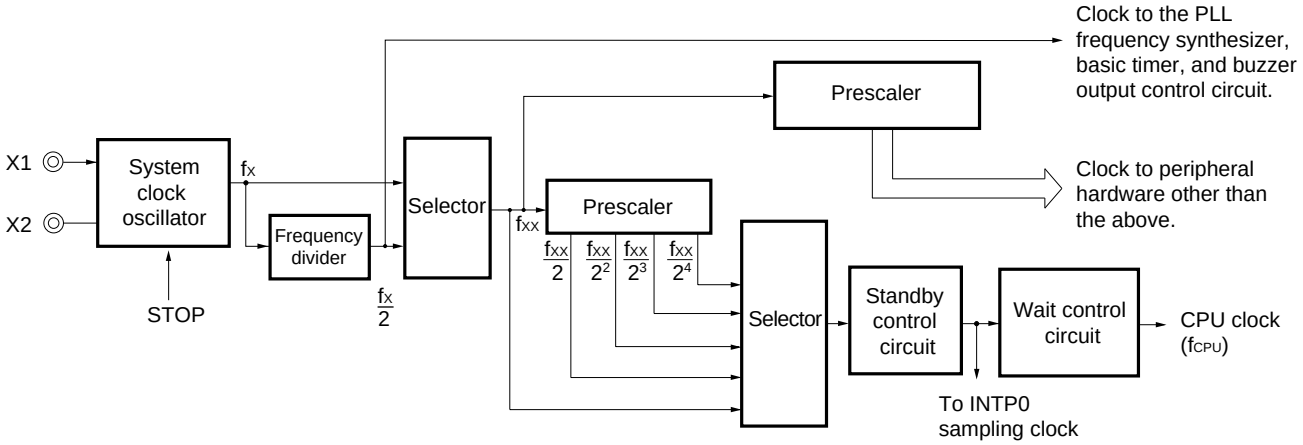
Name	Pin Name	Function
Port 0	P00	Input only
	P01 to P06	Input/output port. Input/output can be specified in 1-bit units.
Port 1	P10 to P15	Input/output port. Input/output can be specified in 1-bit units.
Port 2	P20 to P27	Input/output port. Input/output can be specified in 1-bit units.
Port 3	P30 to P37	Input/output port. Input/output can be specified in 1-bit units.
Port 4	P40 to P47	Input/output port. Input/output can be specified in 8-bit units. The test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port. Input/output can be specified in 1-bit units.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified in 1-bit units. LEDs can be driven directly.
	P64 to P67	Input/output port. Input/output can be specified in 1-bit units.
Port 12	P120 to P125	Input/output port. Input/output can be specified in 1-bit units.
Port 13	P132 to P134	N-ch open-drain output port.

5.2 Clock Generator

The instruction execution time can be changed as follows.

0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (4.5 MHz crystal resonator for system clock.)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Three timer channels are incorporated.

- Basic timer: 1 channel
- 8-bit timer/event counter: 2 channels

Figure 5-2. Basic Timer Block Diagram

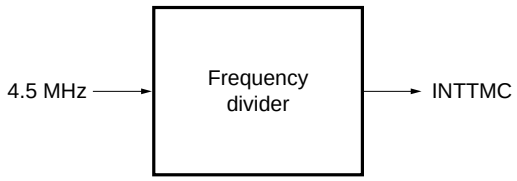
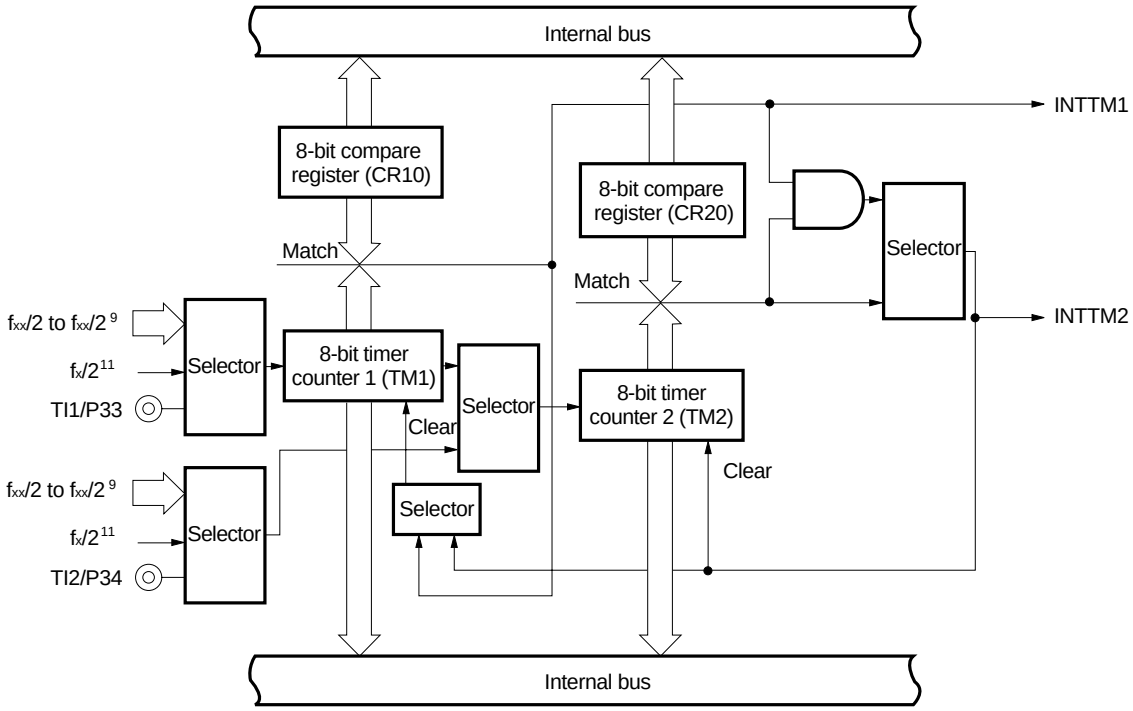


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter

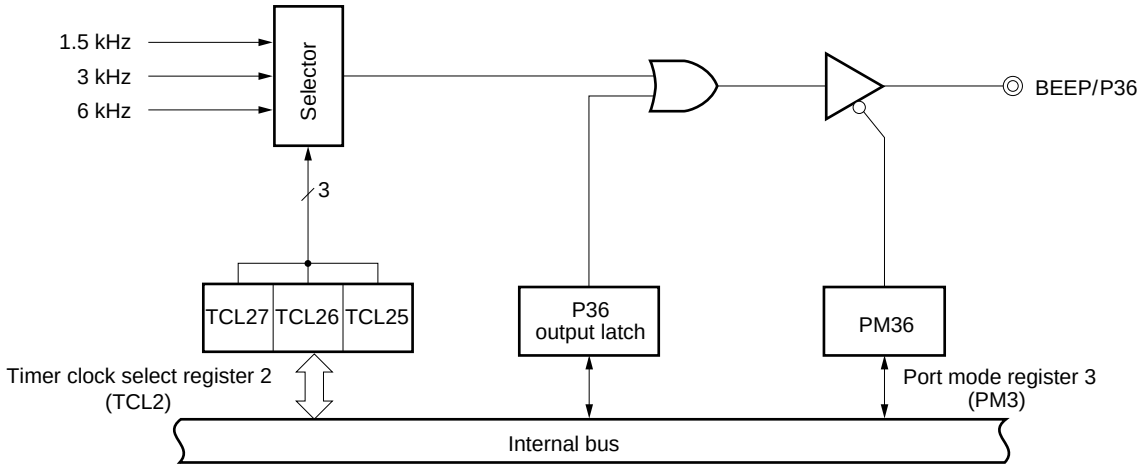


5.4 Buzzer Output Control Circuit

Clocks with the following frequencies can be output as buzzer (BEEP) output.

- 1.5 kHz/3 kHz/6 kHz (4.5 MHz crystal resonator for system clock)

Figure 5-4. Block Diagram of Buzzer Output Control Circuit



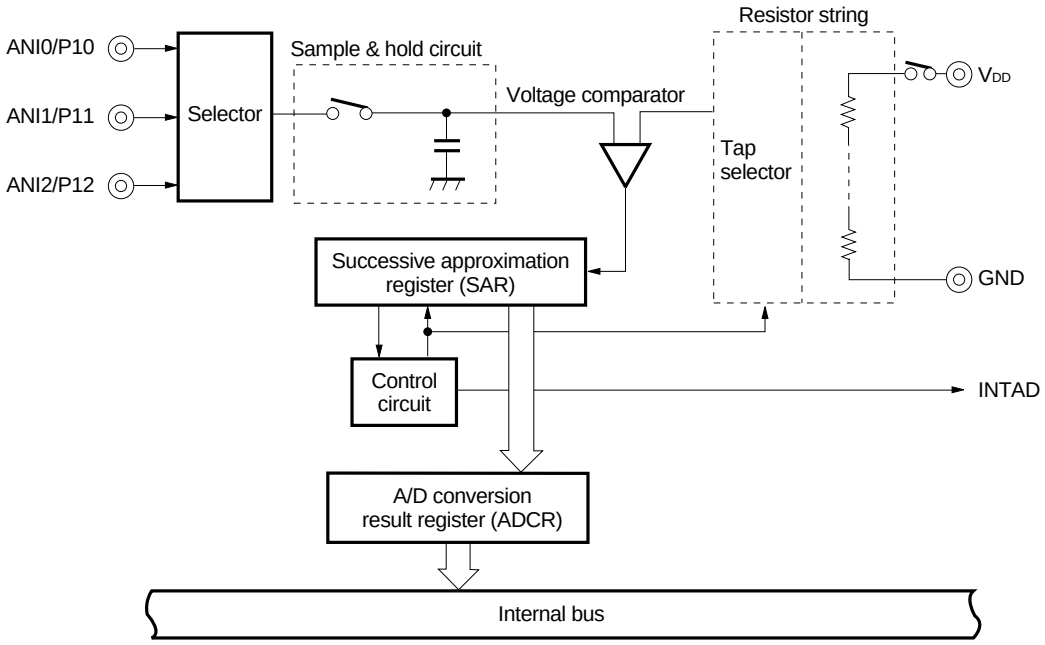
★ 5.5 A/D Converter

An A/D converter consisting of three 8-bit resolution channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-5. A/D Converter Block Diagram

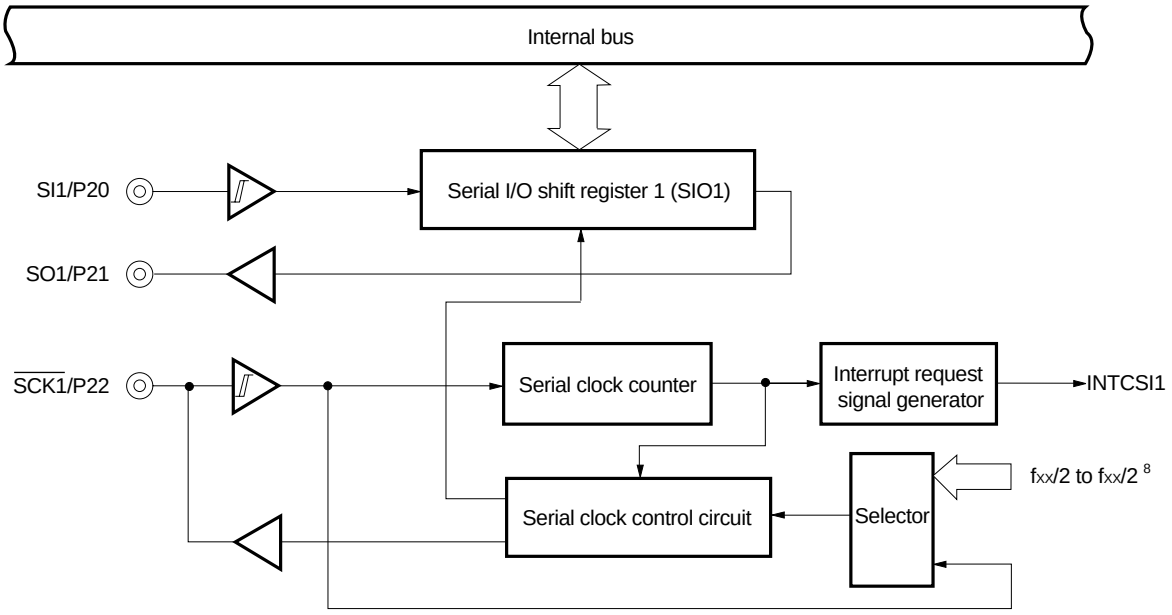


5.6 Serial Interfaces

One clocked serial interface channel is incorporated.

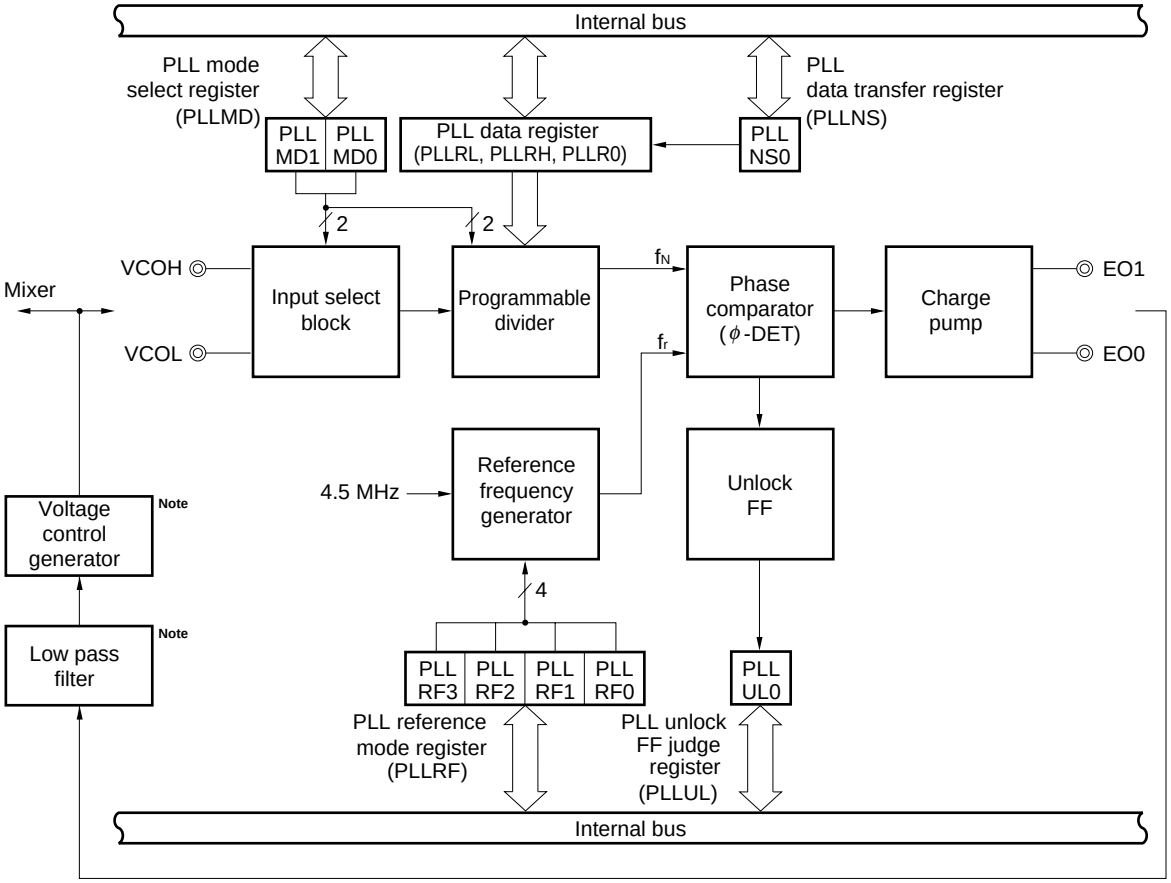
Serial interface channel 1 operates in the 3-wire serial I/O mode where MSB/LSB first can be switched.

Figure 5-6. Block Diagram of Serial Interface Channel 1



5.7 PLL Frequency Synthesizer

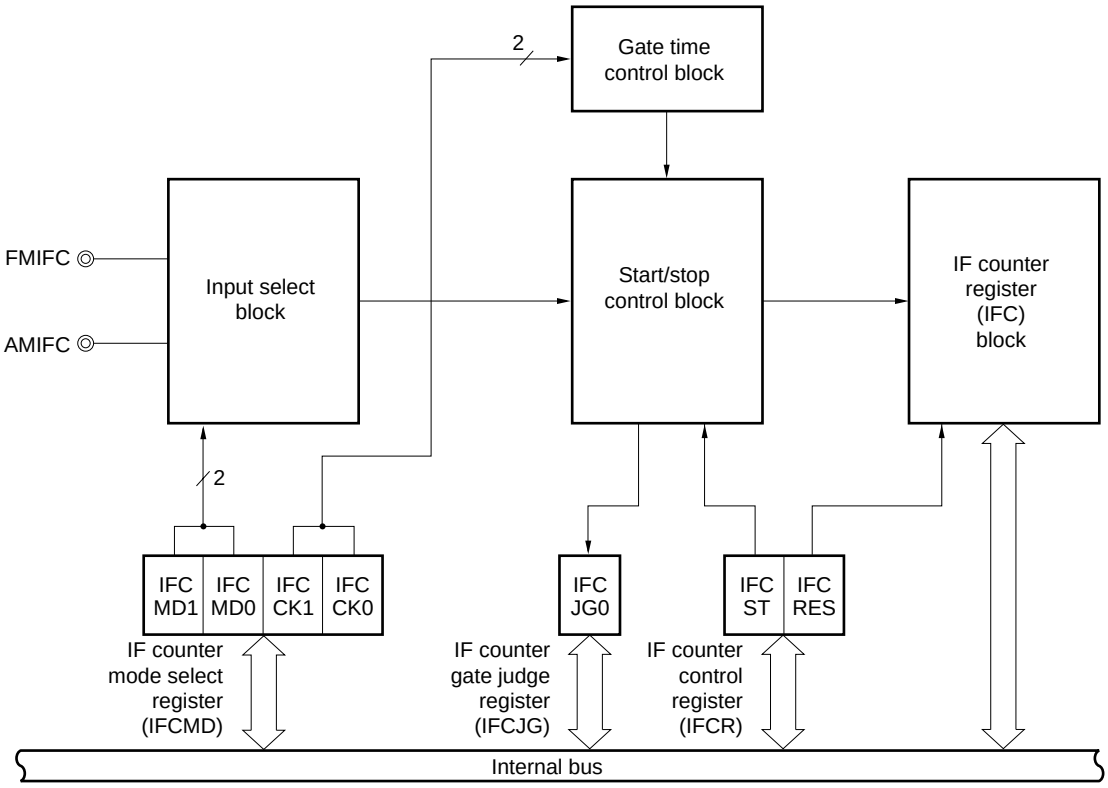
Figure 5-7. Block Diagram of PLL Frequency Synthesizer



Note External circuit

5.8 Frequency Counter

Figure 5-8. Frequency Counter Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 8 interrupt sources are provided, divided into the following two types.

- Maskable: 7
- Software: 1

Table 6-1. Interrupt Source List

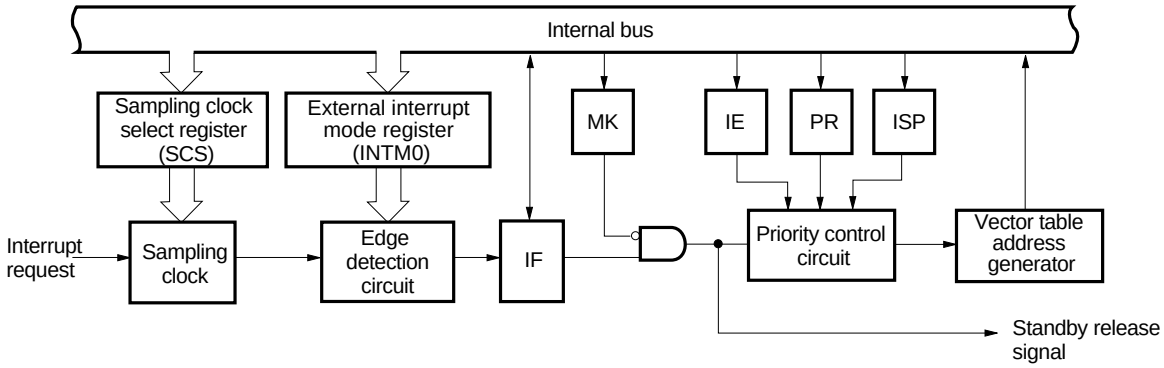
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Maskable	0	INTP0	Pin input edge detection	External	0006H	(A)
	1	INTP1			0008H	(B)
	2	INTCSI1	End of serial interface channel 1 transfer	Internal	0016H	(C)
	3	INTTMC	Generation of matching signal of basic timer		0018H	
	4	INTTM1	Generation of matching signal of 8-bit timer/event counter 1		001CH	
	5	INTTM2	Generation of matching signal of 8-bit timer/event counter 2		001EH	
	6	INTAD	End of conversion by A/D converter		0020H	
Software	—	BRK	Execution of BRK instruction	—	003EH	(D)

Notes 1. The default priority is a priority order when several maskable interrupts are generated at the same time. 0 is the highest order and 6 is the lowest order.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) External maskable interrupt (INTP0)



(B) External maskable interrupt (INTP1)

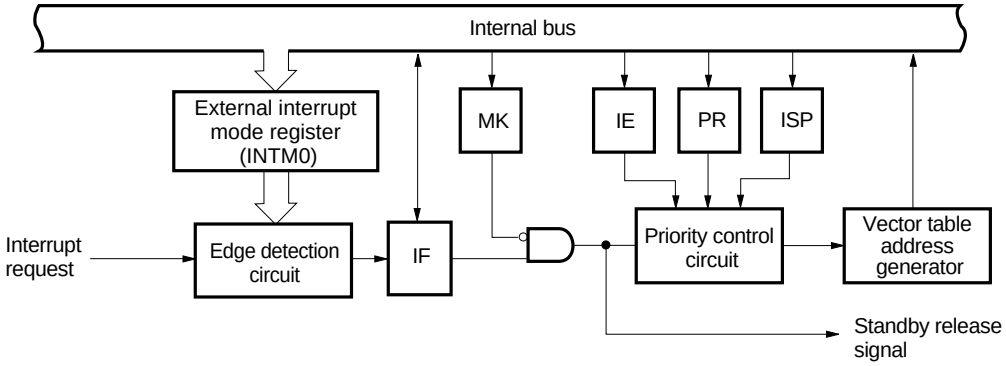
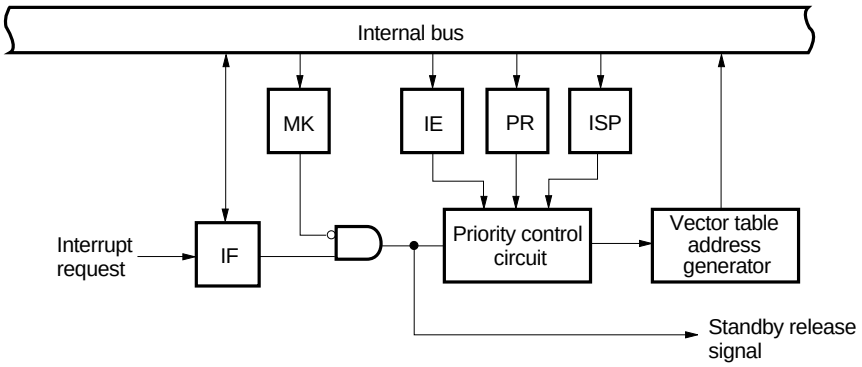
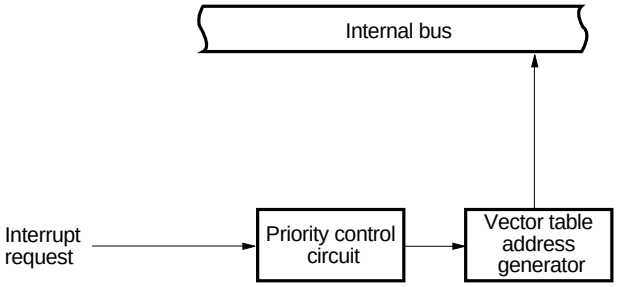


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(C) Internal maskable interrupt



(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

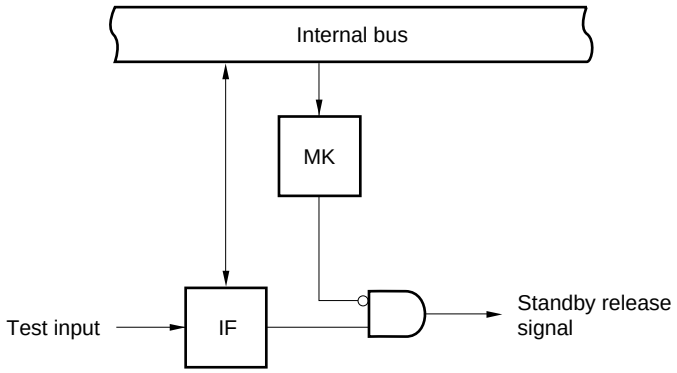
6.2 Test Function

Table 6-2 shows a test function available.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Basic Configuration of Test Function



IF: Test input flag

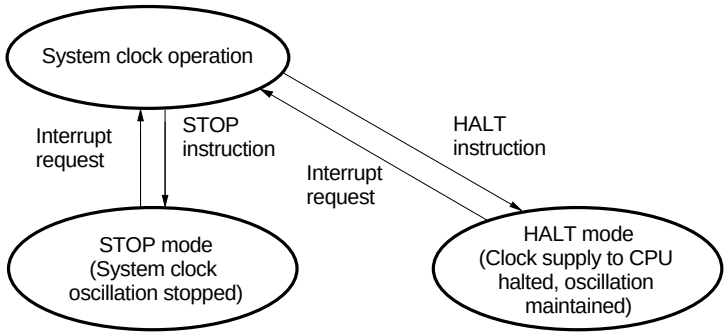
MK: Test mask flag

7. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by Power On Clear (POC).

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output withstand voltage	V_{BDS}	P132 to P134	N-ch open drain	–0.3 to V_{DD} + 0.3	V
★ Analog input voltage	V_{AN}	P10 to P12	Analog input pin	–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P125		–15	mA
		Total for P10 to P15, P20 to P27, P40 to P47, P50 to P55, P132 to P134		–15	mA
Output current, low	I_{OL}**Note**	Per pin	Peak value	15	mA
			rms value	7.5	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Recommended Supply Voltage Ranges (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	During CPU operation and PLL operation.	4.5		5.5	V
	V_{DD2}	While the CPU is operating and the PLL is stopped. Cycle time: $T_{CY} \geq 0.89$ μs	3.5		5.5	V
	V_{DD3}	While the CPU is operating and the PLL is stopped. Cycle time: T_{CY} = 0.44 μs	4.5		5.5	V

Remark T_{CY}: Cycle time (minimum instruction execution time)

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V) (1/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch open drain)		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0		0.3V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.15V_{DD}	V
	V_{IL3}	P60 to P63 (N-ch open drain)		0		0.2V_{DD}	V
Output voltage, high	V_{OH1}		4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OH} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P120 to P125, P132 to P134	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, N-ch open drain, pulled-up (R = 1 KΩ)			0.2V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	$V_{IN} = V_{DD}$			3	μA
	I_{LIH2}	P60 to P63	$V_{IN} = V_{DD}$			80	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	P60 to P63				–3[Note]	μA
Output leakage current, high	I_{LOH}	P132 to P134	$V_{OUT} = V_{DD}$			3	μA
Output leakage current, low	I_{LOL}	P132 to P134	V_{OUT} = 0 V			–3	μA
Output off leakage current	I_{LOF}	EO0, EO1	$V_{OUT} = V_{DD}$, V_{OUT} = 0 V			±1	μA

Note When an input instruction is executed to P60 to P63, a low-level input leakage current of –200 μA (MAX.) flows only for one clock. At times other than this 1-clock interval, a –3 μA (MAX.) current flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Reference Characteristics (T_A = 25°C, V_{DD} = 5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH1}	EO0	$V_{OUT} = V_{DD}$ – 1 V		–4		mA
		EO1		–1.8			mA
Output current, low	I_{OL1}	EO0	V_{OUT} = 1 V		6		mA
		EO1		3.5			mA

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	While the CPU is operating and the PLL is stopped f_X = 4.5 MHz operation	T_{CY} = 0.89 μs[Note 2]		2.5	15	mA
	I_{DD2}		T_{CY} = 0.44 μs[Note 3] V_{DD} = 4.5 to 5.5 V		4.0	27	mA
	I_{DD3}	While the CPU is operating and the PLL is stopped HALT Mode Pin X1 sine wave input V_{IN} = V_{DD}. f_X = 4.5 MHz operation	T_{CY} = 0.89 μs[Note 2]		0.7	1.5	mA
	I_{DD4}		T_{CY} = 0.44 μs[Note 3] V_{DD} = 4.5 to 5.5 V		1.0	2.0	mA
Data retention power supply voltage	V_{DDR1}	When the crystal oscillation is operating	T_{CY} = 0.44 μs	4.5		5.5	V
	V_{DDR2}		T_{CY} = 0.89 μs	3.5		5.5	V
	V_{DDR3}	When the crystal oscillation is stopped When power off by power on clear is detected		2.6		5.5	V
Data retention power supply current	I_{DDR1}	When the crystal oscillation is stopped	T_A = 25°C, V_{DD} = 5 V		2	4	μA
	I_{DDR2}				2	30	μA

Notes 1. The current flowing to the ports is not included.

2. When the processor clock control register (PCC) is set to 00H, and the oscillation mode select register (OSMS) is set to 00H.

3. When PCC is set to 00H and OSMS is set to 01H.

Remarks 1. T_{CY}: Cycle time (minimum instruction execution time)

2. f_X: System clock oscillation frequency.

Reference Characteristics (T_A = 25°C, V_{DD} = 5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD5}	During CPU operation and PLL operation. VCOH pin sine wave input f_{IN} = 130 MHz, V_{IN} = 0.15 V_{p-p}	T_{CY} = 0.44 μs[Note]		7		mA

Note When the processor clock control register (PCC) is set to 00H, and the oscillation mode select register (OSMS) is set to 01H.

Remark T_{CY}: Cycle time (minimum instruction execution time)

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note 1, f_X = 4.5 MHz operation		0.89		14.22	μs
		$f_{XX} = f_X$ Note 2, f_X = 4.5 MHz operation	4.5 V ≤ V_{DD} ≤ 5.5 V	0.44		7.11	μs
			3.5 V ≤ V_{DD} < 4.5 V	0.89		7.11	μs
TI1, TI2 input frequency	f_{TI}	4.5 V ≤ V_{DD} ≤ 5.5 V		0		4.5	MHz
		3.5 V ≤ V_{DD} < 4.5 V		0		275	kHz
TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	4.5 V ≤ V_{DD} ≤ 5.5 V		111			ns
		3.5 V ≤ V_{DD} < 4.5 V		1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0		$8/f_{sam}$ Note 3			μs
		INTP1		10			μs
$\overline{RESET}$ low level width	t_{RSL}			10			μs

Notes 1. When the oscillation mode select register (OSMS) is set to 00H.

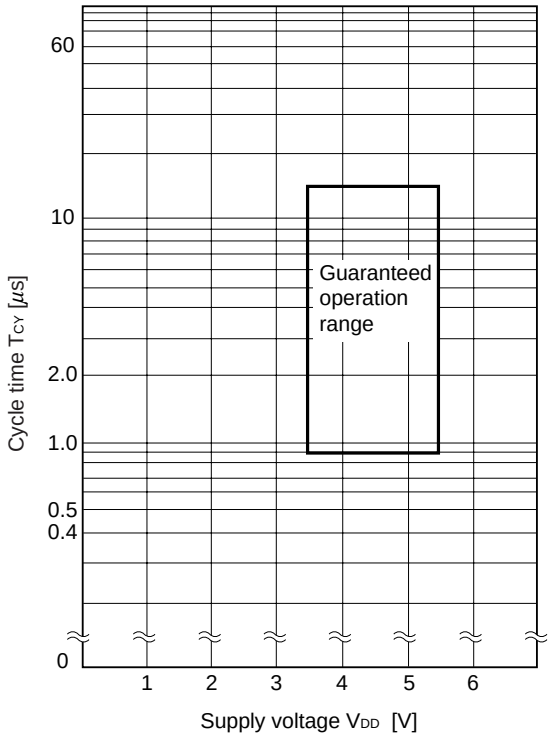
2. When OSMS is set to 01H.

3. Selection of $f_{sam} = f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, $f_{XX}/128$ is possible with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS) (when N = 0 to 4).

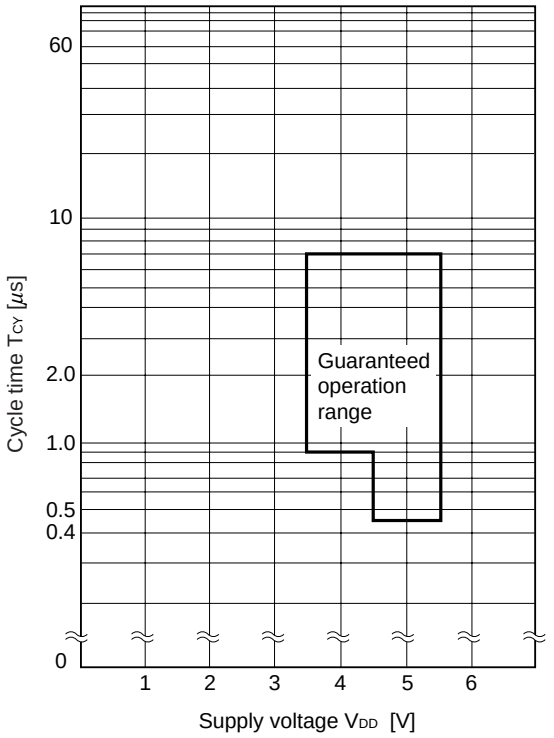
Remarks 1. f_{XX}: System clock frequency (f_X or $f_X/2$)

2. f_X: System clock oscillation frequency

T_{CY} vs. V_{DD} (At $f_{XX} = f_X/2$ system clock operation)



T_{CY} vs. V_{DD} (At $f_{XX} = f_X$ system clock operation)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH1}, t_{KL1}	4.5 V ≤ V_{DD} ≤ 5.5 V	t_{KCY9}/2 – 50			ns
		3.5 V ≤ V_{DD} < 4.5 V	t_{KCY9}/2 – 100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI1}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO1}	C = 100 pF**Note**			300	ns

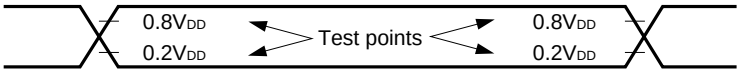
Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

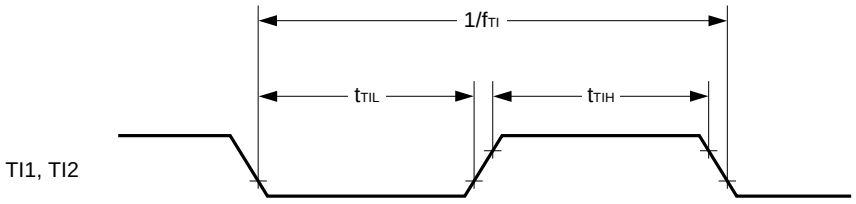
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK2}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI2}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO2}	C = 100 pF**Note**			300	ns
$\overline{SCK1}$ rise/fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of the SO1 output line.

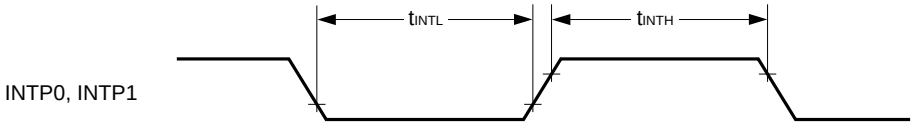
AC Timing Test Points (excluding X1 input)



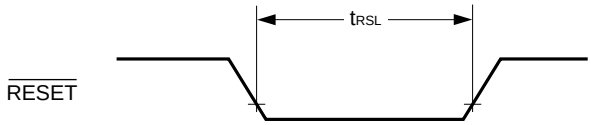
TI Timing



Interrupt Input Timing

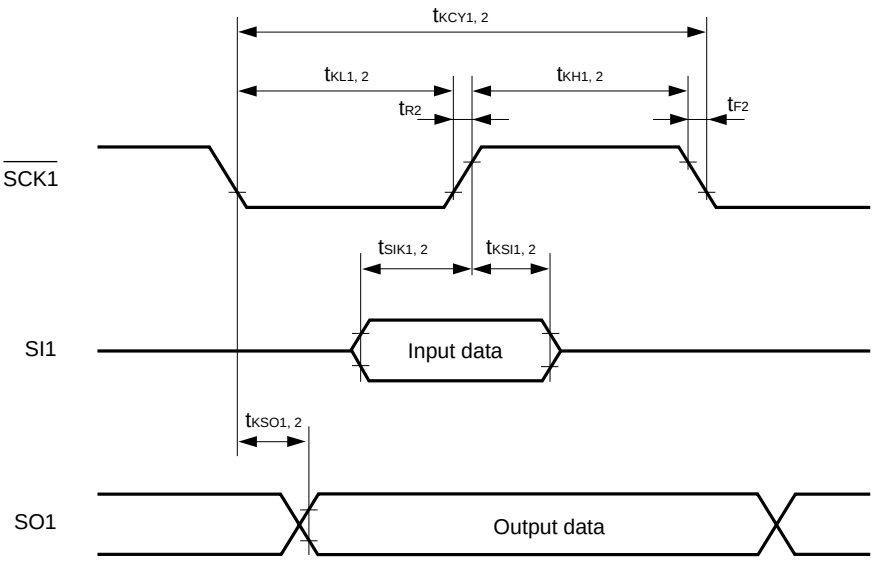


$\overline{\text{RESET}}$ Input Timing



Serial Transfer Timing

3-wire serial I/O mode:



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Conversion overall error					±3.0	LSB
Conversion time	t_{CONV}		22.2		44.4	μs
Sampling time	t_{SAMP}		15/f_{XX}			μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Remarks 1. f_{XX}: System clock frequency (f_X/2)

2. f_X: System clock oscillation frequency

PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin MF mode Sine wave input V_{IN} = 0.1 V_{p-p}	0.5		3	MHz
	f_{IN2}	VCOL pin HF mode Sine wave input V_{IN} = 0.2 V_{p-p}	9		55	MHz
	f_{IN3}	VCOH pin VHF mode Sine wave input V_{IN} = 0.15 V_{p-p}	60		160	MHz

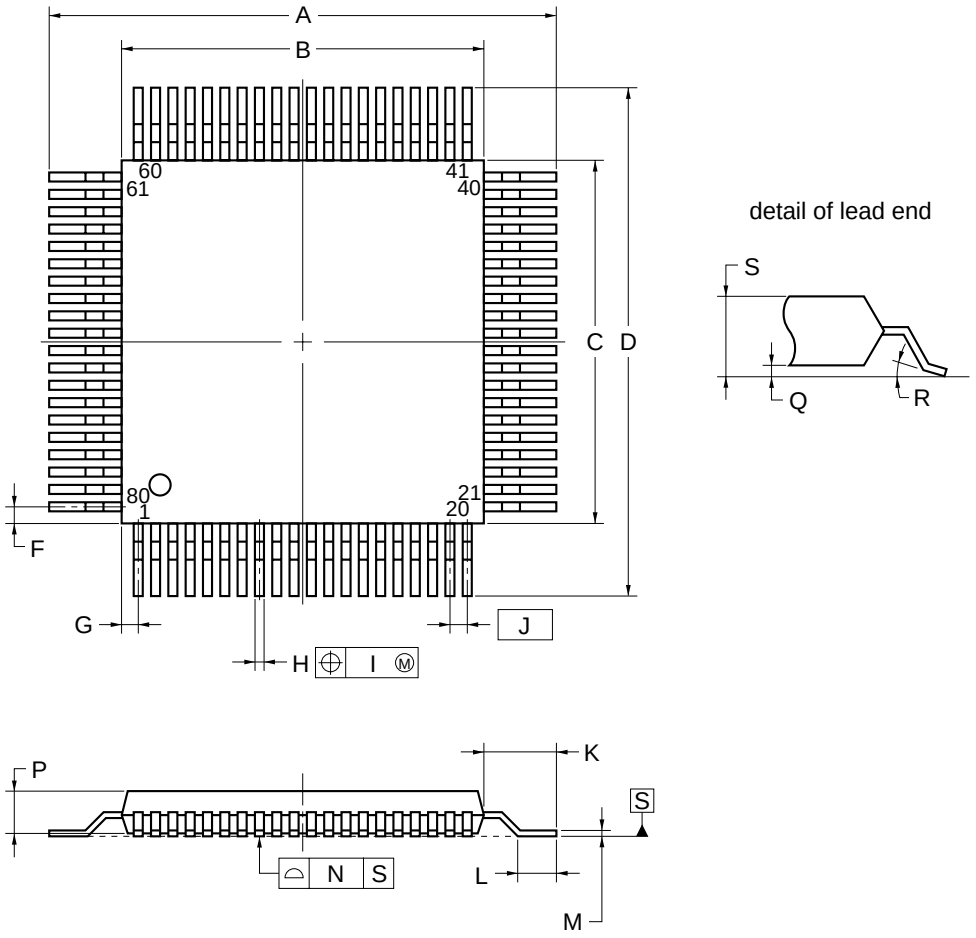
IFC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN4}	AMIFC pin AMIF count mode Sine wave input V_{IN} = 0.1 V_{p-p}**Note**	0.4		0.5	MHz
	f_{IN5}	FMIFC pin FMIF count mode Sine wave input V_{IN} = 0.1 V_{p-p}**Note**	10		11	MHz
	f_{IN6}	FMIFC pin AMIF count mode Sine wave input V_{IN} = 0.1 V_{p-p}**Note**	0.4		0.5	MHz

Note The condition of a sine wave input of V_{IN} = 0.1 V_{p-p} is the standard value of this device during standalone operation, so in consideration of the effect of noise, operation of an input amplitude condition of V_{IN} = 0.15 V_{p-p} is recommended.

11. PACKAGE DRAWINGS

80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.2±0.4
B	14.0±0.2
C	14.0±0.2
D	17.2±0.4
F	0.825
G	0.825
H	0.30±0.10
I	0.13
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

S80GC-65-3B9-6

12. RECOMMENDED SOLDERING CONDITIONS

The μPD178002 and 178003 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD178002GC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)
μPD178003GC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES AMONG μPD178003 AND μPD178018A SUBSERIES

Items \ Product Name		μPD178003 Subseries	μPD178018A Subseries		
		μPD178003	μPD178006A	μPD178018A	μPD178P018A
ROM		24 Kbytes (Mask ROM)	48 Kbytes (Mask ROM)	60 Kbytes (Mask ROM)	60 Kbytes (One-time PROM)
RAM	High-speed RAM	512 bytes	1024 byte		
	Buffer RAM	Not provided	32 bytes		
	Expanded RAM	Not provided		2048 bytes	
Timer		3 channels • Basic timer: 1 channel • 8-bit timer/event counter: 2 channels	5 channels • Basic timer: 1 channel • 8-bit timer/event counter: 2 channels • 8-bit timer: 1 channel • Watchdog timer: 1 channel		
Serial interface		1 channel • 3-wire mode: 1 channel	2 channels • 3-wire/SBI/2-wire/I^2C bus mode selectable: 1 channel • 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes provided on chip): 1 channel		
★ A/D converter		3 channels	6 channels		
D/A converter (PWM output)		Not provided	Provided		
EO1 pin output circuit		Buffer type (high impedance function not supported)		Buffer type (high impedance function supported)	

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD178003 Subseries. Also refer to **(5) Cautions on using development tools**.

(1) Language processing software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF178018	Device file for μPD178003 and μPD178018A Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(2) PROM writing tools

PG-1500	PROM programmer
PG-178P018GC	Programmer adapters connected to PG-1500
PA-178P018KK-T	
PG-1500 controller	PG-1500 control program

★ **(3) Debugging tools**

- **When IE-78K0-NS in-circuit emulator is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA**Note**	Performance board for enhancing and extending the function of the IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC of PC-9800 series as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™-compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter required when using a PCI bus incorporated computer as host machine
IE-178018-NS-EM1	Emulation board to emulate μPD178003, 178018A Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-3B9 type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF178018	Device file for μPD178003 and μPD178018A Subseries

Note Under development

- **When IE-78001-R-A in-circuit emulator is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT-compatible as host machine (ISA bus supported)
★ IE-70000-PCI-IF	Adapter required when using a PCI bus incorporated computer as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-178018-NS-EM1	Emulation board to emulate μPD178003, 178018A Subseries
IE-78K0-R-EX1	Emulation probe conversion board required when using IE-178018-NS-EM1 on IE-78001-R-A
IE-178018-R-EM	Emulation board to emulate μPD178003, 178018A Subseries
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9 type)
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-3B9 type)
EV-9900	Tool used for removing μPD178P018AKK-T from EV-9200GC-80
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF178018	Device file for μPD178003 and μPD178018A Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools

- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF178018.
- The RX78K/0 is used in combination with the RA78K0 and the DF178018.
- The NP-80GC is a product made by Naito Densei Machida Mfg. Co., Ltd (TEL +81-44-822-3813). Contact an NEC distributor regarding the purchase of this product.
- For third party development tools, see the **Single-chip Microcontroller Development Tools Selection Guide (U11069E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine / [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT-compatible [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™ and Solaris™] NEWS (RISC)™ [NEWS-OS™]
RA78K0	√Note	√
CC78K0	√Note	√
PG-1500 controller	√Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX C. RELATED DOCUMENTS

Documents Related to Devices

	Document Name		Document No.	
			English	Japanese
	μPD178P018A Data Sheet		U12642E	U12642J
★	μPD178003 Subseries User's Manual		U13033E	U13033J
	78K/0 Series User's Manual—Instruction		U12326E	U12326J
	78K/0 Series Instruction Set		—	U10904J
	78K/0 Series Instruction Table		—	U10903J
	78K/0 Series Application Note	Basics (II)	U10121E	U10121J

Documents Related to Development Tools (User's Manuals)

	Document Name		Document No.	
			English	Japanese
	RA78K0 Assembler Package	Operation	U11802E	U11802J
		Assembly Language	U11801E	U11801J
		Structured Assembly Language	U11789E	U11789J
	RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
	CC78K0 C Compiler	Operation	U11517E	U11517J
		Language	U11518E	U11518J
	PG-1500 PROM Programmer		U11940E	U11940J
	PG-1500 Controller PC-9800 series (MS-DOS) Based		EEU-1291	EEU-704
	PG-1500 Controller IBM PC series (PC DOS) Based		U10540E	EEU-5008
★	IE-78K0-NS		—	U13731J
	IE-78001-R-A		To be prepared	To be prepared
	IE-78K0-R-EX1		To be prepared	To be prepared
★	IE-178018-NS-EM1		U14012E	U14012J
	IE-178018-R-EM		U10668E	U10668J
	EP-78230		EEU-1515	EEU-985
	SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
	SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
★	ID78K0-NS Integrated Debugger Windows Based	Reference	U12900E	U12900J
	ID78K0 Integrated Debugger EWS Based	Reference	—	U11151J
	ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J
	ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-Time OS	Fundamentals	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

Other Related Documents

Document Name	Document No.	
	English	Japanese
★ SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	—	U11416J

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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