NEC

MOS INTEGRATED CIRCUIT

μPD17202AGF-011

4-BIT SINGLE-CHIP MICROCONTROLLER WITH LCD CONTROLLER/DRIVER AND KEY SCAN CIRCUIT FOR FPC (FRONT PANEL CONTROLLER)

The μPD17202AGF-011 is a CMOS microcontroller for the FPC (Front Panel Controller) of a car stereo system.

This microcontroller is housed in a 64-pin QFP and is provided with an LCD controller/driver and key scan circuit, enabling the reduction of the amount of wiring between the front panel of the car stereo system and the master microcontroller.

FEATURES

- LCD controller/driver : Can display up to 75 segments.
  1/3 duty, 1/3 bias, frame frequency: 325.5 Hz
- Key scan circuit : Can read up to 30 (5 × 6) keys.
- LED output : 1 pin
- 3-wire serial communication mode : CLOCK, DATA, and LOAD pins
- Supply voltage : V_{DD} = 4.5 to 5.5 V
- System clock : f_X = 8 MHz

ORDERING INFORMATION

Part Number	Package
μPD17202AGF-011-3BE	64-pin plastic QFP (14 × 20 mm, 1.0-mm pitch)

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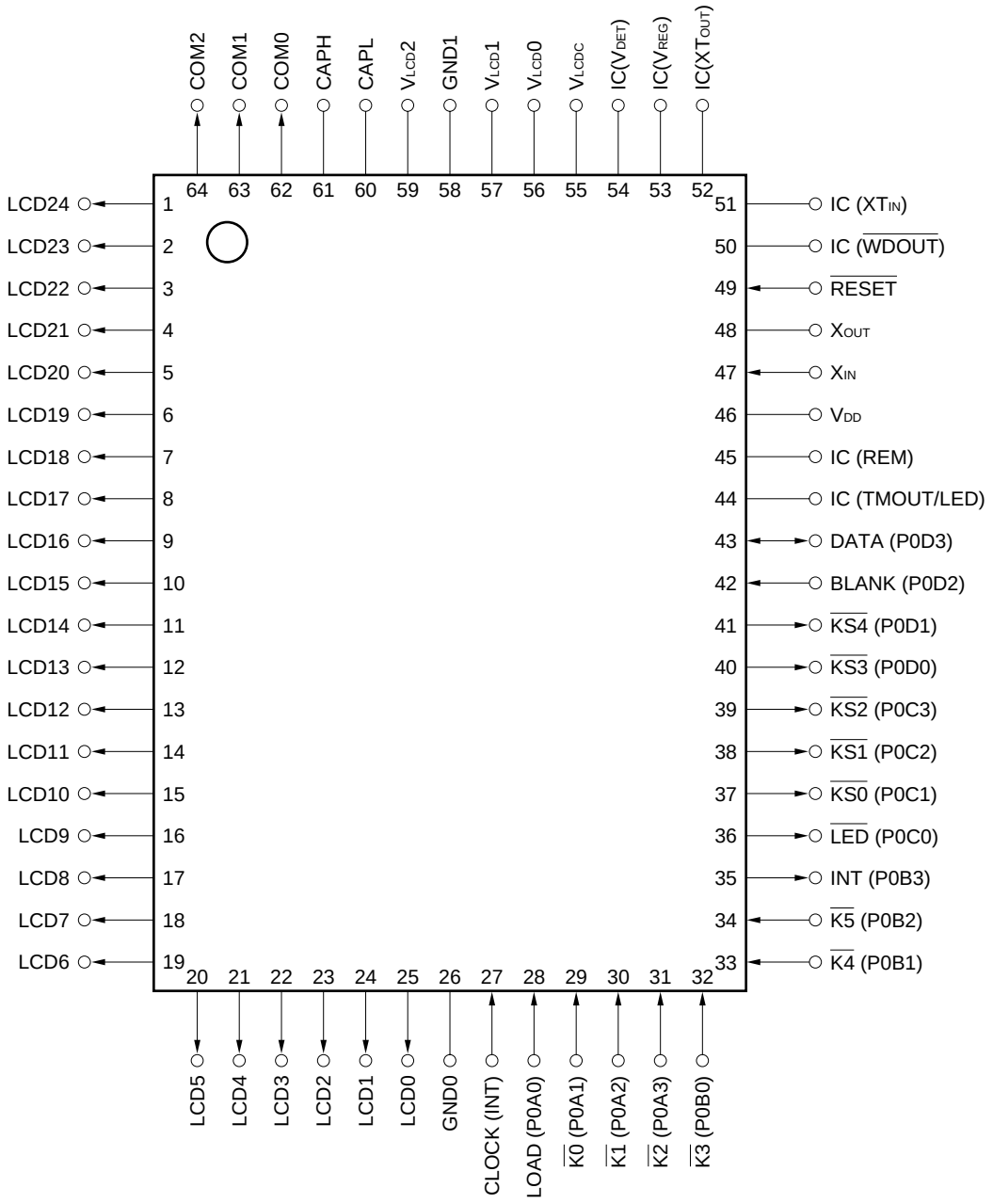
Date Published May 1997 N
Printed in Japan

PIN CONFIGURATION (Top View)

64-pin plastic QFP (14 × 20 mm, 1.0-mm pitch)
μPD17202AGF-011-3BE



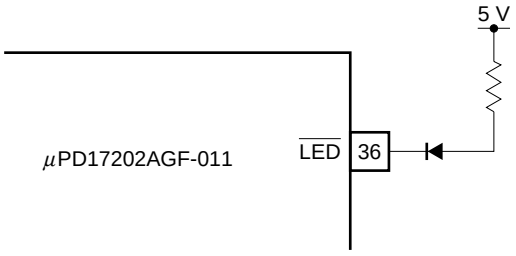
Remarks 1. IC: Internally Connected

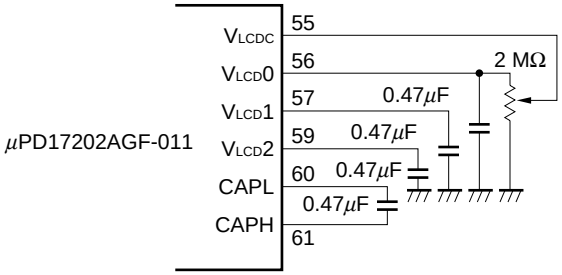
2. ( ): Pin names of μPD17202AGF-×××-3BE

CONTENTS

1. PIN FUNCTION

1.1 Pin Function List

Pin No.	Symbol	Pin Name	Description	I/O Format
1 to 25	LCD24 to LCD0	LCD segment signal output	These pins output segment signals to an LCD panel. They are used to control the display on the LCD panel by forming a matrix with COM0 through COM2 (pins 62 through 64).	CMOS push-pull output
26 58	GND0 GND1	Ground	Ground pin	–
27	CLOCK	Clock input	Serial communication clock input. Data is input to or output from the DATA pin (pin 43) at the rising edge of the clock input to this pin.	Input
28	LOAD	Load input	Serial communication load input. Commands are executed and the output status is cleared in synchronization with the rising edge of this pin. While this pin is high, clock input is invalid. This pin is connected to an internal pull-up resistor.	Input
29 to 34	$\overline{K0}$ to $\overline{K5}$	Key return signal input	These pins input key return signals from a key matrix. These pins are connected to an internal pull-down resistor.	Input
35	INT	Key scan end signal output	This pin outputs a key scan end signal to the master microcontroller. It goes high when key scanning has ended after execution of a key data output command. This pin goes low at the rising edge of the LOAD pin (pin 28) after data has been output. While this pin is low, key data cannot be correctly output. The initial value of this pin is the low level. Be sure to connect a pull-down resistor to this pin.	CMOS push-pull output
36	$\overline{LED}$	LED output	This pin is connected to an LED that is used to check connection with the master microcontroller. When this pin is low, the LED lights. This pin is output depending on the LED data value of display data input (data A, refer to **4.2 LCD Display Data Configuration**). This pin is floated in the initial status. 	N-ch open-drain output
37 to 41	$\overline{KS0}$ to $\overline{KS4}$	Key source output	These pins output key source signals to a key matrix.	N-ch open-drain output

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin Name</th><th>Description</th><th>I/O Format</th></tr>
<tr><td>42</td><td>BLANK</td><td>Blank input</td><td>By connecting an external controller to this pin, the display of the LCD panel can be turned ON/OFF.
<table><tr><th>Input level</th><th>LCD display status</th></tr><tr><td>Low</td><td>Lights</td></tr><tr><td>High</td><td>Extinguishes</td></tr></table>To control this pin, connect it to an external controller via pull-up resistor; otherwise, connect it to GND via pull-down resistor.</td><td>Input</td></tr>
<tr><td>43</td><td>DATA</td><td>Serial data I/O</td><td>Serial communication data I/O pin.
This pin outputs data from the rising edge of the LOAD pin (pin 28) after a key data output signal has been received, to the next rising edge; otherwise, it inputs data.</td><td>N-ch open-drain output</td></tr>
<tr><td>44, 45</td><td rowspan="4">IC</td><td rowspan="4">Internally connected</td><td>Connect nothing to these pins.</td><td rowspan="4">–</td></tr>
<tr><td>50, 51</td><td>Connect these pins to GND via pull-down resistor.</td></tr>
<tr><td>52, 53</td><td>Short-circuit pins 52 and 53.</td></tr>
<tr><td>54</td><td>Connect this pin to V_{DD}.</td></tr>
<tr><td>46</td><td>V_{DD}</td><td>Power supply</td><td>This is a common power supply pin (V_{DD} = 2.2 to 5.5 V).</td><td>–</td></tr>
<tr><td>47</td><td>X_{IN}</td><td rowspan="2">Crystal resonator</td><td rowspan="2">These pins are used to connect a crystal resonator.
Connect an 8-MHz ceramic oscillator or crystal resonator to these pins. The accuracy of the watch is influenced only by the oscillation frequency of the oscillator.</td><td>Input</td></tr>
<tr><td>48</td><td>X_{OUT}</td><td>–</td></tr>
<tr><td>49</td><td>$\overline{RESET}$</td><td>Reset input</td><td>Reset input.</td><td>Input</td></tr>
<tr><td>55</td><td>V_{LCDC}</td><td>LCD reference voltage adjustment</td><td>This pin is used to adjust the reference voltage for the LCD driver.
Example
 
</td><td>–</td></tr>
<tr><td>56
57
59</td><td>$V_{LCD}0$
$V_{LCD}1$
$V_{LCD}2$</td><td>LCD regulator</td><td>LCD regulator pin.</td><td>–</td></tr>
<tr><td>60
61</td><td>CAPL
CAPH</td><td>LCD boosting capacitor</td><td>These pins connect a capacitor used to boost the LCD driver voltage.
Connect a capacitor of 0.47 μF between the CAPL and CAPH pins.</td><td>–</td></tr>
<tr><td>62
to
64</td><td>COM0
to
COM2</td><td>Common signal output of LCD controller/driver</td><td>These pins output the common signals of the LCD controller/driver.</td><td>CMOS 3-state output</td></tr>
</table>

2. CONFIGURATION OF KEY MATRIX

2.1 Layout of Key Matrix

The μPD17202AGF-011 can be used to configure a key matrix of up to 30 keys, KEY0 through KEY29, by using the $\overline{KS0}$ through $\overline{KS4}$ pins (key source pins) and $\overline{K0}$ through $\overline{K5}$ pins (key return pins).

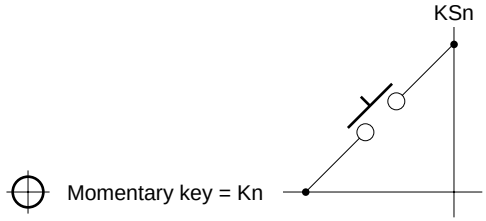
Keys KEY0 through KEY29 are allocated as shown below. The details of each key can be set arbitrarily.

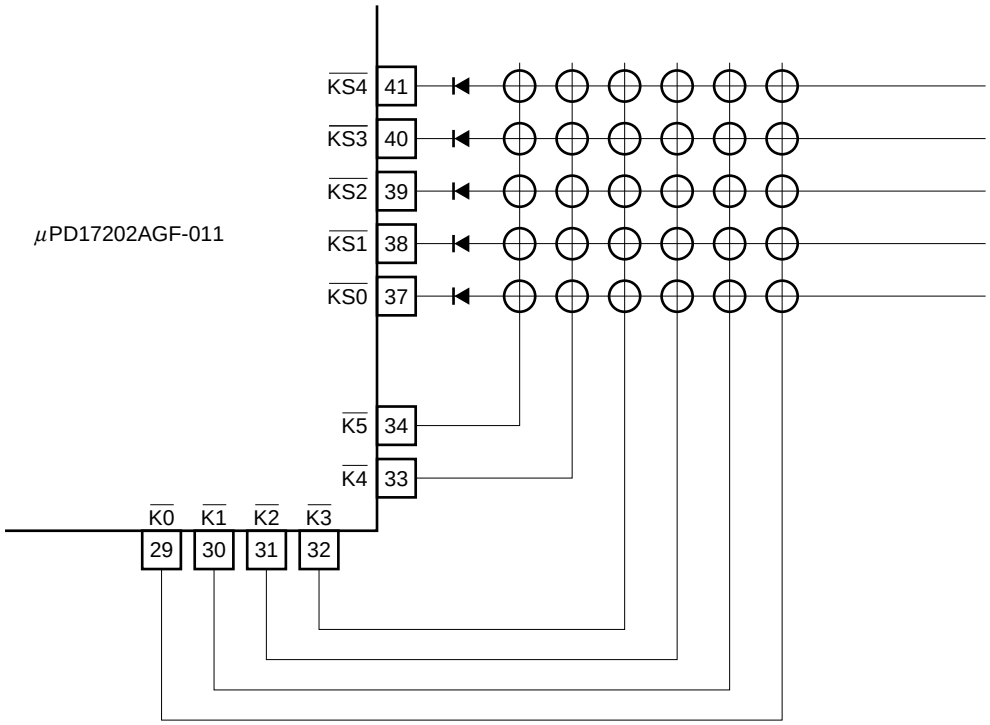
Input Pin (Pin No.) / Output Pin (Pin No.)	$\overline{K0}$ (29)	$\overline{K1}$ (30)	$\overline{K2}$ (31)	$\overline{K3}$ (32)	$\overline{K4}$ (33)	$\overline{K5}$ (34)
$\overline{KS0}$ (37)	KEY0	KEY1	KEY2	KEY3	KEY4	KEY5
$\overline{KS1}$ (38)	KEY6	KEY7	KEY8	KEY9	KEY10	KEY11
$\overline{KS2}$ (39)	KEY12	KEY13	KEY14	KEY15	KEY16	KEY17
$\overline{KS3}$ (40)	KEY18	KEY19	KEY20	KEY21	KEY22	KEY23
$\overline{KS4}$ (41)	KEY24	KEY25	KEY26	KEY27	KEY28	KEY29

Remark Numbers in brackets ( ) are pin numbers.

2.2 Connection of Key Matrix

An example of connection of the key matrix is shown below.





3. KEY SCAN

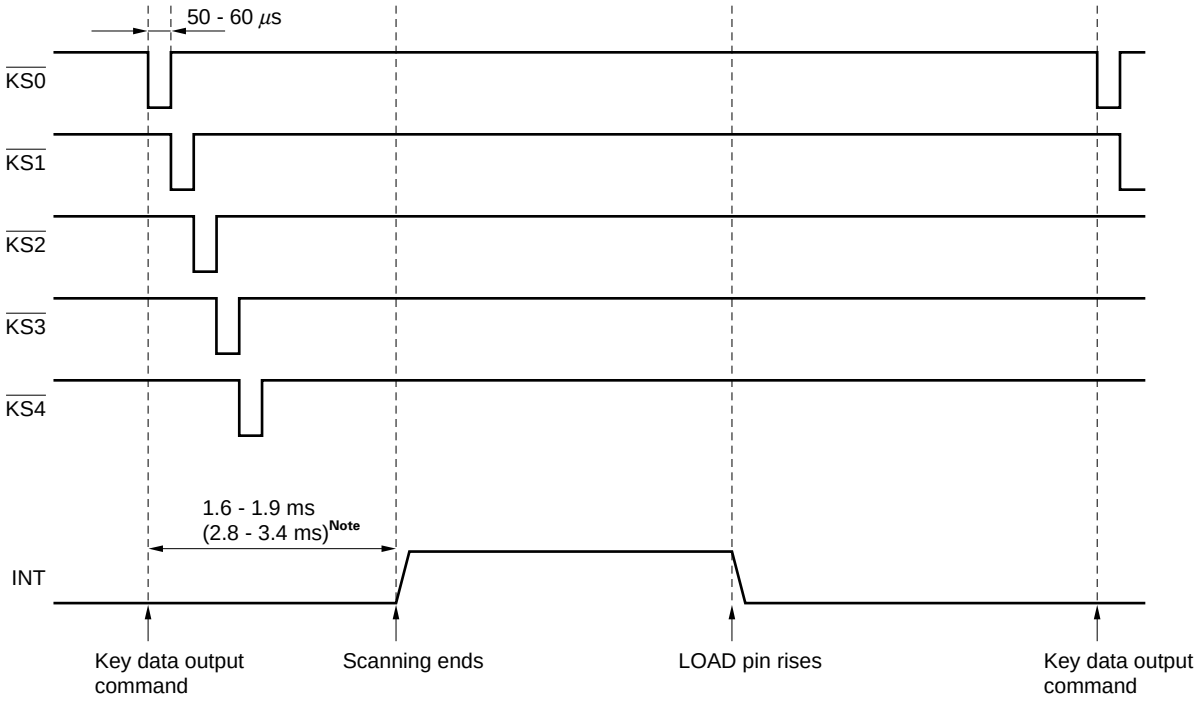
3.1 Key Scan Function

Key scanning is started when a key data output command is executed.

The INT pin (pin 35) goes high when key scanning has ended.

The INT pin goes low when the LOAD pin (pin 28) goes high.

Figure 3-1. Timing Chart of Key Scanning



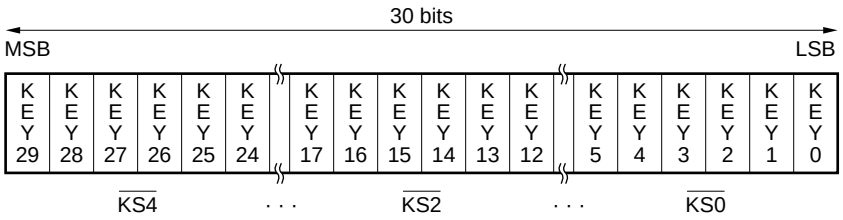
Note The value in brackets ( ) is when “display data input + key data output” is executed.

3.2 Data Configuration

The data output by the key data output command consists of 30 bits.

The contents of the output data are as shown below.

Figure 3-2. Configuration of Output Data (Key Data Output)



The status of the output data can be identified by the data of each bit as shown below.

Data	Status
0	Key off
1	Key on

4. LCD DISPLAY FUNCTION

4.1 Configuration of LCD Data Segment and LCD Panel Display Data

The segments consisting of LCD0 through LCD24 pins and COM0 through COM2 pins correspond to the LCD panel display data as shown in the table below.

Table 4-1 Configuration of LCD Segment and **Table 4-2 Display Data Table** correspond to each other. Any LCD display setting can be performed based on these tables.

Table 4-1. Configuration of LCD Segment

Common Pin (Pin No.) / Segment Pin (Pin No.)	COM0 (62)	COM1 (63)	COM2 (64)
LCD0 (25)	B4	A0	B0
LCD1 (24)	A3	A1	B1
LCD2 (23)	A4	A2	B2
LCD3 (22)	B9	A5	B5
LCD4 (21)	A8	A6	B6
LCD5 (20)	A9	A7	B7
LCD6 (19)	B14	A10	B10
LCD7 (18)	A13	A11	B11
LCD8 (17)	A14	A12	B12
LCD9 (16)	B19	A15	B15
LCD10 (15)	A18	A16	B16
LCD11 (14)	A19	A17	B17
LCD12 (13)	B24	A20	B20
LCD13 (12)	A23	A21	B21
LCD14 (11)	A24	A22	B22
LCD15 (10)	B33	B38	B28
LCD16 (9)	B29	A25	B25
LCD17 (8)	A28	A26	B26
LCD18 (7)	A29	A27	B27
LCD19 (6)	B34	A30	B30
LCD20 (5)	A33	A31	B31
LCD21 (4)	A34	A32	B32
LCD22 (3)	B39	A35	B35
LCD23 (2)	A38	A36	B36
LCD24 (1)	A39	A37	B37

Table 4-2. Display Data Table

Segment / Data Name	A	B
D40	A0	B0
D39	A1	B1
D38	A2	B2
D37	A3	B3 Note
D36	A4	B4
D35	A5	B5
D34	A6	B6
D33	A7	B7
D32	A8	B8 Note
D31	A9	B9
D30	A10	B10
D29	A11	B11
D28	A12	B12
D27	A13	B13 Note
D26	A14	B14
D25	A15	B15
D24	A16	B16
D23	A17	B17
D22	A18	B18 Note
D21	A19	B19
D20	A20	B20
D19	A21	B21
D18	A22	B22
D17	A23	B23 Note
D16	A24	B24
D15	A25	B25
D14	A26	B26
D13	A27	B27
D12	A28	B28
D11	A29	B29
D10	A30	B30

Segment / Data Name	A	B
D9	A31	B31
D8	A32	B32
D7	A33	B33
D6	A34	B34
D5	A35	B35
D4	A36	B36
D3	A37	B37
D2	A38	B38
D1	A39	B39

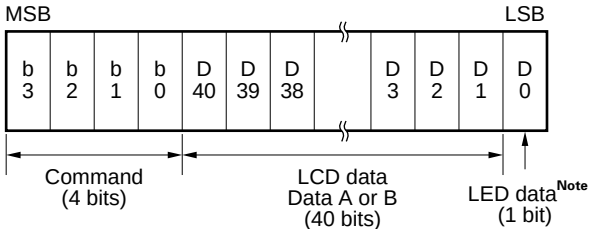
Note The data of segments B3, B8, B13, B18, and B23 are invalid. Do not input anything for these data.

4.2 LCD Display Data Configuration

LCD display data is divided into two parts, A and B, for transmission (refer to **Table 4-2 Display Data Table**).

The data consists of a command (4 bits), LCD data (40 bits), and LED data (1 bit), or a total of 45 bits (only when data A is transmitted. Data B consists of 44 bits, excluding LED data (1 bit)).

Figure 4-1. Configuration of Input Data for LCD Display



Note D0 (= LED data) is necessary only when data A is transmitted.

The status of the data can be identified by the data of each bit (0 or 1) as shown below.

Data	Status
0	Extinguishers
1	Lights

The last 4 bits of the input data is read at the rising edge of the LOAD pin (pin 28) as a command, and the previous data is displayed on the LCD when display data input is identified.

When a low level is input to the BLANK pin (pin 42), the LCD display is turned ON (the LED also lights when data A is transmitted). When a high level is input to the BLANK pin, the LCD display is turned OFF (refer to **5.2 Serial Data Output**).

Setting of the BLANK pin does not affect any operations other than the LCD display.

The LCD display data is extinguished in the initial status (even if the BLANK pin is low level).

The configuration of the LCD display data commands (4 bits of MSB) is shown below.

Table 4-3. Serial Data I/O Commands

Command				Operation
b3	b2	b1	b0	
0	0	1	0	Inputs display data (data A)
0	0	1	1	Inputs display data (data B)
0	1	0	×	Outputs key data
0	1	1	0	Inputs display data (A) + outputs key data
0	1	1	1	Inputs display data (B) + outputs key data
1	1	0	×	Outputs key data
1	1	1	×	Outputs key data
Others				Setting prohibited

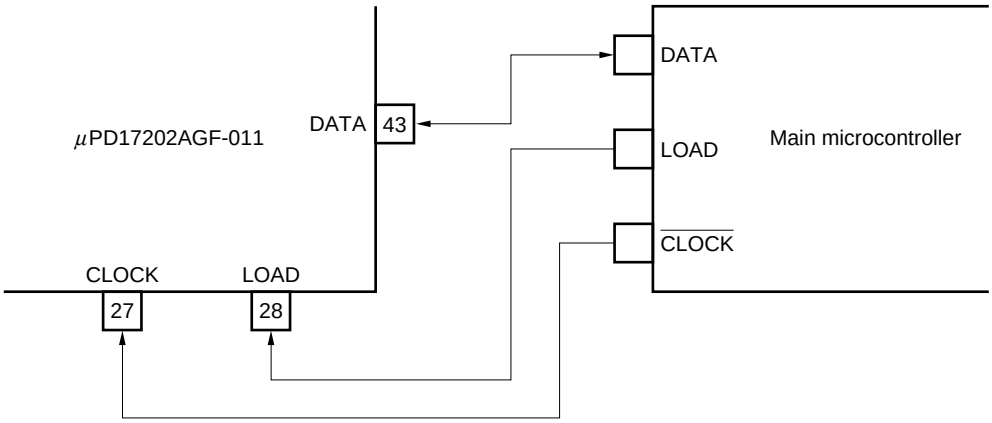
×: Undefined

5. SERIAL DATA COMMUNICATION

The μPD17202AGF-011 inputs or outputs data from or to the main microcontroller through 3-wire serial communication, using the CLOCK (pin 27), DATA (pin 43), and LOAD (pin 28) pins.

Figure 5-1 shows connection between the μPD17202AGF-011 and main microcontroller.

Figure 5-1. Connection between μPD17202AGF-011 and Main Microcontroller



5.1 Serial Data Input

The serial data is input in synchronization with the rising of the CLOCK pin (pin 27) in the input status (the initial status is “input”).

The last 4 bits read at the rising edge of the LOAD pin (pin 28) are identified and processed as a command.

Figure 5-2 shows the timing chart of serial data input.

Table 5-1 lists the serial data I/O commands.

Figure 5-2. Timing Chart of Serial Data Input

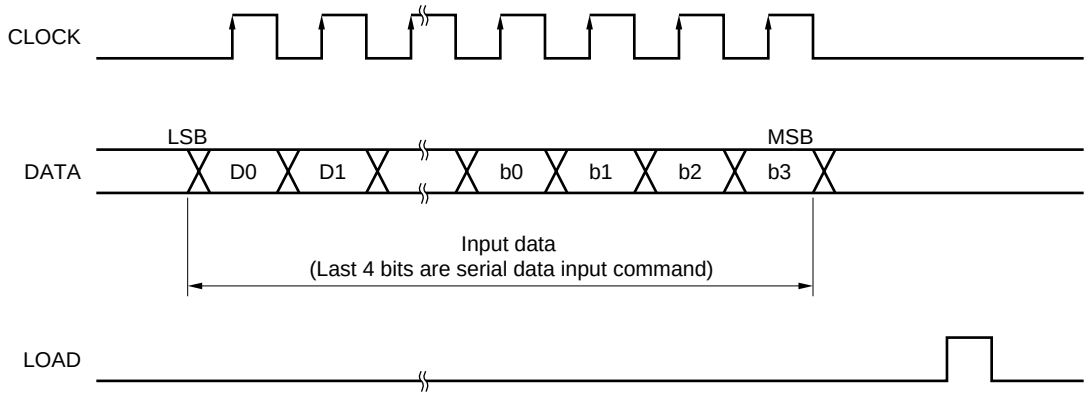


Table 5-1. Serial Data I/O Commands

Command				Operation
b3	b2	b1	b0	
0	0	1	0	Inputs display data (data A)
0	0	1	1	Inputs display data (data B)
0	1	0	×	Outputs key data
0	1	1	0	Inputs display data (A) + outputs key data
0	1	1	1	Inputs display data (B) + outputs key data
1	1	0	×	Outputs key data
1	1	1	×	Outputs key data
Others				Setting prohibited

×: Undefined

Remarks 1. For the data configuration of display data input, refer to **4. LCD DISPLAY FUNCTION**.

2. For the data configuration of key data output, refer to **3. KEY SCAN**.

3. Execute display data input before key data output.

4. If a pulse is input to the LOAD pin without display data input, the device does not operate.

5. The device does not operate when data other than an I/O command is input.

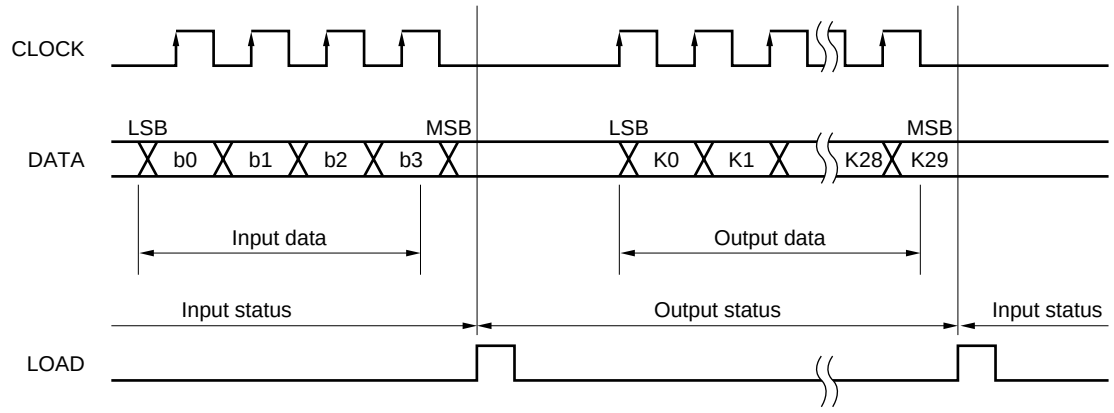
5.2 Serial Data Output

Serial data is output in synchronization with the rising of the CLOCK pin (pin 27) in the output status (the output status is established only when the key data output command is executed).

Serial data is output in the following procedure. Figure 5-3 shows the timing chart of serial data output.

<1> Input a key data output command.
<2> Input a pulse to the LOAD pin (pin 28) (the output status is established when this pin goes high).
<3> Input the clock (data is output in synchronization with the rising of the clock).
<4> Input a pulse to the LOAD pin (the input status is established when this pin goes high).

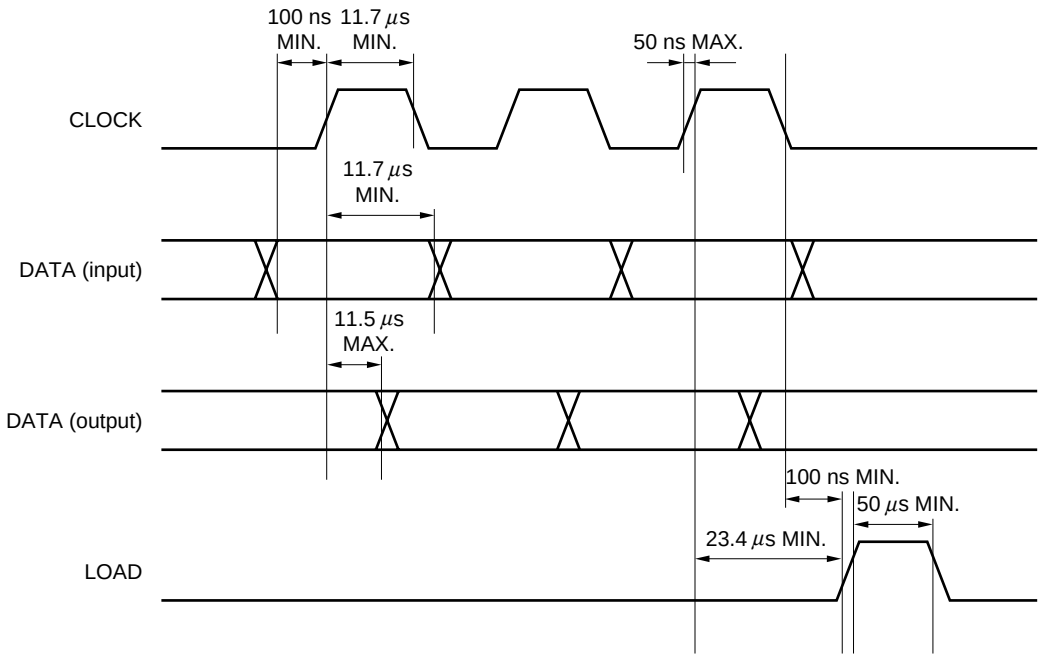
Figure 5-3. Timing Chart of Serial Data Output



5.3 Timing Chart of Serial Data Communication

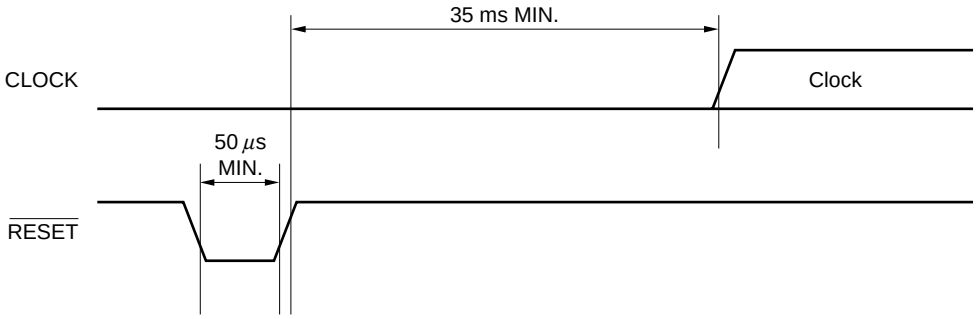
The I/O timing charts of the respective pins during serial data communication are shown below.

(1) Serial data I/O

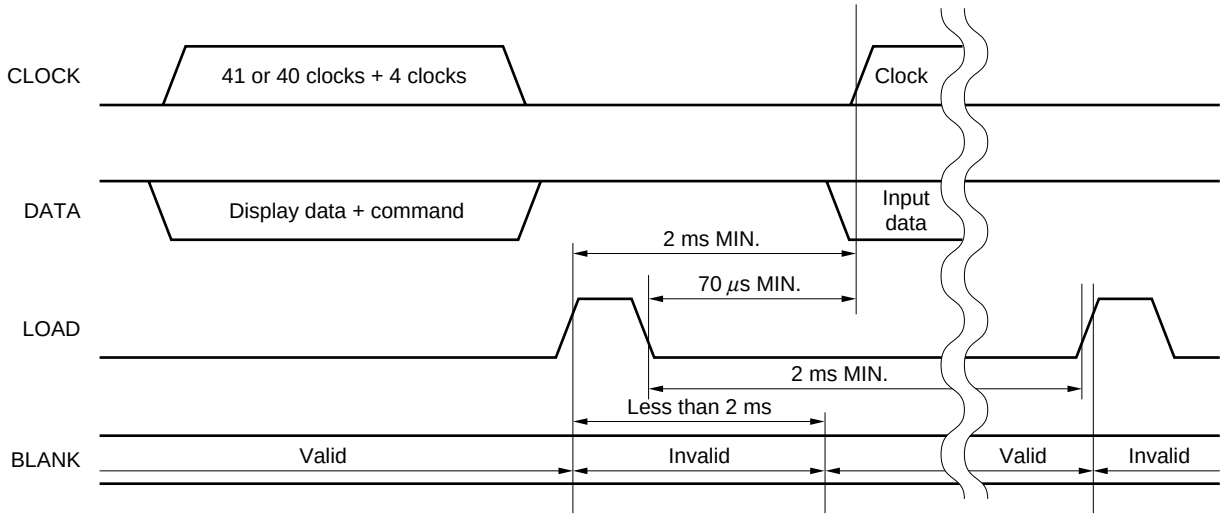


Remark Maximum clock frequency: 43 kHz

(2) On reset execution



(3) On execution of display data input

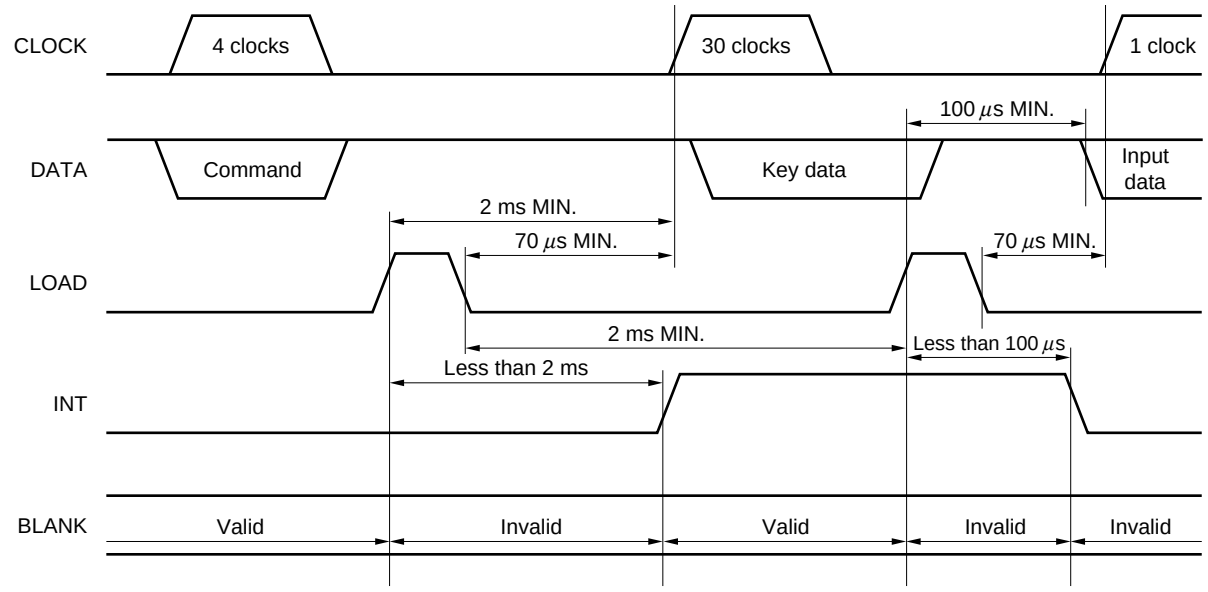


BLANK pin

Valid : The device operates within 50 μs after the value of the BLANK pin has been changed. If the clock is input to the CLOCK pin, however, the higher the clock frequency, the slower the operation (example: operates within 1 ms at 43 kHz).

Invalid : The device does not operate even if the value of the BLANK pin has been changed. If the value of the pin is changed during this period, the device operates after the pin value has become valid.

(4) On execution of key data output

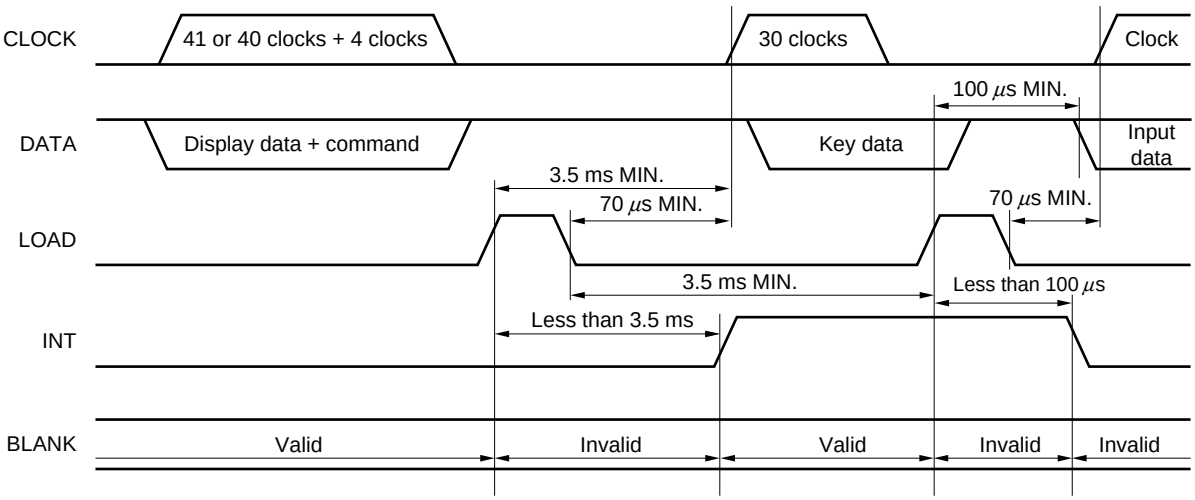


BLANK pin

Valid : The device operates within 50 μs after the value of the BLANK pin has been changed. If the clock is input to the CLOCK pin, however, the higher the clock frequency, the slower the operation (example: operates within 1 ms at 43 kHz).

Invalid : The device does not operate even if the value of the BLANK pin has been changed. If the value of the pin is changed during this period, the device operates after the pin value has become valid.

(5) On execution of display data input + key data

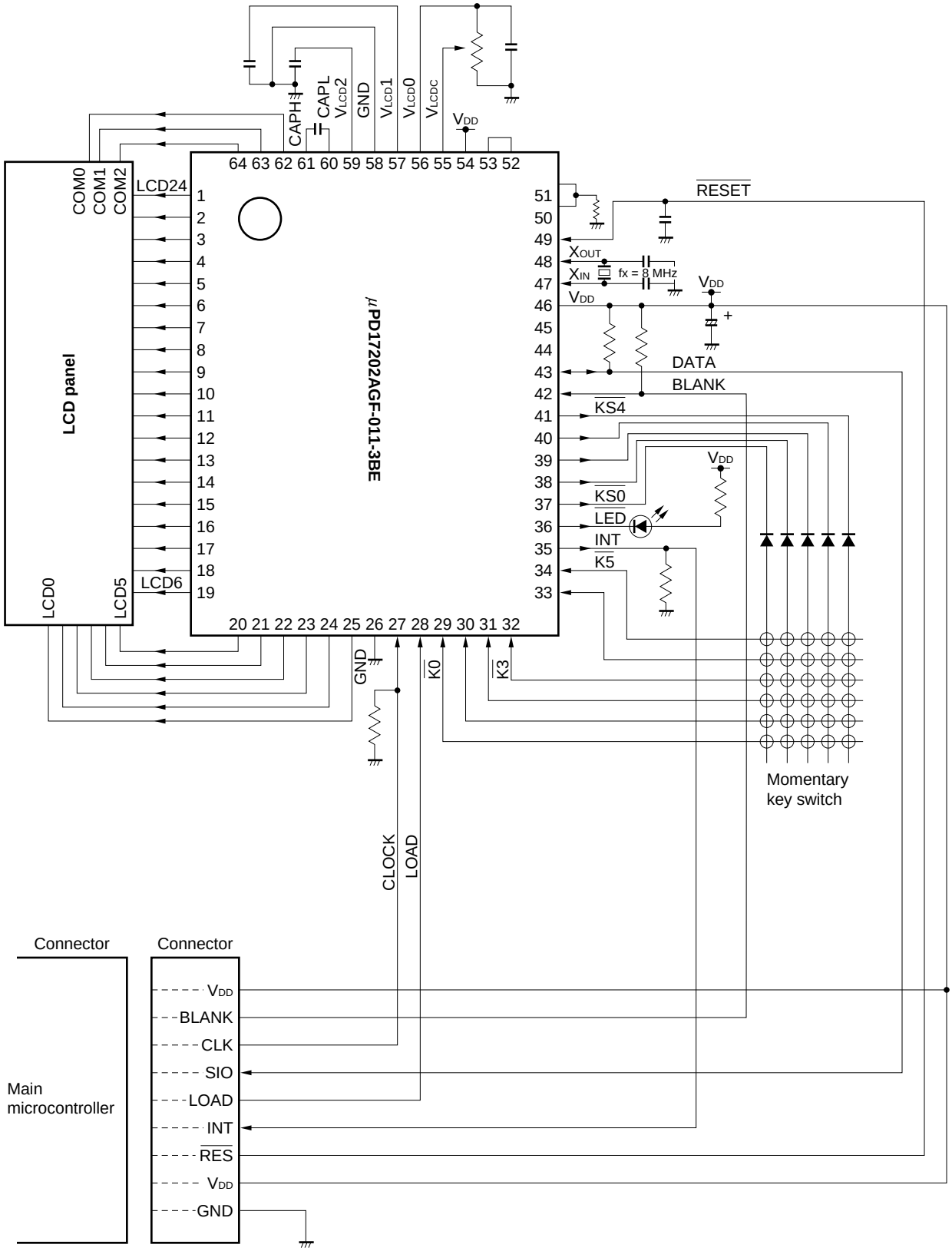


BLANK pin

Valid : The device operates within 50 μs after the value of the BLANK pin has been changed. If the clock is input to the CLOCK pin, however, the higher the clock frequency, the slower the operation (example: operates within 1 ms at 43 kHz).

Invalid : The device does not operate even if the value of the BLANK pin has been changed. If the value of the pin is changed during this period, the device operates after the pin value has become valid.

6. APPLICATION CIRCUIT EXAMPLE



7. ELECTRICAL SPECIFICATIONS (preliminary)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	REM pin	Peak	–30	mA
			r.m.s value	–20	mA
		1 pin (other than REM pin)	Peak	–7.5	mA
			r.m.s value	–5.0	mA
		All pins (except REM pin)	Peak	–22.5	mA
			r.m.s value	–15.0	mA
Low-level output current	I_{OL}	1 pin	Peak	7.5	mA
			r.m.s value	5.0	mA
		All pins	Peak	30	mA
			r.m.s value	20	mA
Operating temperature	T_A			—20 to +75	°C
Storage temperature	T_{stg}			–40 to +125	°C

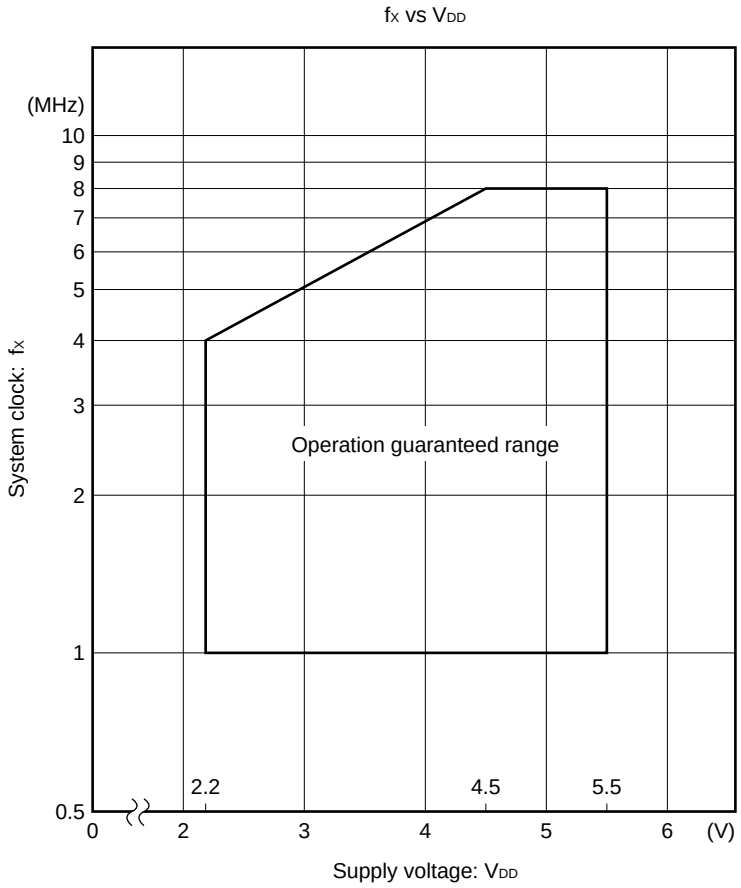
Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be affected. The absolute maximum ratings, therefore, define the values exceeding which the product may be physically damaged. Be sure to use the product without ever exceeding these values.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

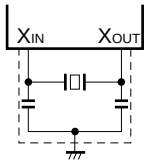
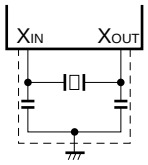
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	INT and $\overline{\text{RESET}}$ pins			10	pF
	C_{PIN}	Other than INT and $\overline{\text{RESET}}$ pins			10	pF

Recommended Operation Range (T_A = –20 to +75 ˚C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD0}	Where system clock is f_X = 4 MHz	2.2	3.0	5.5	V
	V_{DD1}	Where system clock is f_X = 8 MHz	4.5	5.0	5.5	V
System clock oscillation frequency	f_X		1.0	4.0	8.0	MHz



System Clock Oscillation Circuit Characteristics (T_A = –20 to +75 °C, V_{DD} = 2.2 to 5.5 V)

Oscillator	Recommended Constants	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator **Note 1**		Oscillation frequency (f_X) **Note 2**		1.0	4.0	8.0	MHz
		Oscillation stabilization time **Note 3**	After V_{DD} has reached MIN. value of oscillation voltage range			4	ms
Crystal resonator **Note 1**		Oscillation frequency (f_X) **Note 2**		1.0	4.0	8.0	MHz
		Oscillation stabilization time **Note 3**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms

Notes 1. Use of the ceramic resonator and crystal resonator shown on the next page is recommended.

2. The oscillation frequency only indicates the characteristics of the oscillation circuit. For the instruction execution time, refer to **Recommended Operation Range**.

3. The oscillation stabilization time is the time required for oscillation to stabilize after V_{DD} application or release of the STOP mode.

Caution When using the system clock oscillation circuit, wire the portion indicated by the dotted lines in the above figures to avoid adverse influence from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines. Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as GND. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

Recommended Oscillator

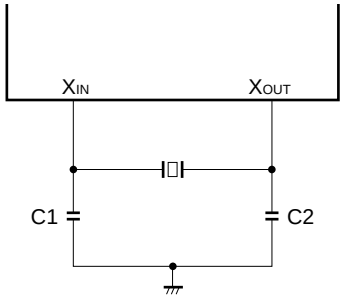
Ceramic resonator

Manufacturer	Part Number	External Capacitance (pF)		Oscillation Voltage Range (V)		Remark
		C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSA3.58MG	30	30	2.0	6.0	
	CSA4.00MG	30	30	2.0	6.0	
	CSA4.19MG	30	30	2.0	6.0	
	CST3.58MGW	Unnec-essary	Unnec-essary	2.0	6.0	Capacitor-contained type
	CST4.00MGW			2.0	6.0	
	CST4.19MGW			2.0	6.0	
Kyocera Corp.	KBR3.58MS	33	33	2.0	6.0	
	KBR4.0MS	33	33	2.0	6.0	
	KRB4.19MS	33	33	2.0	6.0	
Toko Ceramic Co. Ltd.	CRHF4.00	18	18	2.0	6.0	
Daishinku Corp.	PRS0400BCSAN	39	33	2.0	6.0	

Crystal resonator

Manufacturer	Frequency (MHz)	Retainer	External Capacitance (pF)		Oscillation Voltage Range (V)		Remark
			C1	C2	MIN.	MAX.	
Kinseki Corp.	4.0	HC-49U-S	22	22	2.0	6.0	

External Circuit Example



DC Characteristics (V_{DD} = 3 V, T_A = –20 to +75 °C, f_X = 4 MHz)

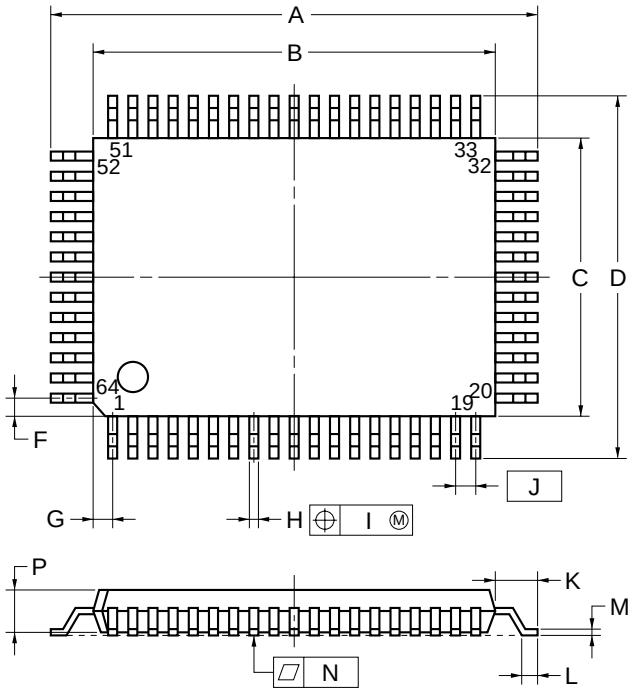
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-voltage detection voltage	V_{DET}	R = 2.2 MΩ		1.3	2.0	2.9	V
High-level input voltage	V_{IH1}	$\overline{RESET}$, INT pins		0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Other than $\overline{RESET}$, INT pins		0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	$\overline{RESET}$, INT pins		0		0.2 V_{DD}	V
	V_{IL2}	Other than $\overline{RESET}$, INT pins		0		0.3 V_{DD}	V
High-level input current	I_{IH1}	INT pin	$V_{IH} = V_{DD}$			0.2	μA
	I_{IH2}	$\overline{RESET}$ pin	$V_{IH} = V_{DD}$			0.2	μA
	I_{IH3}	P0A through P0D pins	$V_{IH} = V_{DD}$			0.2	μA
Low-level input current	I_{IL1}	INT pin	V_{IL} = 0 V			–0.2	μA
	I_{IL2}	$\overline{RESET}$ pin	V_{IL} = 0 V w/o pull-up resistor			–0.2	μA
	I_{IL3}		V_{IL} = 0 V w/pull-up resistor	–30	–60	–120	μA
	I_{IL4}	P0A, P0B pins	V_{IL} = 0 V w/o pull-up resistor			–0.2	μA
	I_{IL5}		V_{IL} = 0 V w/pull-up resistor	–8	–15	–30	μA
	I_{IL6}	P0C, P0D pins	V_{IL} = 0 V			–0.2	μA
High-level output current	I_{OH1}	P0A, P0B pins	$V_{OH} = V_{DD}$ – 0.3 V	–0.6	–2.0	–4.0	mA
	I_{OH2}	REM pin	$V_{OH} = V_{DD}$ – 2.0 V	–7.0	–15.0	–25.0	mA
	I_{OH3}	$\overline{LED}$ pin	$V_{OH} = V_{DD}$ – 0.3 V	–0.3	–1.0	–2.0	mA
Low-level output current	I_{OL1}	P0A, P0B pins	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL2}	P0C, P0D pins	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL3}	REM pin	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
	I_{OL4}	$\overline{LED}$, $\overline{WDOUT}$ pins	V_{OL} = 0.3 V	0.5	1.5	2.5	mA
Supply current	I_{DD1}	Operating mode			0.6	1.5	mA
	I_{DD2}	HALT mode			0.5	1.5	mA
V_{LCDC} voltage	V_{LCDC}	V_{DD} = 3 V, T_A = 25 °C, R1 = R2 = 1 MΩ		0.5	0.6	0.7	V
LCD output voltage variable range	V_{LCD0}	External variable resistor (0 to 2.2 MΩ)		0.8		1.8	V
Doubler output voltage	V_{LCD1}	C1 to C4 = 0.47 μF		1.9 V_{LCD0}	2 V_{LCD0}		V
Tripler output voltage	V_{LCD2}	C1 to C4 = 0.47 μF		2.85 V_{LCD0}	3 V_{LCD0}		V
Common output current	I_{COM}	V_{DS} = 0.2 V		30			μA
Segment output current	I_{LCD}	V_{DS} = 0.2 V		5			μA

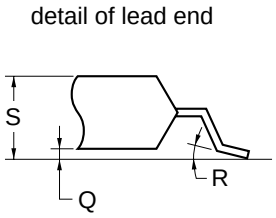
AC Characteristics (T_A = –20 to +75 °C, V_{DD} = 3 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
INT high-, low-level widths	t_{IOH}		50			μs
	t_{IOL}		50			μs
$\overline{RESET}$ low-level width	t_{RSL}		50			μs

8. PACKAGE DRAWINGS

64 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S64GF-100-3B8, 3BE-3

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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J96. 8

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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