DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD16879

MONOLITHIC QUAD H BRIDGE DRIVER CIRCUIT

The μPD16879 is a monolithic quad H bridge driver IC that employs a CMOS control circuit and a MOSFET output circuit. Because it uses MOSFETs in its output stage, this driver IC consumes less power than conventional driver ICs that use bipolar transistors.

Because the μPD16879 controls a motor by inputting serial data, its package has been shrunk and the number of pins reduced. As a result, the performance of the application set can be improved and the size of the set has been reduced.

This IC employs a current-controlled 64-step micro step driving method that drives stepper motor with low vibration.

The μPD16879 is a housed in a 38-pin shrink SOP to contribute to the miniaturization of application set.

This IC can simultaneously drive two stepper motors and is ideal for the mechanisms of camcorders.

FEATURES

- Four H bridge circuits employing power MOS FETs
- Current-controlled 64-step micro step driving
- Motor control by serial data (8 bits × 13 bytes)
  PWM-frequency, output current and number of output pulse can be setting by serial data.
- 3-V power supply.
  Minimum operating voltage: 2.7 V
- Low consumption current.
  V_{DD} pin current (operating mode) : 3 mA (MAX.)
- Power save circuit bult in.
  V_{DD} pin current (power save mode) : 100 μA (MAX.) f_{CLK}: OFF state
  V_{DD} pin current (power save mode) : 300 μA (MAX.) f_{CLK}: 4.5 MHz input
- 38-pin shrink SOP (7.62 mm (300))

ORDERING INFORMATION

Part Number	Package
μPD16879GS-BGG	38-pin plastic shrink SOP (7.62 mm (300))

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

When mounted on a glass epoxy board (100 mm × 100 mm × 1 mm, 15% copper foil)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	Control part	–0.5 to +6.0	V
	V_M	Output part	–0.5 to +11.2	V
Input voltage	V_{IN}		–0.5 to V_{DD} + 0.5	V
Reference voltage	V_{REF}	External input	0.5	V
H bridge drive current	$I_{M(DC)}$	DC	±0.15	A/ch
	$I_{M(pulse)}$	PW < 10 ms, Duty < 5 %	±0.3	A/ch
Power consumption	P_T		1.0	W
Peak junction temperature	$T_{CH(MAX)}$		150	°C
Storage temperature	T_{stg}		–55 ~ +150	°C

RECOMMENDED OPERATING RANGE (T_A = +25°C)

When mounted on a glass epoxy board (100 mm × 100 mm × 1 mm, 15% copper foil)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	Control part	2.7		5.5	V
	V_M	Output part	4.0		11	V
Input voltage	V_{IN}		0		V_{DD}	V
Reference voltage	V_{REF}	External input	225	250	275	mV
EXP pin input voltage	V_{EXPIN}				V_{DD}	V
EXP pin input current	I_{EXPIN}				100	μA
H bridge drive current	$I_{M(DC)}$	DC	–0.1		+0.1	A/ch
	$I_{M(pulse)}$	P_W < 10 ms, Duty < 5%	–0.2		+0.2	A/ch
Clock frequency (OSC_{IN})	f_{CLK}	C_{OSC} = 68 pF, V_{REF} = 250 mV	3.9	4.5	6.0	MHz
Clock frequency amplitude	V_{fCLK}		0.7 × V_{DD}		V_{DD}	V
Serial clock frequency	f_{SCLK}				5.0	MHz
Video sync signal width	$PW_{(VD)}$	f_{CLK} = 4.5 MHz	250			ns
LATCH signal wait time	$t_{(VD-LATCH)}$	Refer to Fig. 1	400			ns
SCLK wait time	$t_{(SCLK-LATCH)}$		400			ns
SDATA setup time	t_{setup}		80			ns
SDATA hold time	t_{hold}		80			ns
Reset signal pulse width	t_{RST}		100			μs
Operating temperautre	T_A		–10		85	°C
Peak junction temperature	$T_{CH(MAX)}$				125	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, T_A = 25°C, V_{DD} = 3 V, V_M = 5.4 V, f_{CLK} = 4.5 MHz, C_{OSC} = 68 pF, C_{FIL} = 1000 pF, V_{REF} = 250 mV, EVR = 100 mV (10000))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Off state V_M pin current	$I_{MO(RESET)}$	No load, Reset period			1.0	μA
Operating state V_{DD} pin current	I_{DD}	Output open			3.0	mA
V_{DD} pin current	$I_{DD(RESET)}$	Reset period			100	μA
Power save state V_{DD} pin current	$I_{DD(PS)1}$	t_{CLK} = off			100	μA
	$I_{DD(PS)2}$	f_{CLK} = 4.5 MHZ			300	μA
High level input voltage	V_{IH}	LATCH, SCLK, SDATA, V_D, $\overline{V_D}$ RESET, OSC_{IN}, V_{REFsel}	0.7 × V_{DD}			V
Low level input voltage	V_{IL}				0.3 × V_{DD}	V
Input hysteresis vosltage	V_H			0.3		V
Monitor output voltage 1 (EXTOUT α, β)	$V_{OM\alpha(H)}$ $V_{OM\beta(H)}$	4th byte	0.9 × V_{DD}			V
	$V_{OM\alpha(L)}$ $V_{OM\beta(L)}$		–0.3		0.1 × V_{DD}	V
Monitor output voltage 2 (EXP 0,1 open drain)	$V_{OEXP(H)}$	Pull up (V_{DD})	0.9 × V_{DD}			V
	$V_{OEXP(L)}$	I_{OEXP} = 100 μA			0.1 × V_{DD}	V
High level input current	I_{IH}	V_{IN} = V_{DD}			1.0	μA
Low level input current	I_{IL}	V_{IN} = 0	–1.0			μA
Reset pin high level input current	$I_{IH(RST)}$	V_{RST} = V_{DD}			1.0	μA
Reset pin low level input current	$I_{IL(RST)}$	V_{RST} = 0	–1.0			μA
H bridge ON resistance	R_{ON}	I_M = 100 mA, upper + lower			6.0	Ω
Chopping frequency Note 1	f_{OSC}		Refer to table 1 (TYP.)			kHz
Internal reference voltage	V_{REF}		225	250	275	mV
V_D delay time Note 2	Δt_{VD}				250	ns
Sin wave peak output current (reference value) Note 3	I_M	L = 15 mH/R = 70 Ω (1 kHz) R_S = 6.8 Ω, f_{OSC} = 72.58 kHz EVR = 220 mV (11100)		53		mA
FIL pin voltage Note 4	V_{EVR}	EVR = 200 mV (11010) V_{REF} = 250 mV external input	370	400	430	mV
FIL pin step voltage Note 4	$V_{EVRSTEP}$	Minimum step		20		mV
H bridge turn on time Note 5	t_{ONH}	I_M = 100 mA			2.0	μs
H bridge turn off time Note 5	t_{OFFH}				2.0	μs

Notes 1. When data are less than 7 (000111), PWM chopping doesn't do it, and output pulse doesn't occur. When data are beyong 49, PWM chopping frequency becomes a 225 kHz fixation.

2. By OSC_{IN} and V_D sync circuit

3. FB pin is monitored.

4. FIL pin is monitored. A voltage about twice that of the EVR value is output to the FIL pin.

5. 10% to 90% of the pulse peak value without filter capacitor (C_{FIL})

Fig 1. Delay Time of Serial Data

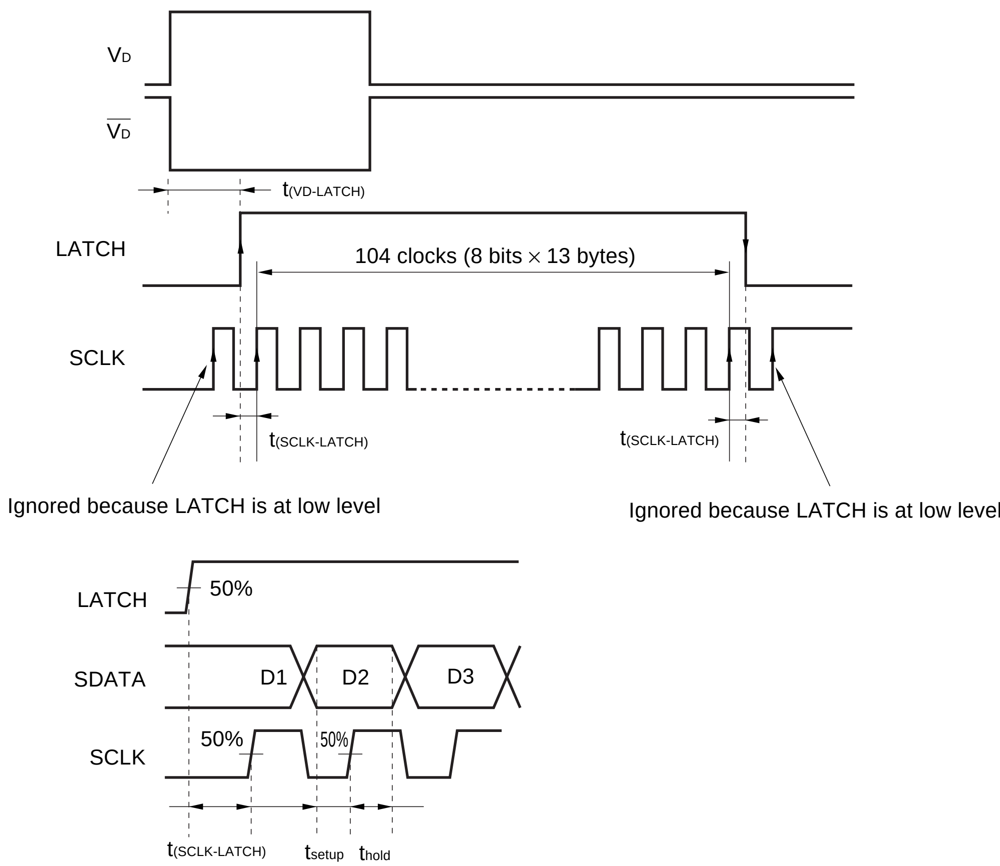


Table 1. Chopping Frequency (3rd byte D5 to D0 bit data, f_{CLK} = 4.5 MHz) Typical Value

Input data D5 to D0 bit	Chopping frequency (kHz)	Input data D5 to D0 bit	Chopping frequency (kHz)
001000	35.71	011101	132.35
001001	40.18	011110	132.35
001010	45.00	011111	140.63
001011	50.00	100000	140.63
001100	53.57	100001	150.00
001101	59.21	100010	150.00
001110	62.50	100011	160.71
001111	68.18	100100	160.71
010000	72.58	100101	160.71
010001	77.59	100110	173.08
010010	80.36	100111	173.08
010011	86.54	101000	173.08
010100	90.00	101001	187.50
010101	93.75	101010	187.50
010110	97.83	101011	187.50
010111	102.27	101100	204.55
011000	107.14	101101	204.55
011001	112.50	101110	204.55
011010	118.42	101111	204.55
011011	118.42	110000	225.00
011100	125.00		

Note When data are less than 7 (000111), PWM chopping doesn't do it, and output pulse doesn't occur.
When data are beyond 49, PWM chopping frequency becomes a 225 kHz fixation.

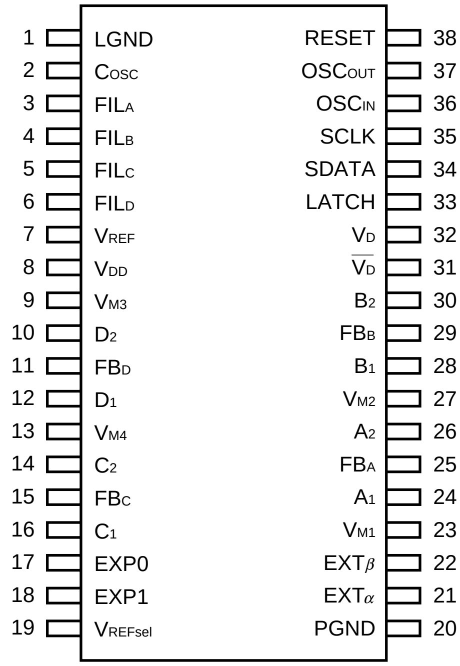
Table 2. Relation Between Rotation Angle, Phase Current, and Vector Quantity (64-DIVISION MICRO STEP)

(Value of μPD16879 for reference)

STEP	Rotation angle (θ)	A phase current			B phase current			Vector quantity
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	TYP.
θ 0	0	–	0	–	–	100	–	100
θ 1	5.6	2.5	9.8	17.0	–	100	–	100.48
θ 2	11.3	12.4	19.5	26.5	93.2	98.1	103	100
θ 3	16.9	22.1	29.1	36.1	90.7	95.7	100.7	100.02
θ 4	22.5	31.3	38.3	45.3	87.4	92.4	97.4	100.02
θ 5	28.1	40.1	47.1	54.1	83.2	88.2	93.2	99.99
θ 6	33.8	48.6	55.6	62.6	78.1	83.1	88.1	99.98
θ 7	39.4	58.4	63.4	68.4	72.3	77.3	82.3	99.97
θ 8	45	65.7	70.7	75.7	65.7	70.7	75.7	99.98
θ 9	50.6	72.3	77.3	82.3	58.4	63.4	68.4	99.97
θ 10	56.3	78.1	83.1	88.1	48.6	55.6	62.6	99.98
θ 11	61.9	83.2	88.2	93.2	40.1	47.1	54.1	99.99
θ 12	67.5	87.4	92.4	97.4	31.3	38.3	45.3	100.02
θ 13	73.1	90.7	95.7	100.7	22.1	29.1	36.1	100.02
θ 14	78.8	93.2	98.1	103	12.4	19.5	26.5	100
θ 15	84.4	–	100	–	2.5	9.8	17.0	100.48
θ 16	90	–	100	–	–	0	–	100

Remark These data do not indicate guaranteed values.

PIN CONFIGURATION



PIN FUNCTION

Package: 38-pin plastic shrink SOP

Pin	Pin name	Pin function
1	LGND	Control circuit GND pin
2	C_{OSC}	Chopping capacitor connection pin
3	FIL_A	α 1 ch filter capacitor connection pin
4	FIL_B	α 2 ch filter capacitor connection pin
5	FIL_C	β 1 ch filter capacitor connection pin
6	FIL_D	β 2 ch filter capacitor connection pin
7	V_{REF}	Reference voltage input pin (250 mV typ)[Note 1]
8	V_{DD}	Control circuit supply voltage input pin
9	V_{M3}	Output circuit supply voltage input pin
10	D_2	β 2 ch output pin
11	FB_D	β 2 ch sense resistor connection pin
12	D_1	β 2 ch output pin
13	V_{M4}	Output circuit supply voltage input pin
14	C_2	β 1 ch output pin
15	FB_C	β 1 ch sense resistor connection pin
16	C_1	β 1 ch ouptut pin
17	EXP0	External extension pin (open drain)
18	EXP1	External extension pin (open drain)
19	V_{REFsel}	Reference voltage select pin[Note 1]
20	PGND	Output circuit GND pin
21	EXT α	α ch logic circuit monitor pin
22	EXT β	β ch logic circuit monitor pin
23	V_{M1}	Output circuit supply voltage input pin
24	A_1	α 1 ch output pin
25	FB_A	α 1 ch sense resistor connection pin
26	A_2	α 1 ch output pin
27	V_{M2}	Output circuit supply voltage input pin
28	B_1	α 2 ch output pin
29	FB_B	α 2 ch sense resistor connection pin
30	B_2	α 2 ch output pin
31	$\overline{V_D}$	Video sync signal input pin[Note 2]
32	V_D	Video sync signal input pin[Note 2]
33	LATCH	LATCH signal input pin
34	SDATA	Serial data input pin
35	SCLK	Serial clock input pin (4.5 MHz typ)
36	OSC_{IN}	Original oscillation input pin (4.5 MHz typ)
37	OSC_{OUT}	Original oscillation output pin
38	RESET	Reset signal input pin

Remark Plural terminal (V_M) is not only 1 terminal and connect all terminals.

Notes 1. A standard voltage to use is chosen.

V_{REFsel}: High level using external input V_{REF}

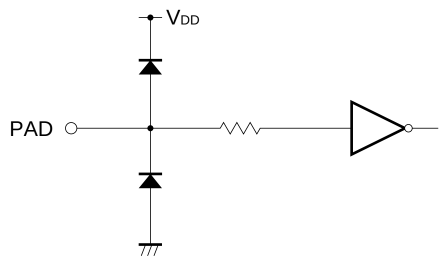
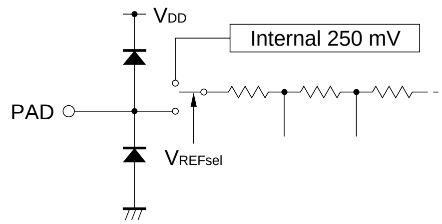
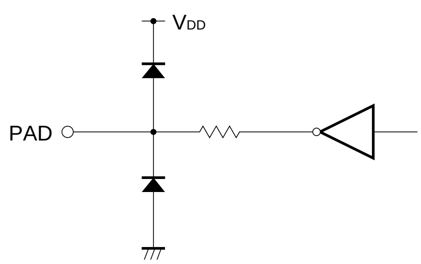
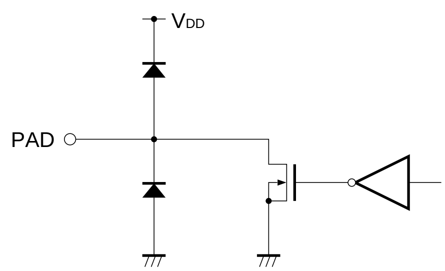
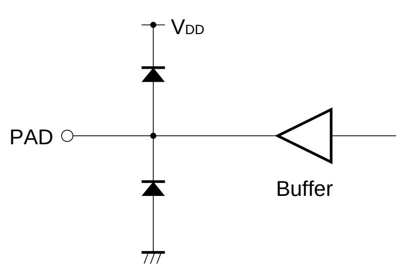
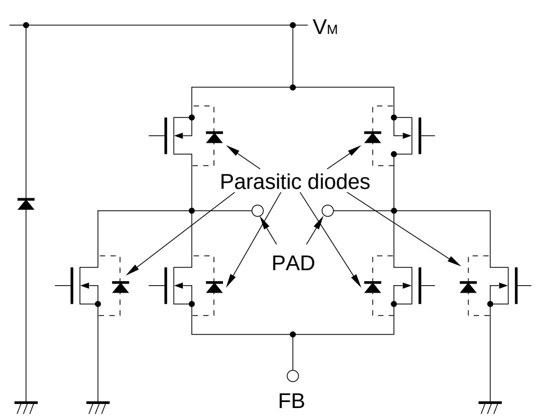
V_{REFsel}: Low level using internal reference voltage (V_{REF} pin fixed GND level)

2. Input the video sync singnal to V_D pin or $\overline{V_D}$ pin. A free terminal is to do the following treatment.

When input V_D: $\overline{V_D}$ pin connect to V_{DD} pin.

When input $\overline{V_D}$: V_D pin connect to GND pin.

I/O PIN EQUIVALENT CIRCUIT

<table>
<tr><th>Pin name</th><th>Equivalent circuit</th><th>Pin name</th><th>Equivalent circuit</th></tr>
<tr><td>V_D
$\overline{V_D}$
LATCH
SDATA
SCLK
OSC_{IN}
RESET
V_{REFsel}</td><td>
</td><td>V_{REF}</td><td>
</td></tr>
<tr><td>OSC_{OUT}
EXTα
EXTβ</td><td>
</td><td>EXP0
EXP1</td><td>
</td></tr>
<tr><td>FIL_A
FIL_B
FIL_C
FIL_D</td><td>
</td><td></td><td></td></tr>
<tr><td>A_1, A_2
B_1, B_2
C_1, C_2
D_1, D_2</td><td colspan="3">
</td></tr>
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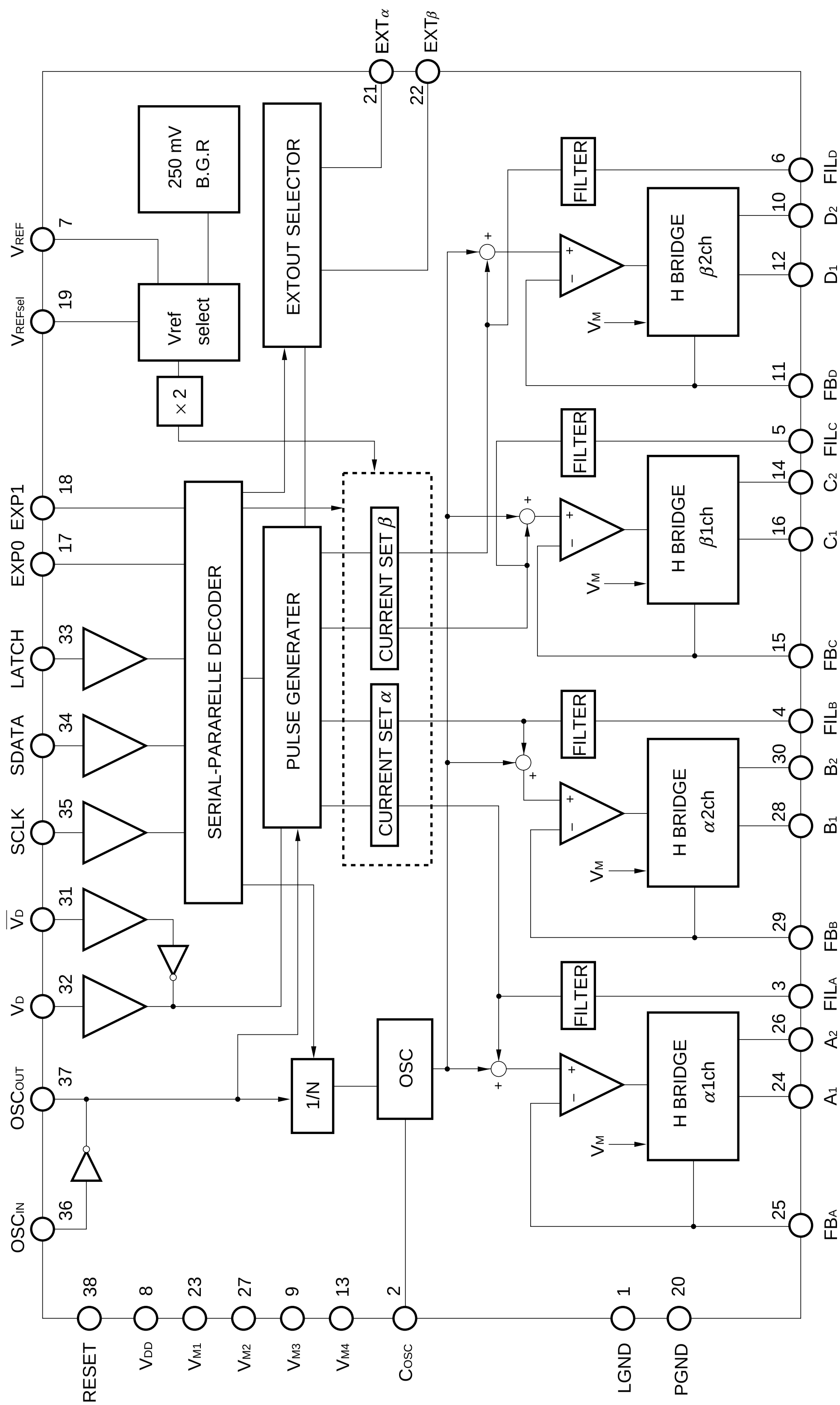
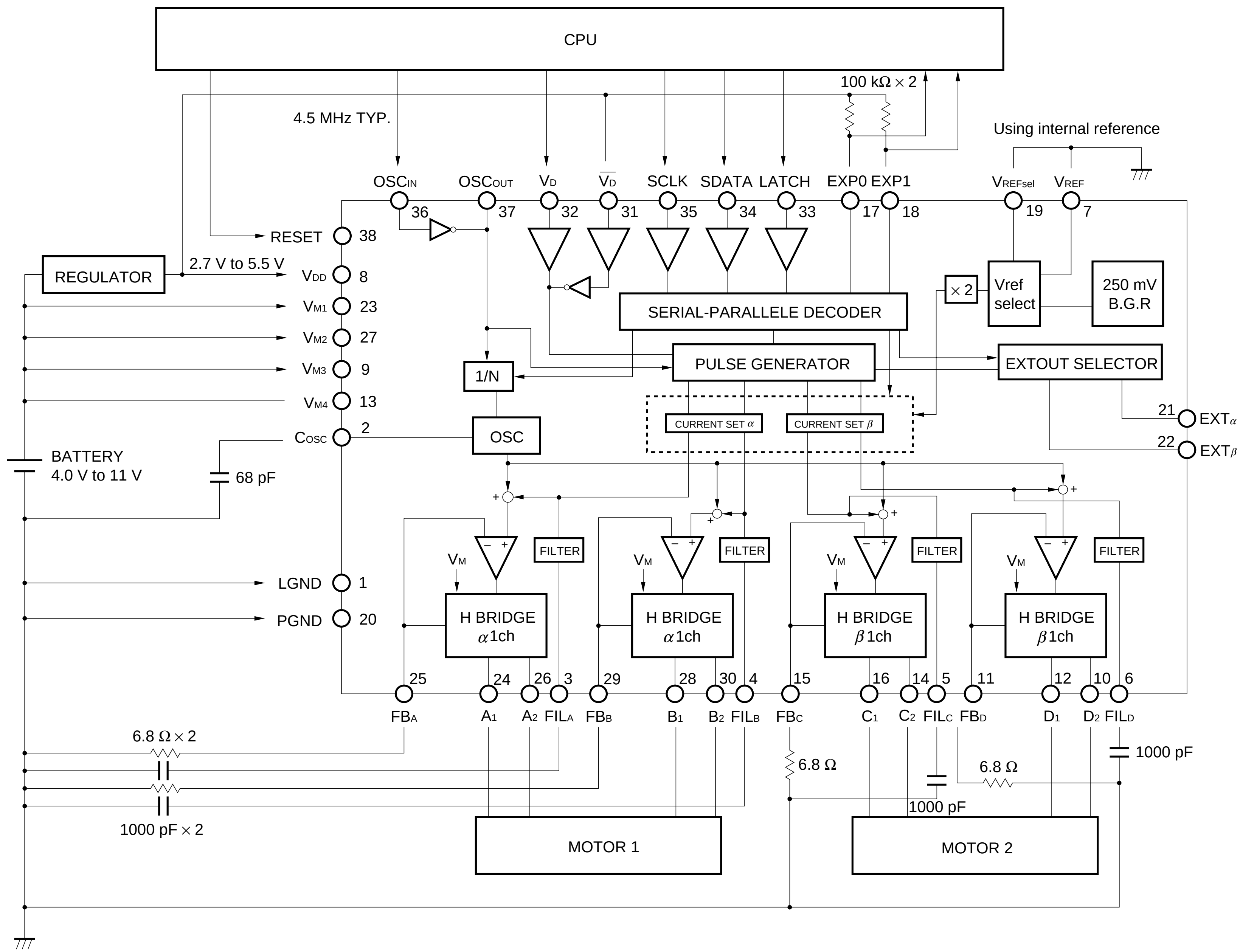
BLOCK DIAGRAM

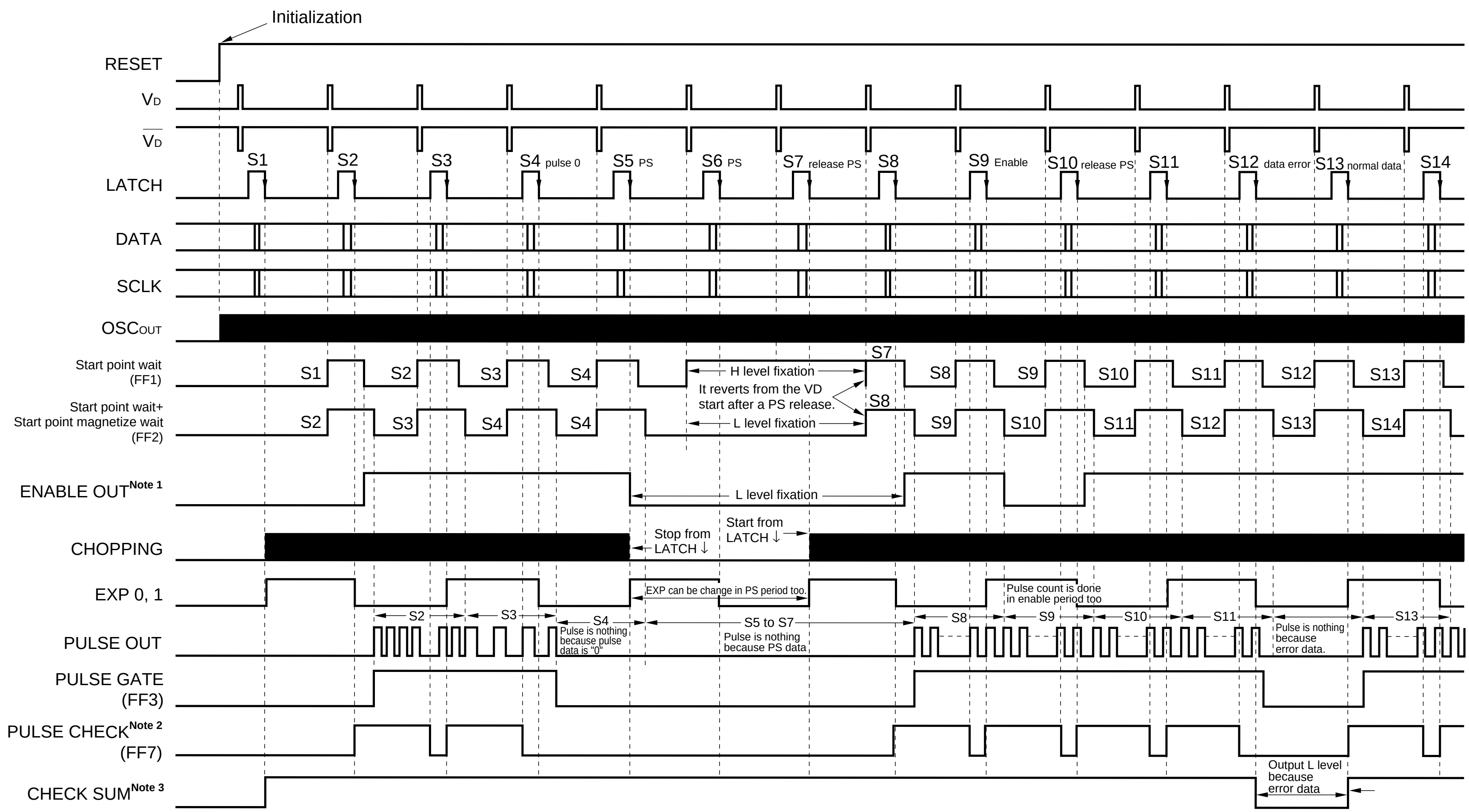


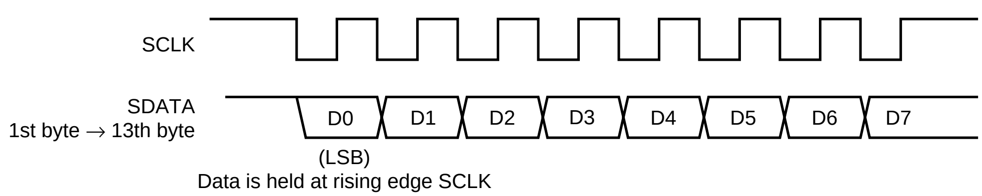
Remark Plural terminal (V_M) is not only 1 terminal and connect all terminals.

EXAMPLE OF STANDARD CONNECTION



TIMING CHART (1)



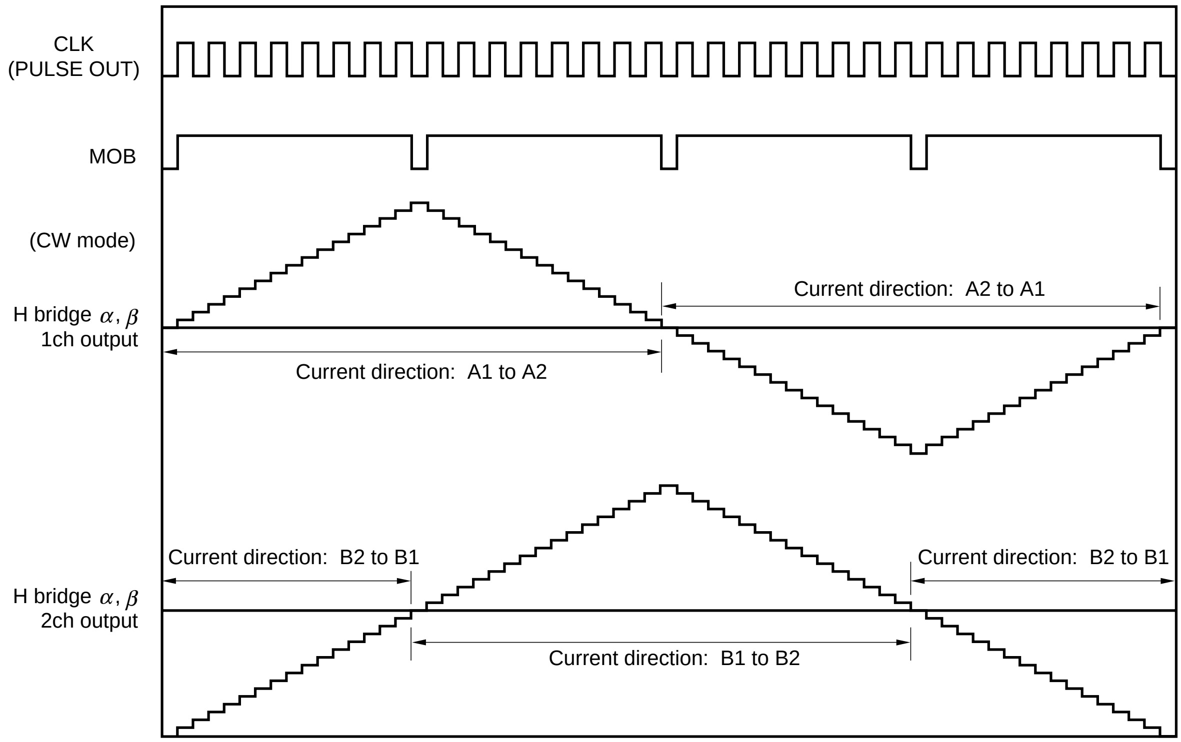


Notes 1. ENABLE is set at the falling edge of FF1 when the level changes from low to high, and at the falling edge of FF2 when the level changes from high to low.

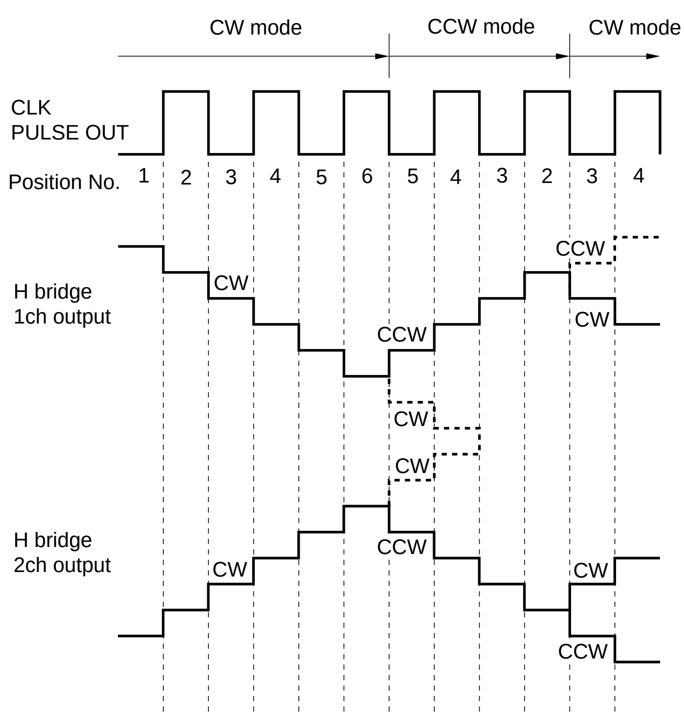
2. FF7 is an output signal that is used to check for the presence or absence of a pulse in the serial data, is updated at the falling edge of LATCH and reset once at the rising edge of LATCH. If CHECK SUM is other than "00h", FF7 goes low, inhibiting pulse output, even if a pulse is generated.

3. CHECK SUM output is updated at the falling edge of LATCH.

TIMING CHART (2)



(Expanded view)



Note CW mode : Position No is incremented.
CCW mode: Position No is decremented.

Remarks **1.** The current value of the actual wave is approximated to the value shown on the page 5.

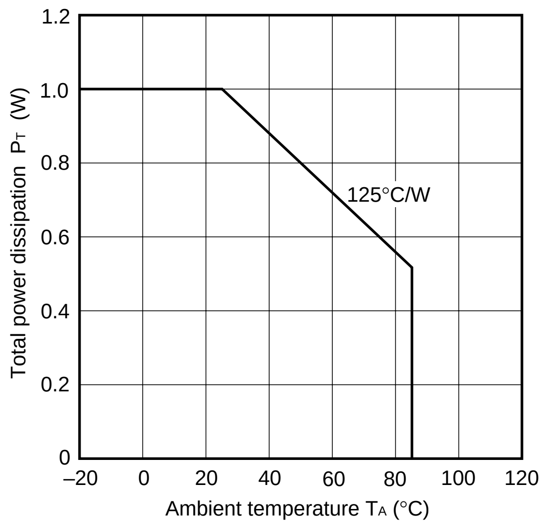
2. The C1, C2, D1, and D2 pins of β channel correspond to the A1, A2, B1, and B2 pins of α channel.

3. The CW mode is set if the D6 bit of the fifth and ninth bytes of the data is “0”.

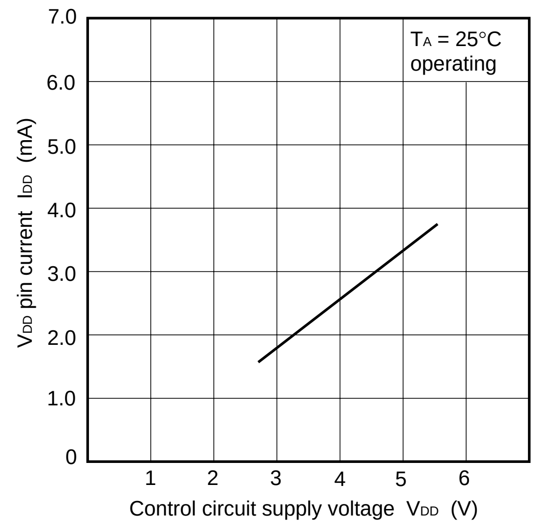
4. The CCW mode is set if the D6 bit of the fifth and ninth bytes of the data is “1”.

STANDARD CHARACTERISTICS CURVES

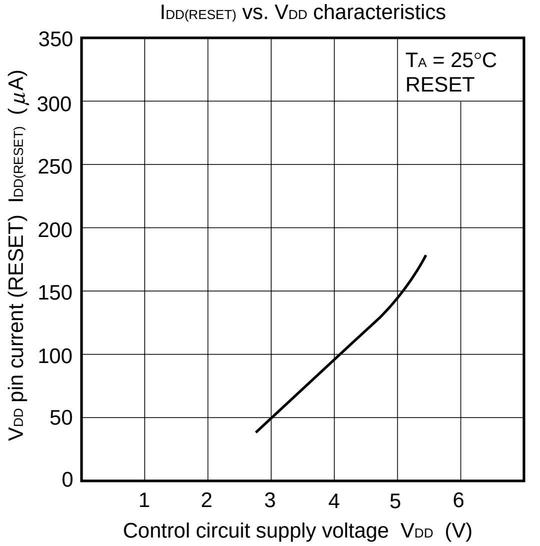
P_T vs. T_A characteristics



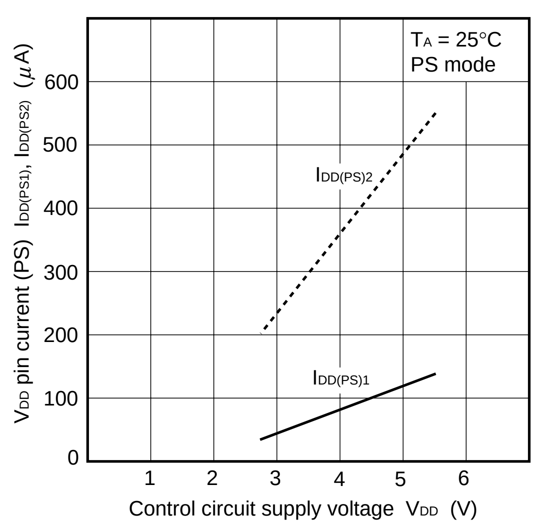
I_{DD} vs. V_{DD} characteristics



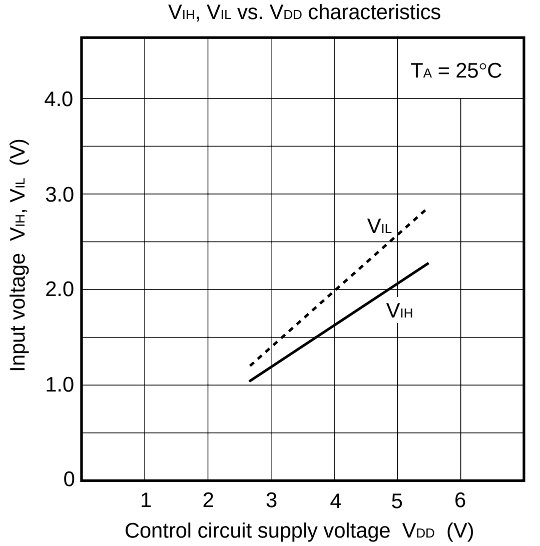
$I_{DD(RESET)}$ vs. V_{DD} characteristics



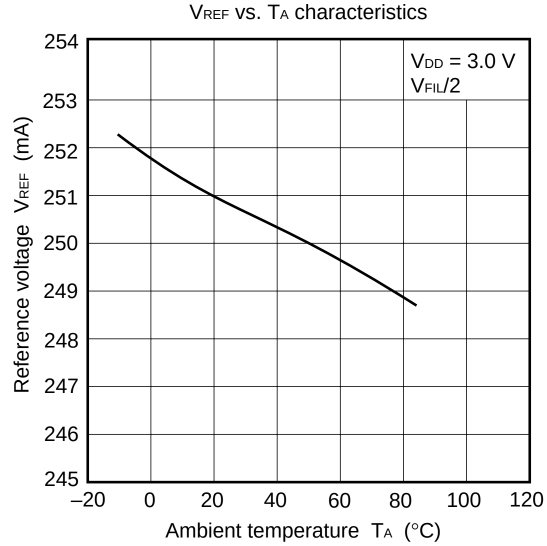
$I_{DD(PS)}$ vs. V_{DD} characteristics



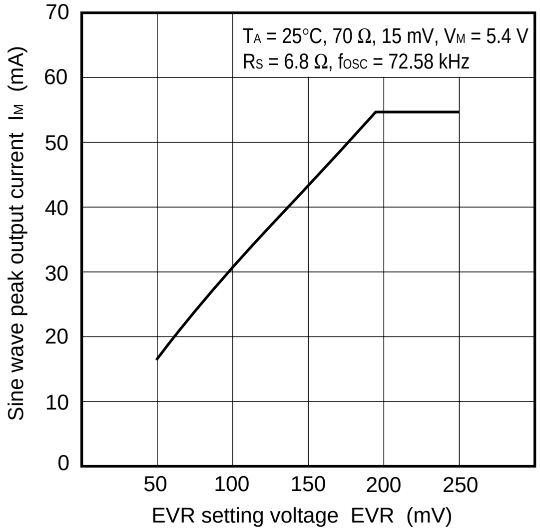
V_{IH}, V_{IL} vs. V_{DD} characteristics



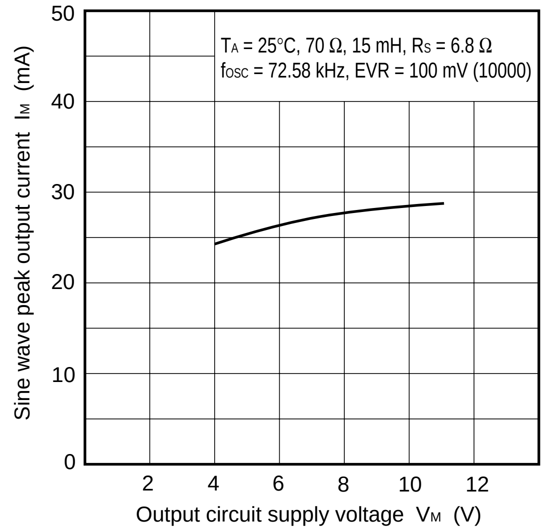
V_{REF} vs. T_A characteristics



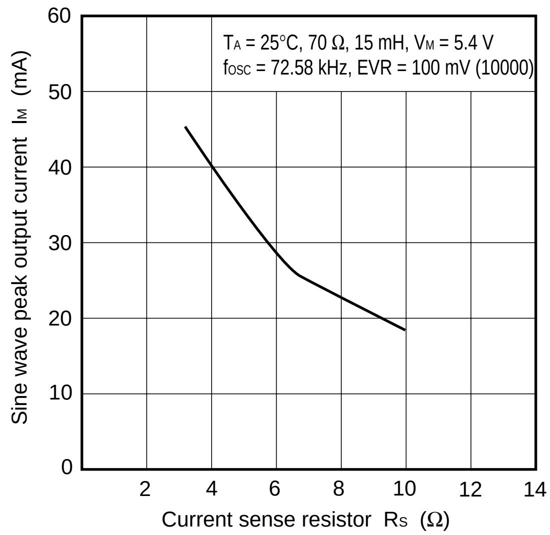
I_M vs. EVR characteristics



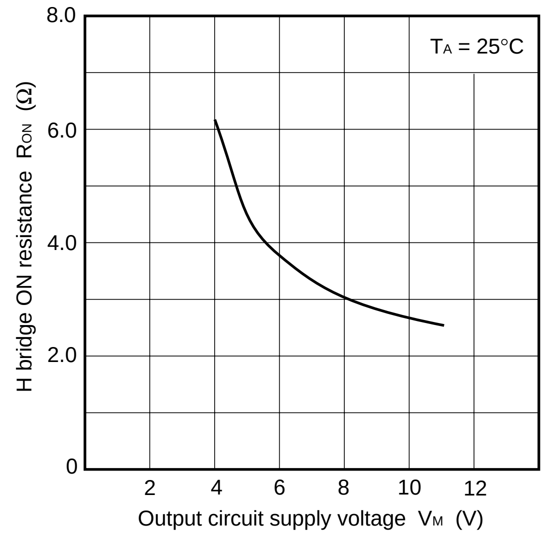
I_M vs. V_M characteristics



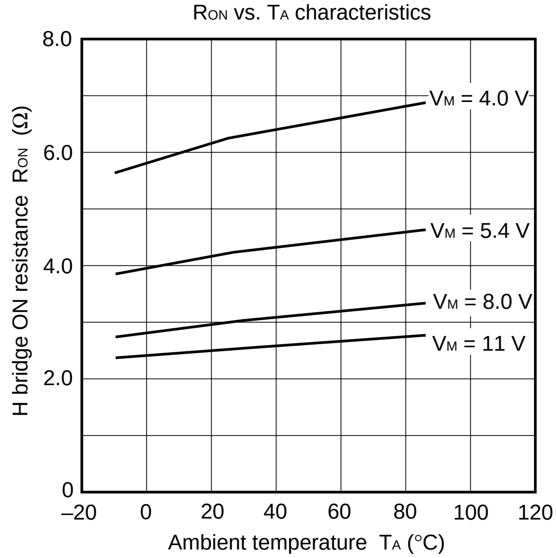
I_M vs. R_S characteristics



R_{ON} vs. V_M characteristics



R_{ON} vs. T_A characteristics



I/F CIRCUIT DATA CONFIGURATION (f_{CLK} = 4.5 MHz EXTERNAL CLOCK INPUT)

Input data consists of serial data (8 bits × 13 bytes).
Input serial data with the LSB first, from the first byte to 13th byte.

[1st byte]

Bit	Data	Function	Setting
D7	8 bit data input[Note]	First point wait	First point wait 227.6 μs to 58.03 ms Setting (1 to 255) Δt = 227.6 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than "0"

[2nd byte]

Bit	Data	Function	Setting
D7	8 bit data input[Note]	First point magnetize wait	First point magnetize wait 227.6 μs to 58.03 ms Setting (1 to 255) Δt = 227.6 μs
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Input other than "0"

[3rd byte]

Bit	Data	Function	Setting
D7	1 or 0	EXP1	Z/L[Note 1]
D6	1 or 0	EXP0	Z/L[Note 1]
D5	6 bit data input	Chopping frequency	Chopping frequency 35.71 kHz to 225 kHz Setting (8 to 48)[Note 2]
D4			
D3			
D2			
D1			
D0			

Notes 1. Z: High impedance/L: low level
2. 0 to 7 input: PWM and pulse out nothing
49 to 63 input: 225 kHz fixed
Refer to 4 page

[4th byte]

Bit	Data	Function	Setting
D7	1 or 0	Power save	OFF/ON[Note 1]
Bit	Data	EXT α Output	EXT β Output
D6	**Note 5**	Enable[Note 2]	Enable[Note 2]
D5	**Note 5**	Rotation[Note 3]	Rotation[Note 3]
D4	**Note 5**	Pulse out	Pulse out
D3	**Note 5**	FF7	FF7
D2	**Note 5**	FF3	FF3
D1	**Note 5**	Checksum[Note 4]	FF2
D0	**Note 5**	Chopping	FF1

Notes 1. Data "1": Normal/Data "0": Power save
2. High: Conducts/Low: Stops
3. High: Reverse (CCW)/Low: Forward (CW)
4. High: Normal data/Low: Error data
5. Select one of D0 to D6 and input "1".
If two or more of D0 to D6 are selected, they are positively ORed for output.

[5th byte]

Bit	Data	Function	Setting
D7	1 or 0	Enable α	α ch ON/OFF
D6	1 or 0	Rotation α	α ch CCW/CW
D5	0	Not use	Not use
D4	5 bit data input	α channel Current set	α channel Current set[Note] EVR: 50 to 250 mV Setting (11 to 31)
D3			
D2			
D1			
D0			

Note Fixed to 50 mV if 0 to 10 input.
Refer to 4 page.

[6th byte]

Bit	Data	Function	Setting
D7	8 bit data input	α channel Pulse Number	α channel Number of pulse in 1 V_D 0 to 1020 pulses Setting (0 to 255) Δn = 4 pulses[Note]
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Output pulse is nothing if data input 256, 512, and 768.

[7th byte]

Bit	Data	Function	Setting
D7	16 bti data low-order 8 bit data input	α channel Pulse Cycle	α channel Pulse cycle 222 ns to 14.563 ms Setting (1 to 65535) Δt = 222 ns
D6			
D5			
D4			
D3			
D2			
D1			
D0			

[8th byte]

Bit	Data	Function	Setting
D7	16 bit data High-order 8 bit data input	α channel Pulse Cycle	α channel Pulse cycle 222 ns to 14.563 ms Setting (1 to 65535) Δt = 222 ns
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note D0 bit of 7th byte is LSB, and D7 bit of 8th byte is MSB.

[9th byte]

Bit	Data	Function	Setting
D7	1 or 0	Enable β	β ch ON/OFF
D6	1 or 0	Rotation β	β ch CCW/CW
D5	0	Not use	Not use
D4	5 bit data input	β channel Current set	β channel Current set[Note] EVR: 50 to 250 mV Setting (11 to 31)
D3			
D2			
D1			
D0			

Note Fixed to 50 mV if 0 to 10 input.
Refer to 4 page.

[10th byte]

Bit	Data	Function	Setting
D7	8 bit data input	β channel Pulse Number	β channel Number of pulse in 1 V_D 0 to 1020 pulses Setting (0 to 255) Δn = 4 pulses[Note]
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Output pulse is nothing if data input 256, 512, and 768.

[11th byte]

Bit	Data	Function	Setting
D7	16 bit data low-order 8 bit data input	β channel Pulse Cycle	β channel Pulse cycle 222 ns to 14.563 ms Setting (1 to 65535) Δt = 222 ns
D6			
D5			
D4			
D3			
D2			
D1			
D0			

[12th byte]

Bit	Data	Function	Setting
D7	16 bit data high-order 8 bit data input	β channel Pulse Cycle	β channel Pulse cycle 222 ns to 14.563 ms Setting (1 to 65535) Δt = 222 ns
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note D0 bit of 11th byte is LSB, and D7 bit of 12th byte is MSB.

[13th byte]

Bit	Data	Function	Setting
D7	8 bit data input	Checksum	Checksum[Note]
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Note Data is input so that the sum of the first through the 13th bytes is 00h.

DATA CONFIGURATION

Input data is composed of the serial data on 8 bits × 13 bytes. Input serial data with the LSB first, i.e., starting from the D0 bit (LSB) of the first byte. Therefore, the D7 bit of the 13th byte is the most significant bit (MSB).

The establishment of the delay time to the output from the power supply injection, chopping frequency, output current, number of pulse, pulse cycle, and so on are possible with this product.

The μPD16879 has an EXT pin for monitoring the internal operations, the parameter to be monitored can be selected by serial data.

The μPD16879 built in power save function. If set power save mode, consumption current decreased to about 1/10.

Input serial data during first point wait time (FF1: high level).

This product uses separated external reference clock (f_{CLK}). If they don't input f_{CLK}, this product can't operate normally.

The establishment value which shows it in this document is at the time of f_{CLK} = 4.5 MHz. Please be careful because establishment value is different in the case of one except for f_{CLK} = 4.5 MHz.

Detail of Data Configuration

Ho to input serial data is below.

[1st byte]

The 1st byte specifies the delay between data being read and data being output. This delay is called the first point wait time, and the motor can be driven from that point at which the first point wait time is "0". This time is counted at the rising edge of V_D (or falling edge of $\overline{V_D}$). The first point wait time can be set to 58.03 ms (when a 4.5 MHz clock input) and can be fine-tuned by means of 8-bit division (227.6 μs step: with 4.5 MHz clock).

Always input data other than "0" to this byte because the first point wait time is necessary for latching data. If "0" is input to this byte, data cannot be updated. Transfer serial data during the first point wait time.

Table 3. 1st Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	MSB							LSB

Data	First point wait
00000000	Prohibition
00001001	About 2.05 ms
11111111	About 58.03 ms
n	N × 1024/4.5 MHz

[2nd byte]

The 2nd byte specifies the delay between the first point wait time being cleared and the output pulse being generated. This time called the first point magnetize wait time, and the output pulse is generated from the point at which the start up wait time. The first point magnetize wait time is counted at the falling edge of the first point wait time. The first point magnetize wait time can be set to 58.03 ms (when a 4.5 MHz clock input) and can be fine-tuned by means of 8-bit division (227.6 μs step: with 4.5 MHz clock).

Always input data other than “0” to this byte because the first point magnetize wait time is necessary for latching data. If “0” is input to this byte, data cannot be updated.

Table 4. 2nd Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

MSB (D7) … LSB (D0)

Data	First point wait
00000000	Prohibition
00101001	About 9.33 ms
11111111	About 58.03 ms
n	N × 1024/4.5 MHz

[3rd byte]

The 3rd byte sets the chopping frequency and external extension pins (EXP0, EXP1).

The chopping frequency sets by bits D0 to D5.

The EXP pins goes low (current sink) when the input data is “0”, and high (high-impedance state) when the input data is “1”. Pull this pin up to V_{DD} for use.

Table 5. 3rd Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

EXP1 sets (D7)
EXP0 sets (D6)
MSB (D5) … LSB (D0): Chopping frequency sets

D7: EXP1 sets “1”: High impedance “0”: Low level (Current sink)

D6: EXP0 sets “1”: High impedance “0”: Low level (Current sink)

The chopping frequency is set to 0 kHz and to a value in the range of 35.71 kHz to 225 kHz (4.5 MHz clock input). Refer to table 1 (4 page).

[4th byte]

The 4th byte selects a parameter to be output EXT α and EXT β pins (logic operation monitor pin). And, power save mode sets too.

Table 6. 4th Byte Data Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Power save sets (D7)
Test parameter select (D6 to D0)

The test parameter is selected by bits D0 to D6. There are two EXT pins. EXT α indicates the operating status of α channel, and EXT β indicates that of β channel. The relationship between each bit and each EXT pin is as shown in Table 7.

Table 7. Output Data of Test Parameter

Bit	Data	EXT α	EXT β
D6	0 or 1	Enable α	Enable β
D5	0 or 1	Rotation α	Rotation β
D4	0 or 1	Pulseout α	Pulseout β
D3	0 or 1	FF7 α	FF7 β
D2	0 or 1	FF3 α	FF3 β
D1	0 or 1	Checksum	FF2
D0	0 or 1	Chopping	FF1

If two or more signals that output signals to EXT α and EXT β are selected, they are positively ORed for output.

The meanings of the symbols listed in Table 7 are as follows:

- Enable : Output setting (High level: Conducts/Low level: Stops)
- Rotation : Rotation setting (High level: Reverse (CCW)/Low level: Forward (CW))
- Pulse out : Output pulse signal
- FF7 : Presence/absence of pulse in LATCH cycle (Outputs H level if output pulse information exists in serial data.)
- FF3 : Pulse gate (output while pulse exists)
- FF2 : Outputs high level during first point wait time + first point magnetize wait time
- FF1 : Outputs high level during first point wait time
- Checksum : Checksum output (High level: when normal data is transmitted/Low level: when abnormal data is transmitted)
- Chopping : Chopping wave output

Power save mode sets by D7 bit.

D7 bit data is “1”: Normal mode

D7 bit data in “0”: Power save mode

When power save mode is selected, circuit consumption current can be reduced. Detail of power save function is refer to “About Power Save Mode (25 page)”.

[5th byte]

The 5th byte sets the enable, rotation, and output current of α channel.

The enable sets by bit D7, the rotation sets by bit D6, and the output current sets by bits D0 to D4. Bit D5 is fixed “0”. Bit D5 isn’t use.

Table 8. 5th Byte Data Configuration (α channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Enable sets (D7)
Rotation sets (D6)
MSB (D4) — LSB (D0): Output current sets

Enable sets by D7 bit.

D7 bit data is “0”: Output high impedance (but, internal counter increase)

D7 bit data is “1”: Output conducts

Rotation sets by D6 bit.

D6 bit data is “0”: Forward turn (CW mode)

D6 bit data is “1”: Reverse turn (CCW mode)

Output current sets by D0 to D4 bits.

The 250 mV (typical) voltage input from external source or internal reference voltage is internally doubled and input to a 5-bit D/A converter. By dividing this voltage by 5-bit data, a current setting reference voltage can be set inside the IC within the range of 100 to 500 mV, in units of 20 mV. If external source is used, the V_{REFsel} pin connects V_{DD} pin. If internal reference voltage is used, the V_{REFsel} pin and V_{REF} pin connect GND pin. The 64 steps micro-step (setting reference voltage is maximum) control is possible.

Table 9. Output Current Setting Reference Voltage Data (α channel data)

EVR setting	D4	D3	D2	D1	D0	FIL pin voltage	EVR setting	D4	D3	D2	D1	D0	FIL pin voltage
50 mV	0	1	0	1	1	100 mV	160 mV	1	0	1	1	0	320 mV
60 mV	0	1	1	0	0	120 mV	170 mV	1	0	1	1	1	340 mV
70 mV	0	1	1	0	1	140 mV	180 mV	1	1	0	0	0	360 mV
80 mV	0	1	1	1	0	160 mV	190 mV	1	1	0	0	1	380 mV
90 mV	0	1	1	1	1	180 mV	200 mV	1	1	0	1	0	400 mV
100 mV	1	0	0	0	0	200 mV	210 mV	1	1	0	1	1	420 mV
110 mV	1	0	0	0	1	220 mV	220 mV	1	1	1	0	0	440 mV
120 mV	1	0	0	1	0	240 mV	230 mV	1	1	1	0	1	460 mV
130 mV	1	0	0	1	1	260 mV	240 mV	1	1	1	1	0	480 mV
140 mV	1	0	1	0	0	280 mV	250 mV	1	1	1	1	1	500 mV
150 mV	1	0	1	0	1	300 mV							

Remark If D0 to D4 bits input “00000” to “01010”, EVR value fixed 50 mV (FIL pin voltage fixed 100 mV). FIL pin (peak voltage) is output about double of EVR setting value.

[6th byte]

The 6th byte sets pulse number during $1V_D$ period of α channel. The pulse number setting 1020 pulses maximum. It is set by eight bits in terms of software. However, the actual circuit uses 10-bit counter with the low-order two bits fixed to “0”. Therefore, the number of pulses that is actually generated during fall edge of the first point wait time + first point magnetize wait time (FF2) cycle is the number of pulses input x 4. The number of pulses can be set in a range of 0 to 1020 and in units of four pulses.

Table 10. 6th Byte Data Configuration (α channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	MSB							LSB

Data	Pulse number/V_D
00000000	0
00000001	4
11111111	1020
n	$n \times 4$

[7th, 8th byte]

The 7th byte and 8th byte set the pulse cycle of the α channel.

The pulse cycle is specified using 16 bits: bits D0 (least significant bit) to D7 of the 7th byte, and bits D0 to D7 (most significant bit) of the 8th byte. The pulse cycle can be set to a value in the range of 222 ns to 14.563 ms in units of 222 ns (with a 4.5 MHz clock).

Table 11 (A). 7th Byte Data Configuration (α channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

LSB (D0)

Table 11 (B). 8th Byte Data Configuration (α channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

MSB (D7)

[9th byte]

The 9th byte sets the enable, rotation, and output current of β channel.

The enable sets by bit D7, the rotation sets by bit D6, and the output current sets by bits D0 to D4. Bit D5 is fixed "0". Bit D5 isn't use.

Table 12. 9th Byte Data Configuration (β channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

Enable sets (D7); Rotation sets (D6); Output current sets: MSB (D4) to LSB (D0)

Enable sets by D7 bit.

D7 bit data is "0": Output high impedance (but, internal counter increase)

D7 bit data is "1": Output conducts

Rotation sets by D6 bit.

D6 bit data is "0": Forward turn (CW mode)

D6 bit data is "1": Reverse turn (CCw mode)

Output current sets by D0 to D4 bits.

The 250 mV (typical) voltage input from external source or internal reference voltage is internally doubled and input to a 5-bit D/A converter. By dividing this voltage by 5-bit data, a current setting reference voltage can be set inside the IC within the range of 100 to 500 mV, in units of 20 mV. If external source is used, the V_{REFsel} pin connects V_{DD} pin. If internal reference voltage is used, the V_{REFsel} pin and V_{REF} pin connect GND pin. The 64 steps micro-step (setting reference voltage is maximum) control is possible.

Table 13. Output Current Setting Reference Voltage Data (β channel data)

EVR setting	D4	D3	D2	D1	D0	FIL pin voltage	EVR setting	D4	D3	D2	D1	D0	FIL pin voltage
50 mV	0	1	0	1	1	100 mV	160 mV	1	0	1	1	0	320 mV
60 mV	0	1	1	0	0	120 mV	170 mV	1	0	1	1	1	340 mV
70 mV	0	1	1	0	1	140 mV	180 mV	1	1	0	0	0	360 mV
80 mV	0	1	1	1	0	160 mV	190 mV	1	1	0	0	1	380 mV
90 mV	0	1	1	1	1	180 mV	200 mV	1	1	0	1	0	400 mV
100 mV	1	0	0	0	0	200 mV	210 mV	1	1	0	1	1	420 mV
110 mV	1	0	0	0	1	220 mV	220 mV	1	1	1	0	0	440 mV
120 mV	1	0	0	1	0	240 mV	230 mV	1	1	1	0	1	460 mV
130 mV	1	0	0	1	1	260 mV	240 mV	1	1	1	1	0	480 mV
140 mV	1	0	1	0	0	280 mV	250 mV	1	1	1	1	1	500 mV
150 mV	1	0	1	0	1	300 mV							

Remark If D0 to D4 bits input “00000” to “01010”, EVR value fixed 50 mV (FIL pin voltage fixed 100 mV). FIL pin (peak voltage) is output about double of EVR setting value.

[10th byte]

The 10th byte sets pulse number during $1V_D$ period of β channel. The pulse number setting 1020 pulses maximum. It is set by eight bits in terms of software. However, the actual circuit uses 10-bit counter with the low-order two bits fixed to “0”. Therefore, the number of pulses that is actually generated during fall edge of the first point wait time + first point magnetize wait time (FF2) cycle is the number of pulses input × 4. The number of pulses can be set in a range of 0 to 1020 and in units of four pulses.

Table 14. 10th Byte Data Configuration (β channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
	MSB							LSB

Data	Pulse number/V_D
00000000	0
00101001	164
11111111	1020
n	n × 4

[11th, 12th byte]

The 11th byte and 12th byte set the pulse cycle of the β channel.

The pulse cycle is specified using 16 bits: bits D0 (least significant bit) to D7 of the 7th byte, and bits D0 to D7 (most significant bit) of the 8th byte. The pulse cycle can be set to a value in the range of 222 ns to 14.563 ms in units of 222 ns (with a 4.5 MHz clock).

Table 15 (A). 11th Byte Data Configuration (β channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

LSB (D0)

Table 15 (B). 12th Byte Data Configuration (β channel data)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Data	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1

MSB (D7)

[13th byte]

The 13th byte is checksum data.

Please input the data that sum of the 1st byte to 13th byte is “0”.

When the sum is “0”, the stepping operation continued. If the sum is not “0” because data transmission is abnormal, the stepping operation is inhibited and EXT pin (at the Checksum selecting) is held at low level.

About Power Save Mode

It is possible that circuit electric current is made small in the power saving (the following PS) mode.

Data maintenance just before the PS mode and the maintenance of the phase position are done in the PS mode. Circuit consumption current in the PS mode becomes 300 μA (MAX.) at the time of the outside clock (OSC_{IN}) = 4.5 MHz, and becomes 100 μA (MAX.) at the time of the outside clock (OSC_{IN}) stopped. It can be reduced in less than 1/10 in normal mode.

(How to be within PS mode)

The establishment of the PS mode is done by a D7 bits of the 4th byte.

Please follow the following process when it is within PS mode.

(1) Normal operation (Pulse number > 1, enable: conducts)

↓

(2-1) Normal operation (Pulse number = 0, enable: conducts)

(2-2) Normal operation (Pulse number = 0, enable: stops)

↓

(3) Please input PS data.

(Effective timing of PS mode)

- Chopping movement stops at the LATCH falling timing which PS data are contained to.
- First point wait count and first point magnetize wait count stop at the next V_D rising timing which PS data are contained to. FF1 is fixed on the high level, and FF2 is fixed on low level.
- Enable becomes low level at the LATCH falling timing which PS data are contained to.
- And, the outside expansion circuit (EXP terminal) works at the time of PS mode too.

(PS mode release movement)

- Chopping movement resumes at the LATCH falling timing which PS release data are contained to.
- First point wait count and first point magnetize wait count resume at the next V_D rising timing which PS release data are contained to.
- Enalbe becomes high level at the first FF1 falling timing which PS release data are contained to. (When enable data is high level)

Data Update Timing

The serial data of this product is set and update at the following timing.

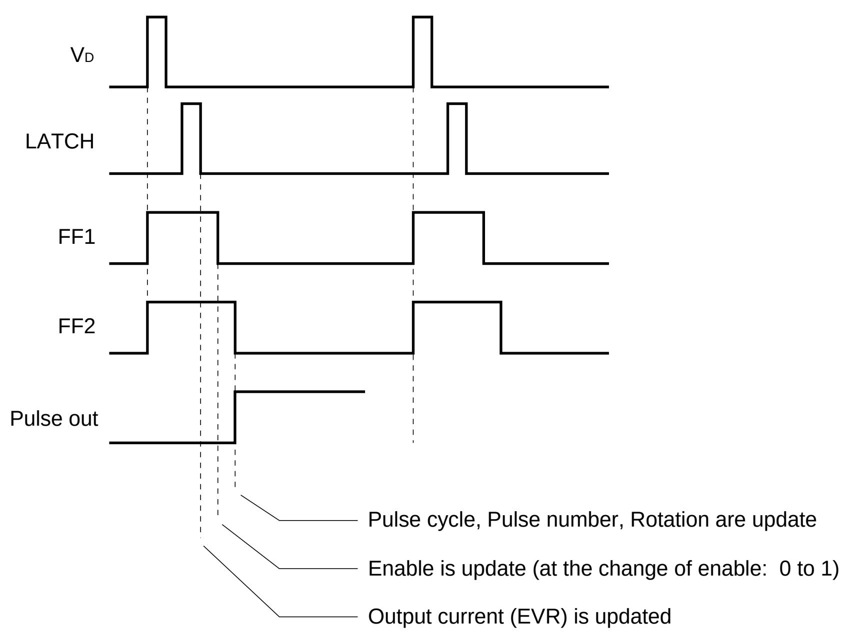
Table 16. Update Timing of The Data (1)

Data	Data set	Update timing
First point wait time	LATCH falling edge	Next V_D rising edge or, next $\overline{V_D}$ falling edge
First point magnetize wait time	LATCH falling edge	FF1 falling edge
EXP	LATCH falling edge	LATCH falling edge
Chopping	LATCH falling edge	LATCH falling edge
Power save	LATCH falling edge	Refer to 25 page

The timing at which data is to be update differ, as shown in Table 17, depending on the enable status.

Table 17. Update Timing of The Data (2)

Change of enable	1 → 1	0 → 1	1 → 0	0 → 0
Pulse cycle	FF2 ↓	FF2 ↓	FF2 ↓	–
Pulse number	FF2 ↓	FF2 ↓	FF2 ↓	–
Rotation	FF2 ↓	FF2 ↓	FF2 ↓	–
Enable	FF2 ↓	FF1 ↓	FF2 ↓	–
EVR	LATCH ↓	LATCH ↓	LATCH ↓	–



Initialization

The IC operation can be initialized as follows:

(1) Turns ON V_{DD}.

(2) Make RESET input low level signal.

In initial mode, the operating status of the IC is as shown in Table 18.

Table 18. Operations in Initial Mode

Item	Specification
Current consumption	100 μA
OSC	Input of external clock is inhibited.
V_D, $\overline{V_D}$	Input inhibited.
FF1 to FF7	Low level
Pulse out	Low level
EXP0, EXP1	Low level in the case of (1) above. Previous value is retained in the case of (2) above.
Serial operation	Can be accessed after initialization in the case of (1) above. Can be accessed after RESET has gone high level in the case of (2) above.

Step pulse output is inhibited and FF7 is made low level if the following conditions are satisfied.

(1) If the set number of pulses (6th/10th byte) is “0”.

(2) If the checksum value is other than “0”.

(3) If the first point wait time (FF1) is set to $1V_D$ or longer.

(4) If the first point wait time + first point magnetize wait time (FF2) is set to $1V_D$ or longer.

(5) If the first point wait time (FF1) is completed earlier than falling timing of LATCH.

(6) If V_D is not input.

Hints on correct use

(1) With this product, input the data for first point wait time and first point magnetize wait time.
Because the serial data are set or updated by these wait times, if the first point wait time and first point magnetize wait time are not input, the data are not updated.

(2) The first point wait time must be longer than LATCH.

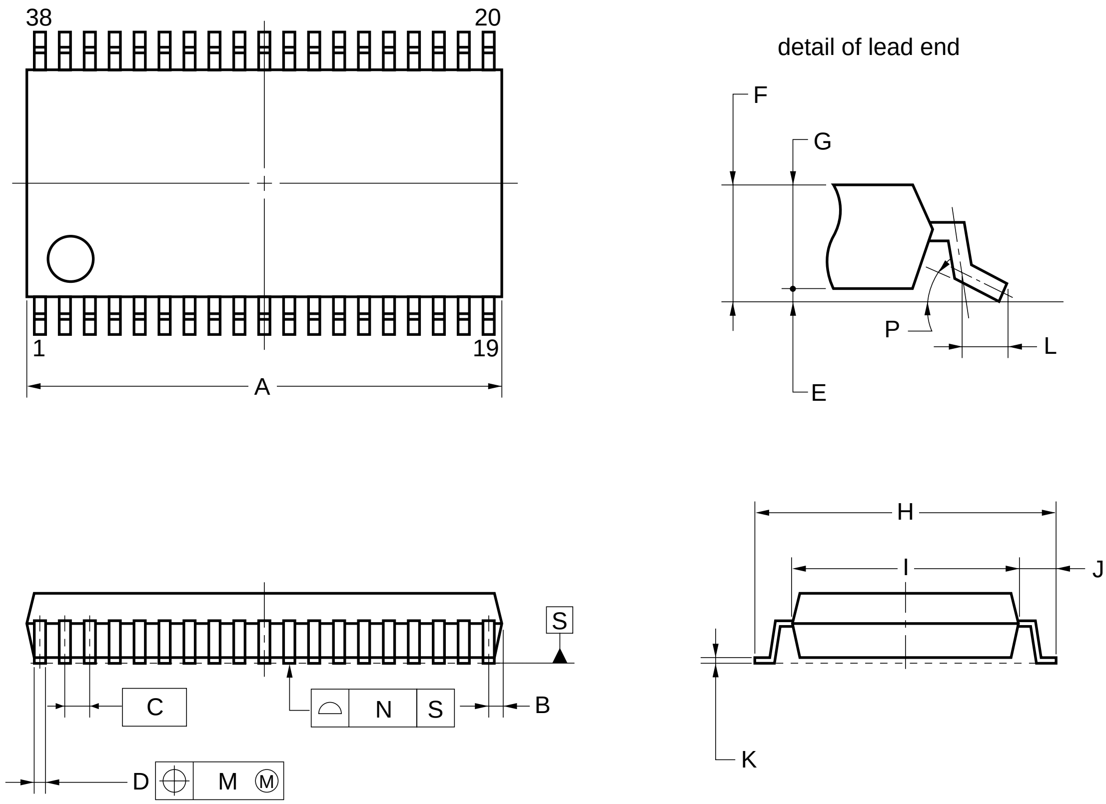
(3) If the falling of the FF2 is the same as the falling of the last output pulse, a count error occurs, and the IC may malfunction.

(4) Transmit the serial data during the first point wait time (FF1). If it is input at any other time, the data may not be transmitted correctly.

(5) If the LGND potential is undefined, the data may not be input correctly. Keep the LGND potential to the minimum level. It is recommended that LGND and PGND be divided for connection (single ground) to prevent the leakage of noise from the output circuit.

PACKAGE DRAWINGS

38-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.7±0.3
B	0.65 MAX.
C	0.65 (T.P.)
D	$0.37^{+0.05}_{-0.1}$
E	0.125±0.075
F	1.675±0.125
G	1.55
H	7.7±0.2
I	5.6±0.2
J	1.05±0.2
K	$0.2^{+0.1}_{-0.05}$
L	0.6±0.2
M	0.10
N	0.10
P	$3°^{+7°}_{-3°}$

P38GS-65-BGG-1

RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.
For soldering methods and conditions other than those recommended, consult NEC.

For details of the recommended soldering conditions, refer to information document **“Semiconductor Device Mounting Technology Manual”**.

Soldering Method	Soldering Conditions	Recommended Condition
Infrared reflow	Package peak temperature: 235°C, Time: 30 secs max. (210°C min.); Number of times: 3 times max.; Number of day: none; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt%, ax.) is recommended	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 secs max. (200°C min.); Number of times: 3 times max.; Number of day: none; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt%, ax.) is recommended.	VP15-00-3
Wave soldering	Package peak temperature: 260°C; Time: 10 secs max.; Preheating temperature: 120°C max; Number of times: once; Flux: Rosin-based flux with little chlorine content (chlorine: 0.2 Wt%, ax.) is recommended.	WS60-00-1

Caution   Do not use two or more soldering methods in combination.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.