NEC

MOS INTEGRATED CIRCUIT

μPD16732E

384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

DESCRIPTION

The μPD16732E is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.1 V to V_{DD2} – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, 45 MHz when driving at 2.3 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA-standard TFT-LCD panels.

FEATURES

- CMOS level input (2.3 to 3.6 V)
- 384 outputs
- Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 2.3 to 3.6 V
- Driver power supply voltage (V_{DD2}): 8.0 to 9.0 V
- Output dynamic range: V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- High-speed data transfer: f_{CLK} = 65 MHz (internal data transfer speed when operating at V_{DD1} = 3.0 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (capable of controlling by each input port) (POL21, POL22)
- Current consumption reduction function (LPC, Bcont)
- Succession of μPD16732B driver

ORDERING INFORMATION

Part Number	Package
μPD16732EN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

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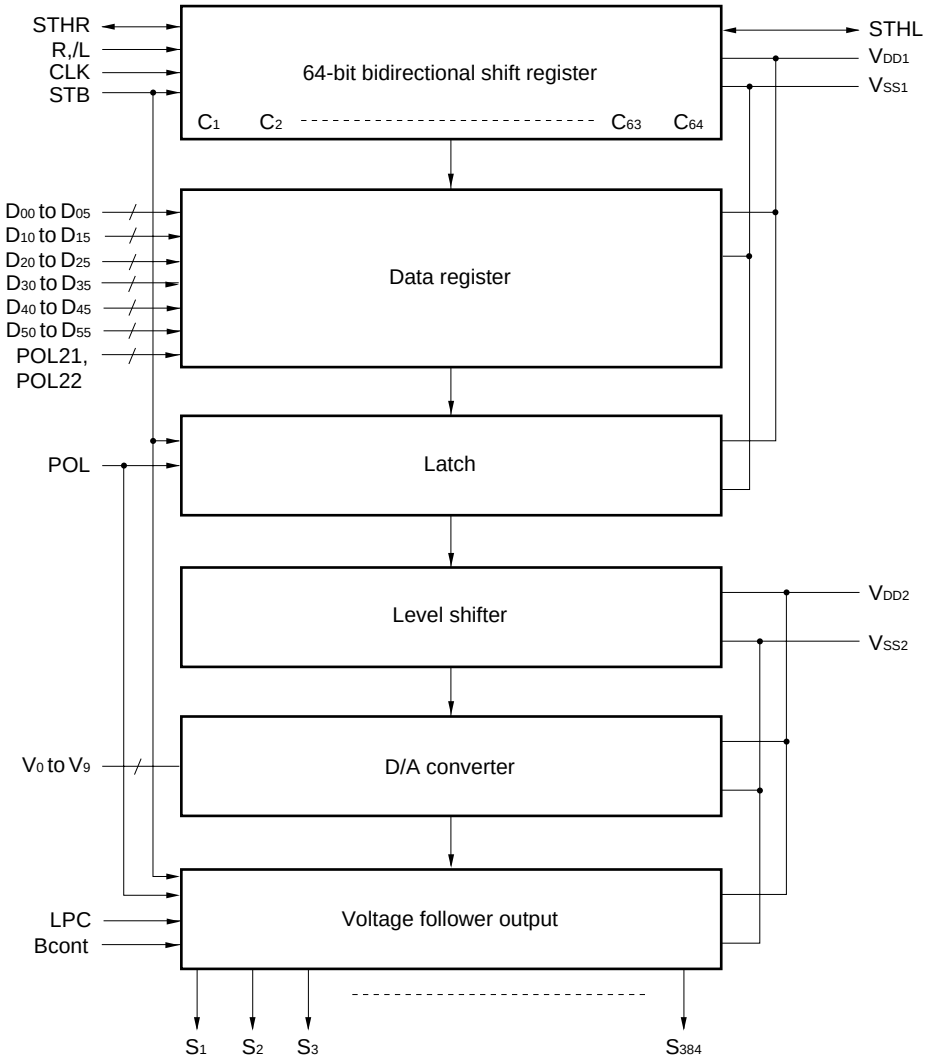
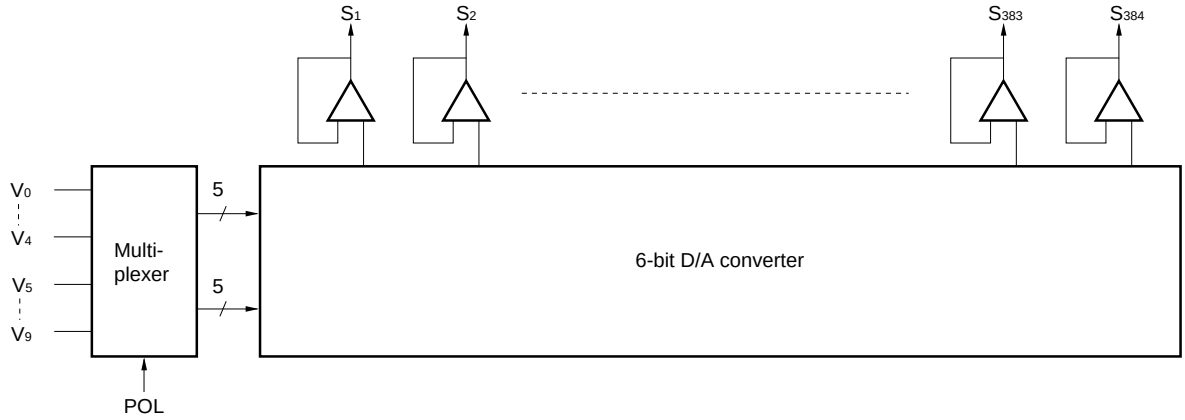
1. BLOCK DIAGRAM



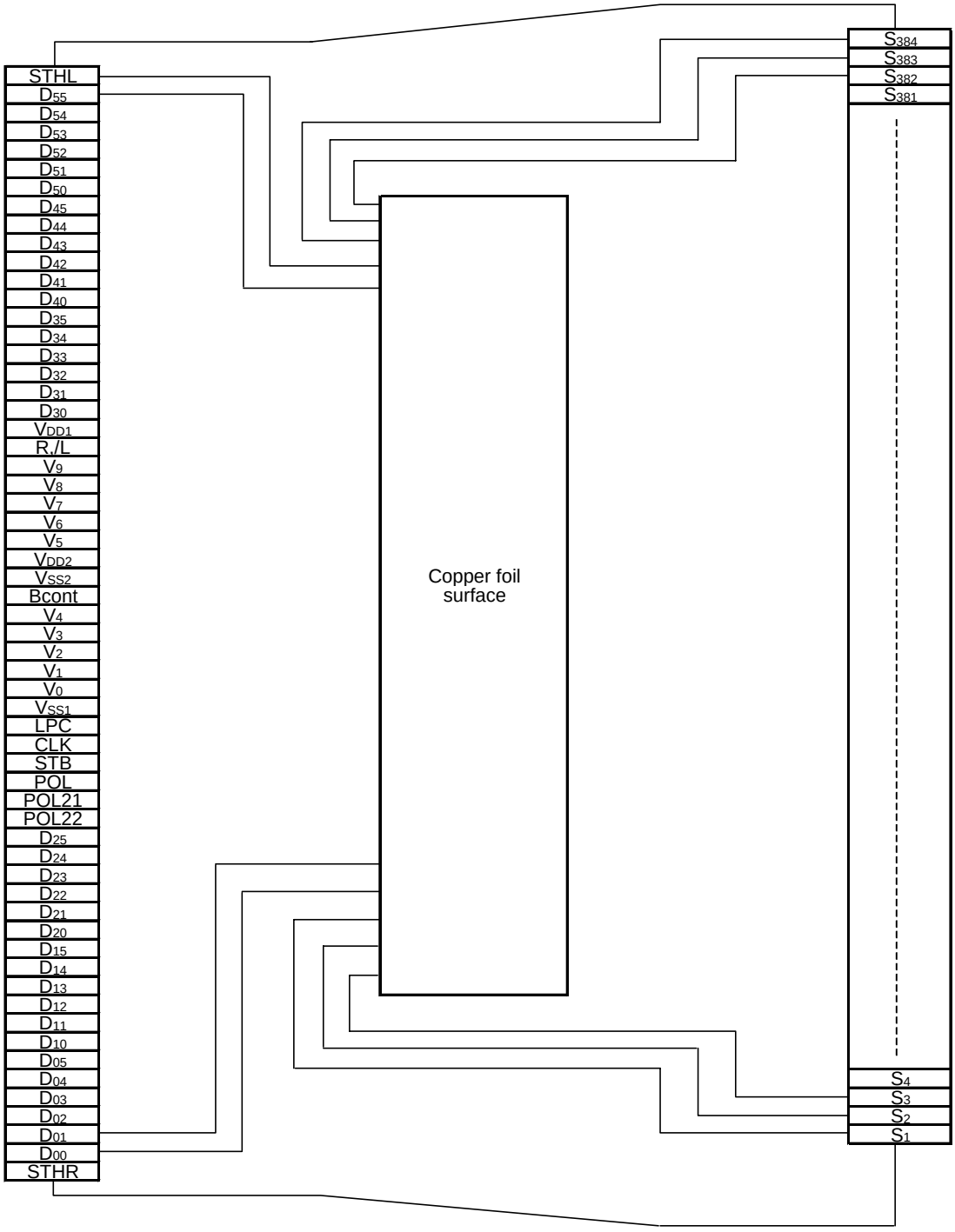
Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (Top of copper foil surface, face-up)

μPD16732EN-xxx: TCP (TAB package)



Remark This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{384}	Driver output	Output	The D/A converted 64-gray-scale analog voltage is output.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25} D_{30} to D_{35} D_{40} to D_{45} D_{50} to D_{55}	Display data input	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D_{X0}: LSB, D_{X5}: MSB
R,/L	Shift direction control	Input	The shift direction control pin of the shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR (input), $S_1 \rightarrow S_{384}$, STHL (output) R,/L = L (left shift) : STHL (input), $S_{384} \rightarrow S_1$, STHR (output)
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when the IC is connected in cascade. Loading of display data starts when a high level is read at the rising edge of CLK. A high level should be input as the pulse of one cycle of the clock signal.
STHL	Left shift start pulse	I/O	If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is valid. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output
CLK	Shift clock	Input	This pi refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. When the 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	Input	POL = L: The S_{2n-1} output uses V_0 to V_4 as the reference supply. The S_{2n} output uses V_5 to V_9 as the reference supply. POL = H: The S_{2n-1} output uses V_5 to V_9 as the reference supply. The S_{2n} output uses V_0 to V_4 as the reference supply. S_{2n-1} indicates the odd output: and S_{2n} indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge.
POL21, POL22	Data inversion	Input	Data inversion can invert when display data is loaded. POL21: D_{00} to D_{05}, D_{10} to D_{15}, D_{20} to D_{25} Data inversion or no inversion of Port1 POL22: D_{30} to D_{35}, D_{40} to D_{45}, D_{50} to D_{55} Data inversion or no inversion of Port2 POL21,POL22 = H: Data inversion loads display data inside the IC. POL21,POL22 = L: Data inversion does not invert input data.
LPC	Low power control	Input	The current consumption is lowered by controlling the constant current source of the output amplifier. In low power mode (LPC = L), the V_{DD2} of static current consumption can be reduced to two thirds of the normal current consumption. This pin is pulled up to the V_{DD1} power supply inside the IC. LPC = H or open: Normal power mode LPC = L: Low power mode
Bcont	Bias control	Input	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor of 10 to 100 kΩ (per IC). When this fine-control function is not required, leave this pin open. Refer to **9. CURRENT CONSUMPTION REDUCTION FUNCTION**

(2/2)

Pin Symbol	Pin Name	I/O	Description
V_0 to V_9	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$ $0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$
V_{DD1}	Logic power supply	–	2.3 to 3.6 V
V_{DD2}	Driver power supply	–	8.0 to 9.0 V
V_{SS1}	Logic ground	–	Grounding
V_{SS2}	Driver ground	–	Grounding

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0 to V_9 in that order. Reverse this sequence to shut down (Simultaneous power application to V_{DD2} and V_0 to V_9 is possible.).

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_9) and V_{SS2}.

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

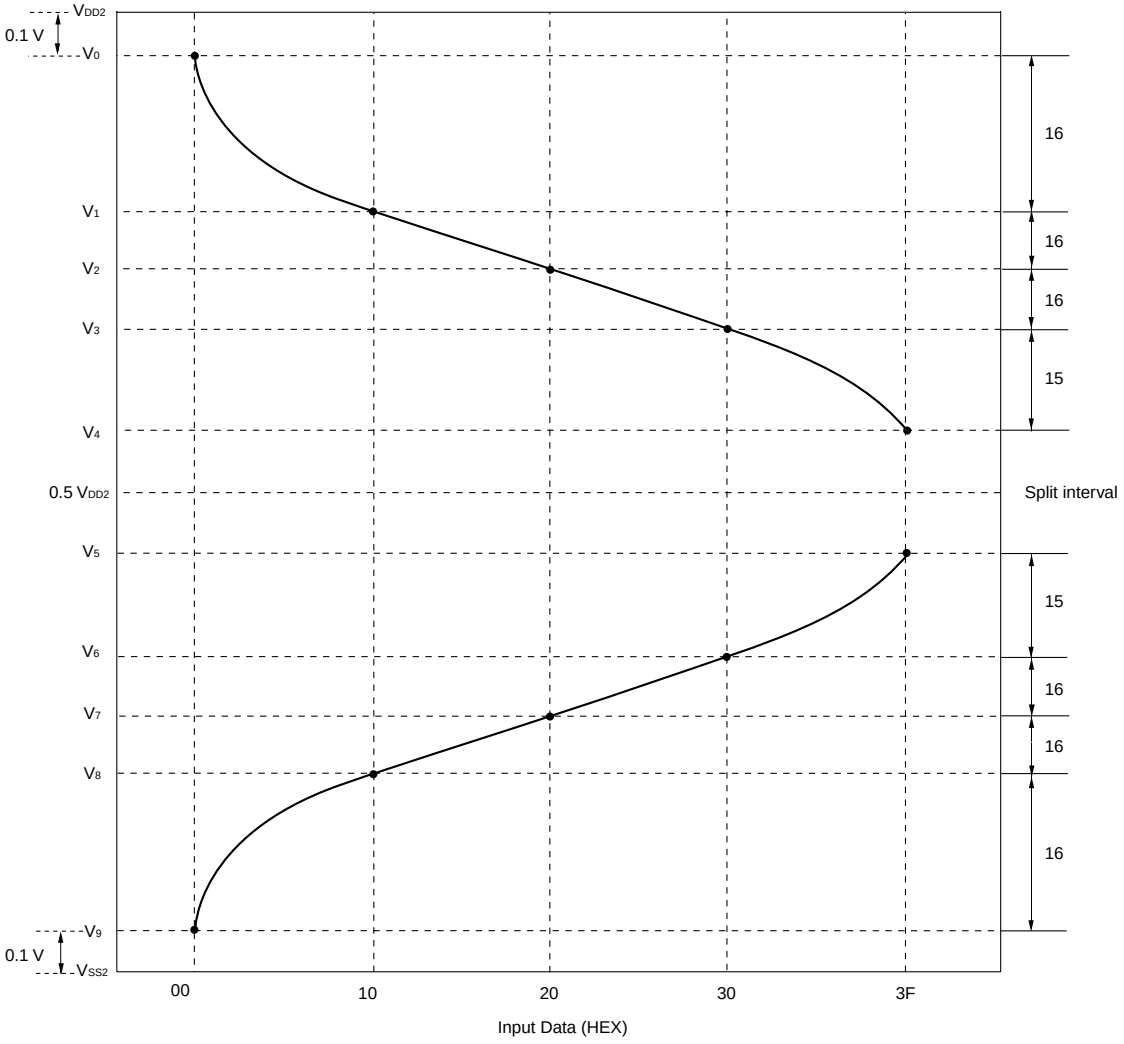
The μPD16732E incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors (r_0 to r_{62}) are designed so that the ratio of LCD panel γ-compensated voltages to V_0' to V_{63}' and V_0" to V_{63}" is almost equivalent as shown in Figure 5-2. For the 2 sets of five γ-compensated power supplies, V_0 to V_4 and V_5 to V_9, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect voltage follower circuit to the γ–corrected power supplies V_1 to V_3 and V_6 to V_8.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and γ-corrected voltages V_0 to V_9 and the input data. Be sure to maintain the voltage relationships as follows.

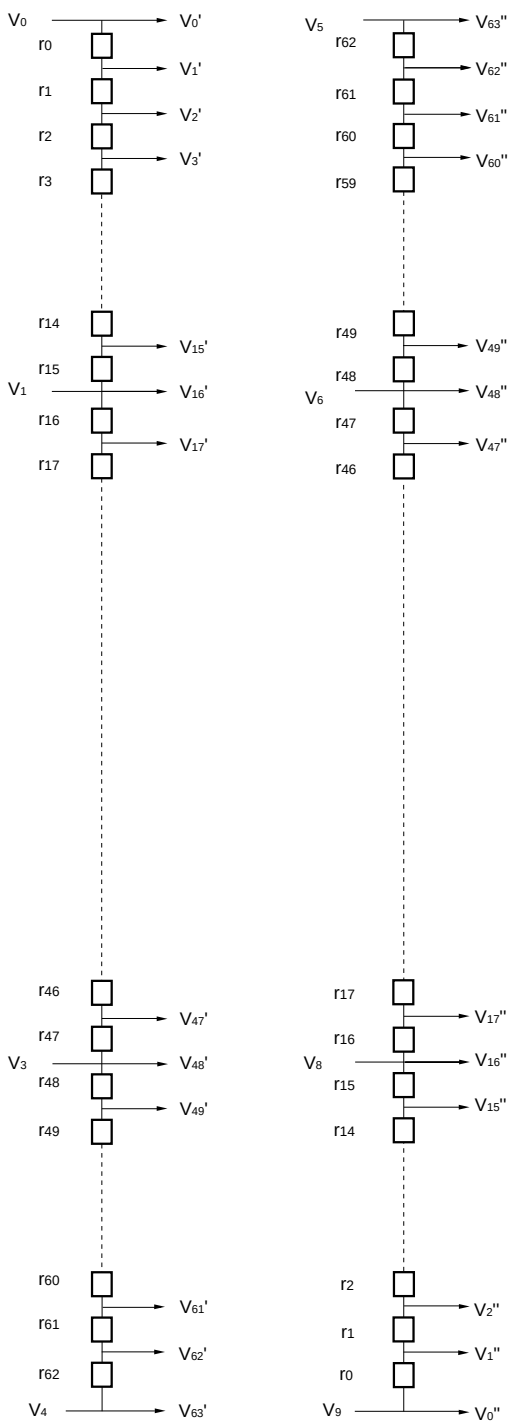
$V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$,
$0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$

Figures 5–2 indicates γ-corrected voltages and ladder resistors ratio. Figures 5–3 indicates the relationship between the input data and output voltage and the resistance values of the resistor string.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies



★ **Figure 5–2. γ-corrected Voltages and Ladder Resistor's Ratio**



rn	Ratio1	Ratio2	Value (Ω)
r0	11.62	0.1114	1766
r1	4.84	0.0464	736
r2	3.72	0.0357	566
r3	3.35	0.0321	509
r4	2.61	0.0250	396
r5	2.24	0.0214	340
r6	1.86	0.0179	283
r7	1.86	0.0179	283
r8	1.49	0.0143	226
r9	1.49	0.0143	226
r10	1.12	0.0107	170
r11	1.12	0.0107	170
r12	1.12	0.0107	170
r13	1.12	0.0107	170
r14	1.12	0.0107	170
r15	1.12	0.0107	170
r16	1.00	0.0096	152
r17	1.00	0.0096	152
r18	1.00	0.0096	152
r19	1.00	0.0096	152
r20	1.00	0.0096	152
r21	1.00	0.0096	152
r22	1.00	0.0096	152
r23	1.00	0.0096	152
r24	1.00	0.0096	152
r25	1.00	0.0096	152
r26	1.00	0.0096	152
r27	1.00	0.0096	152
r28	1.00	0.0096	152
r29	1.00	0.0096	152
r30	1.00	0.0096	152
r31	1.00	0.0096	152
r32	1.03	0.0098	156
r33	1.03	0.0098	156
r34	1.03	0.0098	156
r35	1.03	0.0098	156
r36	1.03	0.0098	156
r37	1.03	0.0098	156
r38	1.03	0.0098	156
r39	1.03	0.0098	156
r40	1.03	0.0098	156
r41	1.03	0.0098	156
r42	1.03	0.0098	156
r43	1.03	0.0098	156
r44	1.03	0.0098	156
r45	1.03	0.0098	156
r46	1.03	0.0098	156
r47	1.03	0.0098	156
r48	1.15	0.0110	175
r49	1.15	0.0110	175
r50	1.15	0.0110	175
r51	1.15	0.0110	175
r52	1.15	0.0110	175
r53	1.53	0.0146	232
r54	1.53	0.0146	232
r55	1.53	0.0146	232
r56	1.53	0.0146	232
r57	1.90	0.0182	289
r58	2.27	0.0218	345
r59	2.64	0.0254	402
r60	2.64	0.0254	402
r61	3.02	0.0290	459
r62	5.74	0.0550	872

Caution There is no connection between V_4 and V_5 terminal in the IC.

Remark The resistance ratio1 is a relative ratio in the case of setting the minimum resistance value to 1.
The resistance ratio2 is a relative ratio in the case of setting the total resistance to 1.

★ **Figure 5–3. Relationship between Input Data and Output Voltage (POL21, POL22 = L)**

(Output Voltage 1) V_{DD2} – 0.1 V ≥ V_5 > V_6 > V_7 > V_8 > V_9 ≥ 0.5 V_{DD2},

(Output Voltage 2) 0.5 V_{DD2} ≥ V_5 > V_6 > V_7 > V_8 > V_9 ≥ V_{SS2} + 0.1 V

Input Data	Output Voltage1		Output Voltage2	
00H	V_0'	V_0	V_0''	V_9
01H	V_1'	$V_1+(V_0-V_1)\times$ 4585/6351	V_1''	$V_9+(V_8-V_9)\times$ 1766/6351
02H	V_2'	$V_1+(V_0-V_1)\times$ 3849/6351	V_2''	$V_9+(V_8-V_9)\times$ 2502/6351
03H	V_3'	$V_1+(V_0-V_1)\times$ 3283/6351	V_3''	$V_9+(V_8-V_9)\times$ 3068/6351
04H	V_4'	$V_1+(V_0-V_1)\times$ 2774/6351	V_4''	$V_9+(V_8-V_9)\times$ 3577/6351
05H	V_5'	$V_1+(V_0-V_1)\times$ 2378/6351	V_5''	$V_9+(V_8-V_9)\times$ 3973/6351
06H	V_6'	$V_1+(V_0-V_1)\times$ 2038/6351	V_6''	$V_9+(V_8-V_9)\times$ 4313/6351
07H	V_7'	$V_1+(V_0-V_1)\times$ 1755/6351	V_7''	$V_9+(V_8-V_9)\times$ 4596/6351
08H	V_8'	$V_1+(V_0-V_1)\times$ 1472/6351	V_8''	$V_9+(V_8-V_9)\times$ 4879/6351
09H	V_9'	$V_1+(V_0-V_1)\times$ 1246/6351	V_9''	$V_9+(V_8-V_9)\times$ 5105/6351
0AH	V_{10}'	$V_1+(V_0-V_1)\times$ 1020/6351	V_{10}''	$V_9+(V_8-V_9)\times$ 5331/6351
0BH	V_{11}'	$V_1+(V_0-V_1)\times$ 850/6351	V_{11}''	$V_9+(V_8-V_9)\times$ 5501/6351
0CH	V_{12}'	$V_1+(V_0-V_1)\times$ 680/6351	V_{12}''	$V_9+(V_8-V_9)\times$ 5671/6351
0DH	V_{13}'	$V_1+(V_0-V_1)\times$ 510/6351	V_{13}''	$V_9+(V_8-V_9)\times$ 5841/6351
0EH	V_{14}'	$V_1+(V_0-V_1)\times$ 340/6351	V_{14}''	$V_9+(V_8-V_9)\times$ 6011/6351
0FH	V_{15}'	$V_1+(V_0-V_1)\times$ 170/6351	V_{15}''	$V_9+(V_8-V_9)\times$ 6181/6351
10H	V_{16}'	V_1	V_{16}''	V_8
11H	V_{17}'	$V_2+(V_1-V_2)\times$ 2280/2432	V_{17}''	$V_8+(V_7-V_8)\times$ 152/2432
12H	V_{18}'	$V_2+(V_1-V_2)\times$ 2128/2432	V_{18}''	$V_8+(V_7-V_8)\times$ 304/2432
13H	V_{19}'	$V_2+(V_1-V_2)\times$ 1976/2432	V_{19}''	$V_8+(V_7-V_8)\times$ 456/2432
14H	V_{20}'	$V_2+(V_1-V_2)\times$ 1824/2432	V_{20}''	$V_8+(V_7-V_8)\times$ 608/2432
15H	V_{21}'	$V_2+(V_1-V_2)\times$ 1672/2432	V_{21}''	$V_8+(V_7-V_8)\times$ 760/2432
16H	V_{22}'	$V_2+(V_1-V_2)\times$ 1520/2432	V_{22}''	$V_8+(V_7-V_8)\times$ 912/2432
17H	V_{23}'	$V_2+(V_1-V_2)\times$ 1368/2432	V_{23}''	$V_8+(V_7-V_8)\times$ 1064/2432
18H	V_{24}'	$V_2+(V_1-V_2)\times$ 1216/2432	V_{24}''	$V_8+(V_7-V_8)\times$ 1216/2432
19H	V_{25}'	$V_2+(V_1-V_2)\times$ 1064/2432	V_{25}''	$V_8+(V_7-V_8)\times$ 1368/2432
1AH	V_{26}'	$V_2+(V_1-V_2)\times$ 912/2432	V_{26}''	$V_8+(V_7-V_8)\times$ 1520/2432
1BH	V_{27}'	$V_2+(V_1-V_2)\times$ 760/2432	V_{27}''	$V_8+(V_7-V_8)\times$ 1672/2432
1CH	V_{28}'	$V_2+(V_1-V_2)\times$ 608/2432	V_{28}''	$V_8+(V_7-V_8)\times$ 1824/2432
1DH	V_{29}'	$V_2+(V_1-V_2)\times$ 456/2432	V_{29}''	$V_8+(V_7-V_8)\times$ 1976/2432
1EH	V_{30}'	$V_2+(V_1-V_2)\times$ 304/2432	V_{30}''	$V_8+(V_7-V_8)\times$ 2128/2432
1FH	V_{31}'	$V_2+(V_1-V_2)\times$ 152/2432	V_{31}''	$V_8+(V_7-V_8)\times$ 2280/2432
20H	V_{32}'	V_2	V_{32}''	V_7
21H	V_{33}'	$V_3+(V_2-V_3)\times$ 2340/2496	V_{33}''	$V_7+(V_6-V_7)\times$ 156/2496
22H	V_{34}'	$V_3+(V_2-V_3)\times$ 2184/2496	V_{34}''	$V_7+(V_6-V_7)\times$ 312/2496
23H	V_{35}'	$V_3+(V_2-V_3)\times$ 2028/2496	V_{35}''	$V_7+(V_6-V_7)\times$ 468/2496
24H	V_{36}'	$V_3+(V_2-V_3)\times$ 1872/2496	V_{36}''	$V_7+(V_6-V_7)\times$ 624/2496
25H	V_{37}'	$V_3+(V_2-V_3)\times$ 1716/2496	V_{37}''	$V_7+(V_6-V_7)\times$ 780/2496
26H	V_{38}'	$V_3+(V_2-V_3)\times$ 1560/2496	V_{38}''	$V_7+(V_6-V_7)\times$ 936/2496
27H	V_{39}'	$V_3+(V_2-V_3)\times$ 1404/2496	V_{39}''	$V_7+(V_6-V_7)\times$ 1092/2496
28H	V_{40}'	$V_3+(V_2-V_3)\times$ 1248/2496	V_{40}''	$V_7+(V_6-V_7)\times$ 1248/2496
29H	V_{41}'	$V_3+(V_2-V_3)\times$ 1092/2496	V_{41}''	$V_7+(V_6-V_7)\times$ 1404/2496
2AH	V_{42}'	$V_3+(V_2-V_3)\times$ 936/2496	V_{42}''	$V_7+(V_6-V_7)\times$ 1560/2496
2BH	V_{43}'	$V_3+(V_2-V_3)\times$ 780/2496	V_{43}''	$V_7+(V_6-V_7)\times$ 1716/2496
2CH	V_{44}'	$V_3+(V_2-V_3)\times$ 624/2496	V_{44}''	$V_7+(V_6-V_7)\times$ 1872/2496
2DH	V_{45}'	$V_3+(V_2-V_3)\times$ 468/2496	V_{45}''	$V_7+(V_6-V_7)\times$ 2028/2496
2EH	V_{46}'	$V_3+(V_2-V_3)\times$ 312/2496	V_{46}''	$V_7+(V_6-V_7)\times$ 2184/2496
2FH	V_{47}'	$V_3+(V_2-V_3)\times$ 156/2496	V_{47}''	$V_7+(V_6-V_7)\times$ 2340/2496
30H	V_{48}'	V_3	V_{48}''	V_6
31H	V_{49}'	$V_4+(V_3-V_4)\times$ 4397/4572	V_{49}''	$V_6+(V_5-V_6)\times$ 175/4572
32H	V_{50}'	$V_4+(V_3-V_4)\times$ 4222/4572	V_{50}''	$V_6+(V_5-V_6)\times$ 350/4572
33H	V_{51}'	$V_4+(V_3-V_4)\times$ 4047/4572	V_{51}''	$V_6+(V_5-V_6)\times$ 525/4572
34H	V_{52}'	$V_4+(V_3-V_4)\times$ 3872/4572	V_{52}''	$V_6+(V_5-V_6)\times$ 700/4572
35H	V_{53}'	$V_4+(V_3-V_4)\times$ 3697/4572	V_{53}''	$V_6+(V_5-V_6)\times$ 875/4572
36H	V_{54}'	$V_4+(V_3-V_4)\times$ 3465/4572	V_{54}''	$V_6+(V_5-V_6)\times$ 1107/4572
37H	V_{55}'	$V_4+(V_3-V_4)\times$ 3233/4572	V_{55}''	$V_6+(V_5-V_6)\times$ 1339/4572
38H	V_{56}'	$V_4+(V_3-V_4)\times$ 3001/4572	V_{56}''	$V_6+(V_5-V_6)\times$ 1571/4572
39H	V_{57}'	$V_4+(V_3-V_4)\times$ 2769/4572	V_{57}''	$V_6+(V_5-V_6)\times$ 1803/4572
3AH	V_{58}'	$V_4+(V_3-V_4)\times$ 2480/4572	V_{58}''	$V_6+(V_5-V_6)\times$ 2092/4572
3BH	V_{59}'	$V_4+(V_3-V_4)\times$ 2135/4572	V_{59}''	$V_6+(V_5-V_6)\times$ 2437/4572
3CH	V_{60}'	$V_4+(V_3-V_4)\times$ 1733/4572	V_{60}''	$V_6+(V_5-V_6)\times$ 2839/4572
3DH	V_{61}'	$V_4+(V_3-V_4)\times$ 1331/4572	V_{61}''	$V_6+(V_5-V_6)\times$ 3241/4572
3EH	V_{62}'	$V_4+(V_3-V_4)\times$ 872/4572	V_{62}''	$V_6+(V_5-V_6)\times$ 3700/4572
3FH	V_{63}'	V_4	V_{63}''	V_5

Caution There is no connection between V_4 and V_5 terminal in the IC.

6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S_1	S_2	S_3	S_4	...	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

(2) R,/L = L (Left shift)

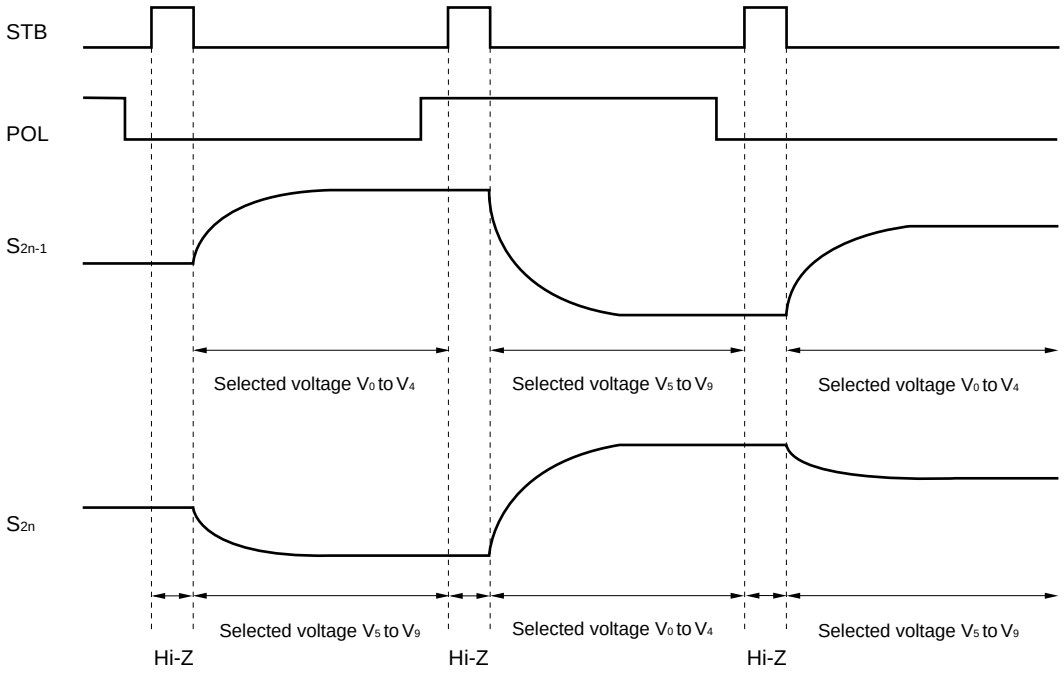
Output	S_1	S_2	S3	S4	...	S_{383}	S_{384}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	D_{30} to D_{35}	...	D_{40} to D_{45}	D_{50} to D_{55}

POL	S_{2n-1} Note	S_{2n} Note
L	V_0 to V_4	V_5 to V_9
H	V_5 to V_9	V_0 to V_4

Note S_{2n-1} (Odd output), S_{2n} (Even output)

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8–1. Output Circuit Block Diagram

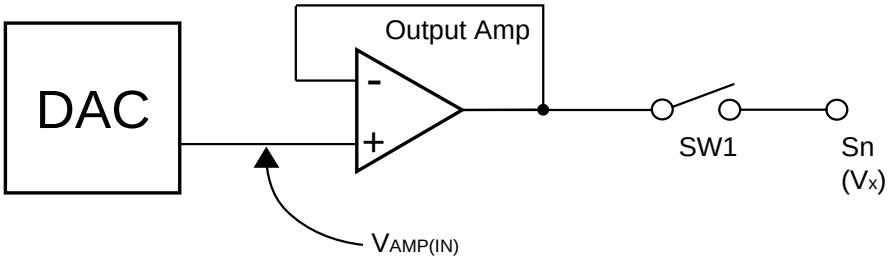
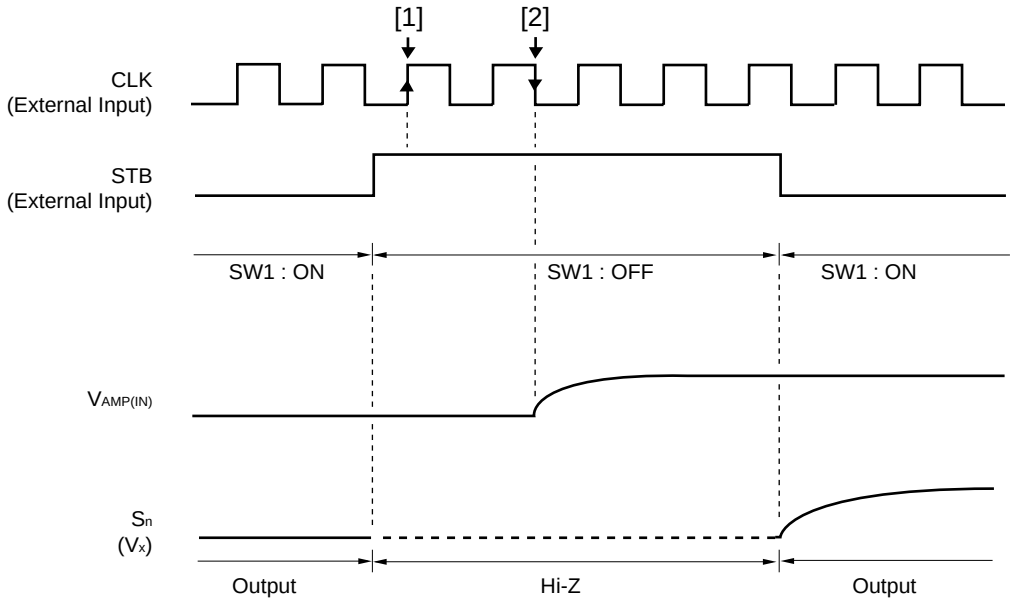


Figure 8–2. Output Circuit Block Diagram



Remarks 1. STB = L: SW1 = ON

STB = H: SW1 = OFF

2. STB = H is acknowledged at timing [1].

3. The display data latch is completed at timing [2] and the input voltage ($V_{AMP(IN)}$: gray-scale level voltage) of the output amplifier changes.

9. CURRENT CONSUMPTION REDUCTION FUNCTION

The μPD16732E has a low power control function (LPC) which can switch the bias current of the output amplifier between two levels and a bias control function (Bcont) which can be used to finely control the bias current.

<Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin. (Bcont: open)

LPC = H or open: normal power mode

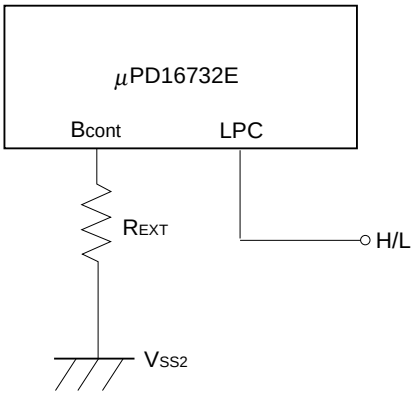
LPC = L: low power mode

The V_{DD2} of static current consumption can be reduced to two thirds of that in normal mode, input a stable DC current (V_{DD1}/V_{SS1}) to this pin.

<Bias current control function (Bcont)>

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential (V_{SS2}) via an external resistor (R_{EXT}). When not using this function, leave this pin open.

Figure 9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control-function.

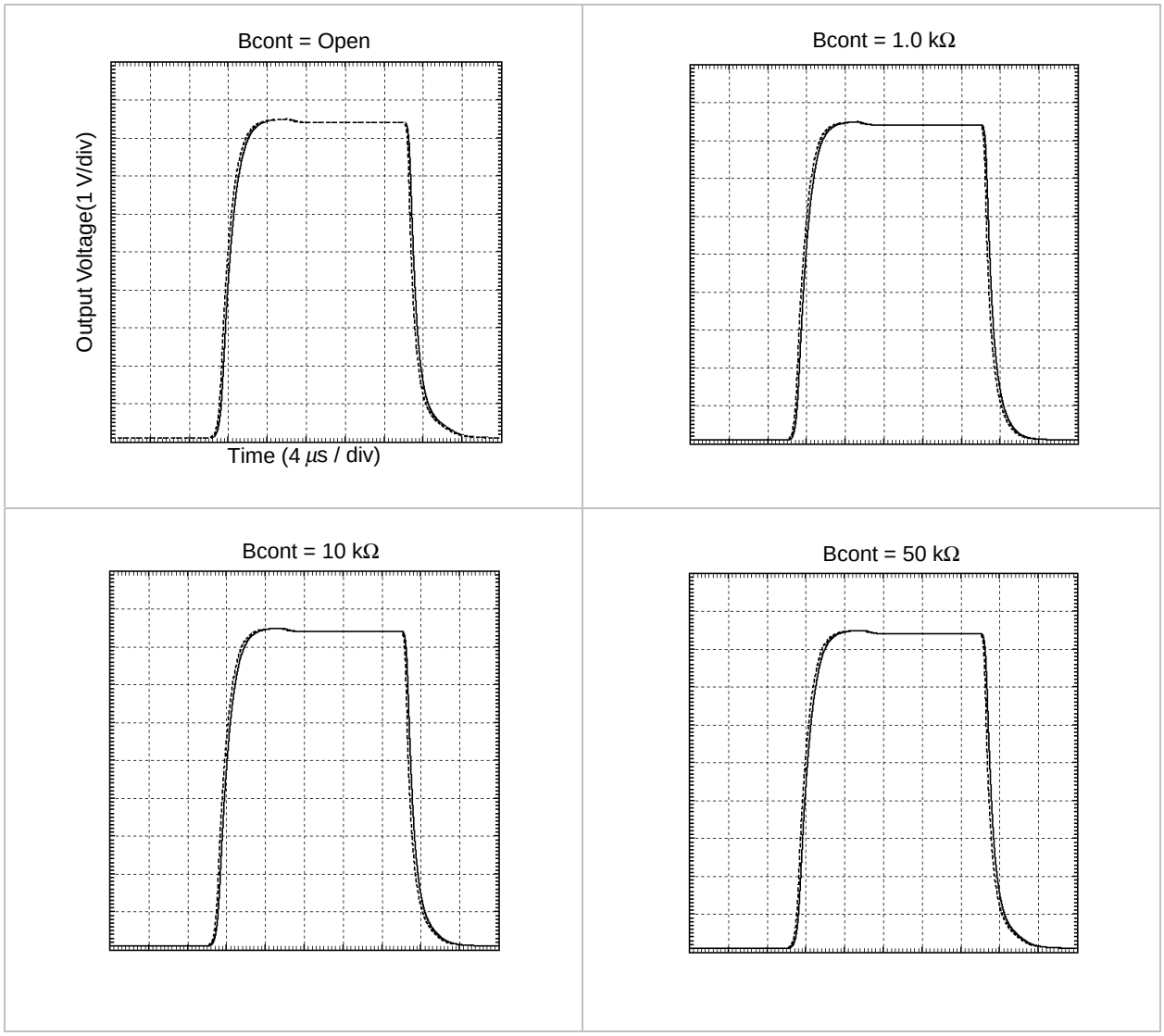
Table 9–1. Current Consumption Regulation Percentage Compared to Normal Mode (V_{DD1} = 3.3 V, V_{DD2} = 8.7 V, LPC = 3.3 V/ 0 V)

R_{EXT} (kΩ)	Current Consumption Regulation Percentage (%)	
	LPC = H	LPC = L
∞ (Open)	100	65
50	110	70
20	115	80
10	120	85

Remark Be aware that the above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

Caution Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

Figure9–2. Output Wave Form (LPC = L)



---------- [1]

———————— [2]

<Test Condition>

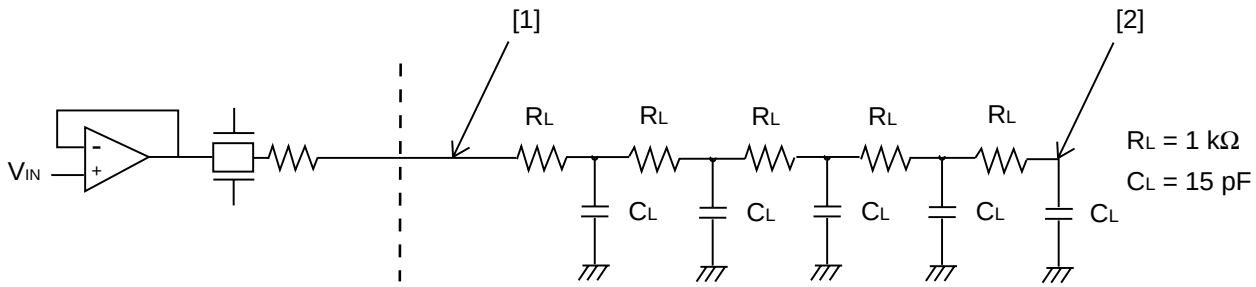
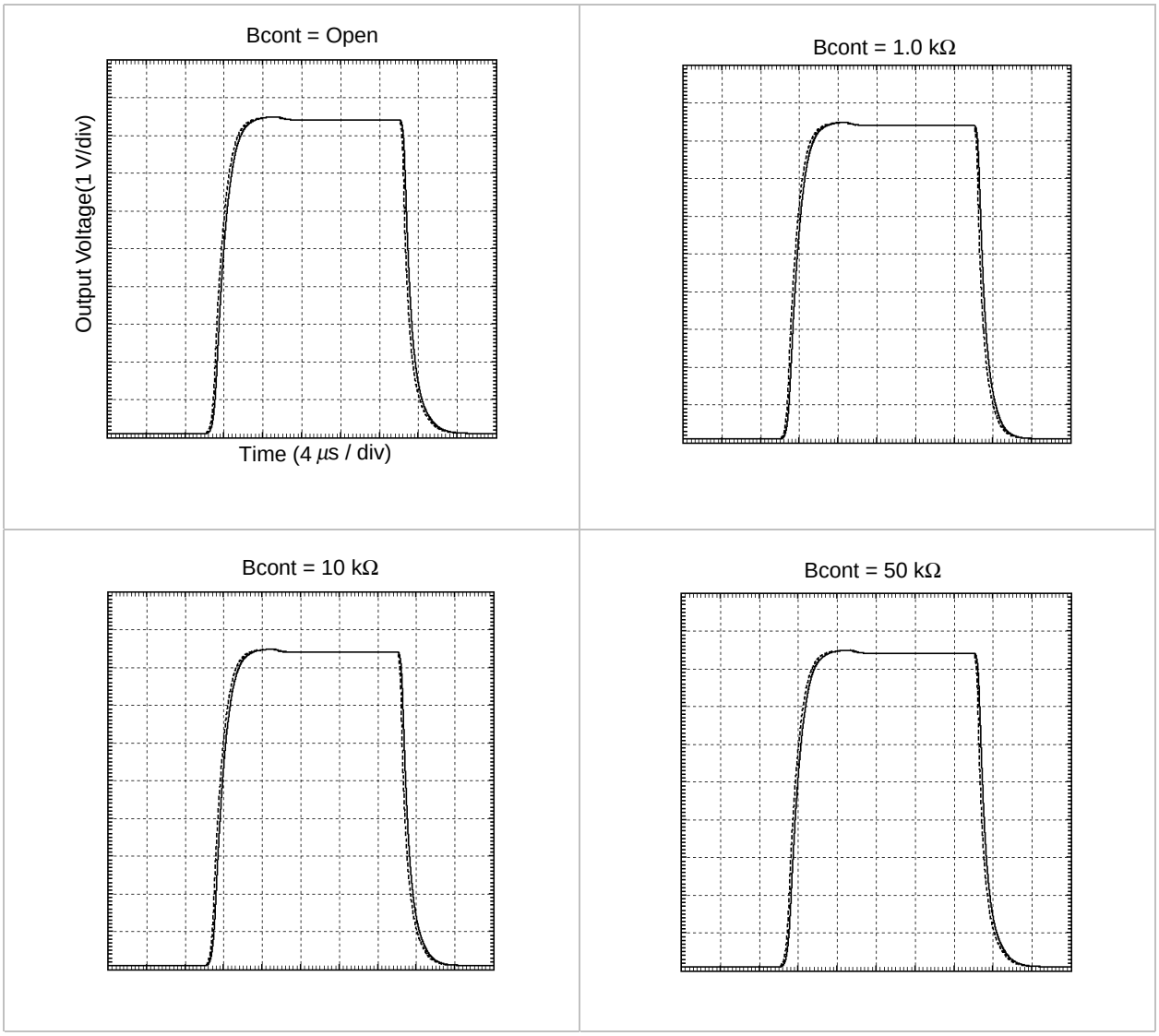


Figure9–3. Output Wave Form (LPC = H)



10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	–0.5 to +4.0	V
Driver Part Supply Voltage	V_{DD2}	–0.5 to +10.0	V
Logic Part Input Voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Input Voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +75	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V_{DD1}		2.3		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.0	8.5	9.0	V
High-Level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V
γ-Corrected Voltage	V_0 to V_4		0.5 V_{DD2}		V_{DD2} – 0.1	V
	V_5 to V_9		V_{SS2} + 0.1		0.5 V_{DD2}	V
Driver Part Output Voltage	V_O		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Clock Frequency	f_{CLK}	2.3 ≤ V_{DD1} < 3.0 V			45	MHz
		3.0 ≤ V_{DD1} ≤ 3.6 V			65	MHz

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.0 to 9.0 V, V_{SS1} = V_{SS2} = 0 V, Unless otherwise specified, LPC = H or open, Bcont = open)

	Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
	Input Leak Current	I_{IL}				±1.0	μA
	High-Level Output Voltage	V_{OH}	STHR (STHL), I_{OH} = 0 mA	V_{DD1} – 0.1			V
	Low-Level Output Voltage	V_{OL}	STHR (STHL), I_{OL} = 0 mA			0.1	V
★	γ-Corrected Resistance	R_γ	V_0 to V_4 = V_5 to V_9 = 4.0 V	8	16	32	Ω
	Driver Output Current	I_{VOH}	V_X = 7.0 V, V_{OUT} = 6.5 V Note			–30	μA
		I_{VOL}	V_X = 1.0 V, V_{OUT} = 1.5 V Note	30			μA
	Output Voltage Deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 8.5 V		±7	±20	mV
	Output Swing Difference Deviation	ΔV_{P-P}	V_{OUT} = 2.0 V, 4.25 V, 6.5 V		±2	±15	mV
	Output Voltage Range	V_O	All input data	0.1		V_{DD2} – 0.1	V
★	Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load		3.0	6.0	mA
★	Driver Part Dynamic Current Consumption	I_{DD21}	V_{DD2} = 8.0 to 9.0 V, with no load, LPC =H, Bcont = open		1.0	6.0	mA
		I_{DD22}	V_{DD2} = 8.0 to 9.0 V, with no load, LPC =L, Bcont = open		2.0	4.0	mA

Note V_X refers to the output voltage of analog output pins S_1 to S_{384}.

V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

Cautions 1. STB cycle is 20 μs, f_{CLK} = 40 MHz

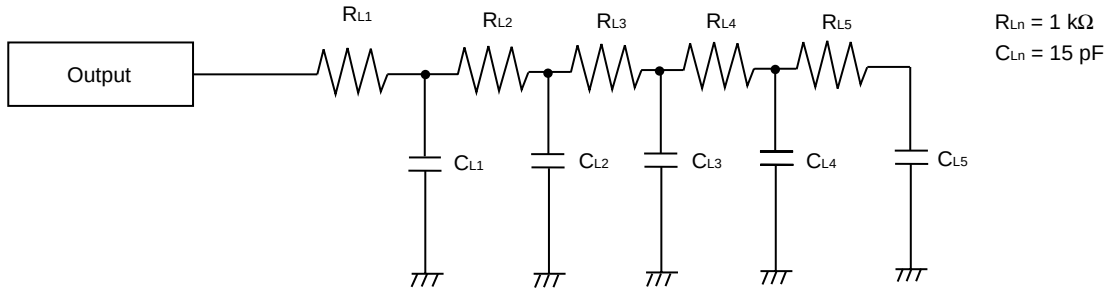
2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.

3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 8.0 to 9.0 V, V_{SS1} = V_{SS2} = 0 V, Unless otherwise specified, LPC = H or open, Bcont = open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t_{PLH1}	C_L = 10 pF, 2.3 ≤ V_{DD1} < 3.0 V		10	17	ns
		C_L = 10 pF, 3.0 ≤ V_{DD1} ≤ 3.6 V		7	10.5	ns
Driver Output Delay Time	t_{PLH2}	C_L = 75 pF, R_L = 5 kΩ		2.5	5	μs
	t_{PLH3}			5	8	μs
	t_{PHL2}			2.5	5	μs
	t_{PHL3}			5	8	μs
Input Capacitance	C_{I1}	Exclude STHR (STHL), T_A = 25°C		5	10	pF
	C_{I2}	STHR (STHL), T_A = 25°C		8	10	pF

<Test Condition>



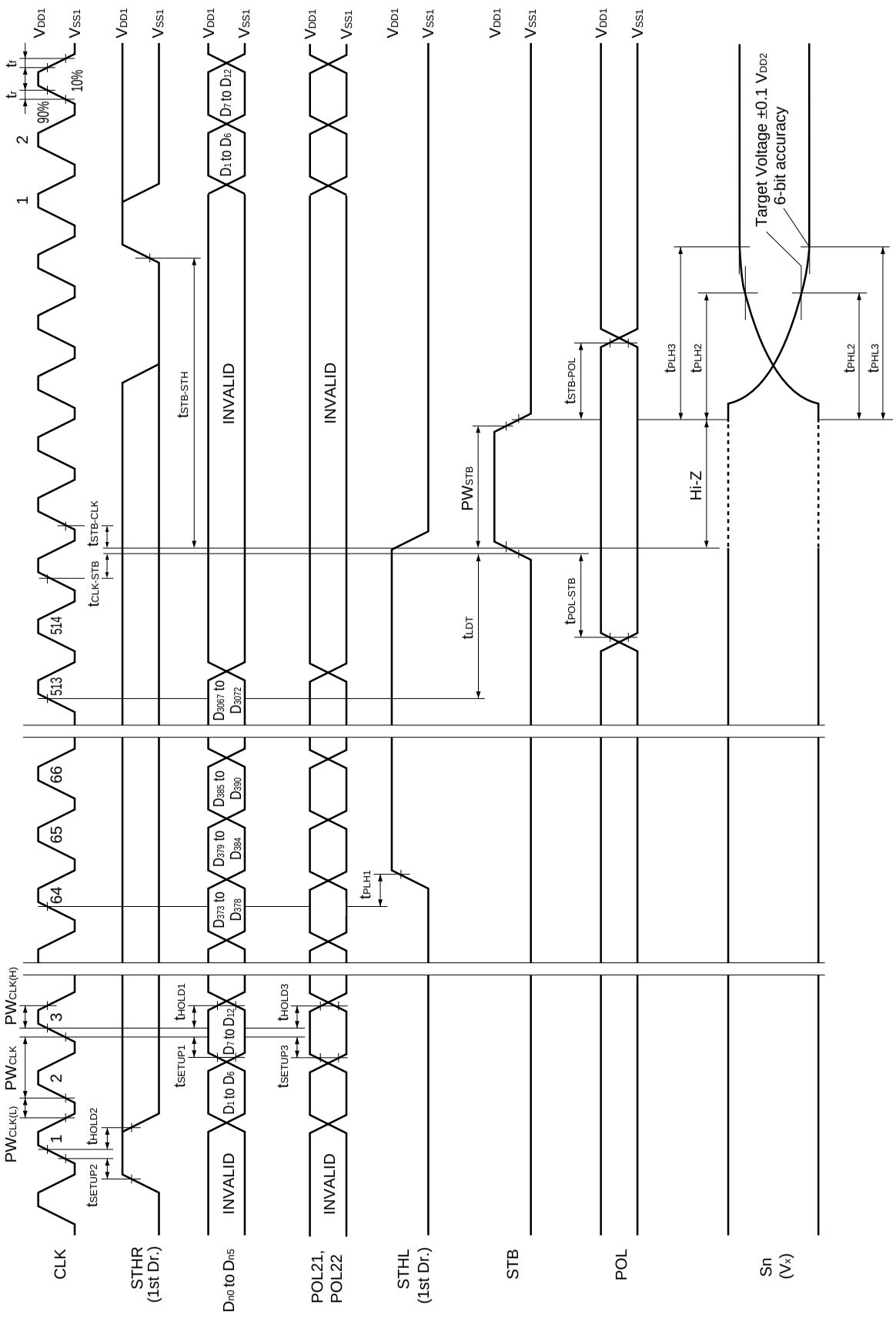
Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{SS1} = 0 V, t_r = t_f = 8.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	2.3 ≤ V_{DD1} < 3.0 V	22			ns
		3.0 ≤ V_{DD1} ≤ 3.6 V	15			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	2.3 ≤ V_{DD1} < 3.0 V	6			ns
		3.0 ≤ V_{DD1} ≤ 3.6 V	4			ns
Data Setup Time	t_{SETUP1}		4			ns
Data Hold Time	t_{HOLD1}		0			ns
Start Pulse Setup Time	t_{SETUP2}		4			ns
Start Pulse Hold Time	t_{HOLD2}		0			ns
POL21/22 Setup Time	t_{SETUP3}		4			ns
POL21/22 Hold Time	t_{HOLD3}		0			ns
STB Pulse Width	PW_{STB}		2			CLK
Last Data Timing	t_{LDT}		2			CLK
CLK-STB Time	$t_{CLK-STB}$	CLK ↑ → STB ↑	6			ns
STB-CLK Time	$t_{STB-CLK}$	STB ↑ → CLK ↑, V_{DD1} = 2.3 to 3.6 V	9			ns
		STB ↑ → CLK ↑, V_{DD1} = 3.0 to 3.6 V	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	STB ↑ → STHR(STHL) ↑	2			CLK
POL-STB Time	$t_{POL-STB}$	POL ↑ or ↓ → STB ↑	–5			ns
STB-POL Time	$t_{STB-POL}$	STB ↓ → POL ↓ or ↑	6			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Switching Characteristic Waveform(R,/L= H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



11. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16732E.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16732EN-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm^2: time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm^2: time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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