

### 480/420-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

#### DESCRIPTION

The  $\mu$  PD16718 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values  $\gamma$ -corrected by an internal D/A converter and 7-by-2 external power modules. Because the output dynamic range is as large as  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 57 MHz when driving at 2.5 V, this driver is applicable to SXGA+/UXGA-standard TFT-LCD panels.

#### FEATURES

- CMOS level input (2.5 to 3.6 V)
- 480/420 Outputs
- Input of 6 bits (gray scale data) by 6 dots
- Capable of outputting 64 values by means of 7-by-2 external power modules (14 units) and a D/A converter (R-DAC)
- Logic power supply voltage ( $V_{DD1}$ ): 2.5 to 3.6 V
- Driver power supply voltage ( $V_{DD2}$ ): 10.0 to 12.5 V
- Output dynamic range  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V
- High-speed data transfer:  $f_{CLK} = 57$  MHz (internal data transfer speed when operating at  $V_{DD1} = 2.5$  V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (capable of controlling by each input port) (POL21, POL22)
- Current consumption control function (LPC)
- TCP/COF package

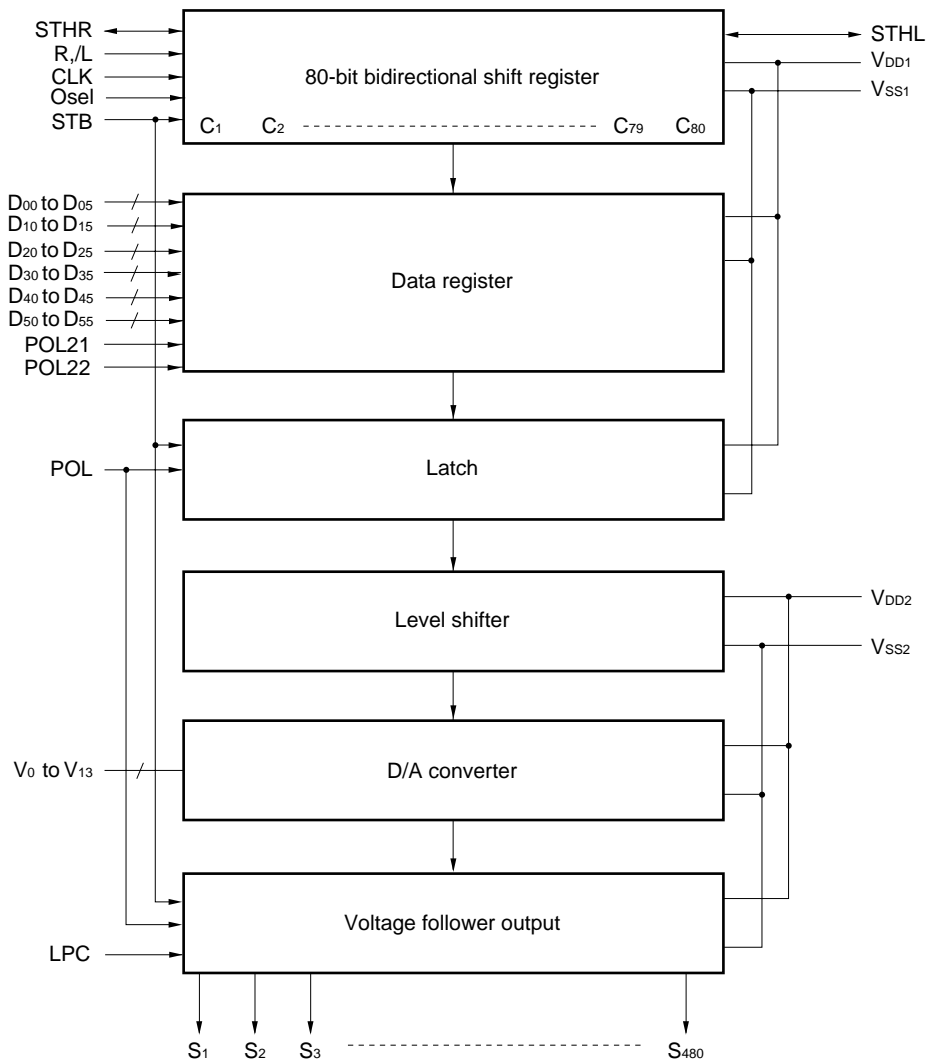
#### ★ ORDERING INFORMATION

Part Number	Package
$\mu$ PD16718N-xxx	TCP (TAB package)
$\mu$ PD16718NL-xxx	COF (Chip on Film) package

**Remark** Consult an our sales representative regarding the TCP/COF.

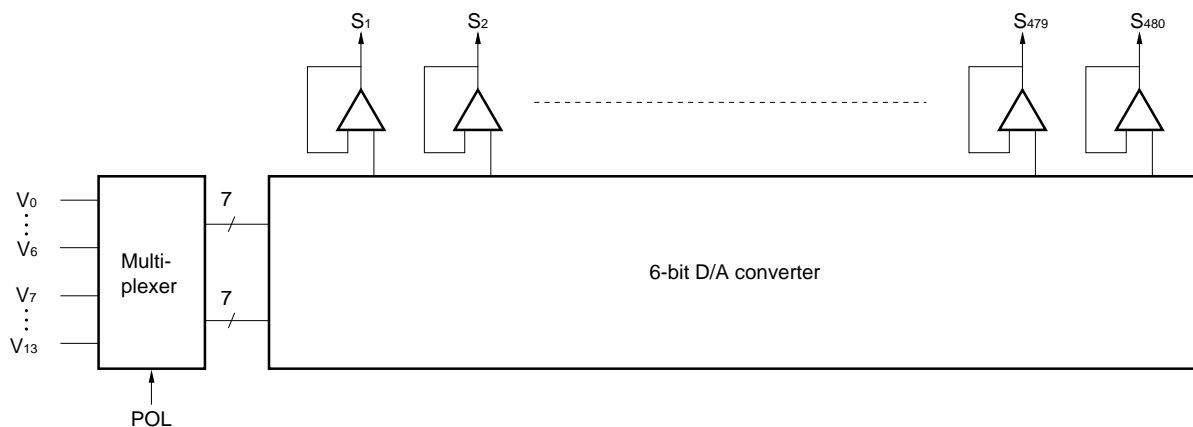
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★ 1. BLOCK DIAGRAM

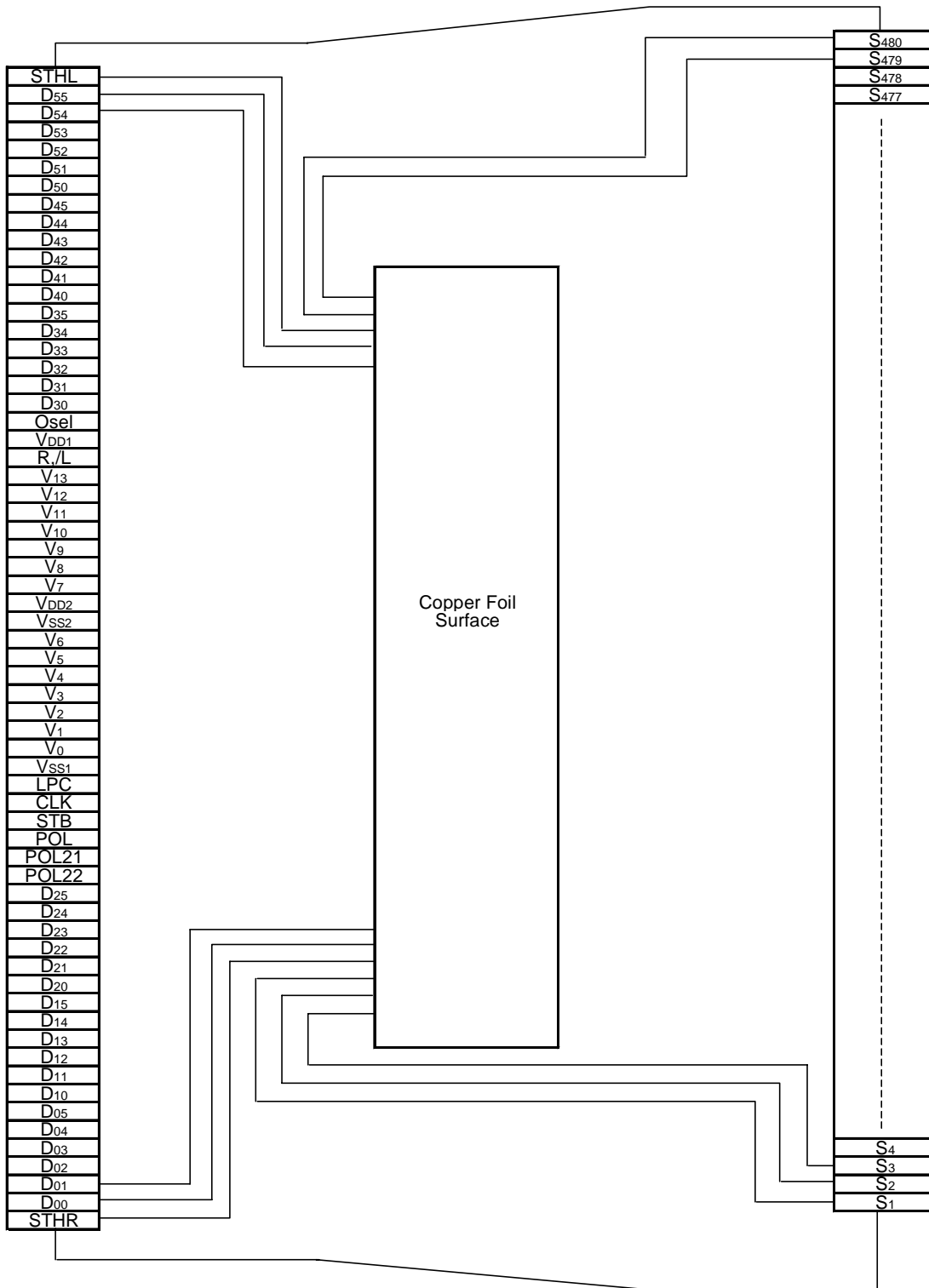


Remark /xxx indicates active low signal.

★ 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD16718) (Copper Foil Surface, Face-up)



**Remark** This figure does not specify the TCP/COF package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S <sub>1</sub> to S <sub>480</sub>	Driver	Output	The D/A converted 64-gray-scale analog voltage is output.
D <sub>00</sub> to D <sub>05</sub>	Display data	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D <sub>X0</sub> : LSB, D <sub>X5</sub> : MSB
D <sub>10</sub> to D <sub>15</sub>			
D <sub>20</sub> to D <sub>25</sub>			
D <sub>30</sub> to D <sub>35</sub>			
D <sub>40</sub> to D <sub>45</sub>			
D <sub>50</sub> to D <sub>55</sub>			
R, <sub>/</sub> L	Shift direction control	Input	Refers to the shift direction control. The shift directions of the shift registers are as follows. R, <sub>/</sub> L = H: STHR input, S <sub>1</sub> → S <sub>480</sub> , STHL output R, <sub>/</sub> L = L: STHL input, S <sub>480</sub> → S <sub>1</sub> , STHR output This pin is pulled up to power supply V <sub>DD1</sub> inside IC.
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade. Loading of display data starts when H is read at the rising edge of CLK. R, <sub>/</sub> L = H (right shift): STHR input, STHL output R, <sub>/</sub> L = L (left shift): STHL input, STHR output
STHL	Left shift start pulse	I/O	A high level should be input as the pulse of one cycle of the clock signal. If the start pulse input is more than 2 CLK, the first 1 CLK of the high-level input is valid.
CLK	Shift clock	Input	Refers to the shift register's shift clock input. The display data is loaded into the data register at the rising edge. At the rising edge of the 80(70) clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. If 82(72)-clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge. ( ) indicates 420 output.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	Input	POL = L : The S <sub>2n-1</sub> output uses V <sub>0</sub> to V <sub>6</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>7</sub> to V <sub>13</sub> as the reference supply. POL = H : The S <sub>2n-1</sub> output uses V <sub>7</sub> to V <sub>13</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>0</sub> to V <sub>6</sub> as the reference supply. S <sub>2n-1</sub> indicates the odd output: and S <sub>2n</sub> indicates the even output. Input of the POL signal is allowed the setup time (t <sub>POL-STB</sub> ) with respect to STB's rising edge.
★ POL21, POL22	Data inversion	Input	Data inversion can invert when display data is loaded. POL21: Invert/not invert of display data D <sub>00</sub> to D <sub>05</sub> , D <sub>10</sub> to D <sub>15</sub> , D <sub>20</sub> to D <sub>25</sub> . POL22: Invert/not invert of display data D <sub>30</sub> to D <sub>35</sub> , D <sub>40</sub> to D <sub>45</sub> , D <sub>50</sub> to D <sub>55</sub> . POL21, POL22 = H: Display data is inverted inside the μ PD16718. POL21, POL22 = L: Display data is not inverted.
Osel	Number of output pins select	input	Osel = H: driver output = 480 ch Osel = L or open: driver output = 420 ch (Output pins S <sub>211</sub> to S <sub>270</sub> are invalid) This pin is pulled down to power supply V <sub>DD1</sub> inside IC.

(2/2)

Pin Symbol	Pin Name	I/O	Description
LPC	Low power control	Input	The current consumption is lowered by controlling the constant current source of the output amplifier and reduced $V_{DD2}$ of normal current. LPC = H or open: Normal power mode LPC = L: Low power mode (about 3/4 of the normal current consumption) This pin is pulled up to the $V_{DD1}$ power supply inside IC.
$V_0$ to $V_{13}$	$\gamma$ -corrected power supplies	–	Input the $\gamma$ -corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1\text{ V}$ and $0.45 \times V_{DD2} \leq V_6 = V_7 \leq 0.55 \times V_{DD2}$ or $V_{DD2} - 0.1\text{ V} \geq V_6 > V_5 > V_4 > V_3 > V_2 > V_1 > V_0 \geq V_{13} > V_{12} > V_{11} > V_{10} > V_9 > V_8 > V_7 \geq V_{SS2} + 0.1\text{ V}$ and $0.45 \times V_{DD2} \leq V_0 = V_{13} \leq 0.55 \times V_{DD2}$
$V_{DD1}$	Logic power supply	–	2.5 to 3.6 V
$V_{DD2}$	Driver power supply	–	10.0 to 12.5 V
$V_{SS1}$	Logic ground	–	Grounding
$V_{SS2}$	Driver ground	–	Grounding

**Cautions** 1. The power start sequence must be  $V_{DD1}$ , logic input, and  $V_{DD2}$  &  $V_0$  to  $V_{13}$  in that order.

Reverse this sequence to shut down. (Simultaneous power application to  $V_{DD2}$  and  $V_0$  to  $V_9$  is possible.)

2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between  $V_{DD1}$ - $V_{SS1}$  and  $V_{DD2}$ - $V_{SS2}$ . Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the  $\gamma$ -corrected power supply terminals ( $V_0, V_1, V_2, \dots, V_{13}$ ) and  $V_{SS2}$ .

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel  $\gamma$ -compensated voltages to  $V_0'$  to  $V_{63}'$  and  $V_0''$  to  $V_{63}''$  is almost equivalent. For the 2 sets of seven  $\gamma$ -compensated power supplies,  $V_0$  to  $V_6$  and  $V_7$  to  $V_{13}$ , respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the  $\gamma$ -compensated power supplies  $V_0$  to  $V_6$  and  $V_7$  to  $V_{13}$ .

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages  $V_{DD2}$  and  $V_{SS2}$ , common electrode potential  $V_{COM}$ , and  $\gamma$ -corrected voltages  $V_0$  to  $V_{13}$  and the input data. Be sure to maintain the voltage relationships as follows:

$$V_{DD2} - 0.1 \text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1 \text{ V} \text{ and}$$

$$0.45 \times V_{DD2} \leq V_6 = V_7 \leq 0.55 \times V_{DD2} \text{ or}$$

$$V_{DD2} - 0.1 \text{ V} \geq V_6 > V_5 > V_4 > V_3 > V_2 > V_1 > V_0 \geq V_{13} > V_{12} > V_{11} > V_{10} > V_9 > V_8 > V_7 \geq V_{SS2} + 0.1 \text{ V} \text{ and}$$

$$0.45 \times V_{DD2} \leq V_0 = V_{13} \leq 0.55 \times V_{DD2}$$

positive side  $> 0.5 V_{DD2} - 0.5V$ , negative side  $> 0.5 V_{DD2} + 0.5 V$ .

Figures 5-2 and 5-3 show the relationship between input data and output voltage. This driver IC is designed for only single-sided mounting

Figure 5-1. Relationship between Input Data and  $\gamma$ - corrected Power Supply

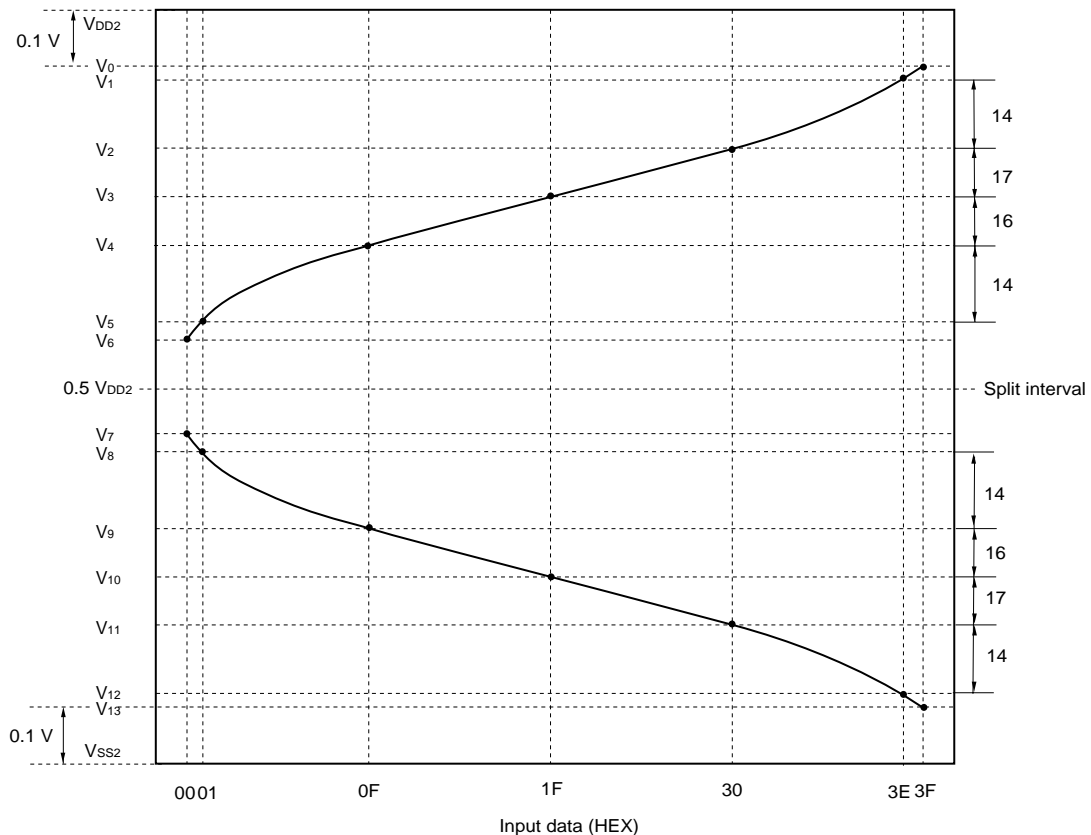
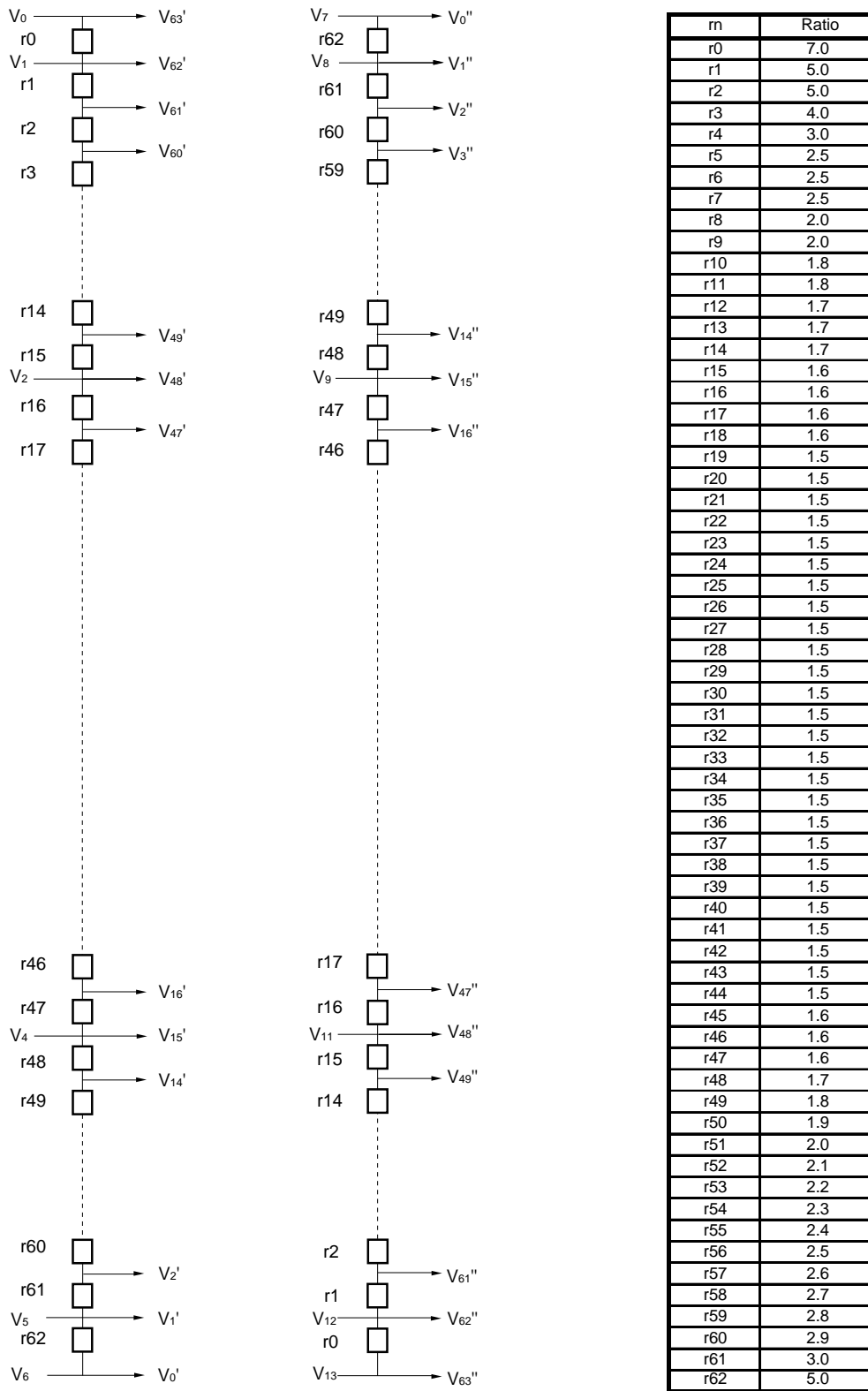


Figure 5-2.  $\gamma$ -corrected Voltages and Ladder Resistors Ratio



**Caution** There is no connection between  $V_6$  and  $V_7$  terminal in the chip.

Figure 5-3. Relationship between Input Data and Output Voltage (POL21, POL22 = L)

(Output Voltage 1)  $V_{DD2} - 0.1\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 \geq 0.5 V_{DD2} - 0.5\text{ V}$

(Output Voltage 2)  $0.5 V_{DD2} + 0.5\text{ V} \geq V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} \geq V_{SS2} + 0.1\text{ V}$

Input Data	Output Voltage1		Output Voltage2	
00H	V <sub>0'</sub>	V <sub>6</sub>	V <sub>0'</sub>	V <sub>7</sub>
01H	V <sub>1'</sub>	V <sub>5</sub>	V <sub>1'</sub>	V <sub>8</sub>
02H	V <sub>2'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>2'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
03H	V <sub>3'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>3'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
04H	V <sub>4'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>4'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
05H	V <sub>5'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>5'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
06H	V <sub>6'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>6'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
07H	V <sub>7'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>7'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
08H	V <sub>8'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>8'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
09H	V <sub>9'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>9'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0AH	V <sub>10'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>10'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0BH	V <sub>11'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>11'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0CH	V <sub>12'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>12'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0DH	V <sub>13'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>13'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0EH	V <sub>14'</sub>	V <sub>5</sub> +(V <sub>4</sub> -V <sub>5</sub> )×	V <sub>14'</sub>	V <sub>9</sub> +(V <sub>8</sub> -V <sub>9</sub> )×
0FH	V <sub>15'</sub>	V <sub>4</sub>	V <sub>15'</sub>	V <sub>9</sub>
10H	V <sub>16'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>16'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
11H	V <sub>17'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>17'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
12H	V <sub>18'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>18'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
13H	V <sub>19'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>19'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
14H	V <sub>20'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>20'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
15H	V <sub>21'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>21'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
16H	V <sub>22'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>22'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
17H	V <sub>23'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>23'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
18H	V <sub>24'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>24'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
19H	V <sub>25'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>25'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1AH	V <sub>26'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>26'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1BH	V <sub>27'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>27'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1CH	V <sub>28'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>28'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1DH	V <sub>29'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>29'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1EH	V <sub>30'</sub>	V <sub>4</sub> +(V <sub>3</sub> -V <sub>4</sub> )×	V <sub>30'</sub>	V <sub>10</sub> +(V <sub>9</sub> -V <sub>10</sub> )×
1FH	V <sub>31'</sub>	V <sub>3</sub>	V <sub>31'</sub>	V <sub>10</sub>
20H	V <sub>32'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>32'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
21H	V <sub>33'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>33'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
22H	V <sub>34'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>34'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
23H	V <sub>35'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>35'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
24H	V <sub>36'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>36'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
25H	V <sub>37'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>37'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
26H	V <sub>38'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>38'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
27H	V <sub>39'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>39'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
28H	V <sub>40'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>40'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
29H	V <sub>41'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>41'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2AH	V <sub>42'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>42'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2BH	V <sub>43'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>43'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2CH	V <sub>44'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>44'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2DH	V <sub>45'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>45'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2EH	V <sub>46'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>46'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
2FH	V <sub>47'</sub>	V <sub>3</sub> +(V <sub>2</sub> -V <sub>3</sub> )×	V <sub>47'</sub>	V <sub>11</sub> +(V <sub>10</sub> -V <sub>11</sub> )×
30H	V <sub>48'</sub>	V <sub>2</sub>	V <sub>48'</sub>	V <sub>11</sub>
31H	V <sub>49'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>49'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
32H	V <sub>50'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>50'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
33H	V <sub>51'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>51'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
34H	V <sub>52'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>52'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
35H	V <sub>53'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>53'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
36H	V <sub>54'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>54'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
37H	V <sub>55'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>55'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
38H	V <sub>56'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>56'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
39H	V <sub>57'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>57'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
3AH	V <sub>58'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>58'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
3BH	V <sub>59'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>59'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
3CH	V <sub>60'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>60'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
3DH	V <sub>61'</sub>	V <sub>2</sub> +(V <sub>1</sub> -V <sub>2</sub> )×	V <sub>61'</sub>	V <sub>12</sub> +(V <sub>11</sub> -V <sub>12</sub> )×
3EH	V <sub>62'</sub>	V <sub>1</sub>	V <sub>62'</sub>	V <sub>12</sub>
3FH	V <sub>63'</sub>	V <sub>0</sub>	V <sub>63'</sub>	V <sub>13</sub>

Caution There is no connection between V<sub>6</sub> and V<sub>7</sub> terminal in the chip.



6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)

Input width: 36 bits (2-pixel data)

R,/L = H (Right shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>479</sub>	S <sub>480</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	...	D <sub>40</sub> to D <sub>45</sub>	D <sub>50</sub> to D <sub>55</sub>

R,/L = L (Left shift)

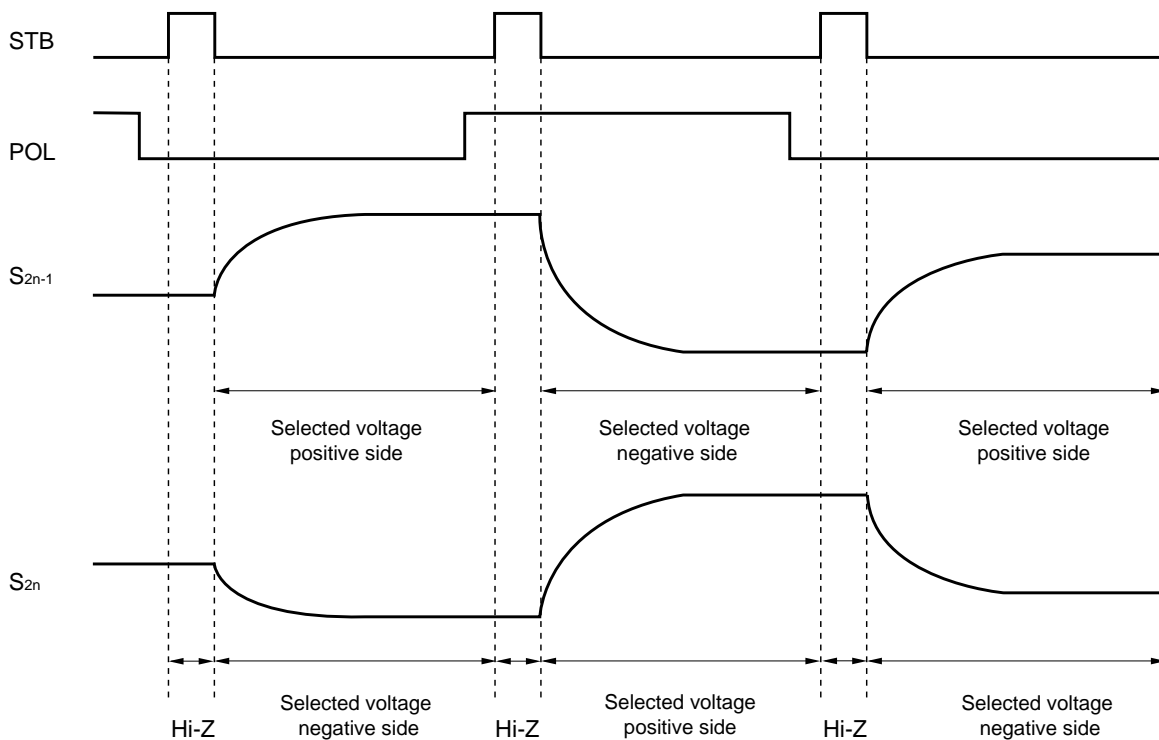
Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>479</sub>	S <sub>480</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	...	D <sub>40</sub> to D <sub>45</sub>	D <sub>50</sub> to D <sub>55</sub>

POL	S <sub>2n-1</sub> <small>Note</small>	S <sub>2n</sub> <small>Note</small>
L	V <sub>0</sub> to V <sub>6</sub>	V <sub>7</sub> to V <sub>13</sub>
H	V <sub>7</sub> to V <sub>13</sub>	V <sub>0</sub> to V <sub>6</sub>

Note S<sub>2n-1</sub> (Odd output), S<sub>2n</sub> (Even output)

★ 7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



## 8. CURRENT CONSUMPTION REDUCTION FUNCTION

The  $\mu$ PD16718 has a low power control function (LPC) which can switch the bias current of the output amplifier between two levels.

### <Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin.

LPC = H or open: low power mode

LPC = L: normal power mode

The  $V_{DD2}$  of static current consumption can be reduced to two thirds of that in normal mode, input a stable DC current ( $V_{DD1}/V_{SS1}$ ) to this pin.

9. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>	-0.5 to +4.0	V
Driver Part Supply Voltage	V <sub>DD2</sub>	-0.5 to +17.0	V
Logic Part Input Voltage	V <sub>I1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Input Voltage	V <sub>I2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Logic Part Output Voltage	V <sub>O1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Output Voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Operating Ambient Temperature	T <sub>A</sub>	-10 to +75	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Range (T<sub>A</sub> = -10 to +75°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>		2.5	3.3	3.6	V
Driver Part Supply Voltage	V <sub>DD2</sub>		10.0	11.5	12.5	V
High-Level Input Voltage	V <sub>IH</sub>		0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Input Voltage	V <sub>IL</sub>		0		0.3 V <sub>DD1</sub>	V
γ-Corrected Voltage	V <sub>0</sub> to V <sub>13</sub>		0.1		V <sub>DD2</sub> - 0.1	V
Driver Part Output Voltage	V <sub>O</sub>		0.1		V <sub>DD2</sub> - 0.1	V
Clock Frequency	f <sub>CLK</sub>	V <sub>DD1</sub> = 2.5 V			57	MHz

**Electrical Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 2.5 to 3.6 V, V<sub>DD2</sub> = 10.0 to 12.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V, LPC = L)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I <sub>IL</sub>	Except Osel, LPC, R,/L			±1.0	μA
Pull-up Resistance Value	R <sub>PU</sub>	LPC, R,/L	100	190	500	kΩ
Pull-downResistance Value	R <sub>PD</sub>	Osel	25	50	150	kΩ
High-Level Output Voltage	V <sub>OH</sub>	STHR (STHL), I <sub>OH</sub> = 0 mA	V <sub>DD1</sub> - 0.1			V
Low-Level Output Voltage	V <sub>OL</sub>	STHR (STHL), I <sub>OL</sub> = 0 mA			0.1	V
γ-Corrected Resistance	I <sub>γ</sub>	V <sub>DD2</sub> = 12.5 V, V <sub>O</sub> to V <sub>6</sub> = V <sub>7</sub> to V <sub>13</sub> = 5.0 V	8.7	14.5	20.3	kΩ
Driver Output Current	I <sub>VOH</sub>	V <sub>X</sub> = 11.0 V, V <sub>OUT</sub> = 10.5 V <sup>Note</sup>		-50	-20	μA
	I <sub>VOL</sub>	V <sub>X</sub> = 0.5 V, V <sub>OUT</sub> = 1.0 V <sup>Note</sup>	20	55		μA
Output Voltage Deviation	ΔV <sub>O</sub>	V <sub>O</sub> = 1.2 V to V <sub>DD2</sub> - 1.2 V		±10	±20	mV
		V <sub>O</sub> = 1.0 to 1.2 V		±13	±25	mV
		V <sub>O</sub> = V <sub>DD2</sub> - 1.2 V to V <sub>DD2</sub> - 1.0 V				
Output swing difference deviation	ΔV <sub>P-P1</sub>	V <sub>O</sub> = 5.4 V to V <sub>DD2</sub> - 5.4 V		±5	±10	mV
		V <sub>O</sub> = 1.9 to 5.4 V		±8	±15	mV
		V <sub>O</sub> = V <sub>DD2</sub> - 5.4 V to V <sub>DD2</sub> - 1.9 V				
	ΔV <sub>P-P3</sub>	V <sub>O</sub> = 1.0 to 1.9 V		±15	±20	mV
		V <sub>O</sub> = V <sub>DD2</sub> - 1.0 V to V <sub>DD2</sub> - 1.9 V				
Logic Part Dynamic Current Consumption	I <sub>DD1</sub>	V <sub>DD1</sub> = 3.3 V		0.6	11	mA
Driver Part Dynamic Current Consumption	I <sub>DD2</sub>	V <sub>DD2</sub> = 11.5 V, with no load, LPC = L		5.4	10	mA

**Note** V<sub>X</sub> refers to the output voltage of analog output pins S<sub>1</sub> to S<sub>480</sub>.

V<sub>OUT</sub> refers to the voltage applied to analog output pins S<sub>1</sub> to S<sub>480</sub>.

**Cautions** 1. f<sub>STB</sub> = 50 kHz, f<sub>CLK</sub> = 40 MHz.

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
3. Refers to the current consumption per driver when cascades are connected under the assumption of UXGA single-sided mounting (10 units).

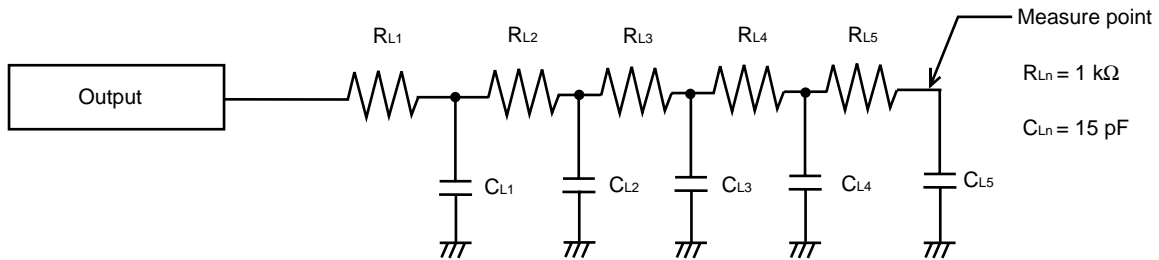
**Electrical Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 2.5 to 3.6 V, V<sub>DD2</sub> = 10.0 to 12.5 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V, LPC = L)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	t <sub>PLH1</sub>	C <sub>L</sub> = 15 pF			15	ns
	t <sub>PKL1</sub>				15	ns
Driver Output Delay Time	t <sub>PLH2</sub> <sup>Note1</sup>	C <sub>L</sub> = 75 pF, R <sub>L</sub> = 5 kΩ		3.8	6	μs
	t <sub>PLH3</sub> <sup>Note2</sup>			6.7	10	μs
	t <sub>PHL2</sub> <sup>Note1</sup>			3.8	6	μs
	t <sub>PHL3</sub> <sup>Note2</sup>			6.1	10	μs
Input Capacitance	C <sub>I1</sub>	STHR (STHL) excluded, T <sub>A</sub> = 25°C			10	pF
	C <sub>I2</sub>	STHR (STHL), T <sub>A</sub> = 25°C			15	pF

**Notes 1.** t<sub>PLH2</sub>/t<sub>PHL2</sub> are specified as the time it takes to reach the target voltage ±10% (condition: V<sub>O</sub> = 0.1 to 12.4 V).

**2.** t<sub>PLH3</sub>/t<sub>PHL3</sub> are specified as the time it takes to reach the target voltage ±2% (condition: V<sub>O</sub> = 0.1 to 12.4 V).

★ <Measurement Condition>



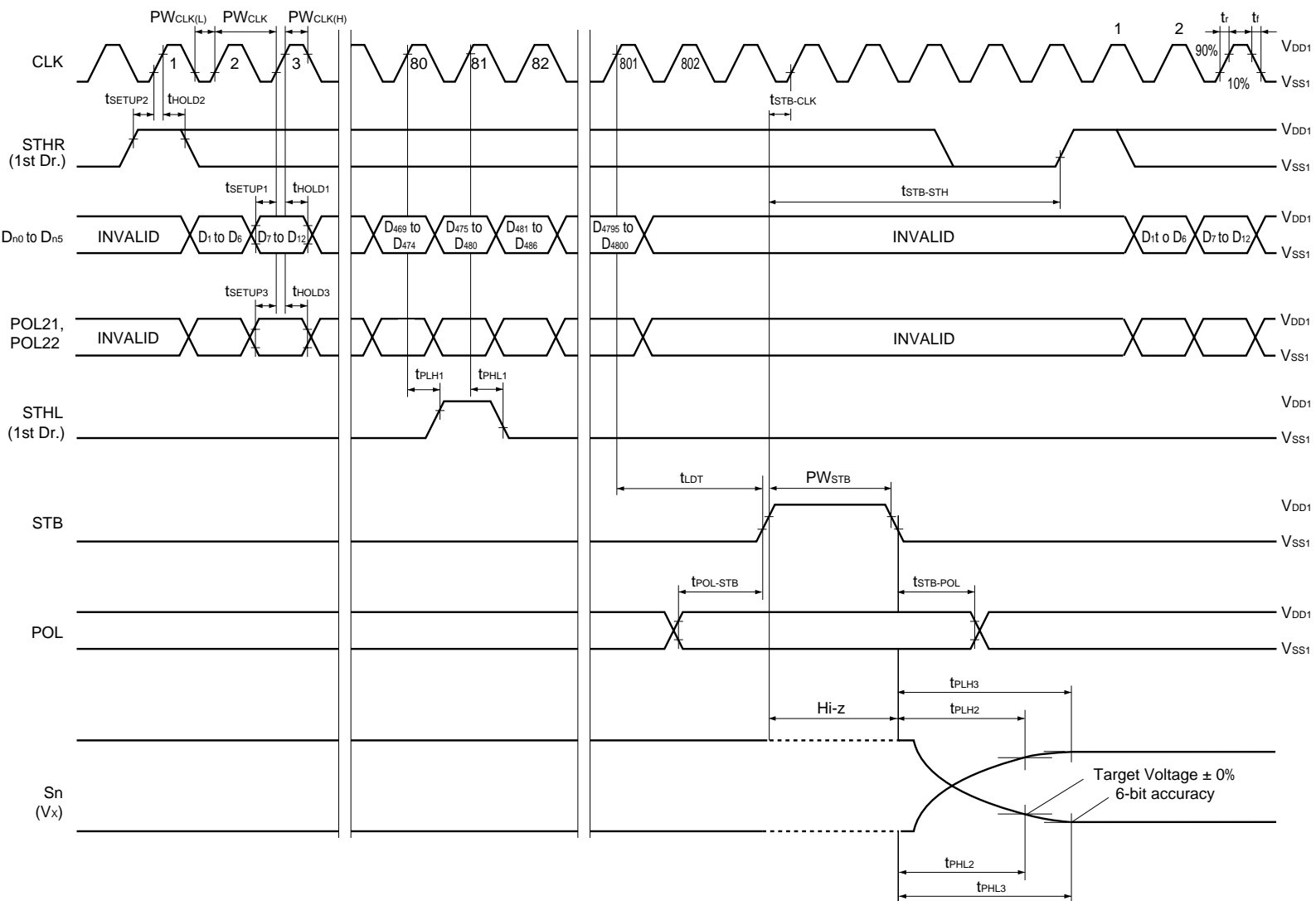
**Timing Requirement ( $T_A = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD1} = 2.5$  to  $3.6$  V,  $V_{SS1} = 0$  V,  $t_r = t_f = 5.0$  ns)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	$PW_{CLK}$		17			ns
Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
Clock Pulse Low Period	$PW_{CLK(L)}$		4			ns
Data Setup Time	$t_{SETUP1}$		3			ns
Data Hold Time	$t_{HOLD1}$		0			ns
Start Pulse Setup Time	$t_{SETUP2}$		3			ns
Start Pulse Hold Time	$t_{HOLD2}$		0			ns
POL21, POL22 Setup Time	$t_{SETUP3}$		3			ns
POL21, POL22 Hold Time	$t_{HOLD3}$		0			ns
STB Pulse Width	$PW_{STB}$		2			CLK
Last Data Timing	$t_{LDT}$		2			CLK
STB-CLK Time	$t_{STB-CLK}$	STB $\uparrow$ $\rightarrow$ CLK $\uparrow$	7			ns
Time between STB and Start Pulse	$t_{STB-STH}$	STB $\uparrow$ $\rightarrow$ STHR (STHL) $\uparrow$	2			CLK
POL-STB Time	$t_{POL-STB}$	POL $\uparrow$ or $\downarrow$ $\rightarrow$ STB $\uparrow$	-5			ns
STB-POL Time	$t_{STB-POL}$	STB $\downarrow$ $\rightarrow$ POL $\downarrow$ or $\uparrow$	6			ns

**Remark** Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .

Switching Characteristics Waveform

Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .



**10. RECOMMENDED SOLDERING CONDITIONS**

The following conditions must be met for soldering conditions of the μPD16718.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

**μPD16718N-xxx: TCP (TAB package)**

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm <sup>2</sup> : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm <sup>2</sup> : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

**Caution** To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.



[MEMO]

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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