DATA SHEET

NEC

# MOS INTEGRATED CIRCUIT

# μPD16716

## 384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

### DESCRIPTION

The μPD16716 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as $V_{SS2}$ + 0.1 V to $V_{DD2}$ – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 70 MHz when driving at 3.0 V, 45 MHz when driving at 2.5 V, this driver is applicable to XGA/SXGA-standard TFT-LCD panels.

### FEATURES

- CMOS level input (2.5 to 3.6 V)
- 384 Outputs
- Input of 6 bits (gray scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter (R-DAC)
- Logic power supply voltage ($V_{DD1}$) : 2.5 to 3.6 V
- Driver power supply voltage ($V_{DD2}$) : 15.0 V ± 0.5 V
- Output dynamic range $V_{SS2}$ + 0.1 V to $V_{DD2}$ – 0.1 V
- High-speed data transfer: $f_{CLK}$ = 70 MHz (internal data transfer speed when operating at $V_{DD1}$ = 3.0 V),
  45 MHz (internal data transfer speed when operating at $V_{DD1}$ = 2.5 V)
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output Voltage polarity inversion function (POL)
- Display data inversion function (capable of controlling by each input port) (POL21, POL22)
- Low power control function (LPC)

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16716N-××× | TCP (TAB package) |

**Remark** The TCP's external shape is customized. To order your TCP's external shape, please contact one of our sales representatives.



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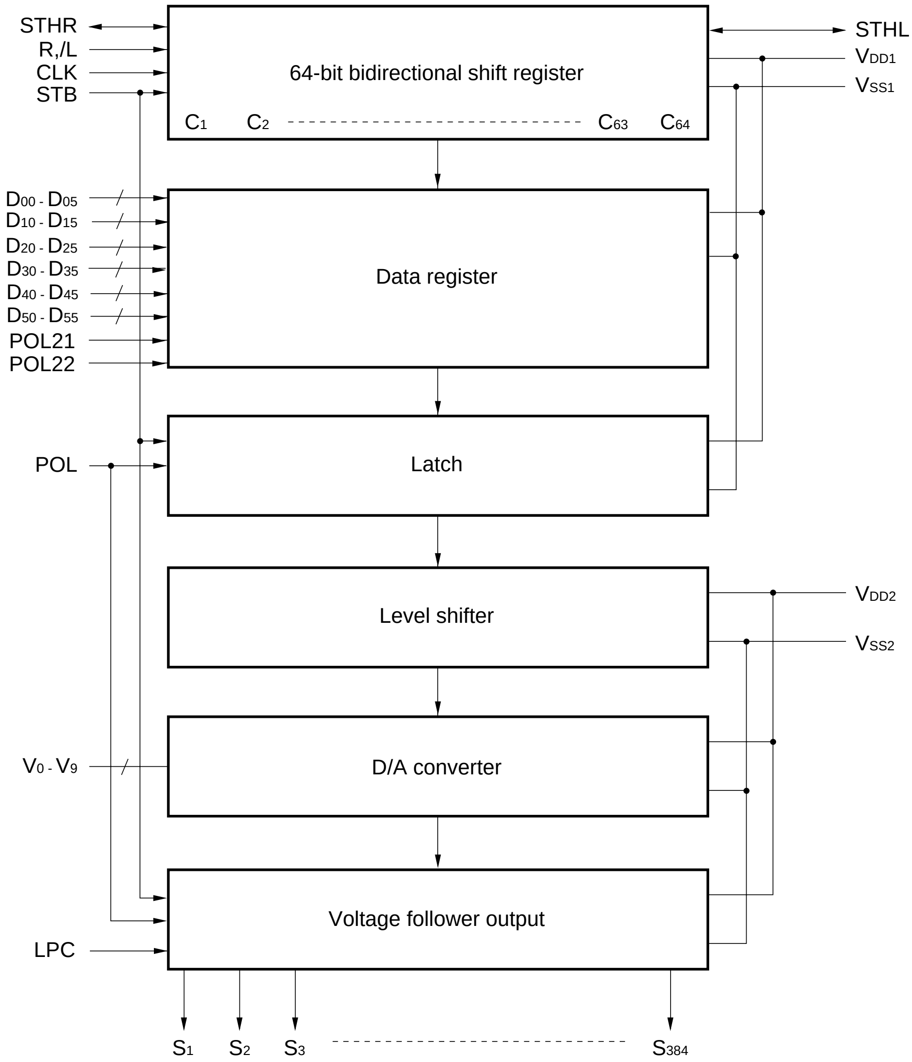
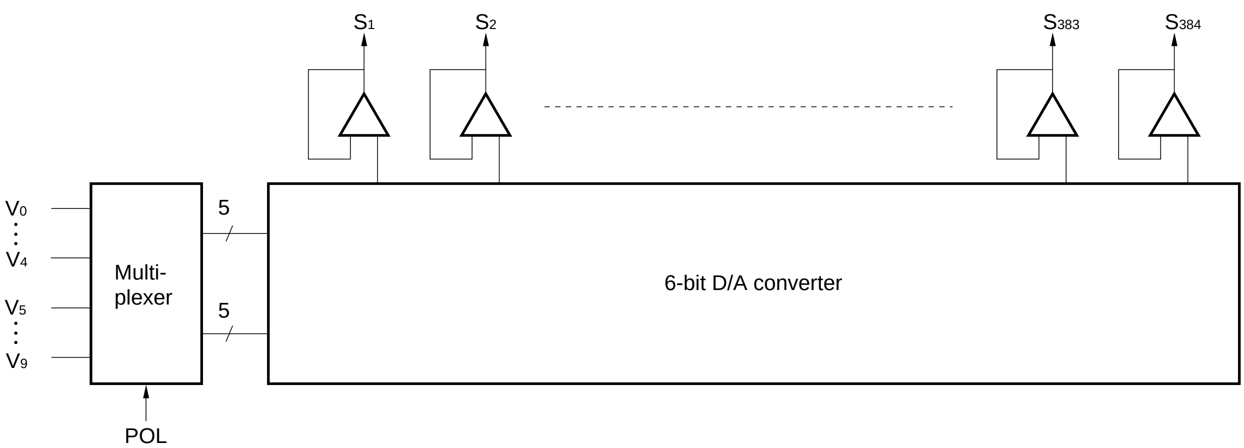
The mark ★ shows major revised points.

## 1. BLOCK DIAGRAM

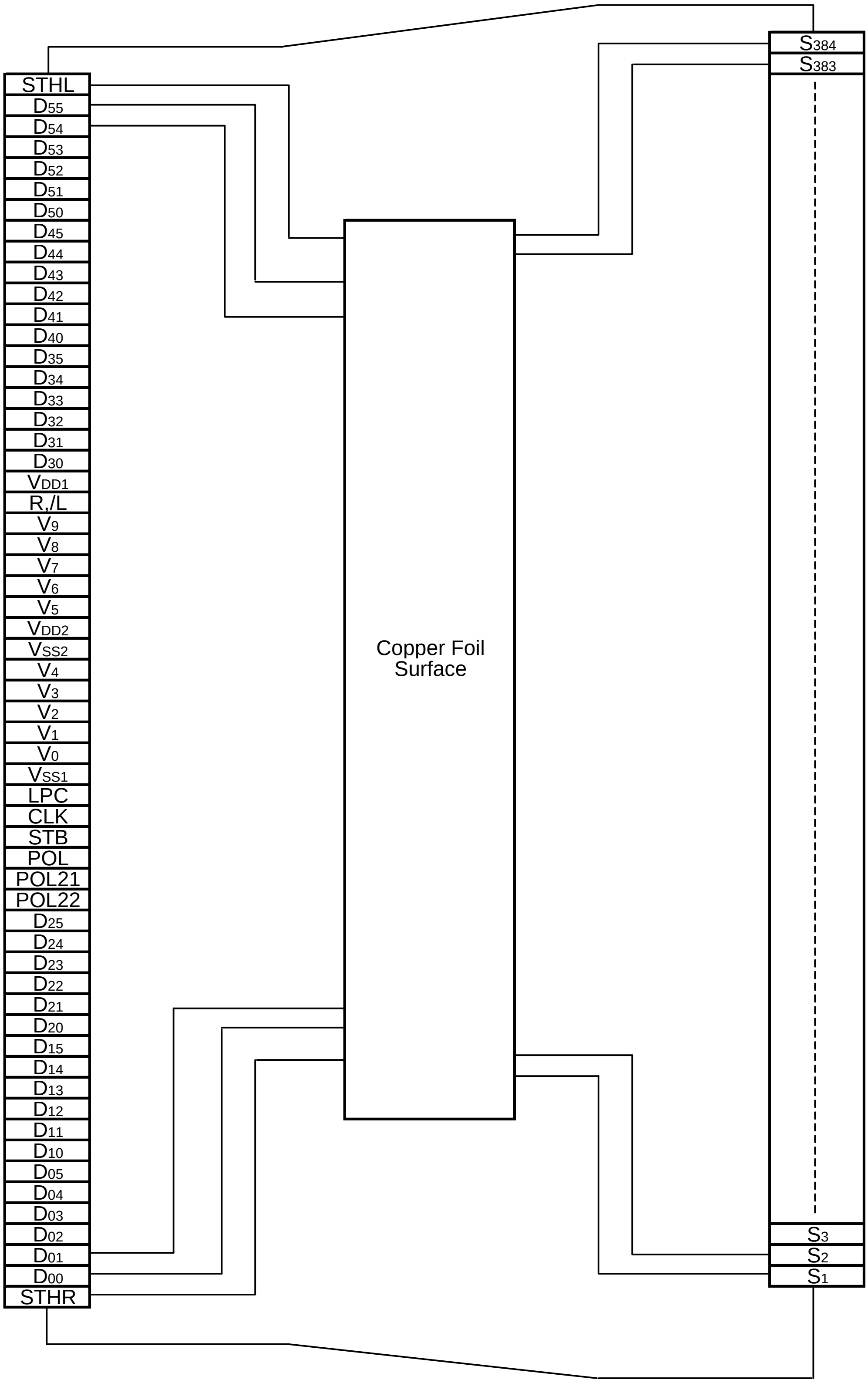



**Remark** /xxx indicates active low signal.

## 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



## 3. PIN CONFIGURATION ($\mu$PD16716N-xxx) (Copper Foil Surface, Face-up)




**Remark** This figure does not specify the TCP package.

## 4. PIN FUNCTIONS

(1/2)

| Pin Symbol | Pin Name | I/O | Description |
|---|---|---|---|
| $S_1$ to $S_{384}$ | Driver | O | The D/A converted 64-gray-scale analog voltage is output. |
| $D_{00}$ to $D_{05}$<br>$D_{10}$ to $D_{15}$<br>$D_{20}$ to $D_{25}$<br>$D_{30}$ to $D_{35}$<br>$D_{40}$ to $D_{45}$<br>$D_{50}$ to $D_{55}$ | Display data | I | The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels).<br>$D_{X0}$: LSB, $D_{X5}$: MSB |
| R,/L | Shift direction control | I | Refers to the shift direction control. The shift directions of the shift registers are as follows.<br>R,/L = H : STHR input, $S_1 \rightarrow S_{384}$, STHL output<br>R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output |
| ★ STHR | Right shift start pulse | I/O | These refer to the start pulse I/O pins when driver ICs are connected in cascade. Loading of display data starts when H is read at the rising edge of CLK.<br>R,/L = H (right shift): STHR input, STHL output<br>R,/L = L (left shift): STHL input, STHR output<br>A high level should be input as the pulse of one cycle of the clock signal.<br>If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is valid. |
| ★ STHL | Left shift start pulse | I/O | |
| CLK | Shift clock | I | Refers to the shift register's shift clock input. The display data is loaded into the data register at the rising edge.<br>At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. ★ If 66-clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge. |
| STB | Latch | I | The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period. |
| POL | Polarity | I | POL = L : The $S_{2n-1}$ output uses $V_0$ to $V_4$ as the reference supply. The $S_{2n}$ output uses $V_5$ to $V_9$ as the reference supply.<br>POL = H : The $S_{2n-1}$ output uses $V_5$ to $V_9$ as the reference supply. The $S_{2n}$ output uses $V_0$ to $V_4$ as the reference supply.<br>$S_{2n-1}$ indicates the odd output: and $S_{2n}$ indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL\text{-}STB}$) with respect to STB's rising edge. |
| ★ POL21, POL22 | Data inversion | I | Data inversion can invert when display data is loaded.<br>POL21: Invert/not invert of display data $D_{00}$ to $D_{05}$, $D_{10}$ to $D_{15}$, $D_{20}$ to $D_{25}$.<br>POL22: Invert/not invert of display data $D_{30}$ to $D_{35}$, $D_{40}$ to $D_{45}$, $D_{50}$ to $D_{55}$.<br>POL21, POL22 = H : Display data is inverted.<br>POL21, POL22 = L : Display data is not inverted. |
| LPC | Low power control | I | The current consumption is lowered by controlling the constant current source of the output amplifier. This pin is pulled up to the $V_{DD1}$ power supply inside the IC.<br>In low power mode (LPC = L), the static current consumption of $V_{DD2}$ reduced to about 2/3 of the normal current consumption.<br>LPC = H or Open : Normal power mode<br>LPC = L : Low power mode |

(2/2)

| Pin Symbol | Pin Name | I/O | Description |
|---|---|---|---|
| $V_0$ to $V_9$ | $\gamma$-corrected power supplies | – | Input the $\gamma$-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$ |
| $V_{DD1}$ | Logic power supply | – | 2.5 V to 3.6 V |
| $V_{DD2}$ | Driver power supply | – | 15.0 V ± 0.5 V |
| $V_{SS1}$ | Logic ground | – | Grounding |
| $V_{SS2}$ | Driver ground | – | Grounding |

**Cautions 1. The power start sequence must be $V_{DD1}$, logic input, and $V_{DD2}$ & $V_0$ to $V_9$ in that order. Reverse this sequence to shut down. (Simultaneous power application to $V_{DD2}$ and $V_0$ to $V_9$ is possible.)**

**2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between $V_{DD1}$-$V_{SS1}$ and $V_{DD2}$-$V_{SS2}$. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the $\gamma$-corrected power supply terminals ($V_0$, $V_1$, $V_2$, ···, $V_9$) and $V_{SS2}$.**

## 5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

This product incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

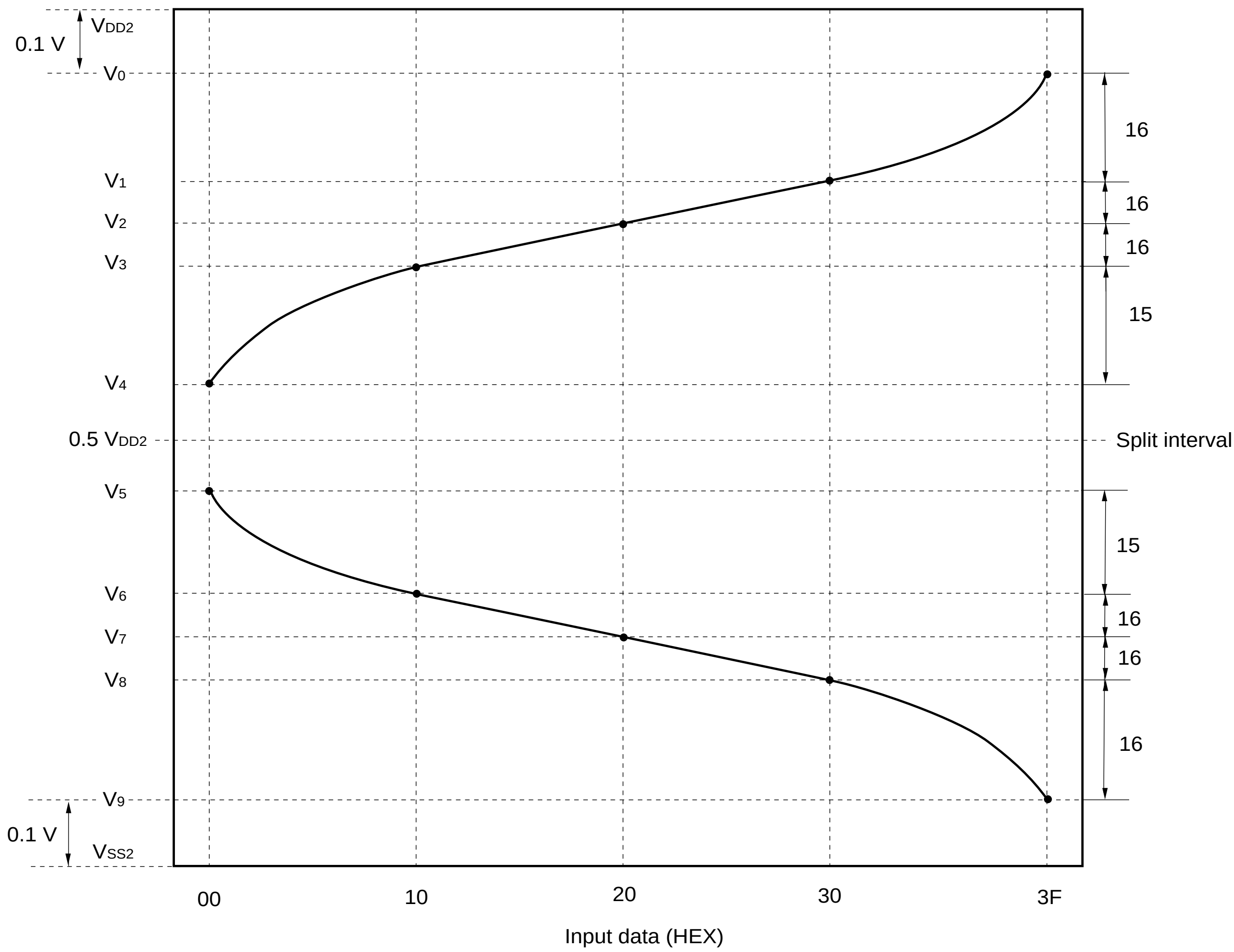
The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel $\gamma$-compensated voltages to $V_0$' to $V_{63}$' and $V_0$'' to $V_{63}$'' is almost equivalent. For the 2 sets of five $\gamma$-compensated power supplies, $V_0$ to $V_4$ and $V_5$ to $V_9$, respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect a voltage follower circuit to the $\gamma$-compensated power supplies $V_1$ to $V_3$ and $V_6$ to $V_8$.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages $V_{DD2}$ and $V_{SS2}$, common electrode potential $V_{COM}$, and $\gamma$-corrected voltages $V_0$ to $V_9$ and the input data. Be sure to maintain the voltage relationships as follows:

$V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\ V$.

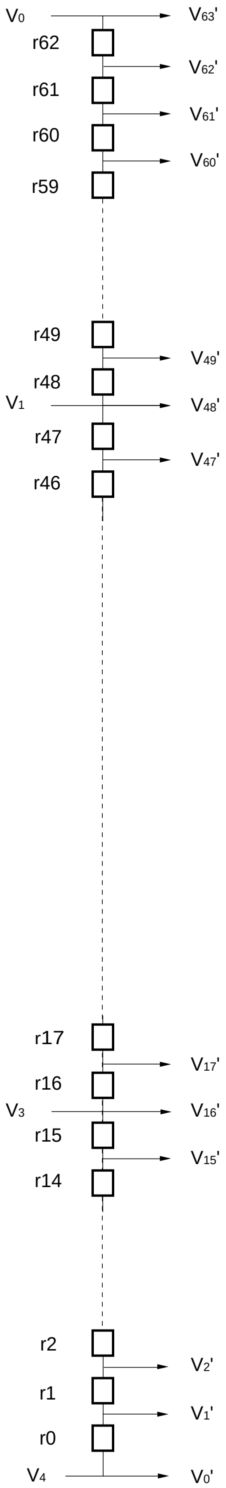
Figures 5–2 and 5–3 show the relationship between input data and output voltage. This driver IC is designed for only single-sided mounting

**Figure 5–1. Relationship between Input Data and $\gamma$- corrected Power Supply**



## Figure 5–2. Relationship between Input Data and Output voltage

**$V_{DD2} - 0.1\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5\ V_{DD2}$, POL21, POL22 = L**



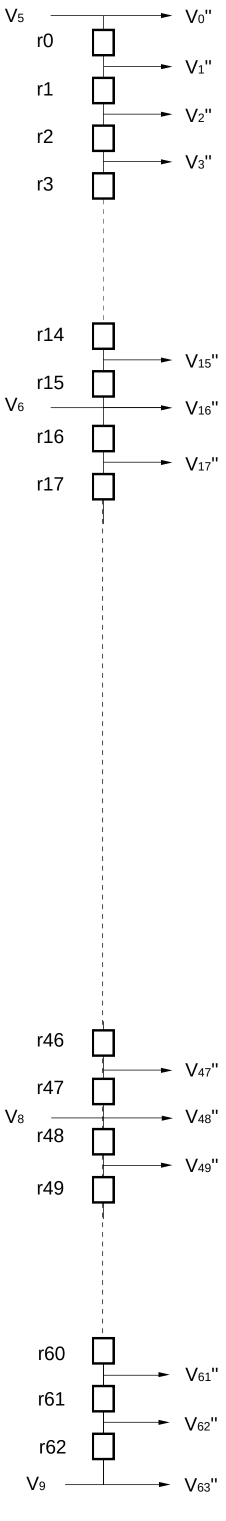

| Data | $D_{X7}$ | $D_{X6}$ | $D_{X5}$ | $D_{X4}$ | $D_{X3}$ | $D_{X2}$ | $D_{X1}$ | $D_{X0}$ | Output Voltage | |
|---|---|---|---|---|---|---|---|---|---|---|
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $V_0'$ | $V_4$ |
| 01H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $V_1'$ | $V_4+(V_3-V_4)$ X 570 / 5520 |
| 02H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | $V_2'$ | $V_4+(V_3-V_4)$ X 1190 / 5520 |
| 03H | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $V_3'$ | $V_4+(V_3-V_4)$ X 1810 / 5520 |
| 04H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | $V_4'$ | $V_4+(V_3-V_4)$ X 2410 / 5520 |
| 05H | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | $V_5'$ | $V_4+(V_3-V_4)$ X 2980 / 5520 |
| 06H | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | $V_6'$ | $V_4+(V_3-V_4)$ X 3320 / 5520 |
| 07H | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $V_7'$ | $V_4+(V_3-V_4)$ X 3560 / 5520 |
| 08H | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | $V_8'$ | $V_4+(V_3-V_4)$ X 3800 / 5520 |
| 09H | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | $V_9'$ | $V_4+(V_3-V_4)$ X 4010 / 5520 |
| 0AH | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | $V_{10}'$ | $V_4+(V_3-V_4)$ X 4220 / 5520 |
| 0BH | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | $V_{11}'$ | $V_4+(V_3-V_4)$ X 4430 / 5520 |
| 0CH | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | $V_{12}'$ | $V_4+(V_3-V_4)$ X 4670 / 5520 |
| 0DH | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | $V_{13}'$ | $V_4+(V_3-V_4)$ X 4880 / 5520 |
| 0EH | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | $V_{14}'$ | $V_4+(V_3-V_4)$ X 5090 / 5520 |
| 0FH | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | $V_{15}'$ | $V_4+(V_3-V_4)$ X 5290 / 5520 |
| 10H | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | $V_{16}'$ | $V_3$ |
| 11H | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | $V_{17}'$ | $V_3+(V_2-V_3)$ X 170 / 2220 |
| 12H | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | $V_{18}'$ | $V_3+(V_2-V_3)$ X 340 / 2220 |
| 13H | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | $V_{19}'$ | $V_3+(V_2-V_3)$ X 490 / 2220 |
| 14H | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | $V_{20}'$ | $V_3+(V_2-V_3)$ X 640 / 2220 |
| 15H | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $V_{21}'$ | $V_3+(V_2-V_3)$ X 790 / 2220 |
| 16H | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | $V_{22}'$ | $V_3+(V_2-V_3)$ X 940 / 2220 |
| 17H | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | $V_{23}'$ | $V_3+(V_2-V_3)$ X 1070 / 2220 |
| 18H | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | $V_{24}'$ | $V_3+(V_2-V_3)$ X 1190 / 2220 |
| 19H | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $V_{25}'$ | $V_3+(V_2-V_3)$ X 1320 / 2220 |
| 1AH | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | $V_{26}'$ | $V_3+(V_2-V_3)$ X 1450 / 2220 |
| 1BH | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | $V_{27}'$ | $V_3+(V_2-V_3)$ X 1570 / 2220 |
| 1CH | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | $V_{28}'$ | $V_3+(V_2-V_3)$ X 1700 / 2220 |
| 1DH | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | $V_{29}'$ | $V_3+(V_2-V_3)$ X 1820 / 2220 |
| 1EH | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | $V_{30}'$ | $V_3+(V_2-V_3)$ X 1940 / 2220 |
| 1FH | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | $V_{31}'$ | $V_3+(V_2-V_3)$ X 2070 / 2220 |
| 20H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $V_{32}'$ | $V_2$ |
| 21H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | $V_{33}'$ | $V_2+(V_1-V_2)$ X 120 / 2100 |
| 22H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | $V_{34}'$ | $V_2+(V_1-V_2)$ X 240 / 2100 |
| 23H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | $V_{35}'$ | $V_2+(V_1-V_2)$ X 360 / 2100 |
| 24H | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | $V_{36}'$ | $V_2+(V_1-V_2)$ X 490 / 2100 |
| 25H | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{37}'$ | $V_2+(V_1-V_2)$ X 610 / 2100 |
| 26H | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $V_{38}'$ | $V_2+(V_1-V_2)$ X 730 / 2100 |
| 27H | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | $V_{39}'$ | $V_2+(V_1-V_2)$ X 850 / 2100 |
| 28H | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | $V_{40}'$ | $V_2+(V_1-V_2)$ X 970 / 2100 |
| 29H | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{41}'$ | $V_2+(V_1-V_2)$ X 1100 / 2100 |
| 2AH | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | $V_{42}'$ | $V_2+(V_1-V_2)$ X 1220 / 2100 |
| 2BH | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | $V_{43}'$ | $V_2+(V_1-V_2)$ X 1350 / 2100 |
| 2CH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | $V_{44}'$ | $V_2+(V_1-V_2)$ X 1480 / 2100 |
| 2DH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | $V_{45}'$ | $V_2+(V_1-V_2)$ X 1610 / 2100 |
| 2EH | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | $V_{46}'$ | $V_2+(V_1-V_2)$ X 1760 / 2100 |
| 2FH | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | $V_{47}'$ | $V_2+(V_1-V_2)$ X 1890 / 2100 |
| 30H | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | $V_{48}'$ | $V_1$ |
| 31H | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | $V_{49}'$ | $V_1+(V_0-V_1)$ X 170 / 4810 |
| 32H | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | $V_{50}'$ | $V_1+(V_0-V_1)$ X 340 / 4810 |
| 33H | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | $V_{51}'$ | $V_1+(V_0-V_1)$ X 490 / 4810 |
| 34H | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | $V_{52}'$ | $V_1+(V_0-V_1)$ X 670 / 4810 |
| 35H | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | $V_{53}'$ | $V_1+(V_0-V_1)$ X 850 / 4810 |
| 36H | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | $V_{54}'$ | $V_1+(V_0-V_1)$ X 1030 / 4810 |
| 37H | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | $V_{55}'$ | $V_1+(V_0-V_1)$ X 1240 / 4810 |
| 38H | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | $V_{56}'$ | $V_1+(V_0-V_1)$ X 1500 / 4810 |
| 39H | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | $V_{57}'$ | $V_1+(V_0-V_1)$ X 1820 / 4810 |
| 3AH | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | $V_{58}'$ | $V_1+(V_0-V_1)$ X 2130 / 4810 |
| 3BH | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | $V_{59}'$ | $V_1+(V_0-V_1)$ X 2450 / 4810 |
| 3CH | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | $V_{60}'$ | $V_1+(V_0-V_1)$ X 2830 / 4810 |
| 3DH | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | $V_{61}'$ | $V_1+(V_0-V_1)$ X 3310 / 4810 |
| 3EH | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | $V_{62}'$ | $V_1+(V_0-V_1)$ X 3880 / 4810 |
| 3FH | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | $V_{63}'$ | $V_0$ |

| rn | (Ω) |
|---|---|
| r0 | 570 |
| r1 | 620 |
| r2 | 620 |
| r3 | 600 |
| r4 | 570 |
| r5 | 340 |
| r6 | 240 |
| r7 | 240 |
| r8 | 210 |
| r9 | 210 |
| r10 | 210 |
| r11 | 240 |
| r12 | 210 |
| r13 | 210 |
| r14 | 200 |
| r15 | 230 |
| r16 | 170 |
| r17 | 170 |
| r18 | 150 |
| r19 | 150 |
| r20 | 150 |
| r21 | 150 |
| r22 | 130 |
| r23 | 120 |
| r24 | 130 |
| r25 | 130 |
| r26 | 120 |
| r27 | 130 |
| r28 | 120 |
| r29 | 120 |
| r30 | 130 |
| r31 | 150 |
| r32 | 120 |
| r33 | 120 |
| r34 | 120 |
| r35 | 130 |
| r36 | 120 |
| r37 | 120 |
| r38 | 120 |
| r39 | 120 |
| r40 | 130 |
| r41 | 120 |
| r42 | 130 |
| r43 | 130 |
| r44 | 130 |
| r45 | 150 |
| r46 | 130 |
| r47 | 210 |
| r48 | 170 |
| r49 | 170 |
| r50 | 150 |
| r51 | 180 |
| r52 | 180 |
| r53 | 180 |
| r54 | 210 |
| r55 | 260 |
| r56 | 320 |
| r57 | 310 |
| r58 | 320 |
| r59 | 380 |
| r60 | 480 |
| r61 | 570 |
| r62 | 930 |
| rtotal | 14650 |

**Caution There is no connection between $V_4$ and $V_5$ terminal in the chip.**

**Figure 5–3. Relationship between Input Data and Output voltage**

**0.5 $V_{DD2} \geq V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2}$ + 0.1 V, POL21, POL22 = L**




| Data | $D_{X5}$ | $D_{X4}$ | $D_{X3}$ | $D_{X2}$ | $D_{X1}$ | $D_{X0}$ | Output Voltage | |
|---|---|---|---|---|---|---|---|---|
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | $V_0''$ | $V_5$ |
| 01H | 0 | 0 | 0 | 0 | 0 | 1 | $V_1''$ | $V_6+(V_5-V_6)$ X 4950 / 5520 |
| 02H | 0 | 0 | 0 | 0 | 1 | 0 | $V_2''$ | $V_6+(V_5-V_6)$ X 4330 / 5520 |
| 03H | 0 | 0 | 0 | 0 | 1 | 1 | $V_3''$ | $V_6+(V_5-V_6)$ X 3710 / 5520 |
| 04H | 0 | 0 | 0 | 1 | 0 | 0 | $V_4''$ | $V_6+(V_5-V_6)$ X 3110 / 5520 |
| 05H | 0 | 0 | 0 | 1 | 0 | 1 | $V_5''$ | $V_6+(V_5-V_6)$ X 2540 / 5520 |
| 06H | 0 | 0 | 0 | 1 | 1 | 0 | $V_6''$ | $V_6+(V_5-V_6)$ X 2200 / 5520 |
| 07H | 0 | 0 | 0 | 1 | 1 | 1 | $V_7''$ | $V_6+(V_5-V_6)$ X 1960 / 5520 |
| 08H | 0 | 0 | 1 | 0 | 0 | 0 | $V_8''$ | $V_6+(V_5-V_6)$ X 1720 / 5520 |
| 09H | 0 | 0 | 1 | 0 | 0 | 1 | $V_9''$ | $V_6+(V_5-V_6)$ X 1510 / 5520 |
| 0AH | 0 | 0 | 1 | 0 | 1 | 0 | $V_{10}''$ | $V_6+(V_5-V_6)$ X 1300 / 5520 |
| 0BH | 0 | 0 | 1 | 0 | 1 | 1 | $V_{11}''$ | $V_6+(V_5-V_6)$ X 1090 / 5520 |
| 0CH | 0 | 0 | 1 | 1 | 0 | 0 | $V_{12}''$ | $V_6+(V_5-V_6)$ X 850 / 5520 |
| 0DH | 0 | 0 | 1 | 1 | 0 | 1 | $V_{13}''$ | $V_6+(V_5-V_6)$ X 640 / 5520 |
| 0EH | 0 | 0 | 1 | 1 | 1 | 0 | $V_{14}''$ | $V_6+(V_5-V_6)$ X 430 / 5520 |
| 0FH | 0 | 0 | 1 | 1 | 1 | 1 | $V_{15}''$ | $V_6+(V_5-V_6)$ X 230 / 5520 |
| 10H | 0 | 1 | 0 | 0 | 0 | 0 | $V_{16}''$ | $V_6$ |
| 11H | 0 | 1 | 0 | 0 | 0 | 1 | $V_{17}''$ | $V_7+(V_6-V_7)$ X 2050 / 2220 |
| 12H | 0 | 1 | 0 | 0 | 1 | 0 | $V_{18}''$ | $V_7+(V_6-V_7)$ X 1880 / 2220 |
| 13H | 0 | 1 | 0 | 0 | 1 | 1 | $V_{19}''$ | $V_7+(V_6-V_7)$ X 1730 / 2220 |
| 14H | 0 | 1 | 0 | 1 | 0 | 0 | $V_{20}''$ | $V_7+(V_6-V_7)$ X 1580 / 2220 |
| 15H | 0 | 1 | 0 | 1 | 0 | 1 | $V_{21}''$ | $V_7+(V_6-V_7)$ X 1430 / 2220 |
| 16H | 0 | 1 | 0 | 1 | 1 | 0 | $V_{22}''$ | $V_7+(V_6-V_7)$ X 1280 / 2220 |
| 17H | 0 | 1 | 0 | 1 | 1 | 1 | $V_{23}''$ | $V_7+(V_6-V_7)$ X 1150 / 2220 |
| 18H | 0 | 1 | 1 | 0 | 0 | 0 | $V_{24}''$ | $V_7+(V_6-V_7)$ X 1030 / 2220 |
| 19H | 0 | 1 | 1 | 0 | 0 | 1 | $V_{25}''$ | $V_7+(V_6-V_7)$ X 900 / 2220 |
| 1AH | 0 | 1 | 1 | 0 | 1 | 0 | $V_{26}''$ | $V_7+(V_6-V_7)$ X 770 / 2220 |
| 1BH | 0 | 1 | 1 | 0 | 1 | 1 | $V_{27}''$ | $V_7+(V_6-V_7)$ X 650 / 2220 |
| 1CH | 0 | 1 | 1 | 1 | 0 | 0 | $V_{28}''$ | $V_7+(V_6-V_7)$ X 520 / 2220 |
| 1DH | 0 | 1 | 1 | 1 | 0 | 1 | $V_{29}''$ | $V_7+(V_6-V_7)$ X 400 / 2220 |
| 1EH | 0 | 1 | 1 | 1 | 1 | 0 | $V_{30}''$ | $V_7+(V_6-V_7)$ X 280 / 2220 |
| 1FH | 0 | 1 | 1 | 1 | 1 | 1 | $V_{31}''$ | $V_7+(V_6-V_7)$ X 150 / 2220 |
| 20H | 1 | 0 | 0 | 0 | 0 | 0 | $V_{32}''$ | $V_7$ |
| 21H | 1 | 0 | 0 | 0 | 0 | 1 | $V_{33}''$ | $V_8+(V_7-V_8)$ X 1980 / 2100 |
| 22H | 1 | 0 | 0 | 0 | 1 | 0 | $V_{34}''$ | $V_8+(V_7-V_8)$ X 1860 / 2100 |
| 23H | 1 | 0 | 0 | 0 | 1 | 1 | $V_{35}''$ | $V_8+(V_7-V_8)$ X 1740 / 2100 |
| 24H | 1 | 0 | 0 | 1 | 0 | 0 | $V_{36}''$ | $V_8+(V_7-V_8)$ X 1610 / 2100 |
| 25H | 1 | 0 | 0 | 1 | 0 | 1 | $V_{37}''$ | $V_8+(V_7-V_8)$ X 1490 / 2100 |
| 26H | 1 | 0 | 0 | 1 | 1 | 0 | $V_{38}''$ | $V_8+(V_7-V_8)$ X 1370 / 2100 |
| 27H | 1 | 0 | 0 | 1 | 1 | 1 | $V_{39}''$ | $V_8+(V_7-V_8)$ X 1250 / 2100 |
| 28H | 1 | 0 | 1 | 0 | 0 | 0 | $V_{40}''$ | $V_8+(V_7-V_8)$ X 1130 / 2100 |
| 29H | 1 | 0 | 1 | 0 | 0 | 1 | $V_{41}''$ | $V_8+(V_7-V_8)$ X 1000 / 2100 |
| 2AH | 1 | 0 | 1 | 0 | 1 | 0 | $V_{42}''$ | $V_8+(V_7-V_8)$ X 880 / 2100 |
| 2BH | 1 | 0 | 1 | 0 | 1 | 1 | $V_{43}''$ | $V_8+(V_7-V_8)$ X 750 / 2100 |
| 2CH | 1 | 0 | 1 | 1 | 0 | 0 | $V_{44}''$ | $V_8+(V_7-V_8)$ X 620 / 2100 |
| 2DH | 1 | 0 | 1 | 1 | 0 | 1 | $V_{45}''$ | $V_8+(V_7-V_8)$ X 490 / 2100 |
| 2EH | 1 | 0 | 1 | 1 | 1 | 0 | $V_{46}''$ | $V_8+(V_7-V_8)$ X 340 / 2100 |
| 2FH | 1 | 0 | 1 | 1 | 1 | 1 | $V_{47}''$ | $V_8+(V_7-V_8)$ X 210 / 2100 |
| 30H | 1 | 1 | 0 | 0 | 0 | 0 | $V_{48}''$ | $V_8$ |
| 31H | 1 | 1 | 0 | 0 | 0 | 1 | $V_{49}''$ | $V_9+(V_8-V_9)$ X 4640 / 4810 |
| 32H | 1 | 1 | 0 | 0 | 1 | 0 | $V_{50}''$ | $V_9+(V_8-V_9)$ X 4470 / 4810 |
| 33H | 1 | 1 | 0 | 0 | 1 | 1 | $V_{51}''$ | $V_9+(V_8-V_9)$ X 4320 / 4810 |
| 34H | 1 | 1 | 0 | 1 | 0 | 0 | $V_{52}''$ | $V_9+(V_8-V_9)$ X 4140 / 4810 |
| 35H | 1 | 1 | 0 | 1 | 0 | 1 | $V_{53}''$ | $V_9+(V_8-V_9)$ X 3960 / 4810 |
| 36H | 1 | 1 | 0 | 1 | 1 | 0 | $V_{54}''$ | $V_9+(V_8-V_9)$ X 3780 / 4810 |
| 37H | 1 | 1 | 0 | 1 | 1 | 1 | $V_{55}''$ | $V_9+(V_8-V_9)$ X 3570 / 4810 |
| 38H | 1 | 1 | 1 | 0 | 0 | 0 | $V_{56}''$ | $V_9+(V_8-V_9)$ X 3310 / 4810 |
| 39H | 1 | 1 | 1 | 0 | 0 | 1 | $V_{57}''$ | $V_9+(V_8-V_9)$ X 2990 / 4810 |
| 3AH | 1 | 1 | 1 | 0 | 1 | 0 | $V_{58}''$ | $V_9+(V_8-V_9)$ X 2680 / 4810 |
| 3BH | 1 | 1 | 1 | 0 | 1 | 1 | $V_{59}''$ | $V_9+(V_8-V_9)$ X 2360 / 4810 |
| 3CH | 1 | 1 | 1 | 1 | 0 | 0 | $V_{60}''$ | $V_9+(V_8-V_9)$ X 1980 / 4810 |
| 3DH | 1 | 1 | 1 | 1 | 0 | 1 | $V_{61}''$ | $V_9+(V_8-V_9)$ X 1500 / 4810 |
| 3EH | 1 | 1 | 1 | 1 | 1 | 0 | $V_{62}''$ | $V_9+(V_8-V_9)$ X 930 / 4810 |
| 3FH | 1 | 1 | 1 | 1 | 1 | 1 | $V_{63}''$ | $V_9$ |

| rn | ($\Omega$) |
|---|---|
| r0 | 570 |
| r1 | 620 |
| r2 | 620 |
| r3 | 600 |
| r4 | 570 |
| r5 | 340 |
| r6 | 240 |
| r7 | 240 |
| r8 | 210 |
| r9 | 210 |
| r10 | 210 |
| r11 | 240 |
| r12 | 210 |
| r13 | 210 |
| r14 | 200 |
| r15 | 230 |
| r16 | 170 |
| r17 | 170 |
| r18 | 150 |
| r19 | 150 |
| r20 | 150 |
| r21 | 150 |
| r22 | 130 |
| r23 | 120 |
| r24 | 130 |
| r25 | 130 |
| r26 | 120 |
| r27 | 130 |
| r28 | 120 |
| r29 | 120 |
| r30 | 130 |
| r31 | 150 |
| r32 | 120 |
| r33 | 120 |
| r34 | 120 |
| r35 | 130 |
| r36 | 120 |
| r37 | 120 |
| r38 | 120 |
| r39 | 120 |
| r40 | 130 |
| r41 | 120 |
| r42 | 130 |
| r43 | 130 |
| r44 | 130 |
| r45 | 150 |
| r46 | 130 |
| r47 | 210 |
| r48 | 170 |
| r49 | 170 |
| r50 | 150 |
| r51 | 180 |
| r52 | 180 |
| r53 | 180 |
| r54 | 210 |
| r55 | 260 |
| r56 | 320 |
| r57 | 310 |
| r58 | 320 |
| r59 | 380 |
| r60 | 480 |
| r61 | 570 |
| r62 | 930 |
| rtotal | 14650 |

**Caution There is no connection between $V_4$ and $V_5$ terminal in the chip.**

## 6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format: 6 bits × 2 RGBs (6 dots)
Input width : 36 bits (2-pixel data)

**R,/L = H (Right shift)**

| Output | $S_1$ | $S_2$ | $S_3$ | $S_4$ | ... | $S_{383}$ | $S_{384}$ |
|---|---|---|---|---|---|---|---|
| Data | $D_{00}$ to $D_{05}$ | $D_{10}$ to $D_{15}$ | $D_{20}$ to $D_{25}$ | $D_{30}$ to $D_{35}$ | ... | $D_{40}$ to $D_{45}$ | $D_{50}$ to $D_{55}$ |

**R,/L = L (Left shift)**

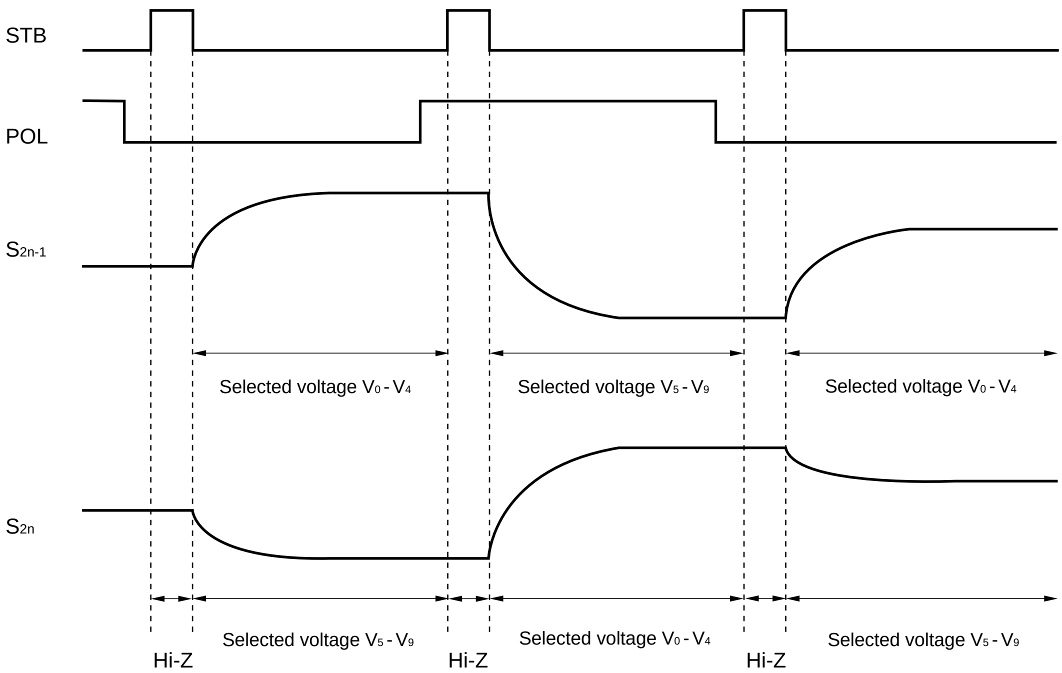
| Output | $S_1$ | $S_2$ | $S_3$ | $S_4$ | ... | $S_{383}$ | $S_{384}$ |
|---|---|---|---|---|---|---|---|
| Data | $D_{00}$ to $D_{05}$ | $D_{10}$ to $D_{15}$ | $D_{20}$ to $D_{25}$ | $D_{30}$ to $D_{35}$ | ... | $D_{40}$ to $D_{45}$ | $D_{50}$ to $D_{55}$ |

| POL | $S_{2n-1}$ Note | $S_{2n}$ Note |
|---|---|---|
| L | $V_0$ to $V_4$ | $V_5$ to $V_9$ |
| H | $V_5$ to $V_9$ | $V_0$ to $V_4$ |

**Note** $S_{2n-1}$ (Odd output), $S_{2n}$ (Even output)

## 7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



## 8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

**Figure 8–1. Output Circuit Block Diagram**

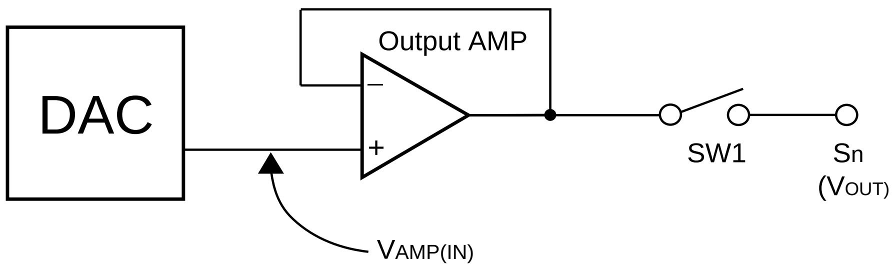
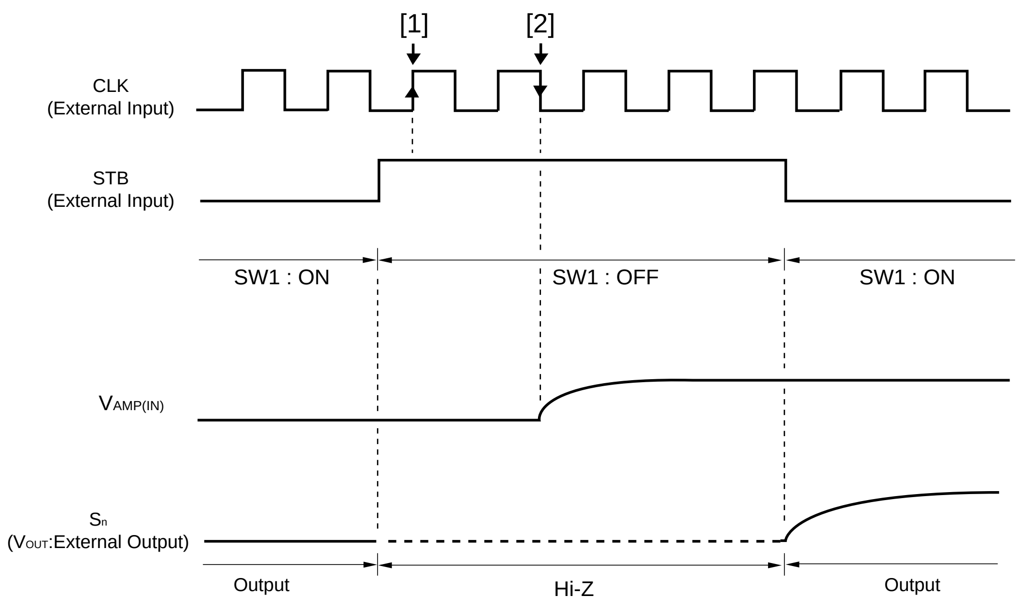



**Figure 8–2. Output Circuit Timing Waveform**




**Remarks 1.** STB = L : SW1 = ON

STB = H : SW1 = OFF

**2.** STB = "H" is acknowledged at timing [1].

**3.** The display data latch is completed at timing [2] and the input voltage ($V_{AMP(IN)}$ : gray-scale level voltage) of the output amplifier changes.

## 9. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings ($T_A$ = +25°C, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD1}$ | –0.5 to +4.0 | V |
| Driver Part Supply Voltage | $V_{DD2}$ | –0.5 to +17.0 | V |
| Logic Part Input Voltage | $V_{I1}$ | –0.5 to $V_{DD1}$ + 0.5 | V |
| Driver Part Input Voltage | $V_{I2}$ | –0.5 to $V_{DD2}$ + 0.5 | V |
| Logic Part Output Voltage | $V_{O1}$ | –0.5 to $V_{DD1}$ + 0.5 | V |
| Driver Part Output Voltage | $V_{O2}$ | –0.5 to $V_{DD2}$ + 0.5 | V |
| Operating Ambient Temperature | $T_A$ | –10 to +75 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Recommended Operating Range ($T_A$ = –10 to +75°C, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD1}$ | | 2.5 | | 3.6 | V |
| Driver Part Supply Voltage | $V_{DD2}$ | | 14.5 | 15.0 | 15.5 | V |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 $V_{DD1}$ | | $V_{DD1}$ | V |
| Low-Level Input Voltage | $V_{IL}$ | | 0 | | 0.3 $V_{DD1}$ | V |
| $\gamma$-Corrected Voltage | $V_0$ to $V_9$ | | $V_{SS2}$ + 0.1 | | $V_{DD2}$ – 0.1 | V |
| Driver Part Output Voltage | $V_O$ | | $V_{SS2}$ + 0.1 | | $V_{DD2}$ – 0.1 | V |
| Clock Frequency | $f_{CLK}$ | $V_{DD1}$ = 3.0 V | | | 70 | MHz |
| | | $V_{DD1}$ = 2.5 V | | | 45 | MHz |

★ **Electrical Characteristics ($T_A$ = –10 to +75°C, $V_{DD1}$ = 2.5 to 3.6 V, $V_{DD2}$ = 15.0 V ± 0.5 V, $V_{SS1}$ = $V_{SS2}$ = 0 V, Unless otherwise specified, power mode = normal, Bcont = open)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input Leak Current | $I_{IL}$ | | | | | ±1.0 | μA |
| High-Level Output Voltage | $V_{OH}$ | STHR (STHL), $I_{OH}$ = 0 mA | | $V_{DD1}$ – 0.1 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | STHR (STHL), $I_{OL}$ = 0 mA | | | | 0.1 | V |
| γ-Corrected Supply Current | $I_\gamma$ | $V_{DD2}$ = 15.0 V, $V_0$ to $V_4$ = $V_5$ to $V_9$ = 7.5 V | $V_0$ pin, $V_5$ pin | 200 | | 800 | μA |
| | | | $V_4$ pin, $V_9$ pin | –800 | | –200 | μA |
| Driver Output Current | $I_{VOH}$ | Vx = 14.0 V, $V_{OUT}$ = 13.5 V | | | –75 | –30 | μA |
| | $I_{VOL}$ | Vx = 1.0 V, $V_{OUT}$ = 1.5 V | | 30 | 90 | | μA |
| Output Voltage Deviation | $\Delta V_O$ | $T_A$ = +25°C, $V_{OUT}$ = 3.0 V, 7.5 V, 12.0 V | | | ±10 | ±20 | mV |
| Output swing difference deviation | $\Delta V_{P-P1}$ | $V_{DD1}$ = 3.3 V, $V_{DD2}$ = 15.0 V, $T_A$ = +25°C | $V_{OUT}$ = 7.0 to 8.0 V | | ±5 | ±10 | mV |
| | $\Delta V_{P-P2}$ | | $V_{OUT}$ = 1.6 to 12.8 V | | ±7 | ±13 | mV |
| | $\Delta V_{P-P3}$ | | $V_{OUT}$ = 1.0 to 14.0 V | | ±10 | ±20 | mV |
| Logic Part Dynamic Current Consumption | $I_{DD1}$ | $V_{DD1}$ | | | 5 | 12 | mA |
| Driver Part Dynamic Current Consumption | $I_{DD2}$ | $V_{DD2}$, with no load | | | 8 | 16 | mA |

**Cautions 1. $f_{STB}$ = 64 kHz, $f_{CLK}$ = 54 MHz.**

**2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.**

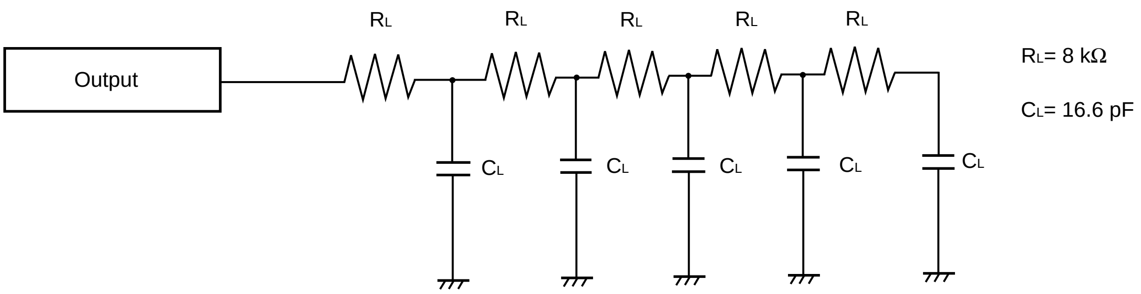
**3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).**

★ **Switching Characteristics ($T_A$ = –10 to +75°C, $V_{DD1}$ = 2.5 to 3.6 V, $V_{DD2}$ = 15.0 V ± 0.5 V, $V_{SS1}$ = $V_{SS2}$ = 0 V , Unless otherwise specified, power mode = normal, Bcont = open)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Start Pulse Delay Time | $t_{PLH1}$ | $C_L$ = 15 pF | | | 12 | ns |
| Driver Output Delay Time | $t_{PLH2}$ | $C_L$ = 83 pF, $R_L$ = 40 kΩ | | | 6 | μs |
| | $t_{PLH3}$ Note | | | | 12 | μs |
| | $t_{PHL2}$ | | | | 7 | μs |
| | $t_{PHL3}$ Note | | | | 12 | μs |
| Input Capacitance | $C_{I1}$ | STHR (STHL) excluded, $T_A$ = +25°C | | 5 | 10 | pF |
| | $C_{I2}$ | STHR (STHL),$T_A$ = +25°C | | 10 | 15 | pF |

**Note** $t_{PLH3}$/$t_{PHL3}$ are specified as the time it takes to reach the target voltage ±2%.

**<Measurement Condition>**



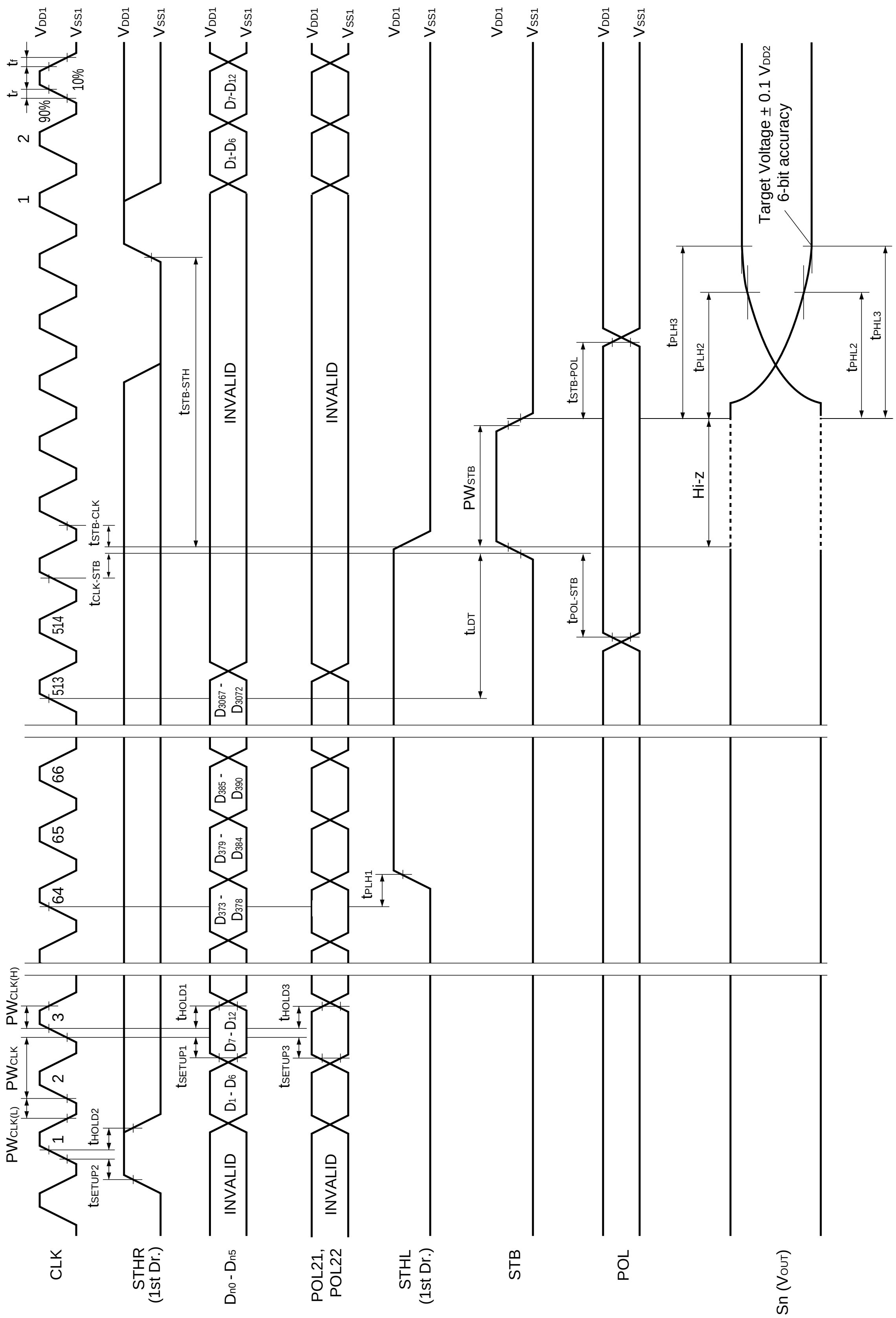
**Timing Requirement ($T_A$ = –10 to +75°C, $V_{DD1}$ = 2.5 to 3.6 V, $V_{SS1}$ = 0 V, $t_r$ = $t_f$ = 5.0 ns)**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock Pulse Width | $PW_{CLK}$ | $V_{DD1}$ = 3.3 V ± 0.3 V | 14 | | | ns |
| | | $V_{DD1}$ = 2.5 to 3.0 V | 22 | | | ns |
| Clock Pulse High Period | $PW_{CLK(H)}$ | | 4 | | | ns |
| Clock Pulse Low Period | $PW_{CLK(L)}$ | | 4 | | | ns |
| Data Setup Time | $t_{SETUP1}$ | | 2 | | | ns |
| Data Hold Time | $t_{HOLD1}$ | | 2 | | | ns |
| Start Pulse Setup Time | $t_{SETUP2}$ | | 2 | | | ns |
| Start Pulse Hold Time | $t_{HOLD2}$ | | 2 | | | ns |
| POL21, POL22 Setup Time | $t_{SETUP3}$ | | 2 | | | ns |
| POL21, POL22 Hold Time | $t_{HOLD3}$ | | 2 | | | ns |
| STB Pulse Width | $PW_{STB}$ | | 1.5 | | | μs |
| Last Data Timing | $t_{LDT}$ | | 2 | | | CLK |
| CLK-STB Time | $t_{CLK-STB}$ | CLK ↑ → STB ↑ | 4 | | | ns |
| STB-CLK Time | $t_{STB-CLK}$ | STB ↑ → CLK ↑ | 4 | | | ns |
| Time between STB and Start Pulse | $t_{STB-STH}$ | STB ↑ → STHR (STHL) ↑ | 2 | | | CLK |
| POL-STB Time | $t_{POL-STB}$ | POL ↑ or ↓ → STB ↑ | –5 | | | ns |
| STB-POL Time | $t_{STB-POL}$ | STB ↓ → POL ↓ or ↑ | 4 | | | ns |

**Remark** Unless otherwise specified, the input level is defined to be $V_{IH}$ = 0.7 $V_{DD1}$, $V_{IL}$ = 0.3 $V_{DD1}$.

**Switching Characteristics Waveform**

Unless otherwise specified, the input level is defined to be $V_{IH} = 0.7\ V_{DD1}$, $V_{IL} = 0.3\ V_{DD1}$.



## 10. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16716.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

**μPD16716N-××× : TCP (TAB package)**

| Mounting Condition | Mounting Method | Condition |
| --- | --- | --- |
| Thermocompression | Soldering | Heating tool 300 to 350°C: heating for 2 to 3 seconds: pressure 100g (per solder) |
| | ACF (Adhesive Conductive Film) | Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm$^2$ : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm$^2$ : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.) |

**Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.**

**[MEMO]**

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents**

**NEC Semiconductor Device Reliability / Quality Control System (C10983E)**

**Quality Grades to NEC's Semiconductor Devices (C11531E)**