NEC

MOS INTERGRATED CIRCUIT

μPD16686, 16687

1/128 DUTY LCD CONTROLLER/DRIVER WITH FOUR-LEVEL GRAY SCALE, ON-CHIP RAM

DESCRIPTION

The μPD16686 and 16687 are controller/drivers which include display RAM for full-dot LCDs that can provide a four-level gray scale display. These ICs are able to drive full-dot LCDs that contain up to 128 x 128 dots.

FEATURES

- μPD16686: COM outputs configured on both sides of chip
- μPD16687: COM outputs configured on one side of chip
- LCD controller/driver with on-chip display RAM
- Can operate using single power supply (logic system) in range from +1.7 to +3.6 V.
- On-chip booster: Switchable from x2 to x9 modes
- Dot display RAM: 128 x 128 x 2 bits
- Selection of four levels of gray scales from among 33 possible levels (four-frame rate control + 8 pulse width modulation)
- Full dot outputs: 128 segment outputs and 128 common outputs
- Static icon outputs: 20 segment outputs and 2 common outputs (same signal is output)
- Serial data input and 8-bit parallel data input (i80 series interface and M68 series interface)
- On-chip voltage divider resistor
- Selectable bias levels: 1/12 to 1/7 bias (normal display), 1/6 or 1/5 bias (partial display)
- Duty settings: 1/128 to 1/1 duty
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μ PD16686P	Chip
μ PD16686W	Wafer
μ PD16687P	Chip
μ PD16687W	Wafer

Remark Purchasing the chip/wafer entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

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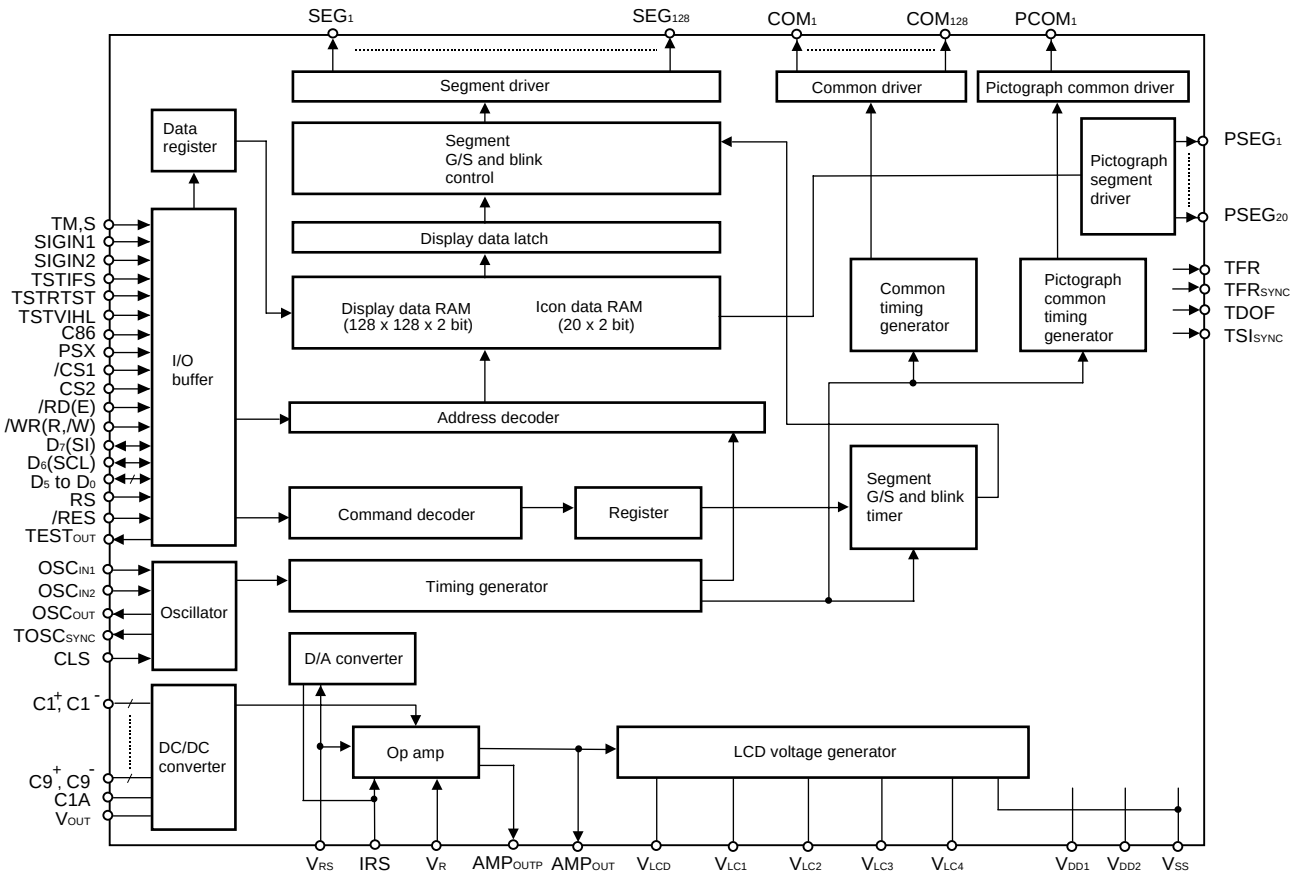
The mark ★ shows major revised points.

★ BLOCK DIAGRAM



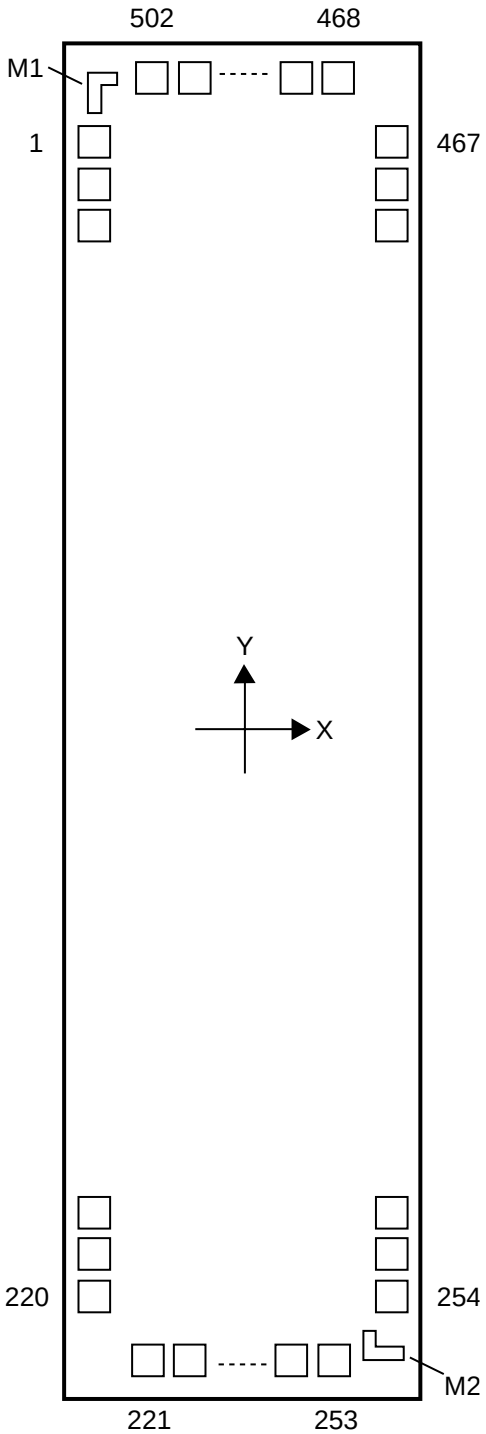
Remark /xxx indicates active low signals.

★ PIN CONFIGURATION (PAD LAYOUT)

(1) μPD16686

Chip size : 3.04 x 13.98 mm^2

Chip thickness : 485 μm (TYP.)



▪ **μPD16686 Pad Layout (1/3)**

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
1	DUMMY	B	-1385.000	6575.000
2	DUMMY	A	-1385.000	6480.000
3	DUMMY	A	-1385.000	6420.000
4	DUMMY	A	-1385.000	6360.000
5	DUMMY	A	-1385.000	6300.000
6	DUMMY	A	-1385.000	6240.000
7	DUMMY	A	-1385.000	6180.000
8	DUMMY	A	-1385.000	6120.000
9	DUMMY	A	-1385.000	6060.000
10	DUMMY	A	-1385.000	6000.000
11	DUMMY	A	-1385.000	5940.000
12	DUMMY	A	-1385.000	5880.000
13	DUMMY	A	-1385.000	5820.000
14	DUMMY	A	-1385.000	5760.000
15	PSEG1	A	-1385.000	5700.000
16	PSEG1	A	-1385.000	5640.000
17	PSEG2	A	-1385.000	5580.000
18	PSEG2	A	-1385.000	5520.000
19	PSEG3	A	-1385.000	5460.000
20	PSEG3	A	-1385.000	5400.000
21	PSEG4	A	-1385.000	5340.000
22	PSEG4	A	-1385.000	5280.000
23	PSEG5	A	-1385.000	5220.000
24	PSEG5	A	-1385.000	5160.000
25	PSEG6	A	-1385.000	5100.000
26	PSEG6	A	-1385.000	5040.000
27	PSEG7	A	-1385.000	4980.000
28	PSEG7	A	-1385.000	4920.000
29	PSEG8	A	-1385.000	4860.000
30	PSEG8	A	-1385.000	4800.000
31	PSEG9	A	-1385.000	4740.000
32	PSEG9	A	-1385.000	4680.000
33	PSEG10	A	-1385.000	4620.000
34	PSEG10	A	-1385.000	4560.000
35	VSS	A	-1385.000	4500.000
36	VRS	A	-1385.000	4440.000
37	VRS	A	-1385.000	4380.000
38	DUMMY	A	-1385.000	4320.000
39	AMPOUTP	A	-1385.000	4260.000
40	AMPOUTP	A	-1385.000	4200.000
41	AMPOUT	A	-1385.000	4140.000
42	AMPOUT	A	-1385.000	4080.000
43	VR	A	-1385.000	4020.000
44	VR	A	-1385.000	3960.000
45	VLC4	A	-1385.000	3900.000
46	VLC4	A	-1385.000	3840.000
47	VLC3	A	-1385.000	3780.000
48	VLC3	A	-1385.000	3720.000
49	VLC2	A	-1385.000	3660.000
50	VLC2	A	-1385.000	3600.000
51	VLC1	A	-1385.000	3540.000
52	VLC1	A	-1385.000	3480.000
53	VLCD	A	-1385.000	3420.000
54	VLCD	A	-1385.000	3360.000
55	VSS	A	-1385.000	3300.000
56	VOUT	A	-1385.000	3240.000
57	VOUT	A	-1385.000	3180.000
58	VSS	A	-1385.000	3120.000
59	DUMMY	A	-1385.000	3060.000
60	DUMMY	A	-1385.000	3000.000
61	DUMMY	A	-1385.000	2940.000
62	C9-	A	-1385.000	2880.000
63	C9-	A	-1385.000	2820.000
64	C9+	A	-1385.000	2760.000
65	C9+	A	-1385.000	2700.000
66	C8-	A	-1385.000	2640.000
67	C8-	A	-1385.000	2580.000
68	C8+	A	-1385.000	2520.000
69	C8+	A	-1385.000	2460.000
70	C7-	A	-1385.000	2400.000
71	C7-	A	-1385.000	2340.000
72	C7+	A	-1385.000	2280.000
73	C7+	A	-1385.000	2220.000
74	C6-	A	-1385.000	2160.000
75	C6-	A	-1385.000	2100.000
76	C6+	A	-1385.000	2040.000
77	C6+	A	-1385.000	1980.000
78	C5-	A	-1385.000	1920.000
79	C5-	A	-1385.000	1860.000
80	C5+	A	-1385.000	1800.000
81	C5+	A	-1385.000	1740.000
82	C4-	A	-1385.000	1680.000
83	C4-	A	-1385.000	1620.000
84	C4+	A	-1385.000	1560.000
85	C4+	A	-1385.000	1500.000
86	C3-	A	-1385.000	1440.000
87	C3-	A	-1385.000	1380.000
88	C3+	A	-1385.000	1320.000
89	C3+	A	-1385.000	1260.000
90	C2-	A	-1385.000	1200.000
91	C2-	A	-1385.000	1140.000
92	C2+	A	-1385.000	1080.000
93	C2+	A	-1385.000	1020.000
94	C1-	A	-1385.000	960.000
95	C1-	A	-1385.000	900.000
96	C1+	A	-1385.000	840.000
97	C1+	A	-1385.000	780.000
98	C1A	A	-1385.000	720.000
99	C1A	A	-1385.000	660.000
100	VDD2	A	-1385.000	600.000
101	VDD2	A	-1385.000	540.000
102	VDD2	A	-1385.000	480.000
103	VDD1	A	-1385.000	420.000
104	VDD1	A	-1385.000	360.000
105	VDD1	A	-1385.000	300.000
106	VSS	A	-1385.000	240.000
107	VSS	A	-1385.000	180.000
108	VSS	A	-1385.000	120.000
109	CLS	A	-1385.000	60.000
110	CLS	A	-1385.000	0.000
111	VDD1	A	-1385.000	-60.000
112	TM,S	A	-1385.000	-120.000
113	TM,S	A	-1385.000	-180.000
114	VSS	A	-1385.000	-240.000
115	C86	A	-1385.000	-300.000
116	C86	A	-1385.000	-360.000
117	PSX	A	-1385.000	-420.000
118	PSX	A	-1385.000	-480.000
119	VDD1	A	-1385.000	-540.000
120	IRS	A	-1385.000	-600.000
121	IRS	A	-1385.000	-660.000
122	VSS	A	-1385.000	-720.000
123	/CS1	A	-1385.000	-780.000
124	/CS1	A	-1385.000	-840.000
125	CS2	A	-1385.000	-900.000
126	CS2	A	-1385.000	-960.000
127	VDD1	A	-1385.000	-1020.000
128	/RES	A	-1385.000	-1080.000
129	/RES	A	-1385.000	-1140.000
130	RS	A	-1385.000	-1200.000
131	RS	A	-1385.000	-1260.000
132	VSS	A	-1385.000	-1320.000
133	/WR (R,/W)	A	-1385.000	-1380.000
134	/WR (R,/W)	A	-1385.000	-1440.000
135	/RD (E)	A	-1385.000	-1500.000
136	/RD (E)	A	-1385.000	-1560.000
137	VDD1	A	-1385.000	-1620.000
138	D7 (SI)	A	-1385.000	-1680.000
139	D7 (SI)	A	-1385.000	-1740.000
140	D6 (SCL)	A	-1385.000	-1800.000
141	D6 (SCL)	A	-1385.000	-1860.000
142	D5	A	-1385.000	-1920.000
143	D5	A	-1385.000	-1980.000
144	D4	A	-1385.000	-2040.000
145	D4	A	-1385.000	-2100.000
146	D3	A	-1385.000	-2160.000
147	D3	A	-1385.000	-2220.000
148	D2	A	-1385.000	-2280.000
149	D2	A	-1385.000	-2340.000
150	D1	A	-1385.000	-2400.000
151	D1	A	-1385.000	-2460.000
152	D0	A	-1385.000	-2520.000
153	D0	A	-1385.000	-2580.000
154	TFRSYNC	A	-1385.000	-2640.000
155	TFRSYNC	A	-1385.000	-2700.000
156	TFR	A	-1385.000	-2760.000
157	TFR	A	-1385.000	-2820.000
158	TDOF	A	-1385.000	-2880.000
159	TDOF	A	-1385.000	-2940.000
160	OSCIN1	A	-1385.000	-3000.000
161	OSCIN1	A	-1385.000	-3060.000
162	OSCIN2	A	-1385.000	-3120.000
163	OSCIN2	A	-1385.000	-3180.000
164	OSCOUT	A	-1385.000	-3240.000
165	OSCOUT	A	-1385.000	-3300.000
166	TOSCSYNC	A	-1385.000	-3360.000
167	TOSCSYNC	A	-1385.000	-3420.000
168	TSISYNC	A	-1385.000	-3480.000
169	TSISYNC	A	-1385.000	-3540.000
170	VSS	A	-1385.000	-3600.000
171	SIGIN1	A	-1385.000	-3660.000
172	SIGIN1	A	-1385.000	-3720.000
173	VDD1	A	-1385.000	-3780.000
174	SIGIN2	A	-1385.000	-3840.000
175	SIGIN2	A	-1385.000	-3900.000
176	VSS	A	-1385.000	-3960.000
177	TESTOUT	A	-1385.000	-4020.000
178	TESTOUT	A	-1385.000	-4080.000
179	TSTIFS	A	-1385.000	-4140.000
180	TSTIFS	A	-1385.000	-4200.000
181	TSTRTST	A	-1385.000	-4260.000
182	TSTRTST	A	-1385.000	-4320.000
183	TSTVIHL	A	-1385.000	-4380.000
184	TSTVIHL	A	-1385.000	-4440.000
185	VSS	A	-1385.000	-4500.000
186	PSEG11	A	-1385.000	-4560.000
187	PSEG11	A	-1385.000	-4620.000
188	PSEG12	A	-1385.000	-4680.000
189	PSEG12	A	-1385.000	-4740.000
190	PSEG13	A	-1385.000	-4800.000
191	PSEG13	A	-1385.000	-4860.000
192	PSEG14	A	-1385.000	-4920.000
193	PSEG14	A	-1385.000	-4980.000
194	PSEG15	A	-1385.000	-5040.000
195	PSEG15	A	-1385.000	-5100.000
196	PSEG16	A	-1385.000	-5160.000
197	PSEG16	A	-1385.000	-5220.000
198	PSEG17	A	-1385.000	-5280.000
199	PSEG17	A	-1385.000	-5340.000
200	PSEG18	A	-1385.000	-5400.000
201	PSEG18	A	-1385.000	-5460.000
202	PSEG19	A	-1385.000	-5520.000
203	PSEG19	A	-1385.000	-5580.000
204	PSEG20	A	-1385.000	-5640.000
205	PSEG20	A	-1385.000	-5700.000
206	DUMMY	A	-1385.000	-5760.000
207	DUMMY	A	-1385.000	-5820.000
208	DUMMY	A	-1385.000	-5880.000
209	DUMMY	A	-1385.000	-5940.000
210	DUMMY	A	-1385.000	-6000.000

▪ **μPD16686 Pad Layout (2/3)**

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
211	DUMMY	A	-1385.000	-6060.000
212	DUMMY	A	-1385.000	-6120.000
213	DUMMY	A	-1385.000	-6180.000
214	DUMMY	A	-1385.000	-6240.000
215	DUMMY	A	-1385.000	-6300.000
216	DUMMY	A	-1385.000	-6360.000
217	DUMMY	A	-1385.000	-6420.000
218	DUMMY	A	-1385.000	-6480.000
219	DUMMY	A	-1385.000	-6540.000
220	DUMMY	B	-1385.000	-6635.000
221	DUMMY	B	-1185.000	-6766.600
222	DUMMY	A	-1090.000	-6766.600
223	PCOM1	A	-1030.000	-6766.600
224	PCOM1	A	-970.000	-6766.600
225	COM41	A	-910.000	-6766.600
226	COM42	A	-850.000	-6766.600
227	COM43	A	-790.000	-6766.600
228	COM44	A	-730.000	-6766.600
229	COM45	A	-670.000	-6766.600
230	COM46	A	-610.000	-6766.600
231	COM47	A	-550.000	-6766.600
232	COM48	A	-490.000	-6766.600
233	COM49	A	-430.000	-6766.600
234	COM50	A	-370.000	-6766.600
235	COM51	A	-310.000	-6766.600
236	COM52	A	-250.000	-6766.600
237	COM53	A	-190.000	-6766.600
238	COM54	A	-130.000	-6766.600
239	COM55	A	-70.000	-6766.600
240	COM56	A	-10.000	-6766.600
241	COM57	A	50.000	-6766.600
242	COM58	A	110.000	-6766.600
243	COM59	A	170.000	-6766.600
244	COM60	A	230.000	-6766.600
245	COM61	A	290.000	-6766.600
246	COM62	A	350.000	-6766.600
247	COM63	A	410.000	-6766.600
248	COM64	A	470.000	-6766.600
249	COM65	A	530.000	-6766.600
250	COM66	A	590.000	-6766.600
251	COM67	A	650.000	-6766.600
252	DUMMY	B	745.000	-6766.600
253	DUMMY	B	875.000	-6766.600
254	DUMMY	B	1005.000	-6766.600
255	DUMMY	B	1296.600	-6495.000
256	DUMMY	B	1296.600	-6365.000
257	DUMMY	A	1296.600	-6270.000
258	COM68	A	1296.600	-6210.000
259	COM69	A	1296.600	-6150.000
260	COM70	A	1296.600	-6090.000
261	COM71	A	1296.600	-6030.000
262	COM72	A	1296.600	-5970.000
263	COM73	A	1296.600	-5910.000
264	COM74	A	1296.600	-5850.000
265	COM75	A	1296.600	-5790.000
266	COM76	A	1296.600	-5730.000
267	COM77	A	1296.600	-5670.000
268	COM78	A	1296.600	-5610.000
269	COM79	A	1296.600	-5550.000
270	COM80	A	1296.600	-5490.000
271	COM82	A	1296.600	-5430.000
272	COM84	A	1296.600	-5370.000
273	COM86	A	1296.600	-5310.000
274	COM88	A	1296.600	-5250.000
275	COM90	A	1296.600	-5190.000
276	COM92	A	1296.600	-5130.000
277	COM94	A	1296.600	-5070.000
278	COM96	A	1296.600	-5010.000
279	COM98	A	1296.600	-4950.000
280	COM100	A	1296.600	-4890.000

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
281	COM102	A	1296.600	-4830.000
282	COM104	A	1296.600	-4770.000
283	COM106	A	1296.600	-4710.000
284	COM108	A	1296.600	-4650.000
285	COM110	A	1296.600	-4590.000
286	COM112	A	1296.600	-4530.000
287	COM114	A	1296.600	-4470.000
288	COM116	A	1296.600	-4410.000
289	COM118	A	1296.600	-4350.000
290	COM120	A	1296.600	-4290.000
291	COM122	A	1296.600	-4230.000
292	COM124	A	1296.600	-4170.000
293	COM126	A	1296.600	-4110.000
294	COM128	A	1296.600	-4050.000
295	DUMMY	A	1296.600	-3990.000
296	DUMMY	A	1296.600	-3930.000
297	DUMMY	A	1296.600	-3870.000
298	SEG128	A	1296.600	-3810.000
299	SEG127	A	1296.600	-3750.000
300	SEG126	A	1296.600	-3690.000
301	SEG125	A	1296.600	-3630.000
302	SEG124	A	1296.600	-3570.000
303	SEG123	A	1296.600	-3510.000
304	SEG122	A	1296.600	-3450.000
305	SEG121	A	1296.600	-3390.000
306	SEG120	A	1296.600	-3330.000
307	SEG119	A	1296.600	-3270.000
308	SEG118	A	1296.600	-3210.000
309	SEG117	A	1296.600	-3150.000
310	SEG116	A	1296.600	-3090.000
311	SEG115	A	1296.600	-3030.000
312	SEG114	A	1296.600	-2970.000
313	SEG113	A	1296.600	-2910.000
314	SEG112	A	1296.600	-2850.000
315	SEG111	A	1296.600	-2790.000
316	SEG110	A	1296.600	-2730.000
317	SEG109	A	1296.600	-2670.000
318	SEG108	A	1296.600	-2610.000
319	SEG107	A	1296.600	-2550.000
320	SEG106	A	1296.600	-2490.000
321	SEG105	A	1296.600	-2430.000
322	SEG104	A	1296.600	-2370.000
323	SEG103	A	1296.600	-2310.000
324	SEG102	A	1296.600	-2250.000
325	SEG101	A	1296.600	-2190.000
326	SEG100	A	1296.600	-2130.000
327	SEG99	A	1296.600	-2070.000
328	SEG98	A	1296.600	-2010.000
329	SEG97	A	1296.600	-1950.000
330	SEG96	A	1296.600	-1890.000
331	SEG95	A	1296.600	-1830.000
332	SEG94	A	1296.600	-1770.000
333	SEG93	A	1296.600	-1710.000
334	SEG92	A	1296.600	-1650.000
335	SEG91	A	1296.600	-1590.000
336	SEG90	A	1296.600	-1530.000
337	SEG89	A	1296.600	-1470.000
338	SEG88	A	1296.600	-1410.000
339	SEG87	A	1296.600	-1350.000
340	SEG86	A	1296.600	-1290.000
341	SEG85	A	1296.600	-1230.000
342	SEG84	A	1296.600	-1170.000
343	SEG83	A	1296.600	-1110.000
344	SEG82	A	1296.600	-1050.000
345	SEG81	A	1296.600	-990.000
346	SEG80	A	1296.600	-930.000
347	SEG79	A	1296.600	-870.000
348	SEG78	A	1296.600	-810.000
349	SEG77	A	1296.600	-750.000
350	SEG76	A	1296.600	-690.000

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
351	SEG75	A	1296.600	-630.000
352	SEG74	A	1296.600	-570.000
353	SEG73	A	1296.600	-510.000
354	SEG72	A	1296.600	-450.000
355	SEG71	A	1296.600	-390.000
356	SEG70	A	1296.600	-330.000
357	SEG69	A	1296.600	-270.000
358	SEG68	A	1296.600	-210.000
359	SEG67	A	1296.600	-150.000
360	SEG66	A	1296.600	-90.000
361	SEG65	A	1296.600	-30.000
362	SEG64	A	1296.600	30.000
363	SEG63	A	1296.600	90.000
364	SEG62	A	1296.600	150.000
365	SEG61	A	1296.600	210.000
366	SEG60	A	1296.600	270.000
367	SEG59	A	1296.600	330.000
368	SEG58	A	1296.600	390.000
369	SEG57	A	1296.600	450.000
370	SEG56	A	1296.600	510.000
371	SEG55	A	1296.600	570.000
372	SEG54	A	1296.600	630.000
373	SEG53	A	1296.600	690.000
374	SEG52	A	1296.600	750.000
375	SEG51	A	1296.600	810.000
376	SEG50	A	1296.600	870.000
377	SEG49	A	1296.600	930.000
378	SEG48	A	1296.600	990.000
379	SEG47	A	1296.600	1050.000
380	SEG46	A	1296.600	1110.000
381	SEG45	A	1296.600	1170.000
382	SEG44	A	1296.600	1230.000
383	SEG43	A	1296.600	1290.000
384	SEG42	A	1296.600	1350.000
385	SEG41	A	1296.600	1410.000
386	SEG40	A	1296.600	1470.000
387	SEG39	A	1296.600	1530.000
388	SEG38	A	1296.600	1590.000
389	SEG37	A	1296.600	1650.000
390	SEG36	A	1296.600	1710.000
391	SEG35	A	1296.600	1770.000
392	SEG34	A	1296.600	1830.000
393	SEG33	A	1296.600	1890.000
394	SEG32	A	1296.600	1950.000
395	SEG31	A	1296.600	2010.000
396	SEG30	A	1296.600	2070.000
397	SEG29	A	1296.600	2130.000
398	SEG28	A	1296.600	2190.000
399	SEG27	A	1296.600	2250.000
400	SEG26	A	1296.600	2310.000
401	SEG25	A	1296.600	2370.000
402	SEG24	A	1296.600	2430.000
403	SEG23	A	1296.600	2490.000
404	SEG22	A	1296.600	2550.000
405	SEG21	A	1296.600	2610.000
406	SEG20	A	1296.600	2670.000
407	SEG19	A	1296.600	2730.000
408	SEG18	A	1296.600	2790.000
409	SEG17	A	1296.600	2850.000
410	SEG16	A	1296.600	2910.000
411	SEG15	A	1296.600	2970.000
412	SEG14	A	1296.600	3030.000
413	SEG13	A	1296.600	3090.000
414	SEG12	A	1296.600	3150.000
415	SEG11	A	1296.600	3210.000
416	SEG10	A	1296.600	3270.000
417	SEG9	A	1296.600	3330.000
418	SEG8	A	1296.600	3390.000
419	SEG7	A	1296.600	3450.000
420	SEG6	A	1296.600	3510.000

▪ μPD16686 Pad Layout (3/3)

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
421	SEG5	A	1296.600	3570.000
422	SEG4	A	1296.600	3630.000
423	SEG3	A	1296.600	3690.000
424	SEG2	A	1296.600	3750.000
425	SEG1	A	1296.600	3810.000
426	DUMMY	A	1296.600	3870.000
427	DUMMY	A	1296.600	3930.000
428	DUMMY	A	1296.600	3990.000
429	COM127	A	1296.600	4050.000
430	COM125	A	1296.600	4110.000
431	COM123	A	1296.600	4170.000
432	COM121	A	1296.600	4230.000
433	COM119	A	1296.600	4290.000
434	COM117	A	1296.600	4350.000
435	COM115	A	1296.600	4410.000
436	COM113	A	1296.600	4470.000
437	COM111	A	1296.600	4530.000
438	COM109	A	1296.600	4590.000
439	COM107	A	1296.600	4650.000
440	COM105	A	1296.600	4710.000
441	COM103	A	1296.600	4770.000
442	COM101	A	1296.600	4830.000
443	COM99	A	1296.600	4890.000
444	COM97	A	1296.600	4950.000
445	COM95	A	1296.600	5010.000
446	COM93	A	1296.600	5070.000
447	COM91	A	1296.600	5130.000
448	COM89	A	1296.600	5190.000
449	COM87	A	1296.600	5250.000
450	COM85	A	1296.600	5310.000
451	COM83	A	1296.600	5370.000
452	COM81	A	1296.600	5430.000
453	COM40	A	1296.600	5490.000
454	COM39	A	1296.600	5550.000
455	COM38	A	1296.600	5610.000
456	COM37	A	1296.600	5670.000
457	COM36	A	1296.600	5730.000
458	COM35	A	1296.600	5790.000
459	COM34	A	1296.600	5850.000
460	COM33	A	1296.600	5910.000
461	COM32	A	1296.600	5970.000
462	COM31	A	1296.600	6030.000
463	COM30	A	1296.600	6090.000
464	COM29	A	1296.600	6150.000
465	COM28	A	1296.600	6210.000
466	DUMMY	A	1296.600	6270.000
467	DUMMY	B	1296.600	6365.000
468	DUMMY	B	1296.600	6495.000
469	DUMMY	B	1030.000	6766.600
470	DUMMY	B	900.000	6766.600
471	DUMMY	B	770.000	6766.600
472	COM27	A	675.000	6766.600
473	COM26	A	615.000	6766.600
474	COM25	A	555.000	6766.600
475	COM24	A	495.000	6766.600
476	COM23	A	435.000	6766.600
477	COM22	A	375.000	6766.600
478	COM21	A	315.000	6766.600
479	COM20	A	255.000	6766.600
480	COM19	A	195.000	6766.600
481	COM18	A	135.000	6766.600
482	COM17	A	75.000	6766.600
483	COM16	A	15.000	6766.600
484	COM15	A	-45.000	6766.600
485	COM14	A	-105.000	6766.600
486	COM13	A	-165.000	6766.600
487	COM12	A	-225.000	6766.600
488	COM11	A	-285.000	6766.600
489	COM10	A	-345.000	6766.600
490	COM9	A	-405.000	6766.600

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
491	COM8	A	-465.000	6766.600
492	COM7	A	-525.000	6766.600
493	COM6	A	-585.000	6766.600
494	COM5	A	-645.000	6766.600
495	COM4	A	-705.000	6766.600
496	OCM3	A	-765.000	6766.600
497	COM2	A	-825.000	6766.600
498	COM1	A	-885.000	6766.600
499	PCOM1	A	-945.000	6766.600
500	PCOM1	A	-1005.000	6766.600
501	DUMMY	A	-1065.000	6766.600
502	DUMMY	B	-1160.000	6766.600

Pad type A:

Pad size(Al) : 48 x 106 μm2 TYP.
Pad size(Through hall) :10 x 60.48 μm2 TYP.
Bump size : 35 x 92.5 μm2 TYP.
Bump height : 17 μm TYP.

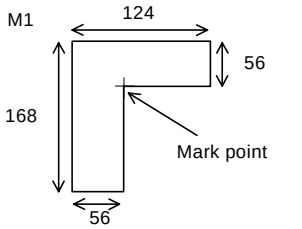
Pad type B:

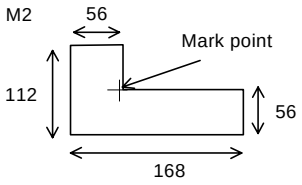
Pad size(Al) : 108 x 106 μm2 TYP.
Pad size(Through hall) :78 x 60.48 μm2 TYP.
Bump size : 110 x 92.5 μm2 TYP.
Bump height : 17 μm TYP.

Alingment mark

	Alingment mark coordinate	
	X [μm]	Y [μm]
M1	-1382.00	6830.00
M2	1220.00	-6760.00

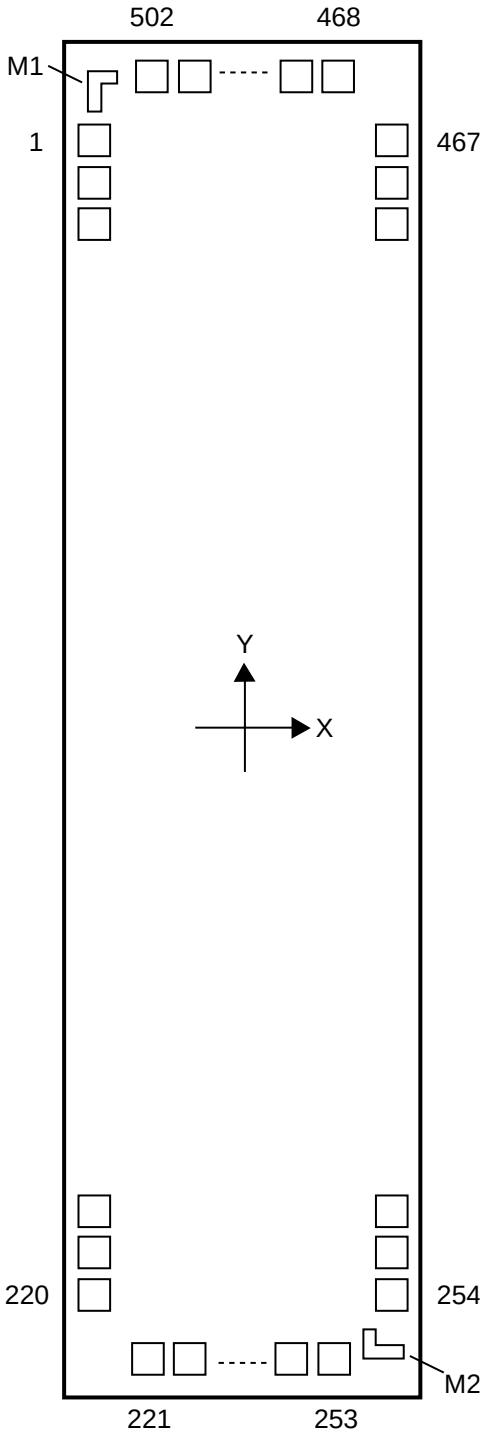
Alingment mark form (μm)





(2) μPD16687

Chip size : 3.04 x 13.98 mm^2
Chip thickness : 485 μm (TYP.)



▪ **μPD16687 Pad Layout (1/3)**

Pad No.	Pin Name	Pad Type	X [mm]	Y [mm]
1	DUMMY	B	-1385.000	6575.000
2	DUMMY	A	-1385.000	6480.000
3	DUMMY	A	-1385.000	6420.000
4	DUMMY	A	-1385.000	6360.000
5	DUMMY	A	-1385.000	6300.000
6	DUMMY	A	-1385.000	6240.000
7	DUMMY	A	-1385.000	6180.000
8	DUMMY	A	-1385.000	6120.000
9	DUMMY	A	-1385.000	6060.000
10	DUMMY	A	-1385.000	6000.000
11	DUMMY	A	-1385.000	5940.000
12	DUMMY	A	-1385.000	5880.000
13	DUMMY	A	-1385.000	5820.000
14	DUMMY	A	-1385.000	5760.000
15	PSEG1	A	-1385.000	5700.000
16	PSEG1	A	-1385.000	5640.000
17	PSEG2	A	-1385.000	5580.000
18	PSEG2	A	-1385.000	5520.000
19	PSEG3	A	-1385.000	5460.000
20	PSEG3	A	-1385.000	5400.000
21	PSEG4	A	-1385.000	5340.000
22	PSEG4	A	-1385.000	5280.000
23	PSEG5	A	-1385.000	5220.000
24	PSEG5	A	-1385.000	5160.000
25	PSEG6	A	-1385.000	5100.000
26	PSEG6	A	-1385.000	5040.000
27	PSEG7	A	-1385.000	4980.000
28	PSEG7	A	-1385.000	4920.000
29	PSEG8	A	-1385.000	4860.000
30	PSEG8	A	-1385.000	4800.000
31	PSEG9	A	-1385.000	4740.000
32	PSEG9	A	-1385.000	4680.000
33	PSEG10	A	-1385.000	4620.000
34	PSEG10	A	-1385.000	4560.000
35	VSS	A	-1385.000	4500.000
36	VRS	A	-1385.000	4440.000
37	VRS	A	-1385.000	4380.000
38	DUMMY	A	-1385.000	4320.000
39	AMPOUTP	A	-1385.000	4260.000
40	AMPOUTP	A	-1385.000	4200.000
41	AMPOUT	A	-1385.000	4140.000
42	AMPOUT	A	-1385.000	4080.000
43	VR	A	-1385.000	4020.000
44	VR	A	-1385.000	3960.000
45	VLC4	A	-1385.000	3900.000
46	VLC4	A	-1385.000	3840.000
47	VLC3	A	-1385.000	3780.000
48	VLC3	A	-1385.000	3720.000
49	VLC2	A	-1385.000	3660.000
50	VLC2	A	-1385.000	3600.000
51	VLC1	A	-1385.000	3540.000
52	VLC1	A	-1385.000	3480.000
53	VLCD	A	-1385.000	3420.000
54	VLCD	A	-1385.000	3360.000
55	VSS	A	-1385.000	3300.000
56	VOUT	A	-1385.000	3240.000
57	VOUT	A	-1385.000	3180.000
58	VSS	A	-1385.000	3120.000
59	DUMMY	A	-1385.000	3060.000
60	DUMMY	A	-1385.000	3000.000
61	DUMMY	A	-1385.000	2940.000
62	C9-	A	-1385.000	2880.000
63	C9-	A	-1385.000	2820.000
64	C9+	A	-1385.000	2760.000
65	C9+	A	-1385.000	2700.000
66	C8-	A	-1385.000	2640.000
67	C8-	A	-1385.000	2580.000
68	C8+	A	-1385.000	2520.000
69	C8+	A	-1385.000	2460.000
70	C7-	A	-1385.000	2400.000

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
71	C7-	A	-1385.000	2340.000
72	C7+	A	-1385.000	2280.000
73	C7+	A	-1385.000	2220.000
74	C6-	A	-1385.000	2160.000
75	C6-	A	-1385.000	2100.000
76	C6+	A	-1385.000	2040.000
77	C6+	A	-1385.000	1980.000
78	C5-	A	-1385.000	1920.000
79	C5-	A	-1385.000	1860.000
80	C5+	A	-1385.000	1800.000
81	C5+	A	-1385.000	1740.000
82	C4-	A	-1385.000	1680.000
83	C4-	A	-1385.000	1620.000
84	C4+	A	-1385.000	1560.000
85	C4+	A	-1385.000	1500.000
86	C3-	A	-1385.000	1440.000
87	C3-	A	-1385.000	1380.000
88	C3+	A	-1385.000	1320.000
89	C3+	A	-1385.000	1260.000
90	C2-	A	-1385.000	1200.000
91	C2-	A	-1385.000	1140.000
92	C2+	A	-1385.000	1080.000
93	C2+	A	-1385.000	1020.000
94	C1-	A	-1385.000	960.000
95	C1-	A	-1385.000	900.000
96	C1+	A	-1385.000	840.000
97	C1+	A	-1385.000	780.000
98	C1A	A	-1385.000	720.000
99	C1A	A	-1385.000	660.000
100	VDD2	A	-1385.000	600.000
101	VDD2	A	-1385.000	540.000
102	VDD2	A	-1385.000	480.000
103	VDD1	A	-1385.000	420.000
104	VDD1	A	-1385.000	360.000
105	VDD1	A	-1385.000	300.000
106	VSS	A	-1385.000	240.000
107	VSS	A	-1385.000	180.000
108	VSS	A	-1385.000	120.000
109	CLS	A	-1385.000	60.000
110	CLS	A	-1385.000	0.000
111	VDD1	A	-1385.000	-60.000
112	TM,S	A	-1385.000	-120.000
113	TM,S	A	-1385.000	-180.000
114	VSS	A	-1385.000	-240.000
115	C86	A	-1385.000	-300.000
116	C86	A	-1385.000	-360.000
117	PSX	A	-1385.000	-420.000
118	PSX	A	-1385.000	-480.000
119	VDD1	A	-1385.000	-540.000
120	IRS	A	-1385.000	-600.000
121	IRS	A	-1385.000	-660.000
122	VSS	A	-1385.000	-720.000
123	/CS1	A	-1385.000	-780.000
124	/CS1	A	-1385.000	-840.000
125	CS2	A	-1385.000	-900.000
126	CS2	A	-1385.000	-960.000
127	VDD1	A	-1385.000	-1020.000
128	/RES	A	-1385.000	-1080.000
129	/RES	A	-1385.000	-1140.000
130	RS	A	-1385.000	-1200.000
131	RS	A	-1385.000	-1260.000
132	VSS	A	-1385.000	-1320.000
133	/WR (R,/W)	A	-1385.000	-1380.000
134	/WR (R,/W)	A	-1385.000	-1440.000
135	/RD (E)	A	-1385.000	-1500.000
136	/RD (E)	A	-1385.000	-1560.000
137	VDD1	A	-1385.000	-1620.000
138	D7 (SI)	A	-1385.000	-1680.000
139	D7 (SI)	A	-1385.000	-1740.000
140	D6 (SCL)	A	-1385.000	-1800.000

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
141	D6 (SCL)	A	-1385.000	-1860.000
142	D5	A	-1385.000	-1920.000
143	D5	A	-1385.000	-1980.000
144	D4	A	-1385.000	-2040.000
145	D4	A	-1385.000	-2100.000
146	D3	A	-1385.000	-2160.000
147	D3	A	-1385.000	-2220.000
148	D2	A	-1385.000	-2280.000
149	D2	A	-1385.000	-2340.000
150	D1	A	-1385.000	-2400.000
151	D1	A	-1385.000	-2460.000
152	D0	A	-1385.000	-2520.000
153	D0	A	-1385.000	-2580.000
154	TFRSYNC	A	-1385.000	-2640.000
155	TFRSYNC	A	-1385.000	-2700.000
156	TFR	A	-1385.000	-2760.000
157	TFR	A	-1385.000	-2820.000
158	TDOF	A	-1385.000	-2880.000
159	TDOF	A	-1385.000	-2940.000
160	OSCIN1	A	-1385.000	-3000.000
161	OSCIN1	A	-1385.000	-3060.000
162	OSCIN2	A	-1385.000	-3120.000
163	OSCIN2	A	-1385.000	-3180.000
164	OSCOUT	A	-1385.000	-3240.000
165	OSCOUT	A	-1385.000	-3300.000
166	TOSCSYNC	A	-1385.000	-3360.000
167	TOSCSYNC	A	-1385.000	-3420.000
168	TSISYNC	A	-1385.000	-3480.000
169	TSISYNC	A	-1385.000	-3540.000
170	VSS	A	-1385.000	-3600.000
171	SIGIN1	A	-1385.000	-3660.000
172	SIGIN1	A	-1385.000	-3720.000
173	VDD1	A	-1385.000	-3780.000
174	SIGIN2	A	-1385.000	-3840.000
175	SIGIN2	A	-1385.000	-3900.000
176	VSS	A	-1385.000	-3960.000
177	TESTOUT	A	-1385.000	-4020.000
178	TESTOUT	A	-1385.000	-4080.000
179	TSTIFS	A	-1385.000	-4140.000
180	TSTIFS	A	-1385.000	-4200.000
181	TSTRTST	A	-1385.000	-4260.000
182	TSTRTST	A	-1385.000	-4320.000
183	TSTVIHL	A	-1385.000	-4380.000
184	TSTVIHL	A	-1385.000	-4440.000
185	VSS	A	-1385.000	-4500.000
186	PSEG11	A	-1385.000	-4560.000
187	PSEG11	A	-1385.000	-4620.000
188	PSEG12	A	-1385.000	-4680.000
189	PSEG12	A	-1385.000	-4740.000
190	PSEG13	A	-1385.000	-4800.000
191	PSEG13	A	-1385.000	-4860.000
192	PSEG14	A	-1385.000	-4920.000
193	PSEG14	A	-1385.000	-4980.000
194	PSEG15	A	-1385.000	-5040.000
195	PSEG15	A	-1385.000	-5100.000
196	PSEG16	A	-1385.000	-5160.000
197	PSEG16	A	-1385.000	-5220.000
198	PSEG17	A	-1385.000	-5280.000
199	PSEG17	A	-1385.000	-5340.000
200	PSEG18	A	-1385.000	-5400.000
201	PSEG18	A	-1385.000	-5460.000
202	PSEG19	A	-1385.000	-5520.000
203	PSEG19	A	-1385.000	-5580.000
204	PSEG20	A	-1385.000	-5640.000
205	PSEG20	A	-1385.000	-5700.000
206	DUMMY	A	-1385.000	-5760.000
207	DUMMY	A	-1385.000	-5820.000
208	DUMMY	A	-1385.000	-5880.000
209	DUMMY	A	-1385.000	-5940.000
210	DUMMY	A	-1385.000	-6000.000

▪ **μPD16687 Pad Layout (2/3)**

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
211	DUMMY	A	-1385.000	-6060.000
212	DUMMY	A	-1385.000	-6120.000
213	DUMMY	A	-1385.000	-6180.000
214	DUMMY	A	-1385.000	-6240.000
215	DUMMY	A	-1385.000	-6300.000
216	DUMMY	A	-1385.000	-6360.000
217	DUMMY	A	-1385.000	-6420.000
218	DUMMY	A	-1385.000	-6480.000
219	DUMMY	A	-1385.000	-6540.000
220	DUMMY	B	-1385.000	-6635.000
221	DUMMY	B	-1185.000	-6766.600
222	DUMMY	A	-1090.000	-6766.600
223	PCOM1	A	-1030.000	-6766.600
224	PCOM1	A	-970.000	-6766.600
225	SEG128	A	-910.000	-6766.600
226	SEG127	A	-850.000	-6766.600
227	SEG126	A	-790.000	-6766.600
228	SEG125	A	-730.000	-6766.600
229	SEG124	A	-670.000	-6766.600
230	SEG123	A	-610.000	-6766.600
231	SEG122	A	-550.000	-6766.600
232	SEG121	A	-490.000	-6766.600
233	SEG120	A	-430.000	-6766.600
234	SEG119	A	-370.000	-6766.600
235	SEG118	A	-310.000	-6766.600
236	SEG117	A	-250.000	-6766.600
237	SEG116	A	-190.000	-6766.600
238	SEG115	A	-130.000	-6766.600
239	SEG114	A	-70.000	-6766.600
240	SEG113	A	-10.000	-6766.600
241	SEG112	A	50.000	-6766.600
242	SEG111	A	110.000	-6766.600
243	SEG110	A	170.000	-6766.600
244	SEG109	A	230.000	-6766.600
245	SEG108	A	290.000	-6766.600
246	SEG107	A	350.000	-6766.600
247	SEG106	A	410.000	-6766.600
248	SEG105	A	470.000	-6766.600
249	SEG104	A	530.000	-6766.600
250	SEG103	A	590.000	-6766.600
251	DUMMY	B	685.000	-6766.600
252	DUMMY	B	815.000	-6766.600
253	DUMMY	B	945.000	-6766.600
254	DUMMY	B	1296.600	-6495.000
255	DUMMY	B	1296.600	-6365.000
256	DUMMY	A	1296.600	-6270.000
257	DUMMY	A	1296.600	-6210.000
258	SEG102	A	1296.600	-6150.000
259	SEG101	A	1296.600	-6090.000
260	SEG100	A	1296.600	-6030.000
261	SEG99	A	1296.600	-5970.000
262	SEG98	A	1296.600	-5910.000
263	SEG97	A	1296.600	-5850.000
264	SEG96	A	1296.600	-5790.000
265	SEG95	A	1296.600	-5730.000
266	SEG94	A	1296.600	-5670.000
267	SEG93	A	1296.600	-5670.000
268	SEG92	A	1296.600	-5550.000
269	SEG91	A	1296.600	-5490.000
270	SEG90	A	1296.600	-5430.000
271	SEG89	A	1296.600	-5370.000
272	SEG88	A	1296.600	-5310.000
273	SEG87	A	1296.600	-5250.000
274	SEG86	A	1296.600	-5190.000
275	SEG85	A	1296.600	-5130.000
276	SEG84	A	1296.600	-5070.000
277	SEG83	A	1296.600	-5010.000
278	SEG82	A	1296.600	-4950.000
279	SEG81	A	1296.600	-4890.000
280	SEG80	A	1296.600	-4830.000
281	SEG79	A	1296.600	-4770.000
282	SEG78	A	1296.600	-4710.000
283	SEG77	A	1296.600	-4650.000
284	SEG76	A	1296.600	-4590.000
285	SEG75	A	1296.600	-4530.000
286	SEG74	A	1296.600	-4470.000
287	SEG73	A	1296.600	-4410.000
288	SEG72	A	1296.600	-4350.000
289	SEG71	A	1296.600	-4290.000
290	SEG70	A	1296.600	-4230.000
291	SEG69	A	1296.600	-4170.000
292	SEG68	A	1296.600	-4110.000
293	SEG67	A	1296.600	-4050.000
294	SEG66	A	1296.600	-3990.000
295	SEG65	A	1296.600	-3930.000
296	SEG64	A	1296.600	-3870.000
297	SEG63	A	1296.600	-3810.000
298	SEG62	A	1296.600	-3750.000
299	SEG61	A	1296.600	-3690.000
300	SEG60	A	1296.600	-3630.000
301	SEG59	A	1296.600	-3570.000
302	SEG58	A	1296.600	-3510.000
303	SEG57	A	1296.600	-3450.000
304	SEG56	A	1296.600	-3390.000
305	SEG55	A	1296.600	-3330.000
306	SEG54	A	1296.600	-3270.000
307	SEG53	A	1296.600	-3210.000
308	SEG52	A	1296.600	-3150.000
309	SEG51	A	1296.600	-3090.000
310	SEG50	A	1296.600	-3030.000
311	SEG49	A	1296.600	-2970.000
312	SEG48	A	1296.600	-2910.000
313	SEG47	A	1296.600	-2850.000
314	SEG46	A	1296.600	-2790.000
315	SEG45	A	1296.600	-2730.000
316	SEG44	A	1296.600	-2670.000
317	SEG43	A	1296.600	-2610.000
318	SEG42	A	1296.600	-2550.000
319	SEG41	A	1296.600	-2490.000
320	SEG40	A	1296.600	-2430.000
321	SEG39	A	1296.600	-2370.000
322	SEG38	A	1296.600	-2310.000
323	SEG37	A	1296.600	-2250.000
324	SEG36	A	1296.600	-2190.000
325	SEG35	A	1296.600	-2130.000
326	SEG34	A	1296.600	-2070.000
327	SEG33	A	1296.600	-2010.000
328	SEG32	A	1296.600	-1950.000
329	SEG31	A	1296.600	-1890.000
330	SEG30	A	1296.600	-1830.000
331	SEG29	A	1296.600	-1770.000
332	SEG28	A	1296.600	-1710.000
333	SEG27	A	1296.600	-1650.000
334	SEG26	A	1296.600	-1590.000
335	SEG25	A	1296.600	-1530.000
336	SEG24	A	1296.600	-1470.000
337	SEG23	A	1296.600	-1410.000
338	SEG22	A	1296.600	-1350.000
339	SEG21	A	1296.600	-1290.000
340	SEG20	A	1296.600	-1230.000
341	SEG19	A	1296.600	-1170.000
342	SEG18	A	1296.600	-1110.000
343	SEG17	A	1296.600	-1050.000
344	SEG16	A	1296.600	-990.000
345	SEG15	A	1296.600	-930.000
346	SEG14	A	1296.600	-870.000
347	SEG13	A	1296.600	-810.000
348	SEG12	A	1296.600	-750.000
349	SEG11	A	1296.600	-690.000
350	SEG10	A	1296.600	-630.000
351	SEG9	A	1296.600	-570.000
352	SEG8	A	1296.600	-510.000
353	SEG7	A	1296.600	-450.000
354	SEG6	A	1296.600	-390.000
355	SEG5	A	1296.600	-330.000
356	SEG4	A	1296.600	-270.000
357	SEG3	A	1296.600	-210.000
358	SEG2	A	1296.600	-150.000
359	SEG1	A	1296.600	-90.000
360	DUMMY	A	1296.600	-30.000
361	DUMMY	A	1296.600	30.000
362	DUMMY	A	1296.600	90.000
363	COM128	A	1296.600	150.000
364	COM127	A	1296.600	210.000
365	COM126	A	1296.600	270.000
366	COM125	A	1296.600	330.000
367	COM124	A	1296.600	390.000
368	COM123	A	1296.600	450.000
369	COM122	A	1296.600	510.000
370	COM121	A	1296.600	570.000
371	COM120	A	1296.600	630.000
372	COM119	A	1296.600	690.000
373	COM118	A	1296.600	750.000
374	COM117	A	1296.600	810.000
375	COM116	A	1296.600	870.000
376	COM115	A	1296.600	930.000
377	COM114	A	1296.600	990.000
378	COM113	A	1296.600	1050.000
379	COM112	A	1296.600	1110.000
380	COM111	A	1296.600	1170.000
381	COM110	A	1296.600	1230.000
382	COM109	A	1296.600	1290.000
383	COM108	A	1296.600	1350.000
384	COM107	A	1296.600	1410.000
385	COM106	A	1296.600	1470.000
386	COM105	A	1296.600	1530.000
387	COM104	A	1296.600	1590.000
388	COM103	A	1296.600	1650.000
389	COM102	A	1296.600	1710.000
390	COM101	A	1296.600	1770.000
391	COM100	A	1296.600	1830.000
392	COM99	A	1296.600	1890.000
393	COM98	A	1296.600	1950.000
394	COM97	A	1296.600	2010.000
395	COM96	A	1296.600	2070.000
396	COM95	A	1296.600	2130.000
397	COM94	A	1296.600	2190.000
398	COM93	A	1296.600	2250.000
399	COM92	A	1296.600	2310.000
400	COM91	A	1296.600	2370.000
401	COM90	A	1296.600	2430.000
402	COM89	A	1296.600	2490.000
403	COM88	A	1296.600	2550.000
404	COM87	A	1296.600	2610.000
405	COM86	A	1296.600	2670.000
406	COM85	A	1296.600	2730.000
407	COM84	A	1296.600	2790.000
408	COM83	A	1296.600	2850.000
409	COM82	A	1296.600	2910.000
410	COM81	A	1296.600	2970.000
411	COM80	A	1296.600	3030.000
412	COM79	A	1296.600	3090.000
413	COM78	A	1296.600	3150.000
414	COM77	A	1296.600	3210.000
415	COM76	A	1296.600	3270.000
416	COM75	A	1296.600	3330.000
417	COM74	A	1296.600	3390.000
418	COM73	A	1296.600	3450.000
419	COM72	A	1296.600	3510.000
420	COM71	A	1296.600	3570.000

▪ μPD16687 Pad Layout (3/3)

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
421	COM70	A	1296.600	3630.000
422	COM69	A	1296.600	3690.000
423	COM68	A	1296.600	3750.000
424	COM67	A	1296.600	3810.000
425	COM66	A	1296.600	3870.000
426	COM65	A	1296.600	3930.000
427	COM64	A	1296.600	3990.000
428	COM63	A	1296.600	4050.000
429	COM62	A	1296.600	4110.000
430	COM61	A	1296.600	4170.000
431	COM60	A	1296.600	4230.000
432	COM59	A	1296.600	4290.000
433	COM58	A	1296.600	4350.000
434	COM57	A	1296.600	4410.000
435	COM56	A	1296.600	4470.000
436	COM55	A	1296.600	4530.000
437	COM54	A	1296.600	4590.000
438	COM53	A	1296.600	4650.000
439	COM52	A	1296.600	4710.000
440	COM51	A	1296.600	4770.000
441	COM50	A	1296.600	4830.000
442	COM49	A	1296.600	4890.000
443	COM48	A	1296.600	4950.000
444	COM47	A	1296.600	5010.000
445	COM46	A	1296.600	5070.000
446	COM45	A	1296.600	5130.000
447	COM44	A	1296.600	5190.000
448	COM43	A	1296.600	5250.000
449	COM42	A	1296.600	5310.000
450	COM41	A	1296.600	5370.000
451	COM40	A	1296.600	5430.000
452	COM39	A	1296.600	5490.000
453	COM38	A	1296.600	5550.000
454	COM37	A	1296.600	5610.000
455	COM36	A	1296.600	5670.000
456	COM35	A	1296.600	5730.000
457	COM34	A	1296.600	5790.000
458	COM33	A	1296.600	5850.000
459	COM32	A	1296.600	5910.000
460	COM31	A	1296.600	5970.000
461	COM30	A	1296.600	6030.000
462	COM29	A	1296.600	6090.000
463	COM28	A	1296.600	6150.000
464	COM27	A	1296.600	6210.000
465	DUMMY	A	1296.600	6270.000
466	DUMMY	B	1296.600	6365.000
467	DUMMY	B	1296.600	6495.000
468	DUMMY	B	970.000	6766.600
469	DUMMY	B	840.000	6766.600
470	DUMMY	B	710.000	6766.600
471	COM26	A	615.000	6766.600
472	COM25	A	555.000	6766.600
473	COM24	A	495.000	6766.600
474	COM23	A	435.000	6766.600
475	COM22	A	375.000	6766.600
476	COM21	A	315.000	6766.600
477	COM20	A	255.000	6766.600
478	COM19	A	195.000	6766.600
479	COM18	A	135.000	6766.600
480	COM17	A	75.000	6766.600
481	COM16	A	15.000	6766.600
482	COM15	A	-45.000	6766.600
483	COM14	A	-105.000	6766.600
484	COM13	A	-165.000	6766.600
485	COM12	A	-225.000	6766.600
486	COM11	A	-285.000	6766.600
487	COM10	A	-345.000	6766.600
488	COM9	A	-405.000	6766.600
489	COM8	A	-465.000	6766.600
490	COM7	A	-525.000	6766.600

Pad No.	Pin Name	Pad Type	X [μm]	Y [μm]
491	COM6	A	-585.000	6766.600
492	COM5	A	-645.000	6766.600
493	COM4	A	-705.000	6766.600
494	OCM3	A	-765.000	6766.600
495	COM2	A	-825.000	6766.600
496	COM1	A	-885.000	6766.600
497	PCOM1	A	-945.000	6766.600
498	PCOM1	A	-1005.000	6766.600
499	DUMMY	A	-1065.000	6766.600
500	DUMMY	B	-1160.000	6766.600

Pad type A:

Pad size(Al) : 48 x 106 μm2 TYP.
Pad size(Through hall) :10 x 60.48 μm2 TYP.
Bump size : 35 x 92.5 μm2 TYP.
Bump height : 17 μm TYP.

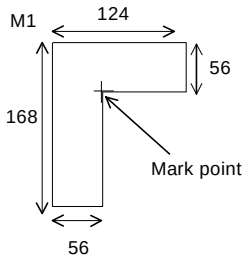
Pad type B:

Pad size(Al) : 108 x 106 μm2 TYP.
Pad size(Through hall) :78 x 60.48 μm2 TYP.
Bump size : 110 x 92.5 μm2 TYP.
Bump height : 17 μm TYP.

Alingment mark

	Alingment mark coordinate	
	X [μm]	Y [μm]
M1	-1382.00	6830.00
M2	1220.00	-6760.00

Alingment mark form (μm)



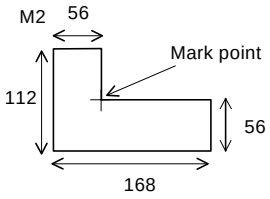


TABLE OF CONTENTS

★ 1. PIN FUNCTIONS

1.1 Power Supply System Pins

Symbol	Name	μPD16686 Pad No.	μPD16687 Pad No.	I/O	Description
V_{DD1}	Logic power supply pin	103 to 105, 111, 119, 127, 137, 173	103 to 105, 111, 119, 127, 137, 173	–	Power supply pin for logic circuit
V_{DD2}	Boost circuit power supply pin	100 to 102	100 to 102	–	Power supply pin for booster
V_{SS}	Logic and driver ground pin	35, 55, 58, 106 to 108, 114, 122, 132, 170, 176, 185	35, 55, 58, 106 to 108, 114, 122, 132, 170, 176, 185	–	Ground pin for logic and driver circuits
V_{OUT}	Driver power supply pin	56, 57	56, 57	–	Power supply pin for driver. Output pin for on-chip booster. Connect a 1 μF boost capacitor between this pin and the GND pin. If not using the on-chip booster, a direct driver power supply can be input.
V_{LCD}, V_{LC1} to V_{LC4}	Reference power supply pins for driver	54 to 45	54 to 45	–	These are reference power supply pins for the LCD driver. Connect a capacitor between these pins and the GND pin if an internal bias has been selected.
$C1^+$, $C1^-$ $C2^+$, $C2^-$ $C3^+$, $C3^-$ $C4^+$, $C4^-$ $C5^+$, $C5^-$ $C6^+$, $C6^-$ $C7^+$, $C7^-$ $C8^+$, $C8^-$ $C9^+$, $C9^-$	Boost capacitor connection pins (1)	97 to 62	97 to 62	–	These are capacitor connection pins for the booster. When using the on-chip booster, connect a 1 μF capacitor between positive (+) and negative (-) pins.
C1A	Boost capacitor connection pin (2)	98, 99	98, 99	–	This is a capacitor connection pin for boost adjustment. When using the on-chip booster, connect a 1 μF capacitor between this pin and the GND pin.

1.2 Logic System Pins

(1/2)

Symbol	Name	μPD16686 Pad No.	μPD16687 Pad No.	I/O	Description
PSX	Select data transfer	117, 118	117, 118	Input	This pin is used to select between parallel data input and serial data input. PSX = H: Parallel data input PSX = L: Serial data input
/CS1, CS2	Chip select	123, 124, 125, 126	123, 124, 125, 126	Input	These pins are used for chip select signals. When /CS1 = L (CS2 = H), the chip is active and can perform data input/output operations including command and data I/O.
/RD (E)	Read (enable)	135, 136	135, 136	Input	When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is L. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable write operations. Data is written at the falling edge of this signal.
/WR (R,/W)	Write (read/write)	133, 134	133, 134	Input	When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When 68 series parallel data transfer (R,/W) has been selected, this pin is used to determine the direction of data transfer. 0: Write 1: Read
C86	Select interface	115, 116	115, 116	Input	This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). 0: Selects i80 series CPU mode 1: Selects M68 series CPU mode
D_0 to D_5, D_6 (SCL) D_7 (SI)	Data bus (serial clock) (serial input)	153 to 138	153 to 138	I/O	These pins comprise an 8-bit bidirectional data bus that connects to an 8-bit or 16-bit standard CPU bus. When the serial interface has been selected (PSX = L), D_6 functions as a serial clock input pin (SCL) and D_7 functions as a serial data input pin (SI). In either case, pins D_0 to D_5 are in high impedance mode. When the chip is not selected, D_0 to D_7 are in high impedance mode.
RS	Index register/data, command selection	130, 131	130, 131	Input	Usually, this pin is connected to the LSB of the standard CPU address bus and is used to distinguish between data from index registers and data/commands. RS = H: Indicates that data from D_0 to D_7 is data/command RS = L: Indicates that data from D_0 to D_7 is index register contents

(2/2)

Symbol	Name	μPD16686 Pad No.	μPD16687 Pad No.	I/O	Description
/RES	Reset	128, 129	128, 129	Input	When /RES is low, an internal reset is performed. The reset operation is executed at the /RES signal level.
CLS	Select clock division	109, 110	109, 110	Input	This pin is used to select whether or not to use the divider within the display clock oscillator. CLS = H: Use divider CLS = L: Do not use divider When using an external clock, the CLS = L setting is input via the OSC_{IN1} and OSC_{IN2} pins as normal and partial clocks respectively. When CLS = H, clock input is via the OSC_{IN1} pin only.
IRS	V_{LCD} regulation	120, 121	120, 121	Input	This pin is used to select the resistor that is used for V_{LCD} voltage regulation. IRS = H: Uses internal resistor IRS = L: Does not use internal resistor. The V_{LCD} voltage level is regulated using the external voltage division resistor that is connected to the V_R pin.
SIGIN1, SIGIN2	Signature setting pins	171, 172, 174, 175	171, 172, 174, 175	Input	These pins can be used to set a unique signature for the IC. The signal set via these pins can subsequently be read from the signature read register (R45).
OSC_{IN1}	Oscillation signal pins	160, 161	160, 161	Input	A resistor can be inserted between OSC_{IN1} and OSC_{OUT}, and OSC_{IN2} and OSC_{OUT}. When using an external oscillator, a clock signal is input via the OSC_{IN} pins according to the CLS pin's status and the OSC_{OUT} pin is left unconnected. The wiring between OSC_{IN1}-OSC_{OUT} and OSC_{IN2}-OSC_{OUT} must be as short as possible, and use after proper evalluation.
OSC_{IN2}		162, 163	162, 163	Input	
OSC_{OUT}		164, 165	164, 165	Output	

1.3 Driver-Related Pins

Symbol	Name	μPD16686 Pad No.	μPD16687 Pad No.	I/O	Description
SEG_1 to SEG_{128}	Segment	425 to 298	359 to 258, 250 to 225	Output	Segment output pins
COM_1 to COM_{128}	Common	498 to 472, 465 to 429, 294 to 258, 251 to 225	363 to 464, 471 to 496	Output	Common output pins
$PSEG_1$ to $PSEG_{20}$	Static segment	15 to 34, 186 to 205	15 to 34, 186 to 205	Output	Segment output pins for static icon
$PCOM_1$	Static common	223, 224, 499, 500	223, 224, 497, 498	Output	Common output pins for static icon (Same driver waveform is output from two pins.)
V_{RS}	Op amp input	36, 37	36, 37	Input	These are op amp input pins for regulating the driving voltage of the LCD. V_{RS} is a reference voltage input for the LCD voltage regulation amplifier. When using the internal drive circuit (i.e., when OP1 = 1), we recommend inserting a 0.1 to 1 μF capacitor between this pin and GND. V_R is an input for the op amp's feedback connection. Insert this pin between GND and AMP_{OUT} when using the feedback resistor for this input. This pin is valid only when not using an internal resistor for V_{LCD} voltage regulation (i.e., when IRS = L). This pin cannot be used when using the internal resistor for V_{LCD} voltage regulation (i.e., when IRS = H).
V_R		43, 44	43, 44		
AMP_{OUT}	Op amp output	41, 42	41, 42	Output	These are op amp output pins for regulating the driving voltage of the LCD. When not using an internal resistor for V_{LCD} voltage regulation (i.e., when IRS = L), these outputs are connected to the LCD drive voltage regulation resistor (see **3.6.3 Voltage regulator**). NEC recommends inserting a 0.1 to 1 μF capacitor between these pins in order to stabilize the internal op amp's output.
AMP_{OUTP}		39, 40	39, 40		
DUMMY	Dummy pin	1 to 14, 38, 59 to 61, 206 to 222, 252 to 257, 295 to 297, 426 to 428, 466 to 471, 501, 502,	1 to 14, 38, 59 to 61, 206 to 222, 251 to 257, 360 to 362, 465 to 470, 499, 500	–	Dummy pin These pins are not connected inside IC. Usually, leave these pins open.

1. 4 Test Pins

Symbol	Name	μPD16686 Pad No.	μPD16686 Pad No.	I/O	Description
$TEST_{OUT}$	Test output	177, 178	177, 178	Output	These pins are used when the IC is in test mode.
TFR	Test output	156, 157	156, 157	Output	Usually, leave them open.
TFR_{SYNC}	Test output	154, 155	154, 155	Output	
TDOF	Test output	158, 159	158, 159	Output	
TSI_{SYNC}	Test output	168, 169	168, 169	Output	
TM,S	Test input	112, 113	112, 113	Input	This pin is used when the IC is in test mode. Usually, connect to V_{DD1}.
$TOSC_{SYNC}$	Test output	166, 167	166, 167	Output	This test output pin is used when the IC is in test mode. Usually, leave it open.
TSTIFS TSTRTST TSTVIHL	Test input	179, 180, 181, 182, 183, 184	179, 180, 181, 182, 183, 184	Input	These pins are used to set a test mode for the IC. Normally, connect these pins to V_{SS}.

2. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit type of each pin and recommended connection of unused pins are described below.

Pin Name	Input Type	I/O	Recommended Connection of Unused Pins	Notes
PSX	Schmitt trigger	Input	Mode setting pin	**Note 1**
/CS1	Filter	Input	Connect to V_{SS}	–
CS2	Filter	Input	Connect to V_{DD1}	**–**
/RD(E)	Filter	Input	Connect to V_{DD1} (i80 series interface), connect to V_{DD1} or V_{SS} (serial interface)	**–**
/WR(R,/W)	Filter	Input	Connect to V_{DD1} or V_{SS} (serial interface)	–
C86	Schmitt trigger	Input	Mode setting pin	**Note 1**
D_0 to D_5	Filter	I/O	Leave open	**–**
D_6(SCL)	Filter	I/O	**–**	**–**
D_7(SI)	Filter	I/O	**–**	**–**
RS	Filter	Input	Register setting pin	**Note 2**
$TEST_{OUT}$	–	Output	Leave open	–
/RES	Schmitt trigger	Input	Connect to V_{DD1}	**–**
CLS	Schmitt trigger	Input	Mode setting pin	**Note 1**
IRS	Schmitt trigger	Input	Mode setting pin	**Note 1**
SIGIN1	Schmitt trigger	Input	Connect to V_{DD1} or V_{SS}	**–**
SIGIN2	Schmitt trigger	Input	Connect to V_{DD1} or V_{SS}	**–**
OSC_{IN1}	CMOS	Input	–	–
OSC_{IN2}	CMOS	Input	Connect to V_{DD1} or V_{SS} (CLS = H)	**–**
OSC_{OUT}	**–**	Output	Leave open (when using external clock)	**–**
★ TFR	CMOS	Output	Leave open	–
★ TFR_{SYNC}	CMOS	Output	Leave open	**–**
★ TDOF	CMOS	Output	Leave open	–
★ TSI_{SYNC}	CMOS	Output	Leave open	–
★ TM,S	Schmitt trigger	Input	Connect to V_{DD1}	**–**
★ $TOSC_{SYNC}$	**–**	Output	Leave open	**–**
TSTIFS	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	–
TSTRTST	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	**–**
TSTVIHL	Schmitt trigger	Input	Connect to V_{SS} (during normal use)	**–**

Notes 1. Connect to either V_{DD1} or V_{SS}, depending on the mode setting.

2. Input either V_{DD1} or V_{SS} output from CPU, depending on the mode setting.

3. DESCRIPTION OF FUNCTIONS

3.1 CPU Interface

3.1.1 Selection of interface type

The μPD16686, 16687 chips transfer data using an 8-bit bidirectional data bus (D_7 to D_0) or a serial data input (SI). Setting the polarity of the PSX pin as either H (high) or L (low) selects between 8-bit parallel or serial data input, as shown in the following table.

PSX	CS	RS	/RD	/WR	C86	D_7	D_6	D_5 to D_0
H: Parallel input	CS	RS	/RD	/WR	C86	D_7	D_6	D_5 to D_0
L: Serial input	CS	RS	**Note1**	**Note1**	**Note1**	SI	SCL	Hi-Z**Note2**

Notes 1. Fixed as either H or L

2. Hi-Z: High impedance

3.1.2 Parallel interface

When the parallel interface has been selected (PSX = H), setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see table below).

C86	CS	RS	/RD	/WR	D_7 to D_0
H: M68 series CPU	CS	RS	E	R,/W	D_7 to D_0
L: i80 series CPU	CS	RS	/RD	/WR	D_7 to D_0

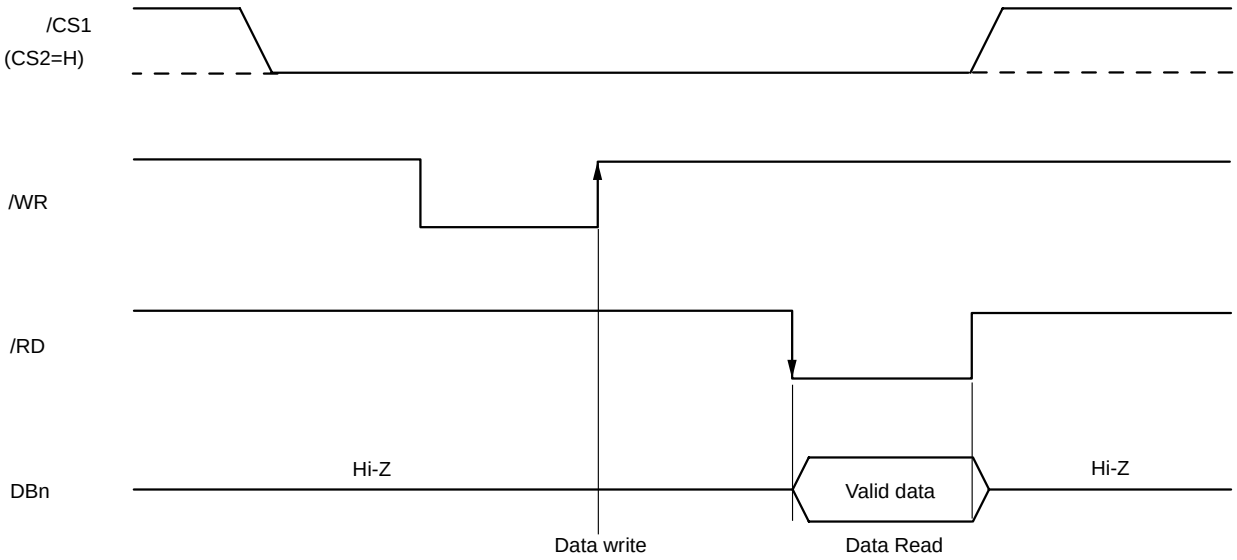
The data bus signal is identified according to the combination of the RS, /RD(E), and /WR(R,/W) signals, as shown in the following table.

Common	M68	i80		Function
RS	R,/W	/RD	/WR	
1	1	0	1	Reads display data and registers
1	0	1	0	Writes display data and registers
0	1	0	1	Prohibited
0	0	1	0	Writes to control index register

(1) i80 series parallel interface

When i80 series parallel data transfer has been selected, data is written to the μPD16686, 16687 at the rising edge of the /WR signal. The data is output to the data bus when the /RD signal is L.

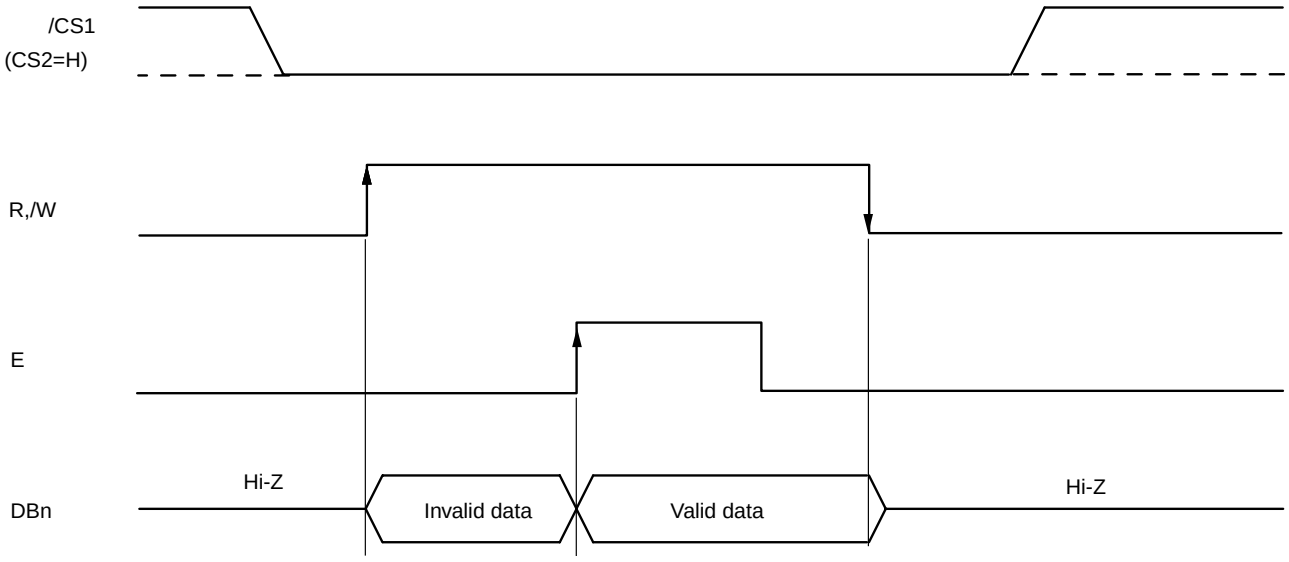
Figure 3-1. i80 Series Interface Data Bus Status



(2) M68 series parallel interface

When M68 series parallel data transfer has been selected, data is written at the falling edge of the E signal when the R,/W signal is L. During the data read operation, the data bus enters the output status when the R,/W signal is H, outputs valid data at the rising edge of the E signal, and enters the high-impedance state at the falling edge of the R,/W signal (R,/W = L)

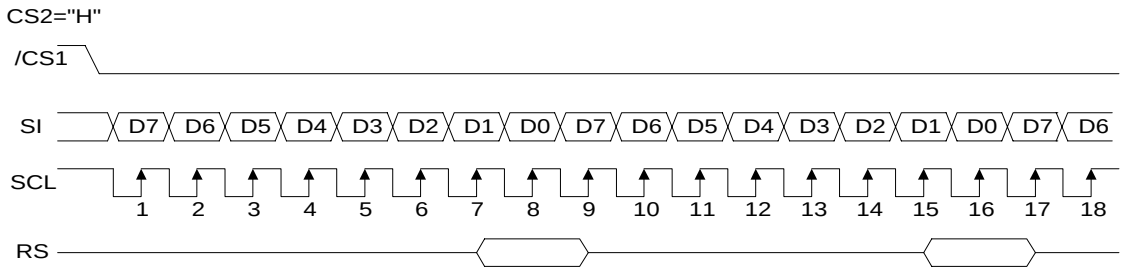
Figure 3-2. M68 Series Interface Data Bus Status



3.1.3 Serial interface

When the serial interface has been selected (PSX = L), if the chip is active (/CS1 = L, CS2 = H), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read from D_7 and then from D_6 to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing. RS input is used to judge serial input data as display data or command data: when RS = H the data is display/command data and when RS = L the data is index data. When the chip enters active mode, RS input is read at the rising edge after every eighth serial clock and is then used to judge the serial input data. The serial interface signal chart is shown below.

Figure 3-3. Serial Interface Signal Chart



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. NEC recommends checking operation with the actual device.

3.1.4 Chip select

The μPD16686, 16687 have two chip select pins (/CS1 and CS2). The CPU parallel interface or serial interface can be used only when /CS1 = L and CS2 = H. When chip select is inactive, D_0 to D_7 are set to high impedance (invalid) and input of RS, /RD, or /WR is not active. If serial interface mode has been set, the shift register and counter are both reset.

3.1.5 Display data RAM and on-chip register access

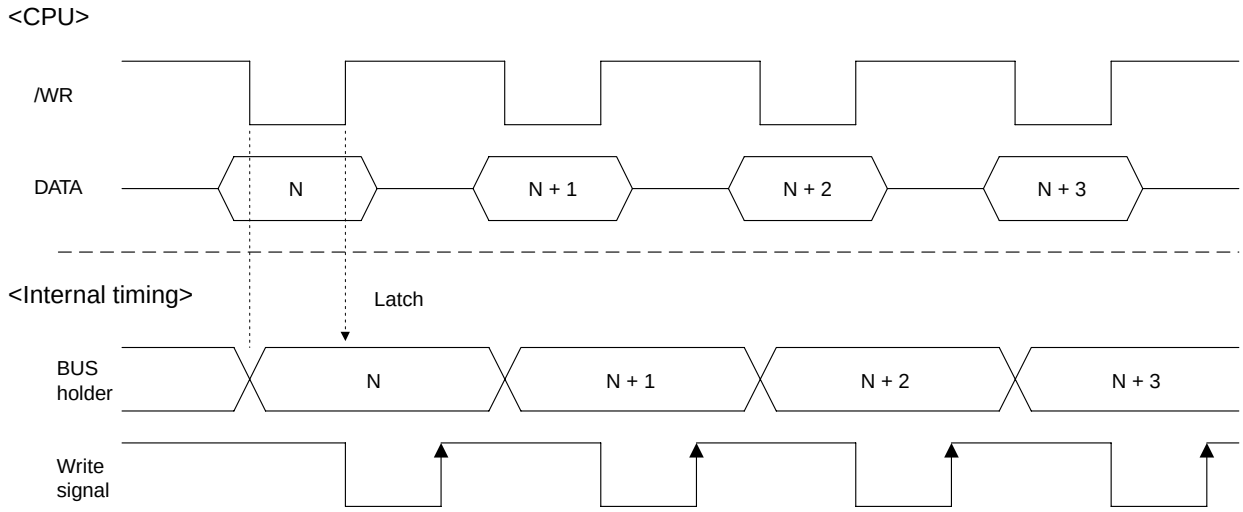
Because only the required cycle time (t_{cyc}) is saisfied when accessing the μPD16686, 16687 from the CPU, high-speed data transfer is possible. There is no need to consider any wait time. No dummy data is needed when writing data. Even when data is read, there is no need for dummy data except in the display memory access register (R11).

In other words, dummy data is required only when reading data from the display memory access register (R11).

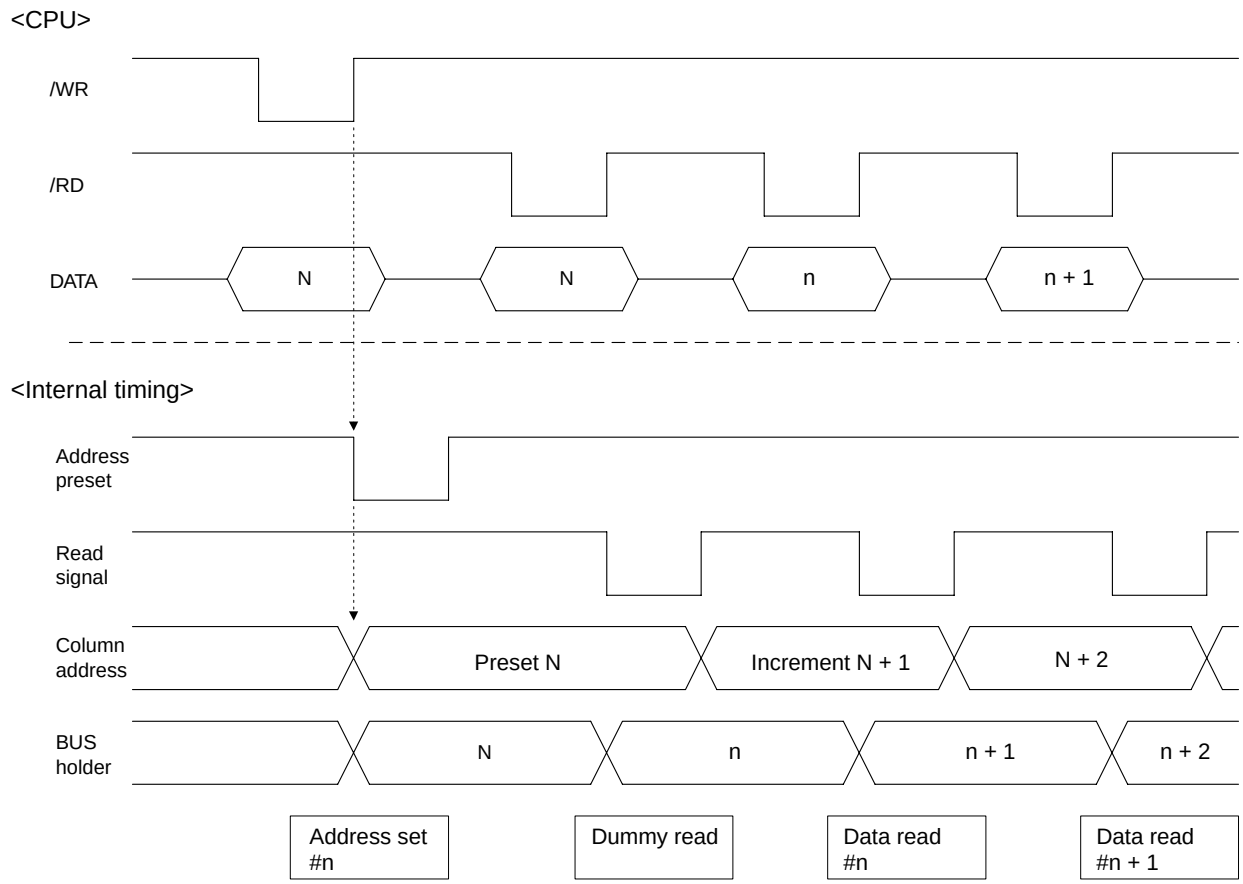
Figure 3-4 illustrates this relationship.

Figure 3-4. Write and Read (1/2)

Write

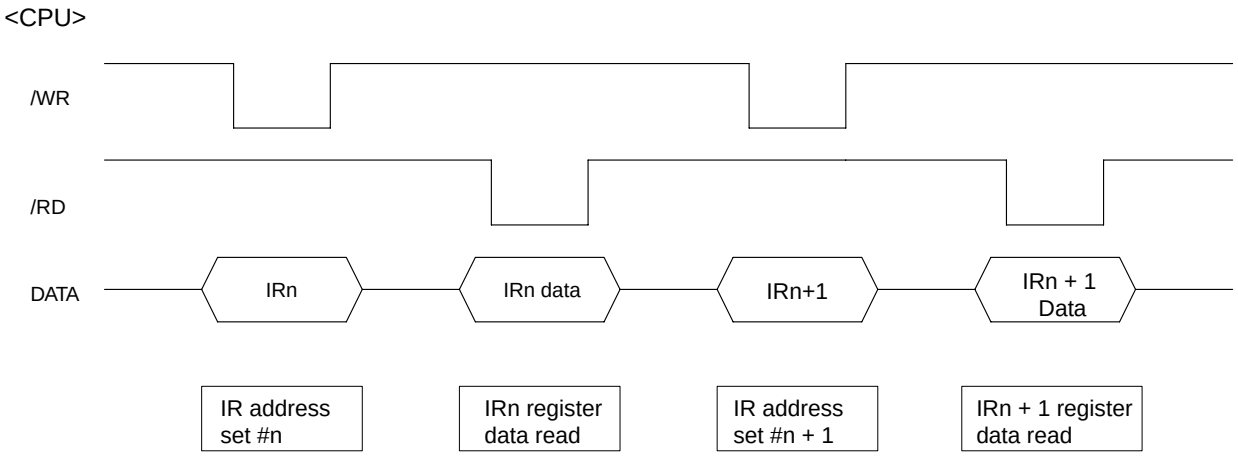


Read (display memory access register)



★ **Figure 3-4. Write and Read (2/2)**

Read (other than display memory access register)



3.2 Display Data RAM

3.2.1 Display data RAM

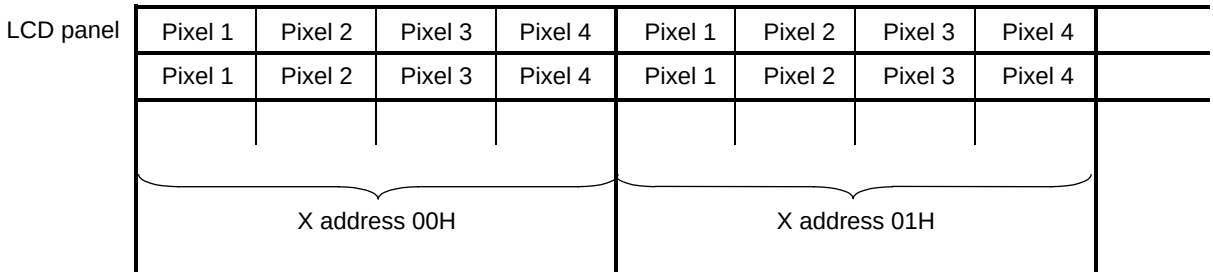
This is the RAM that is used to store the display's dot data. The RAM configuration is 256 bits (32 x 8 bits) x 128 bits. Any specified bit can be accessed by selecting the corresponding X address and Y address. In the data sent from the CPU, D_0 to D_7 corresponds to SEGx on the LCD display (see Figure 3-5).

The CPU writes data to and reads data from the display RAM via the I/O buffer, and these read/write operations are independent of the signal read operations for the LCD driver. Accordingly, there are no adverse effects (such as flicker) in the LCD display when display data RAM is accessed asynchronously.

Figure 3-5. Display Data RAM

MSB LSB

D_7 D_6	D_5 D_4	D_3 D_2	D_1 D_0
Pixel 1	Pixel 2	Pixel 3	Pixel 4



D_7	D_6	D_5	D_4			
0	1	1	1		0	0
1	0	0	0		0	0
0	0	0	0		0	0
0	1	1	1		0	0
1	0	0	0		0	0

Display data

LCD display

3.2.2 X address circuit

As shown in Figure 3-6, the display data RAM's X address is specified via the X address register (R3). When using X address increment mode (INC = 0: control register 2 (R1)), the specified X address is incremented (by 1) each time a display data read or write operation is executed. The CPU is able to continuously access the display data. The X address is incremented to 1FH, after which the Y address is incremented after each read or write operation and the X address is set back to 00H.

For monochrome (black-and-white) display, the X address is incremented to 0FH, after which the Y address is incremented after each read or write operation and the X address is set back to 00H.

3.2.3 Column address circuit

When displaying the contents of the display data RAM, the column address corresponds to the SEG output, as shown in Figure 3-6. Similarly, the static icon address corresponds to the PSEG output.

As is shown in Tables 3-1 and 3-2, the correspondence between the display RAM's column address and segment output can be inverted using the ADC flag in control register 1 (R0) (segment driver direction selection flag). This reduces the constraints on chip layout when assembling the LCD module.

★ **Table 3-1. Relationship Between Column Address and SEG Output**

SEG Output		SEG_1				SEG_{128}
ADC (D_1)	0	00H	→	Column address	→	7FH
	1	7FH	←	Column address	←	00H

★ **Table 3-2. Relationship Between Column Address for Static Icon and PSEG Output**

PSEG Output		$PSEG_1$				$PSEG_{20}$
ADC (D_1)	0	00H	→	Column address	→	04H
	1	04H	←	Column address	←	00H

3.2.4 Y address circuit

As is shown in Figure 3-6, the Y address register (R4) is used to specify the display data RAM's Y address. When using Y address increment mode (INC = 1: control register 2 (R1)), the specified Y address is incremented (by 1) each time a display data read or write operation is executed. The CPU is able to continuously access the display data. The Y address is incremented to 7FH, after which the X address is incremented after each read or write operation and the Y address is set back to 00H.

3.2.5 Common scan circuit

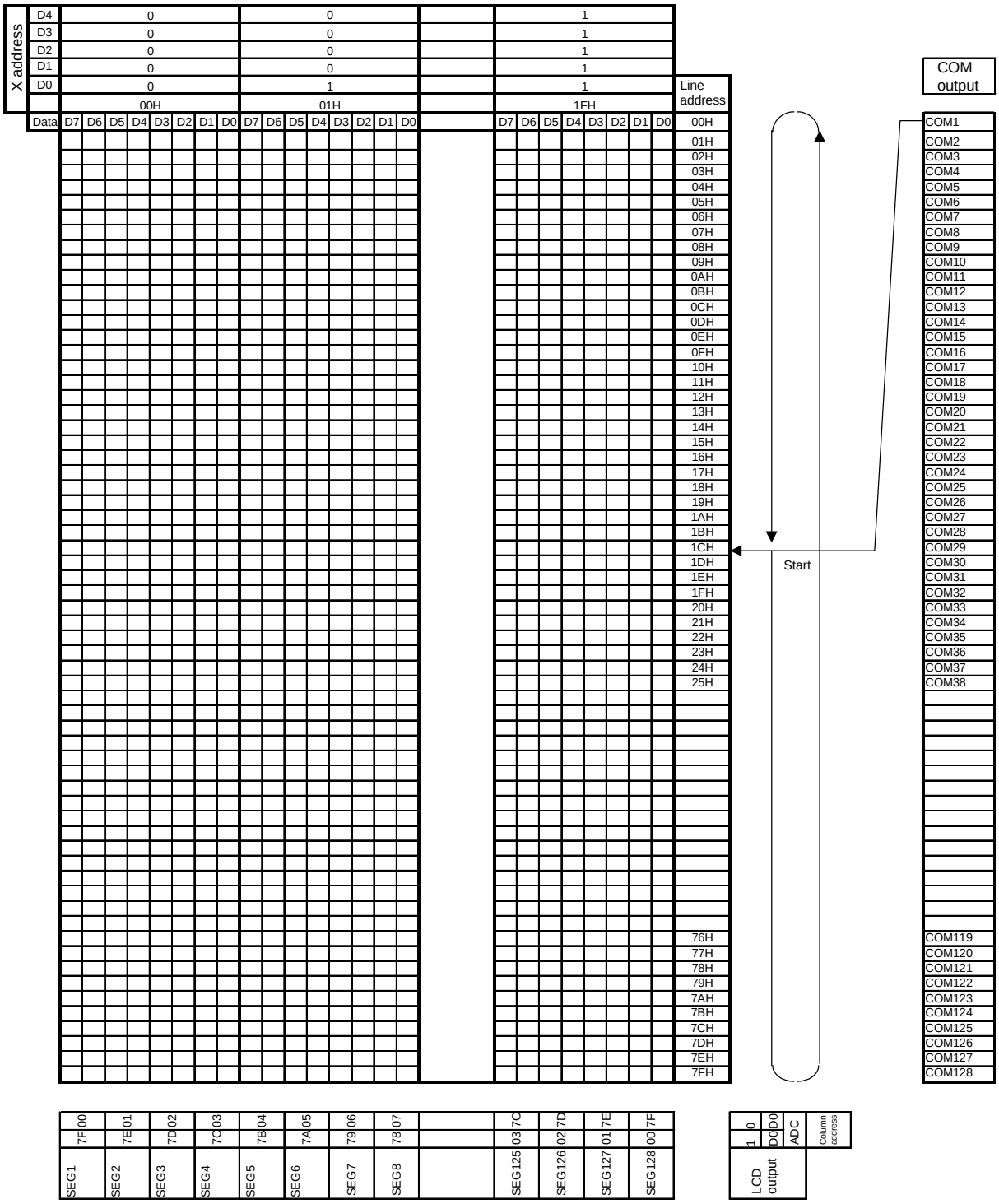
The common scan circuit sets the scan lines for common signals. The scan direction is set using the COMR flag in control register 1 (R0), as shown in Table 3-3.

For example, when using 1/80 duty, when COMR = L the scan direction is $COM_1 \rightarrow COM_{80}$ and when COMR = H, the scan direction is $COM_{80} \rightarrow COM_1$ using the COM_{80} to COM_1 pins.

★ **Table 3-3. Relationship Between Common Scan Circuit and Scan Direction**

COMR (D_0)	0	COM_1	→	COM_{128}
	1	COM_{128}	←	COM_1

Figure 3-6. Configuration of X Address Register



3.2.6 Display start line set

As is shown in Figure 3-6, display start line set specifies the Y address that corresponds to the COM_1 output for displaying the contents of display data RAM. The display start line set (R12) is used to specify the top line in the display. The screen can be scrolled, overwritten, etc. A 7-bit display start address is set to the display start line register.

3.2.7 Display data latch circuit

The display data latch circuit is used for temporary storage of data that is output to the LCD driver from the display data RAM.

The display scan command that sets normal or reverse display mode and the display ON/OFF command control latched data so that there is no effect on the data in the display data RAM.

3.3 Blink/Reverse Display Circuit

The μPD16686, 16687 enable blinking display and reverse display in designated parts of the full dot display. A blinking display is achieved by cycling ON/OFF (level 0 when four-level gray scale mode has been selected) at approximately 1 Hz and reverse display is achieved by inverting the display level value.

The area designated for blinking is specified via the blink start/end line address registers (R14 and R15), the blink X address register (R13), and the blink data memory (R16).

First, the blinking display's start and end line addresses are selected via the blink start/end line address registers. Next, the blink X address register (R13) and the blink data memory (R16) are used to select the column for the blinking display.

The inversion start/end line address registers (R18 and R19), the inverted X address register (R17), and inverted data memory (R20) are used to select the reverse display area.

First, the inversion start/end line address registers (R18 and R19) are set to select the line addresses where the reverse display will start and end. Next, the inverted X address register (R17) and the inverted data memory (R20) are used to select the column for the reverse display. The specified blink/inverted X address is incremented (by 1) with each input of blink/reverse display data.

The blink RAM and inversion RAM, which have a 128 bit (16 x 8 bit) configuration, are used to store data for blinking display and reverse display respectively. To access the desired bit, simply specify the corresponding X address. The blink/reverse data (data bits D_0 to D_7 sent from the CPU) correspond to SEGx on the LCD display, as shown in Figure 3-7.

After the area and data settings are complete, the BLD bit and IVD bit in the control register 1 (R0) are set to H, at which point the blinking and/or reverse display of data begins. Figure 3-8 illustrates the relationship between the start line address, end line address, blink/reverse data, and LCD display.

Table 3-4. Inversion Manipulation and Display

Original Level	After Inversion
Four-level gray scale display mode	
0, 0	1, 1
0, 1	1, 0
1, 0	0, 1
1, 1	0, 0
B/W display mode	
1	0
0	1

Figure 3-7. Correspomdence Between Blink/Reverse Data and Segments

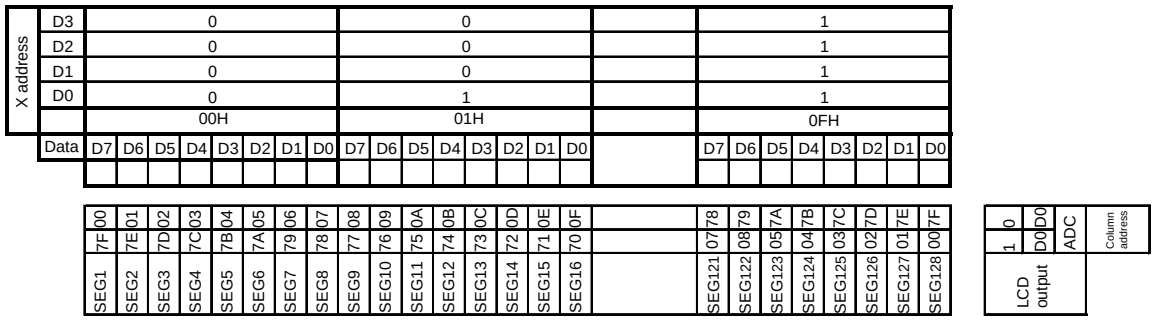
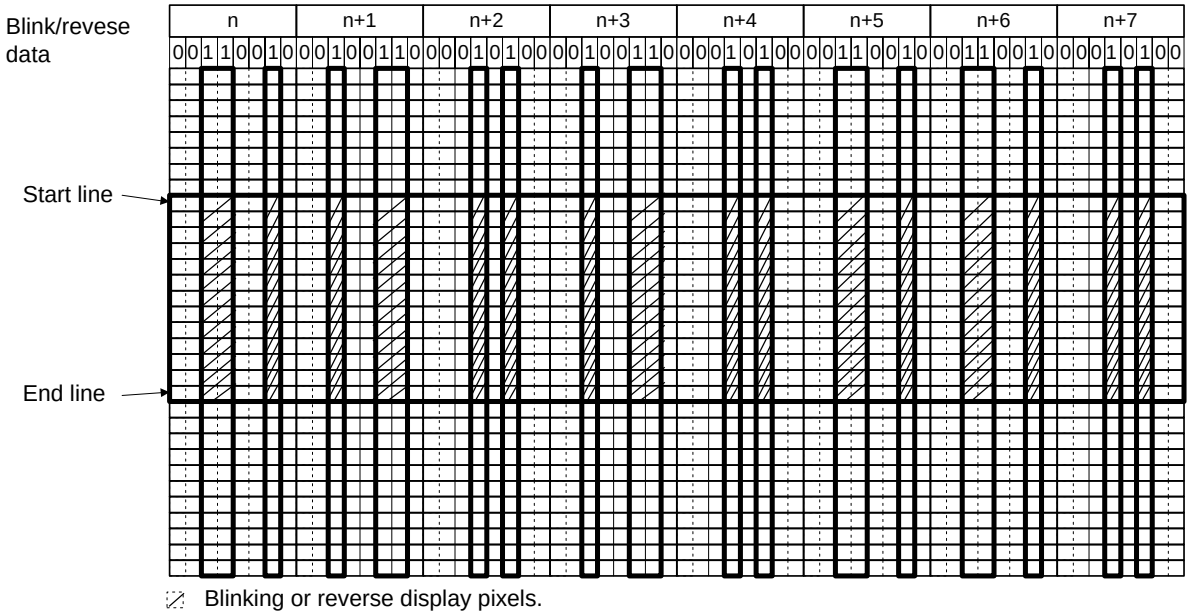
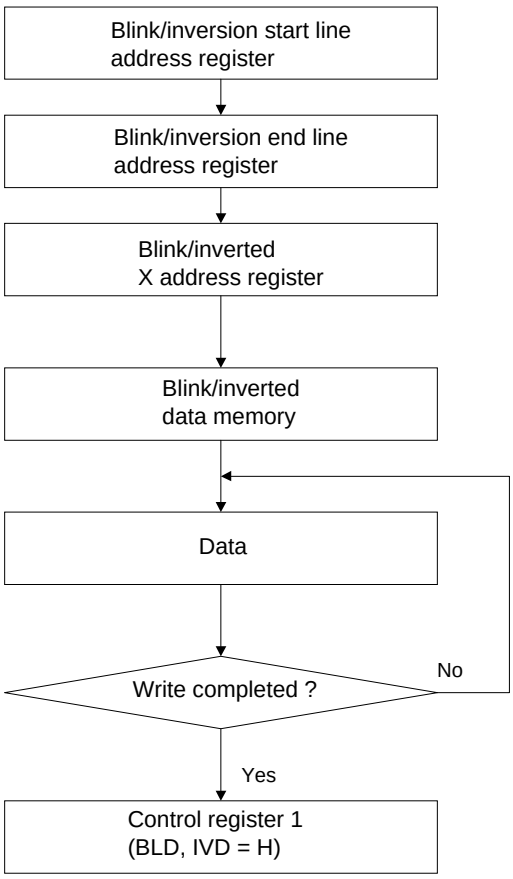


Figure 3-8. Setting Image of Blink/Reverse Display Area



Example of sequence for setting blink/reverse display



3.4 Oscillator

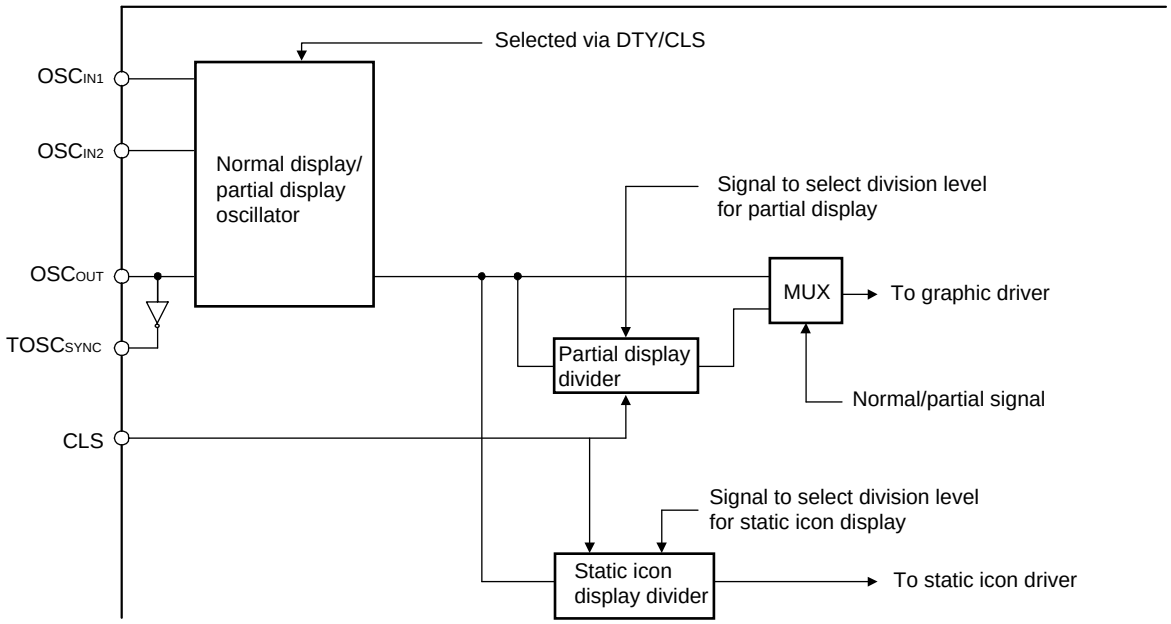
The μPD16686, 16687 include a CR-type oscillator (R external) for normal and partial display, which generates the display clocks.

The clocks from this oscillator are controlled via the CLS pin and the DTY flag in the control register 2 (R1). The clock configuration for the display can be set to suit the target system.

The functions of this circuit are described below.

- The oscillator for normal and partial display is enabled only when resistors RN and RP have been connected. The DTY flag in the control register 2 (R1) and the CLS pin status are used to switch between the oscillation clocks for normal display and partial display modes.
- The divider divides the external clock that has been input for the normal oscillator and the normal display into a clock for partial display. The external clock that is input for the partial oscillator and partial display is also divided for the partial display.
- The division level is automatically set for the divider based on the relationship between the ON/OFF status of the divider setting pin (CLS pin) and the duty of the specified partial display, as shown in Table 3-5.

Figure 3-9. Oscillator Block



The relationship between the frame frequency (f_{FRAME}), oscillation frequency (f_{OSCIN1}), and setting duty (in normal display mode) is described below.

$f_{FRAME} = f_{OSCIN1} \div 8 \div N$ (in four-level gray scale display mode)

$f_{FRAME} = f_{OSCIN1} \div 4 \div N$ (in B/W display mode)

N = 1/N duty (setting duty)

Table 3-5. Setting of Division Level for Partial Display and Static Icon Display (1/2)

In four-level gray scale display mode (GRAY = L, control register 2 (R1))

Display Mode	Normal Display Duty Ratio	Partial Display Duty Ratio	Division Source OSC_{IN1} /OSC_{IN2}	Divider ON/OFF CLS	Normal/Partial Select DTY	Partial Division Ratio	Static Icon Division Ratio	Comments	
Four-level gray scale GRAY = L	1/1 to 1/80	1/38	OSC_{IN1}	L(OFF)	L (Normal)	-	1/12	Static icon frame frequency: f_{OSCIN1} /12(division ratio) /32	
		1/25							
		1/12							
		1/38		H(ON)					
		1/25							
		1/12							
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/4	Partial frame frequency: f_{OSCIN2} /8 /38	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /8 /25	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/12	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38	Static icon frame frequency: f_{OSCIN1} /12(division ratio) /32
		1/25				1/2		Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /25	Static icon frame frequency: f_{OSCIN1} /12(division ratio) /32
		1/12				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN1} /12(division ratio) /32
	1/81 to 1/96	1/38	OSC_{IN1}	L(OFF)	L (Normal)	-	1/16	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32	
		1/25							
		1/12							
		1/38		H(ON)					
		1/25							
		1/12							
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/4	Partial frame frequency: f_{OSCIN2} /8 /38	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /8 /25	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/16	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /25	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
	1/97 to 1/112	1/38	OSC_{IN1}	L(OFF)	L (Normal)	-	1/16	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32	
		1/25							
		1/12							
		1/38		H(ON)					
		1/25							
		1/12							
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/4	Partial frame frequency: f_{OSCIN2} /8 /38	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /8 /25	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/16	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /25	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN1} /16(division ratio) /32
	1/113 to 1/128	1/38	OSCIN1	L(OFF)	L (Normal)	-	1/20	Static icon frame frequency: f_{OSCIN1} /20(division ratio) /32	
		1/25							
		1/12							
		1/38		H(ON)					
		1/25							
		1/12							
		1/38	OSCIN2	L(OFF)	H (Partial)	1/1	1/4	Partial frame frequency: f_{OSCIN2} /8 /38	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /8 /25	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN2} /4(division ratio) /32
		1/38	OSCIN1	H(ON)		1/2	1/20	Partial frame frequency: f_{OSCIN1} /2(division ratio) /8 /38	Static icon frame frequency: f_{OSCIN1} /20(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /8 /25	Static icon frame frequency: f_{OSCIN1} /20(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /8 /12	Static icon frame frequency: f_{OSCIN1} /20(division ratio) /32

Table 3-5. Setting of Division Level for Partial Display and Static Icon Display (2/2)

In black/white display mode (GRAY = H, control register 2 (R1))

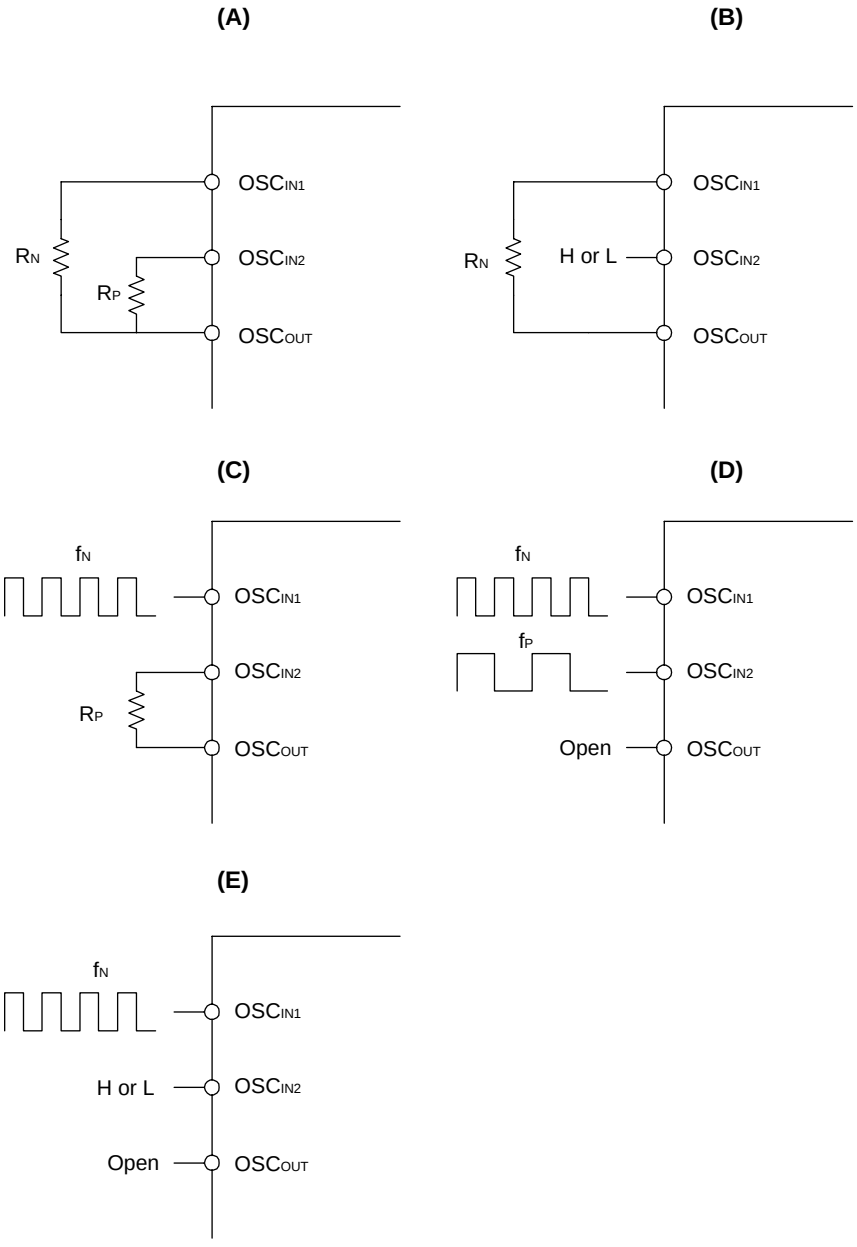
Display Mode	Normal Display Duty Ratio	Partial Display Duty Ratio	Division Source OSC_{IN1} /OSC_{IN2}	Divider ON/OFF CLS	Normal/Partial Select DTY	Partial Division Ratio	Static Icon Division Ratio	Comments
B/W GRAY = H	1/1 to 1/80	1/38	OSC_{IN1}	L(OFF)	L (Normal)	-	1/6	Static icon frame frequency: f_{OSCIN1} /6(division ratio) /32
		1/25						
		1/12						
		1/38		H(ON)				
		1/25						
		1/12						
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/2	Partial frame frequency: f_{OSCIN2} /4 /38 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /4 /25 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/6	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38 ¦ Static icon frame frequency: f_{OSCIN1} /6(division ratio) /32
		1/25				1/2		Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /25 ¦ Static icon frame frequency: f_{OSCIN1} /6(division ratio) /32
		1/12				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN1} /6(division ratio) /32
	1/81 to 1/96	1/38	OSCIN1	L(OFF)	L (Normal)	-	1/8	Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/25						
		1/12						
		1/38		H(ON)				
		1/25						
		1/12						
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/2	Partial frame frequency: f_{OSCIN2} /4 /38 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /4 /25 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/8	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /25 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
	1/97 to 1/112	1/38	OSCIN1	L(OFF)	L (Normal)	-	1/8	Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/25						
		1/12						
		1/38		H(ON)				
		1/25						
		1/12						
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/2	Partial frame frequency: f_{OSCIN2} /4 /38 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /4 /25 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/8	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /25 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN1} /8(division ratio) /32
	1/113 to 1/128	1/38	OSCIN1	L(OFF)	L (Normal)	-	1/10	Static icon frame frequency: f_{OSCIN1} /10(division ratio) /32
		1/25						
		1/12						
		1/38		H(ON)				
		1/25						
		1/12						
		1/38	OSC_{IN2}	L(OFF)	H (Partial)	1/1	1/2	Partial frame frequency: f_{OSCIN2} /4 /38 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/25				1/1		Partial frame frequency: f_{OSCIN2} /4 /25 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/12				1/2		Partial frame frequency: f_{OSCIN2} /2(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN2} /2(division ratio) /32
		1/38	OSC_{IN1}	H(ON)		1/2	1/10	Partial frame frequency: f_{OSCIN1} /2(division ratio) /4 /38 ¦ Static icon frame frequency: f_{OSCIN1} /10(division ratio) /32
		1/25				1/4		Partial frame frequency: f_{OSCIN1} /4(division ratio) /4 /25 ¦ Static icon frame frequency: f_{OSCIN1} /10(division ratio) /32
		1/12				1/8		Partial frame frequency: f_{OSCIN1} /8(division ratio) /4 /12 ¦ Static icon frame frequency: f_{OSCIN1} /10(division ratio) /32

Table 3-6 shows the relationship between the CLS pin, resistors RN and RP, and the display clock circuit.

Table 3-6. Relationship Between CLS Pin/Resistors and Display Clock Circuit.

RN Connection	RP Connection	CLS	Clock for Normal Display	Clock for Partial Display	Use Example (Figure 3-10)
Connected	Connected	L	Internal oscillator	Internal oscillator	A
Connected	Not connected	H	Internal oscillator	Divided from oscillator clock	B
Not connected	Connected	L	External clock	Internal oscillator	C
Not connected	Not connected	L	External clock	External clock	D
Not connected	Not connected	H	External clock	Divided from external clock	E

Figure 3-10. Clock Use Examples



3.5 Display Timing Generator

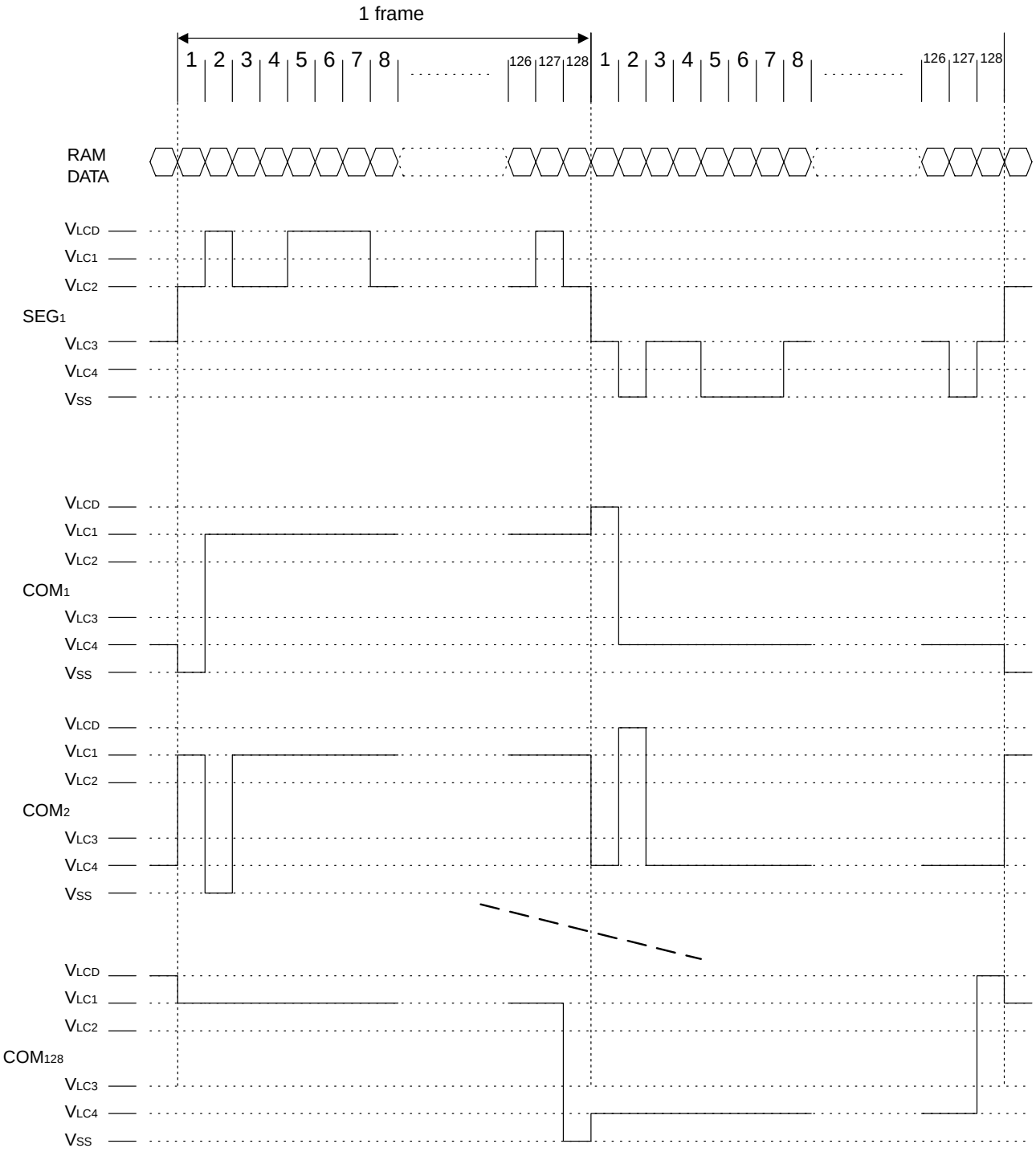
The display timing generator generates timing signals from the display clock to the line address circuit and the display data latch circuit.

Display data is latched into the display data latch circuit in synch with the display clock and is output via segment driver output pins.

Reading of the display data is completely independent of the CPU's accessing of the display data RAM. Consequently, there are no adverse effects (such as flicker) on the LCD panel even when the display data RAM is accessed asynchronously in relation to the LCD contents.

The internal common timing is generated from the display clock. As shown in Figure 3-11, a driver waveform based on the frame AC drive method is generated for the LCD driver.

Figure 3-11. Driver Waveform Based on Frame AC Drive Method



3.6 Power Supply Circuit

3.6.1 Power supply circuit

The power supply circuit supplies the voltage needed to drive the LCD. It includes a booster, voltage regulator, and voltage follower.

In the power supply circuit, the power system control 1 (R32) is used to control the ON/OFF status of the power supply circuit's booster, voltage regulator (also called V regulator), and voltage follower (V/F). This makes it possible to jointly use an external power supply together with certain functions of the on-chip power supply. Table 3-7 shows the function that controls the 3-bit data in the power system control 1 (R32) and Table 3-7 shows a reference chart of combinations.

Table 3-7. Control Values of Bits in Power System Control 1

Item		Status 1	Status 0
OP2	Booster control bit	ON	OFF
OP1	Voltage regulator (V regulator) control bit	ON	OFF
OP0	Voltage follower (V/F) control bit	ON	OFF

Table 3-8. Reference Chart of Combinations

Use Status	OP2	OP1	OP0	Booster	V Regulator	V/F	External Power Supply Input	Boost-Related System Pins
<1> Use on-chip power supply	1	1	1	enable	enable	enable	V_{DD2}	Used
<2> Use V regulator and V/F only	0	1	1	disable	enable	enable	V_{OUT}	Not connected
<3> Use V/F only	0	0	1	disable	disable	enable	V_{OUT}, AMP_{OUT}	Not connected
<4> Use external power supply only	0	0	0	disable	disable	disable	V_{OUT}, V_{LCD} to V_{LC4}	Not connected

Caution The boost-related system pins are indicated as pins $C1^+$, $C1^-$ to $C9^+$, $C9^-$, and C1A.

3.6.2 Booster

A booster that boosts the LCD driving voltage by 2 to 9 times is incorporated in the power supply circuit.
Since the booster uses signals from the on-chip oscillator, either the oscillator must be operating or a display clock must be input from an external source.

The booster uses pins $C1^+$, $C1^-$ to $C9^+$, $C9^-$ for normal boost and pins C1A and V_{DD2} for boost regulation. The wire impedance should be kept as low as possible. The number of boost levels is set using the FBS2, FBS1, and FBS0 flags in power system control 3 (R34), as shown in Table 3-9.

Caution If a capacitor is connected to a boost-related system pin that is not for one of these set boost levels, current consumption may increase. Therefore, do not connect any capacitors beyond the number of set boost levels. This also applies for the CA1 pin, used to regulate the boost levels.

Figure 3-12 describes the connection method for boost levels and capacitors.

The partial booster is settings are made using the BST1 and BST0 flags in the power system control 3 (R34), as shown in Table 3-10.

Figure 3-12. Connection Method for Boost Levels and Capacitors

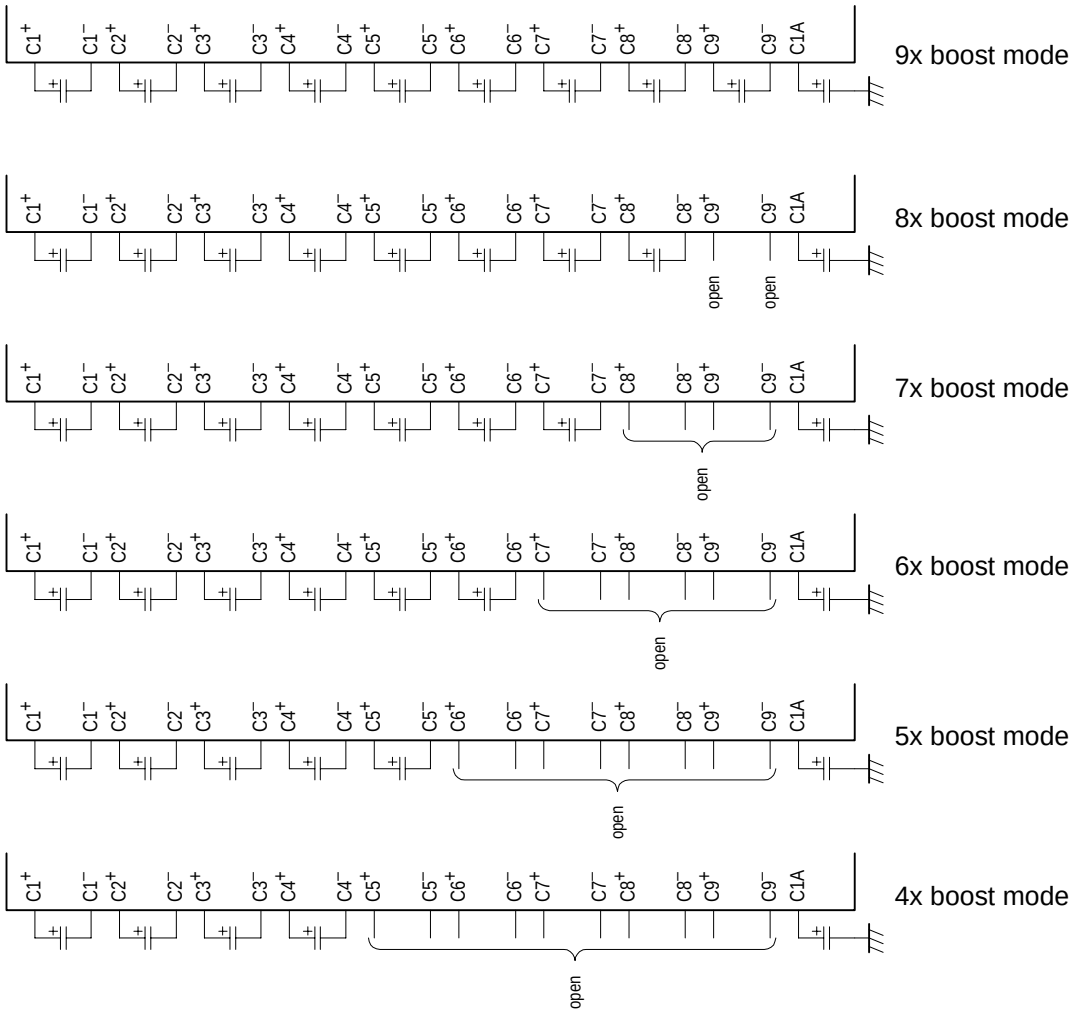


Table 3-9. Boost Level Settings for Normal Display's Booster

FBS2	FBS1	FBS0	Boost Level
0	0	0	4x
0	0	1	5x
0	1	0	6x
0	1	1	7x
1	0	0	8x
1	0	1	9x
1	1	0	Prohibited
1	1	1	Prohibited

Table 3-10. Boost Level Settings for Partial Display's Booster

BST1	BST0	Boost Level
0	0	2x
0	1	3x
1	0	4x
1	1	Prohibited

3.6.3 Voltage regulator

The boost voltage from V_{OUT} is supplied to the voltage regulator and output as the LCD drive voltage V_{LCD}.

Since the μPD16686, 16687 has a 256-step electronic volume function and an on-chip resistor for V_{LCD} voltage regulation, a small number of components can be used to configure a highly accurate voltage regulator.

(1) When using an on-chip resistor for V_{LCD} voltage regulation

The on-chip resistor for V_{LCD} voltage regulation and the electronic volume function can be used to regulate the contrast of the LCD contents by controlling the LCD drive voltage V_{LCD} using commands only. In such cases, no external resistor is needed.

If $V_{LCD} < V_{OUT}$, then the value for V_{LCD} can be determined from the following equation.

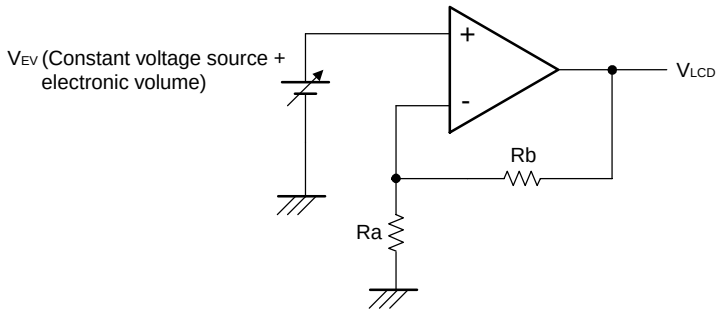
Example Equation $V_{LCD} < V_{OUT}$

$$V_{LCD} = (1 + \frac{Rb}{Ra})\, V_{EV}$$

$$V_{LCD} = (1 + \frac{Rb}{Ra})\,(1 - \frac{\alpha}{384})\, V_{REG}$$

Remark $V_{EV} = (1 - \frac{\alpha}{384})\, V_{REG}$

Figure 3-13. When Using On-Chip Resistor for V_{LCD} Voltage Regulation



V_{REG} is the IC's on-chip constant voltage source, for which three types of temperature characteristic curves are available. These temperature characteristic curves can be adjusted via settings in the power system control 1 (R32) (TSC1, TCS0), as shown in Table 3-11.

Table 3-11 shows the V_{REG} voltage when T_A = 25°C.

Table 3-11. V_{REG} Voltage When T_A = 25°C

Status	TCS1	TCS0	Temperature Curve	Unit	V_{REG} (TYP.)	Unit
Internal power supply	0	0	–0.09	%, °C	0.88	V
	0	1	–0.11		0.80	
	1	0	–0.12		0.75	
	1	1	External inputs		–	

α is the electronic volume register (R35) value. Any of 256 statuses can be set as the fetched status for α corresponding to the data set to the 8-bit electronic control register. α values based on settings in the electronic volume register (R35: normal display mode) and partial electronic volume register (R36: partial display mode) are listed in Table 3-12 on the next page.

Table 3-12. α Values Based on Settings in Electronic Volume Register

Register								α
EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0	
0	0	0	0	0	0	0	0	384
0	0	0	0	0	0	0	1	254
0	0	0	0	0	0	1	0	253
0	0	0	0	0	0	1	1	252
				:				:
1	1	1	1	1	1	0	1	2
1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	0

Rb/Ra is an on-chip resistance factor used for the V_{LCD} voltage regulator. This factor can be controlled at eight levels based on settings in power control 2 (R33) ([VRR2, VRR1, VRR0]: normal display mode and [PVR2, PVR1, PVR0]: partial display mode). Reference voltage values (1 + Rb/Ra) are determined based on 4-bit data set to V_{LCD}'s on-chip resistance factor register, as shown in Table 3-13.

Table 3-13. Determination of Reference Voltage Values Based on Settings in On-Chip Resistance Factor Register

Register			1+Rb/Ra
VRR2	VRR1	VRR0	
PVR2	PVR1	PVR0	
0	0	0	5
0	0	1	8
0	1	0	12
0	1	1	13
1	0	0	16
1	0	1	19
1	1	0	21
1	1	1	24

(2) When using an external resistor (instead of using the on-chip resistor for V_{LCD} voltage regulation)

Instead of using only the on-chip resistor setting for V_{LCD} voltage regulation (IRS = L), resistors (Ra', Rb' and Rc') can be added between V_{SS} and V_R, between AMP_{OUTP} and AMP_{OUT}, and between V_R and AMP_{OUT} to set the LCD drive voltage V_{LCD}. In such cases, the electronic volume function can be used to control the LCD drive voltage V_{LCD} and to regulate the contrast of the LCD contents via commands.

In addition, the μPD16686, 16687 enable selection between two display values (for normal display and partial display).

The value is set using an external division resistor and is automatically selected by the DTY flag in the control register 2 (R1).

The V_{LCD} value can be determined using **Example 1** (DTY = 0) and **Example 2** (DTY = 1) if it is within the range of $V_{LCD} < V_{OUT}$.

Example 1. DTY = 0, normal display mode

$$V_{LCD} = \left(1 + \frac{Rb'}{Ra'}\right) V_{EV}$$

$$V_{LCD} = \left(1 + \frac{Rb'}{Ra'}\right) \left(1 - \frac{\alpha}{384}\right) V_{REG}$$

Remark $V_{EV} \left(1 - \frac{\alpha}{384}\right) V_{REG}$

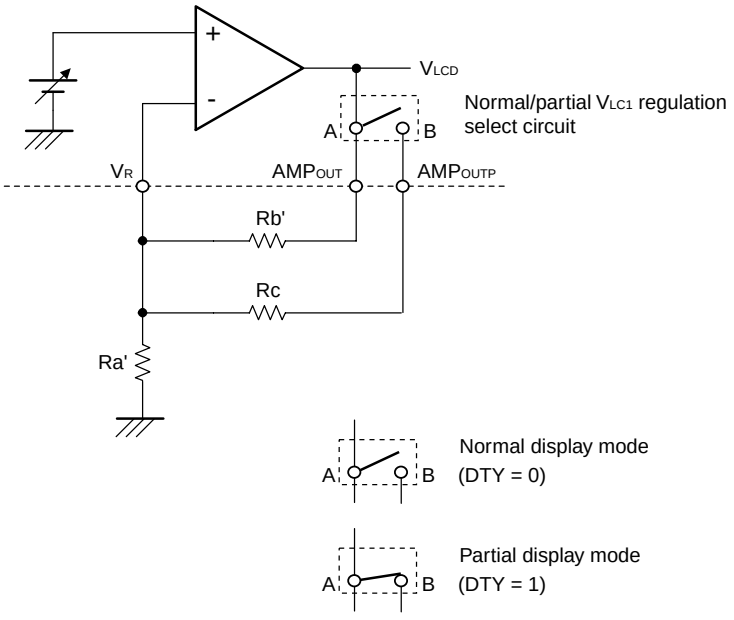
Example 2. DTY = 1, partial display mode

$$V_{LCD} = \left(1 + \frac{Rb' \times Rc}{Ra'(Rb' + Rc)}\right) V_{EV}$$

$$V_{LCD} = \left(1 + \frac{Rb' \times Rc}{Ra'(Rb' + Rc)}\right) \left(1 - \frac{\alpha}{384}\right) V_{REG}$$

Remark $V_{EV} = \left(1 - \frac{\alpha}{384}\right) V_{REG}$

Figure 3-14. When Using External Resistor



3.6.4 Use of op amp for level power supply control

Although the μPD16686, 16687 include a circuit designed for low power consumption (HPM1, HPM0 = 0, 0), display quality problems may occur when a large-load LCD panel is used. In such cases, the display quality and power consumption level can be improved by setting. The HPM1 and HPM0 flags in the power system control 1(R32) to "0, 1" to "1, 1" to switch to the op amp driver capacity for mode settings shown in Table 3-14. Check the actual display quality before deciding which mode to set.

If setting high power mode still does not sufficiently improve the display quality, the LCD drive voltage must be provided from an external power source.

Table 3-14. Op Amp Mode Setting

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Low power mode
1	0	High power mode
1	1	For power activation

3.6.5 Application examples of power supply circuits

Figures 3-15 to 3-19 show application examples of power supply circuits.

Figure 3-15. IRS = H, [OP2, OP1, OP0] = [1, 1, 1]

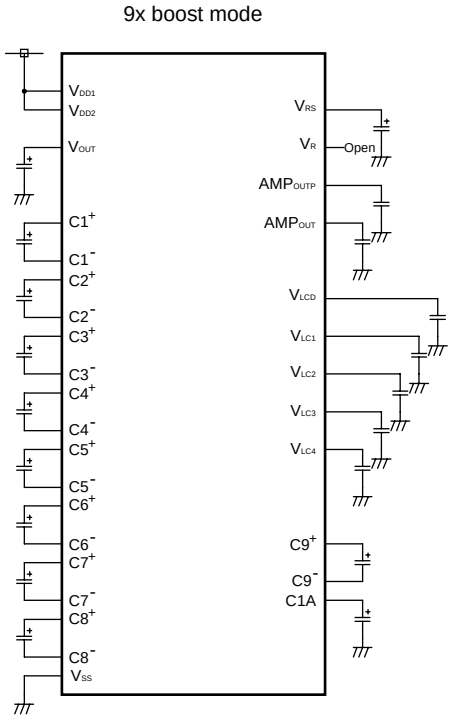


Figure 3-16. IRS = L, [OP2, OP1, OP0] = [1, 1, 1]

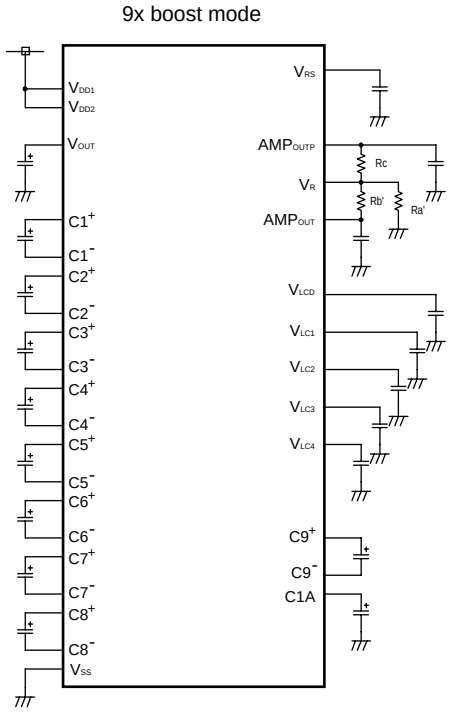


Figure 3-17. IRS = H, [OP2, OP1, OP0] = [0, 1, 1]

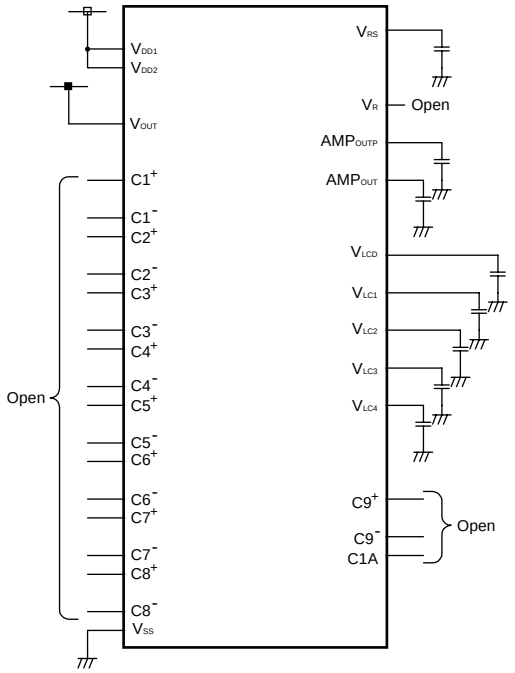


Figure 3-18. IRS = L, [OP2, OP1, OP0] = [0, 0, 1]

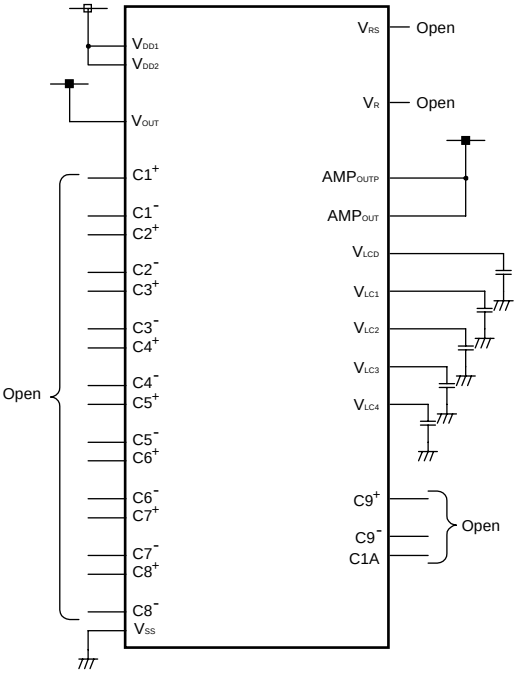
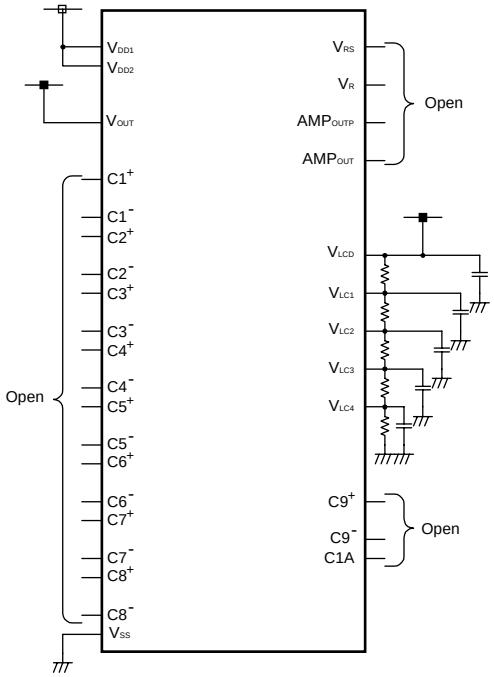


Figure 3-19. IRS = L, [OP2, OP1, OP0] = [0, 0, 0]



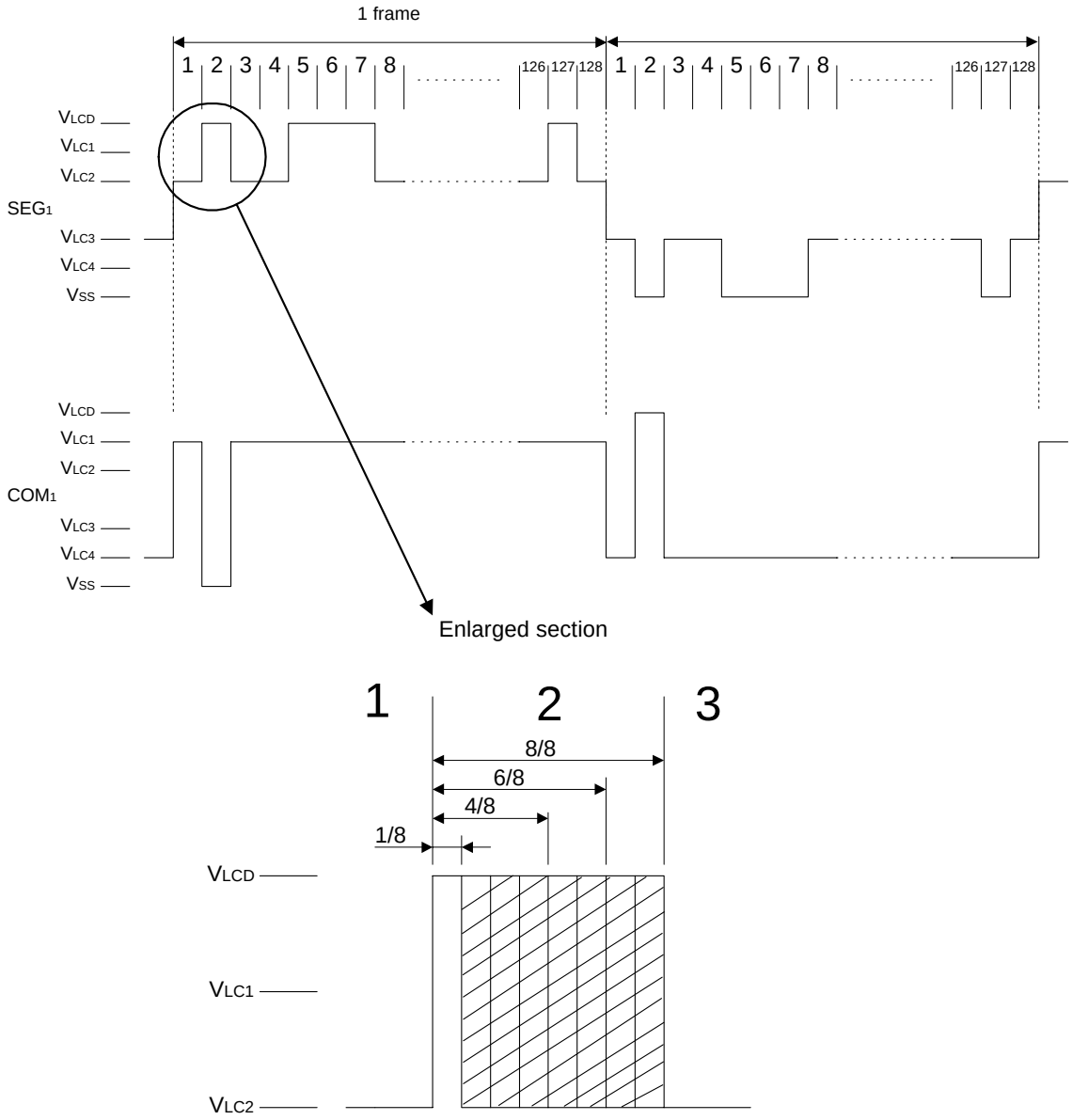
3.7 LCD Display Drivers

μPD16686, 16687 include both a full dot driver and a static driver icon driver. The full dot driver has a 33-level gray-scale palette (eight levels of pulse width modulation plus four-frame rate control), from which four levels of gray scale can be selected and registered as the IC's output gray-scale palette. The icon driver has a gray-scale palette with 32-level pulse width modulation, from which four levels of gray scale can be selected and registered for use as the IC's output gray-scale palette.

3.7.1 Full-dot pulse width modulation

The μPD16686, 16687's pulse width modulator divides the normal LCD display signal's segment pulse width by eight and outputs in synch with the dot output timing based on the ratio (1/8 to 8/8 pulses) for the gray-scale palette that has been selected via a command.

Figure 3-20. Full-Dot Pulse Width Modulation



Caution There is no pulse width modulation for common outputs.

The output pulses are output as odd-numbered lines/even-numbered lines or as even-numbered lines/odd-numbered lines, as shown in Figure 3-21. The pulse rising edge and falling edge combinations for each frame are listed in Table 3-15.

Figure 3-21. Example of Pulse Width Modulated Output

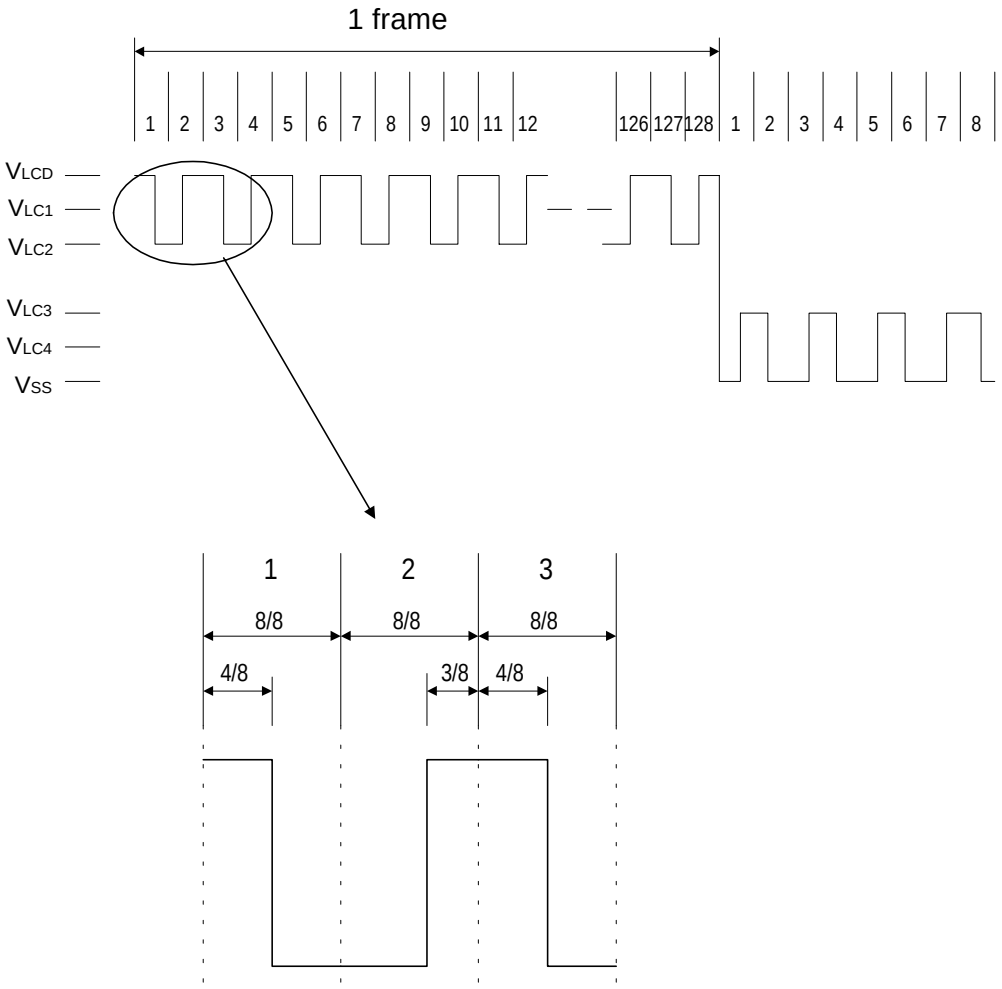


Table 3-15. Example of Pulse Width Modulated Output (1/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
0	4n+1	0	0	0	0	0	0	0	0
	4n+2	0	0	0	0	0	0	0	0
	4n+3	0	0	0	0	0	0	0	0
	4n+4	0	0	0	0	0	0	0	0
1	4n+1	↑1	↓1	0	0	0	0	0	0
	4n+2	0	0	0	0	↓1	↑1	0	0
	4n+3	0	0	0	0	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	0	0	0	0
2	4n+1	↑1	↓1	0	0	↑1	↓1	0	0
	4n+2	↓1	↑1	0	0	↓1	↑1	0	0
	4n+3	0	0	↓1	↑1	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	0	0	↑1	↓1
3	4n+1	↑1	↓1	↓1	↑1	↑1	↓1	0	0
	4n+2	↓1	↑1	0	0	↓1	↑1	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	0	0	↓1	↑1
	4n+4	0	0	↑1	↓1	↓1	↑1	↑1	↓1
4	4n+1	↑1	↓1	↓1	↑1	↑1	↓1	↓1	↑1
	4n+2	↓1	↑1	↑1	↓1	↓1	↑1	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	↑1	↓1	↓1	↑1
	4n+4	↓1	↑1	↑1	↓1	↓1	↑1	↑1	↓1
5	4n+1	↑2	↓2	↓1	↑1	↑1	↓1	↓1	↑1
	4n+2	↓1	↑1	↑1	↓1	↓2	↑2	↑1	↓1
	4n+3	↑1	↓1	↓1	↑1	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓1	↑1	↑1	↓1
6	4n+1	↑2	↓2	↓1	↑1	↑2	↓2	↓1	↑1
	4n+2	↓2	↑2	↑1	↓1	↓2	↑2	↑1	↓1
	4n+3	↑1	↓1	↓2	↑2	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓1	↑1	↑2	↓2
7	4n+1	↑2	↓2	↓2	↑2	↑2	↓2	↓1	↑1
	4n+2	↓2	↑2	↑1	↓1	↓2	↑2	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑1	↓1	↓2	↑2
	4n+4	↓1	↑1	↑2	↓2	↓2	↑2	↑2	↓2
8	4n+1	↑2	↓2	↓2	↑2	↑2	↓2	↓2	↑2
	4n+2	↓2	↑2	↑2	↓2	↓2	↑2	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑2	↓2	↓2	↑2
	4n+4	↓2	↑2	↑2	↓2	↓2	↑2	↑2	↓2
9	4n+1	↑3	↓3	↓2	↑2	↑2	↓2	↓2	↑2
	4n+2	↓2	↑2	↑2	↓2	↓3	↑3	↑2	↓2
	4n+3	↑2	↓2	↓2	↑2	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓2	↑2	↑2	↓2
10	4n+1	↑3	↓3	↓2	↑2	↑3	↓3	↓2	↑2
	4n+2	↓3	↑3	↑2	↓2	↓3	↑3	↑2	↓2
	4n+3	↑2	↓2	↓3	↑3	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓2	↑2	↑3	↓3

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

Table 3-15. Example of Pulse Width Modulated Output (2/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
11	4n+1	↑3	↓3	↓3	↑3	↑3	↓3	↓2	↑2
	4n+2	↓3	↑3	↑2	↓2	↓3	↑3	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑2	↓2	↓3	↑3
	4n+4	↓2	↑2	↑3	↓3	↓3	↑3	↑3	↓3
12	4n+1	↑3	↓3	↓3	↑3	↑3	↓3	↓3	↑3
	4n+2	↓3	↑3	↑3	↓3	↓3	↑3	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑3	↓3	↓3	↑3
	4n+4	↓3	↑3	↑3	↓3	↓3	↑3	↑3	↓3
13	4n+1	↑4	↓4	↓3	↑3	↑3	↓3	↓3	↑3
	4n+2	↓3	↑3	↑3	↓3	↓4	↑4	↑3	↓3
	4n+3	↑3	↓3	↓3	↑3	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓3	↑3	↑3	↓3
14	4n+1	↑4	↓4	↓3	↑3	↑4	↓4	↓3	↑3
	4n+2	↓4	↑4	↑3	↓3	↓4	↑4	↑3	↓3
	4n+3	↑3	↓3	↓4	↑4	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓3	↑3	↑4	↓4
15	4n+1	↑4	↓4	↓4	↑4	↑4	↓4	↓3	↑3
	4n+2	↓4	↑4	↑3	↓3	↓4	↑4	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑3	↓3	↓4	↑4
	4n+4	↓3	↑3	↑4	↓4	↓4	↑4	↑4	↓4
16	4n+1	↑4	↓4	↓4	↑4	↑4	↓4	↓4	↑4
	4n+2	↓4	↑4	↑4	↓4	↓4	↑4	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑4	↓4	↓4	↑4
	4n+4	↓4	↑4	↑4	↓4	↓4	↑4	↑4	↓4
17	4n+1	↑5	↓5	↓4	↑4	↑4	↓4	↓4	↑4
	4n+2	↓4	↑4	↑4	↓4	↓5	↑5	↑4	↓4
	4n+3	↑4	↓4	↓4	↑4	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓4	↑4	↑4	↓4
18	4n+1	↑5	↓5	↓4	↑4	↑5	↓5	↓4	↑4
	4n+2	↓5	↑5	↑4	↓4	↓5	↑5	↑4	↓4
	4n+3	↑4	↓4	↓5	↑5	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓4	↑4	↑5	↓5
19	4n+1	↑5	↓5	↓5	↑5	↑5	↓5	↓4	↑4
	4n+2	↓5	↑5	↑4	↓4	↓5	↑5	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑4	↓4	↓5	↑5
	4n+4	↓4	↑4	↑5	↓5	↓5	↑5	↑5	↓5
20	4n+1	↑5	↓5	↓5	↑5	↑5	↓5	↓5	↑5
	4n+2	↓5	↑5	↑5	↓5	↓5	↑5	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑5	↓5	↓5	↑5
	4n+4	↓5	↑5	↑5	↓5	↓5	↑5	↑5	↓5
21	4n+1	↑6	↓6	↓5	↑5	↑5	↓5	↓5	↑5
	4n+2	↓5	↑5	↑5	↓5	↓6	↑6	↑5	↓5
	4n+3	↑5	↓5	↓5	↑5	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓5	↑5	↑5	↓5

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

Table 3-15. Example of Pulse Width Modulated Output (3/3)

Gray-scale level	COM	1, 2 Frames		3, 4 Frames		5, 6 Frames		7, 8 Frames	
		SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered	SEG Odd Numbered	SEG Even Numbered
22	4n+1	↑6	↓6	↓5	↑5	↑6	↓6	↓5	↑5
	4n+2	↓6	↑6	↑5	↓5	↓6	↑6	↑5	↓5
	4n+3	↑5	↓5	↓6	↑6	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓5	↑5	↑6	↓6
23	4n+1	↑6	↓6	↓6	↑6	↑6	↓6	↓5	↑5
	4n+2	↓6	↑6	↑5	↓5	↓6	↑6	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑5	↓5	↓6	↑6
	4n+4	↓5	↑5	↑6	↓6	↓6	↑6	↑6	↓6
24	4n+1	↑6	↓6	↓6	↑6	↑6	↓6	↓6	↑6
	4n+2	↓6	↑6	↑6	↓6	↓6	↑6	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑6	↓6	↓6	↑6
	4n+4	↓6	↑6	↑6	↓6	↓6	↑6	↑6	↓6
25	4n+1	↑7	↓7	↓6	↑6	↑6	↓6	↓6	↑6
	4n+2	↓6	↑6	↑6	↓6	↓7	↑7	↑6	↓6
	4n+3	↑6	↓6	↓6	↑6	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓6	↑6	↑6	↓6
26	4n+1	↑7	↓7	↓6	↑6	↑7	↓7	↓6	↑6
	4n+2	↓7	↑7	↑6	↓6	↓7	↑7	↑6	↓6
	4n+3	↑6	↓6	↓7	↑7	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓6	↑6	↑7	↓7
27	4n+1	↑7	↓7	↓7	↑7	↑7	↓7	↓6	↑6
	4n+2	↓7	↑7	↑6	↓6	↓7	↑7	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑6	↓6	↓7	↑7
	4n+4	↓6	↑6	↑7	↓7	↓7	↑7	↑7	↓7
28	4n+1	↑7	↓7	↓7	↑7	↑7	↓7	↓7	↑7
	4n+2	↓7	↑7	↑7	↓7	↓7	↑7	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑7	↓7	↓7	↑7
	4n+4	↓7	↑7	↑7	↓7	↓7	↑7	↑7	↓7
29	4n+1	8	8	↓7	↑7	↑7	↓7	↓7	↑7
	4n+2	↓7	↑7	↑7	↓7	8	8	↑7	↓7
	4n+3	↑7	↓7	↓7	↑7	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	↓7	↑7	↑7	↓7
30	4n+1	8	8	↓7	↑7	8	8	↓7	↑7
	4n+2	8	8	↑7	↓7	8	8	↑7	↓7
	4n+3	↑7	↓7	8	8	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	↓7	↑7	8	8
31	4n+1	8	8	8	8	8	8	↓7	↑7
	4n+2	8	8	↑7	↓7	8	8	8	8
	4n+3	8	8	8	8	↑7	↓7	8	8
	4n+4	↓7	↑7	8	8	8	8	8	8
32	4n+1	8	8	8	8	8	8	8	8
	4n+2	8	8	8	8	8	8	8	8
	4n+3	8	8	8	8	8	8	8	8
	4n+4	8	8	8	8	8	8	8	8

Remarks 1. n: Integer from 0 to 31.

2. ↑A: Rising edge of pulse during line A output.

3. ↓A: Rising edge of pulse at start of line A output.

4. A: PWM pulse width (A/8)

3.7.2 Full-dot frame rate control

When combined with pulse width modulation as described in **Table 3-15**, the μPD16686, 16687's frame speed is based on 8-frame cycles. The subsampling pattern is output based on the palette stored in the IC.

Full-Dot Gray-Scale Palette (Output Pulse Width: x/8 Pulses)

Gray Scale	Frames								Comments
	1	2	3	4	5	6	7	8	
Level 0	0	0	0	0	0	0	0	0	OFF data
Level 1	1	1	0	0	0	0	0	0	
Level 2	1	1	0	0	1	1	0	0	
Level 3	1	1	1	1	1	1	0	0	
Level 4	1	1	1	1	1	1	1	1	
Level 5	2	2	1	1	1	1	1	1	
Level 6	2	2	1	1	2	2	1	1	
Level 7	2	2	2	2	2	2	1	1	
Level 8	2	2	2	2	2	2	2	2	
Level 9	3	3	2	2	2	2	2	2	
Level 10	3	3	2	2	3	3	2	2	
Level 11	3	3	3	3	3	3	2	2	
Level 12	3	3	3	3	3	3	3	3	
Level 13	4	4	3	3	3	3	3	3	
Level 14	4	4	3	3	4	4	3	3	
Level 15	4	4	4	4	4	4	3	3	
Level 16	4	4	4	4	4	4	4	4	50%
Level 17	5	5	4	4	4	4	4	4	
Level 18	5	5	4	4	5	5	4	4	
Level 19	5	5	5	5	5	5	4	4	
Level 20	5	5	5	5	5	5	5	5	
Level 21	6	6	5	5	5	5	5	5	
Level 22	6	6	5	5	6	6	5	5	
Level 23	6	6	6	6	6	6	5	5	
Level 24	6	6	6	6	6	6	6	6	
Level 25	7	7	6	6	6	6	6	6	
Level 26	7	7	6	6	7	7	6	6	
Level 27	7	7	7	7	7	7	6	6	
Level 28	7	7	7	7	7	7	7	7	
Level 29	8	8	7	7	7	7	7	7	
Level 30	8	8	7	7	8	8	7	7	
Level 31	8	8	8	8	8	8	7	7	
Level 32	8	8	8	8	8	8	8	8	100%

Remark The gradation in the Comments column are images of the gray-scale level.

3.7.3 Line shift driver

If the frame rate control is performed with equal pulse widths and the same gray scale is displayed on the LCD's full screen, problems such as flickering may occur on the LCD panel. The μPD16686, 16687 provide a line shift driver as a countermeasure against such screen image problems.

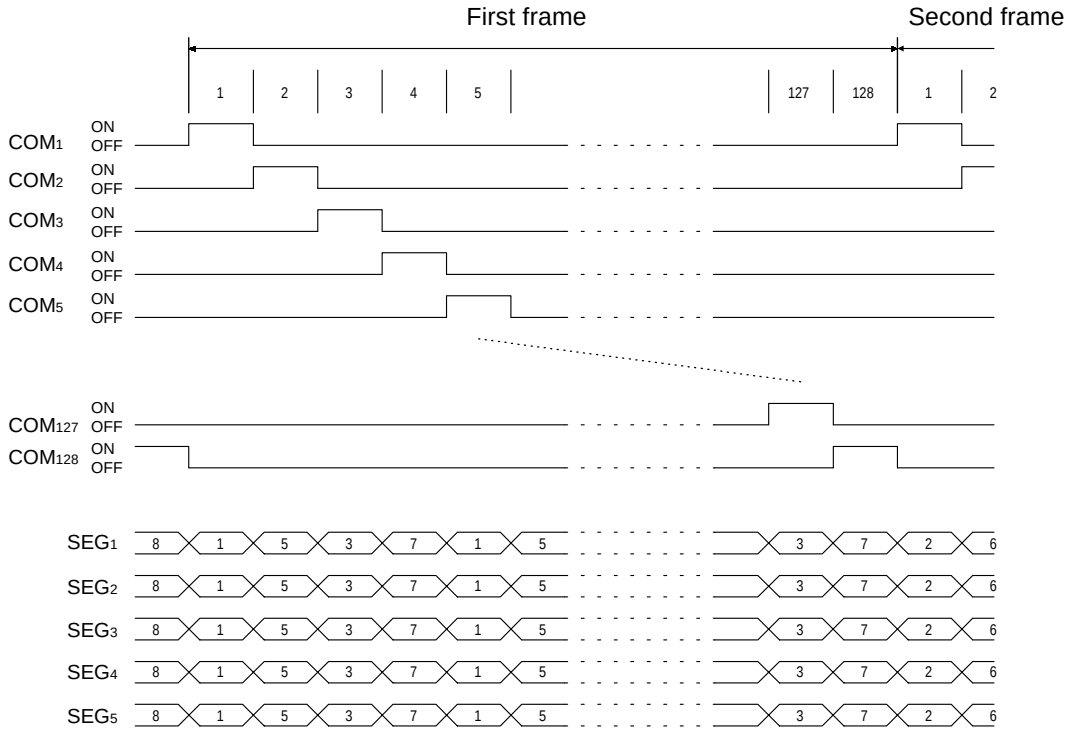
Using 8 frames per cycle, the segment PWM output timing is shifted among the common outputs, as shown in Table 3-16 below.

Table 3-16. Line Shift Driver

	Turn 1								Turn 2											
Frame	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4
COM_1	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_2	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
COM_3	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6
COM_4	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2
COM_5	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_6	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
COM_7	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6
COM_8	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2
COM_9	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4
COM_{10}	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8	F1	F2	F3	F4	F5	F6	F7	F8
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

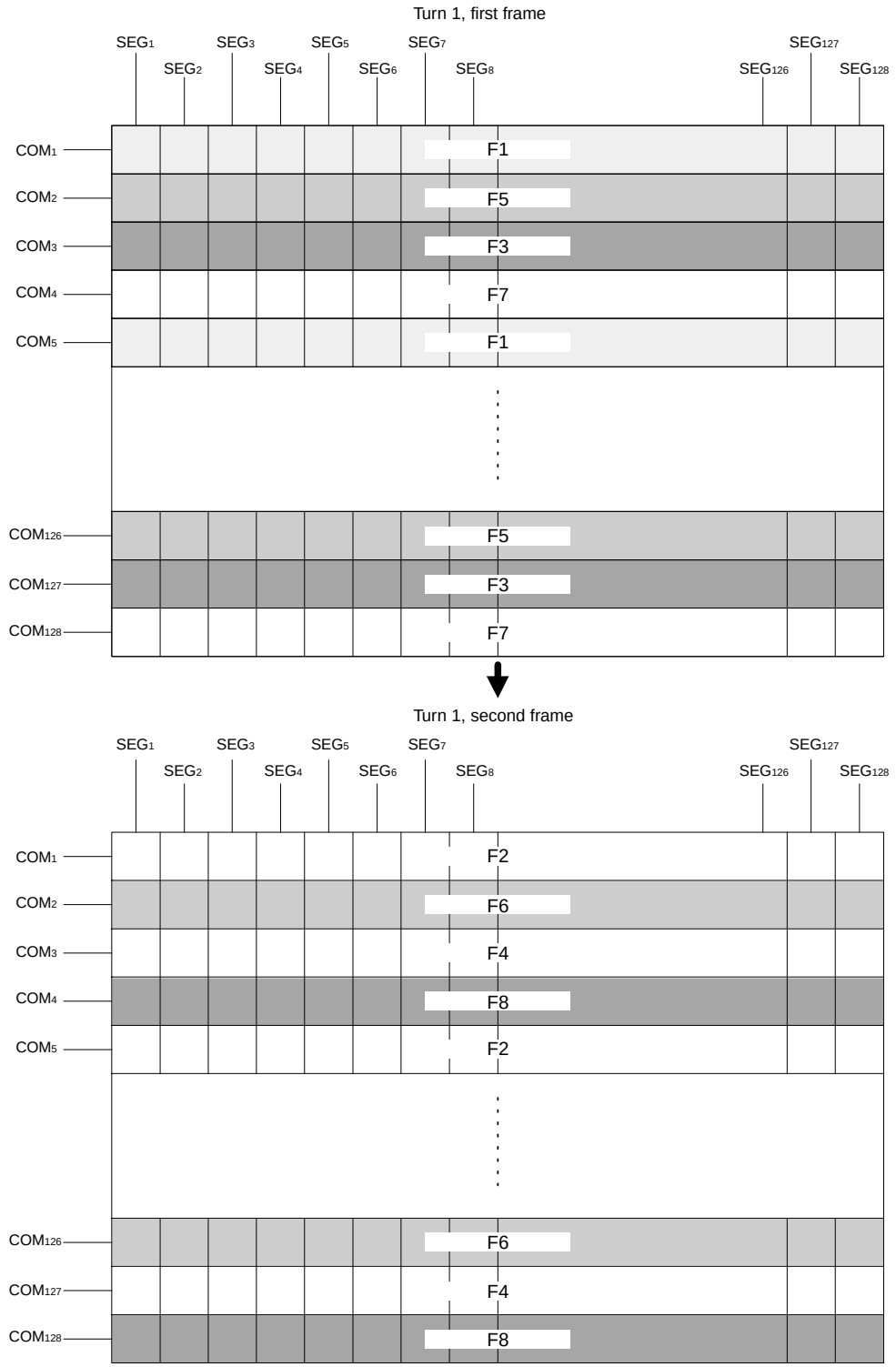
Remark Fx: Pulse width modulated output frame (See **3.7.2 Full-dot frame rate control**).

Figure 3-22. Full Dot Frame Rate Control



Remark Numerical values in the segment data correspond to the gray-scale palette's frame numbers.

Figure 3-23. Line Shift Driver Image



3.7.4 Display size settings

The μPD16686, 16687 can be set for any duty value from 1/1 to 1/128. This duty setting can be made via bits DT6 to DT0 in the duty setting register (R5), as shown in Table 3-17.

Table 3-17. Duty Settings

DT6	DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	0	0	0	0	1/1
0	0	0	0	0	0	1	1/2
0	0	0	0	0	1	0	1/3
0	0	0	0	0	1	1	1/4
			:				:
1	1	1	1	1	0	1	1/126
1	1	1	1	1	1	0	1/127
1	1	1	1	1	1	1	1/128

3.7.5 Setting of LCD AC driver's inversion cycle and AC driver's inversion position

The μPD16686, 16687 enable any setting to be made for the AC driver's inversion position and the inversion position shift amount for each displayed frame via settings made in the AC driver inversion cycle register (R6) and the AC driver inversion position shift register (R7) for normal display mode or via settings made in the partial AC driver inversion cycle register (R8) and the partial AC driver inversion position shift register (R9) for partial display mode.

In normal display mode, the AC driver inversion cycle can be set for any number of inverted (reverse display) lines listed in Table 3-18, based on the NID6 to NID0 bit settings in the AC driver inversion cycle register (R6).

If the screen display size has been changed via settings made in the duty setting register (R5), the NIDn values are automatically overwritten by values from the corresponding DTYn bits.

The shift amount for each displayed frame can be set as shown in Table 3-19 via settings made to bits MSD6 to MSD0 in the AC driver inversion position shift register (R7).

Table 3-18. Settings of AC Driver Inversion Cycle Register (R6)

NID6	NID5	NID4	NID3	NID2	NID1	NID0	Inverted Lines
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
			:				:
1	1	1	1	1	0	1	126
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128

Table 3-19. Settings of AC Driver Inversion Position Shift Register

MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			:				:
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

In partial display mode, the AC driver inversion cycle can be set for any number of inverted (reverse display) lines listed in Table 3-20, based on the PID5 to PID0 bit settings in the partial AC driver inversion cycle register (R8).

The shift amount for each displayed frame can be set as shown in Table 3-21 via settings made to bits PSD5 to PSD0 in the partial AC driver inversion position shift register (R9).

Table 3-20. Settings of Partial AC Driver Inversion Cycle Register (R8)

PID5	PID4	PID3	PID2	PID1	PID0	Inverted Lines
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
		:				:
1	0	0	0	1	1	36
1	0	0	1	0	0	37
1	0	0	1	0	1	38

Table 3-21. Setting of Partial AC Driver Inversion Position Shift Register (R9)

PSD5	PSD4	PSD3	PSD2	PSD1	PSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
			:			:
1	0	0	0	1	1	35
1	0	0	1	0	0	36
1	0	0	1	0	1	37

Be sure to maintain the following relationship among the display size, AC inversion cycle, and AC inversion position.

Display size (duty) ≥ AC inversion cycle ≥ AC inversion shift amount

Caution Setting a small inversion cycle will cause a reduction in the IC's display drive capacity and an increase in the current consumption.
NEC therefore recommends determining the inversion cycle after making a thorough evaluation of the actual LCD panel.

3.8 Display Modes

3.8.1 Partial display mode

The μPD16686, 16687 include a function for outputting a display that uses only part of the LCD panel. The duty setting for partial display mode can be selected as 1/12, 1/25, or 1/38. Parts of the LCD panel that are outside of the specified display area are scanned with non-select waveforms. The partial start line address register (R21) is used to select which part of the LCD panel to use for the partial display. The display area starts from the start line address and includes the number of lines (12, 25, or 38 lines) that has been specified via the partial display mode setting (R10).

When entering this mode, the booster is set to the boost level number that has been set via the power system control 3 (partial display boost register) (R34) and the display start line is fixed as 00H. In addition, the bias level is automatically changed to the value that has been set via the partial display mode setting (R10). The relationship between the oscillator's frequency and the frame frequency in partial mode is also automatically changed.

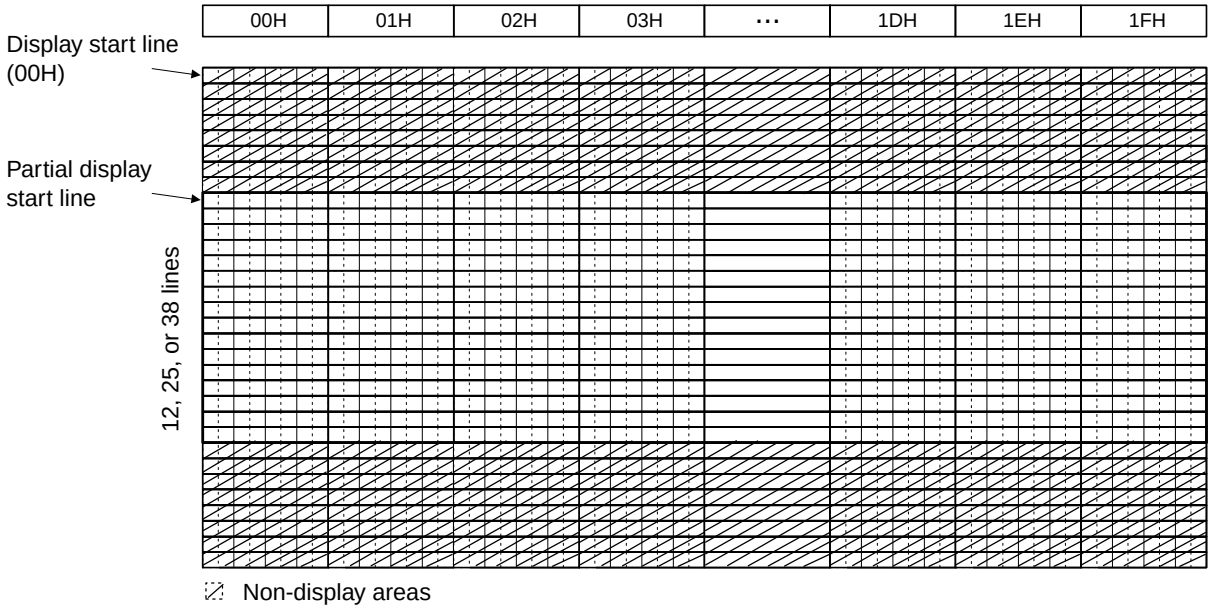
Figure 3-24 shows the mutual relationship between the partial line start address and the LCD display.

When using the partial display mode, the blinking and reverse display functions can be used in the same way as during full-dot display mode.

Caution The LCD driver voltage is lower in partial display mode, because the duty is lower than in normal display mode. There may be restrictions on the useble duty depending on the LCD panel characteristics.

We recommend determining the partial duty after making a thorough evaluation of the actual LCD panel.

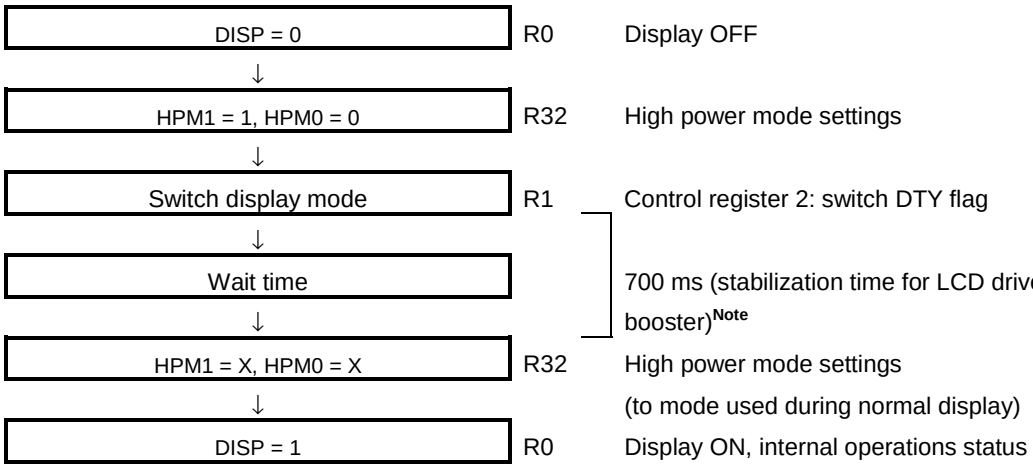
Figure 3-24. Relationship Between Partial Line Start Address and LCD Display (in Partial Display Mode)



Caution In partial display mode, the display start line setting (R12) command is ignored.

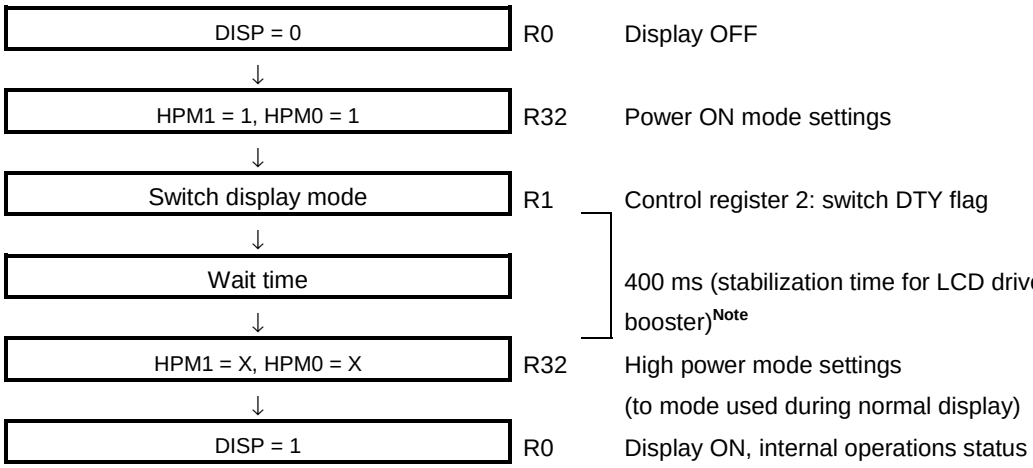
When switching from normal display mode to partial display mode or from partial display mode to normal display mode, if an electric charge remains in the smoothing capacitor that is connected between the LCD drive voltage pins (V_{LCD} to V_{LC4}) and the V_{SS} pin, abnormalities such as a brief all-black display may occur during the mode switching operation. To avoid such abnormalities, we recommend using the following power-on sequence.

Normal display → partial display switch sequence



Note This 700 ms wait time indicates the time for the V_{LCD} level to change from 15 to 6 V and thus varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. Our recommends determining the wait time after making a thorough evaluation of the actual device.

Partial display → Normal display switch sequence



Note This 400 ms wait time indicates the time for the V_{LCD} level to change from 15 V to 6 V and thus varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommends determining the wait time after making a thorough evaluation of the actual device.

3.8.2 Monochrome (black/white) display

The μPD16686, 16687 provide both a four-level gray scale display mode and a monochrome display mode.

To switch to the monochrome display mode, set GRAY = H. The display RAM for one screen of monochrome display mode contents is configured as 128 bits x 128 bits (16 x 8 bits). When using these IC's in monochrome display mode, two screens of data can be written to the display RAM and the two screens can be switched by setting the DSEL bit in the control register 2 (R1). Screen 1 is displayed on the LCD panel when DSEL = L and screen 2 is displayed when DSEL = H.

When writing data, the display RAM uses the same X address (00H to 0FH) and Y address and the BWW bit value in the control register 2 (R1) determines which of the two screens the data will be written to: when BWW = L, data is written to screen 1 and when BWW = H, data is written to screen 2, as shown in Figure 3-25.

When accessing a specified bit, specify both the X address and Y address. The display data in D_0 to D_7 (sent from the CPU) corresponds to the SEGx portions of the LCD display, as shown in Figure 3-26. Figure 3-27 shows the relationship between the display data in monochrome display mode and the page/column addresses.

Figure 3-25. Display RAM Image in Monochrome (Black/White) Mode

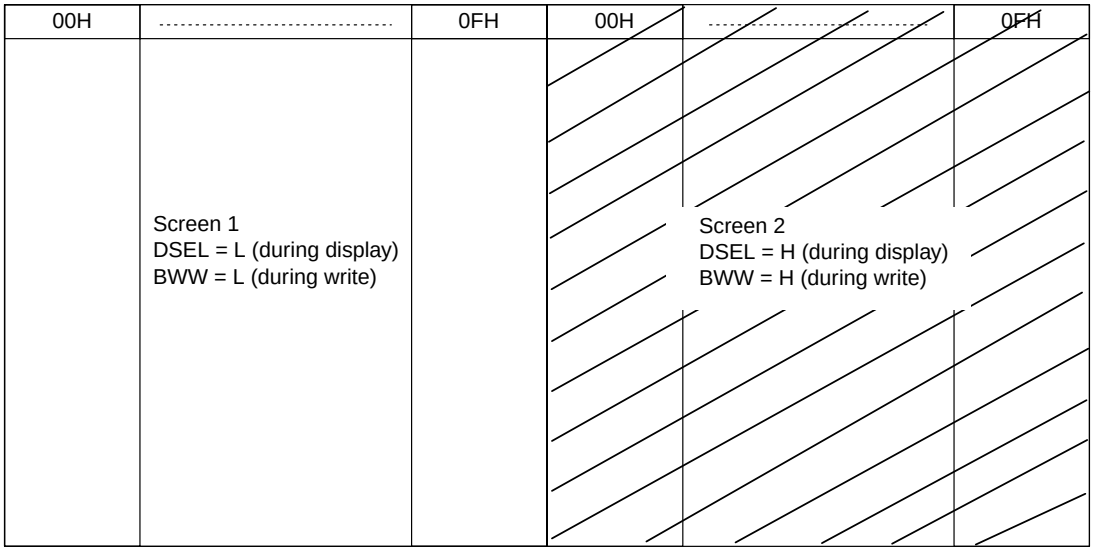
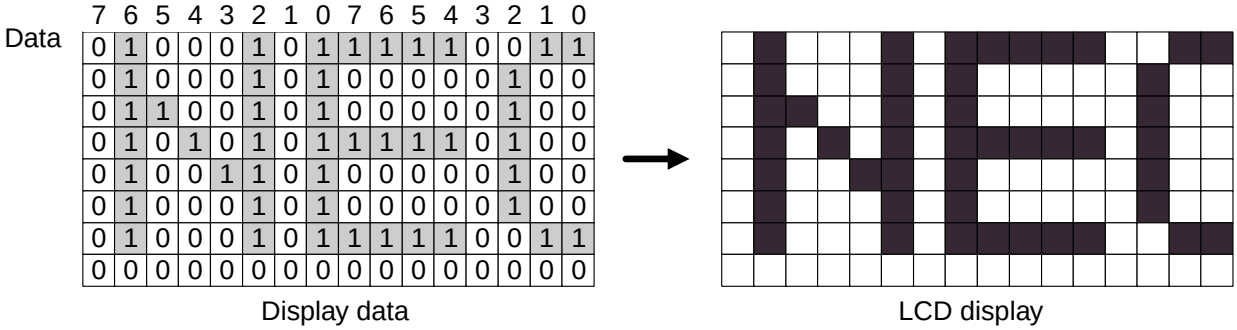
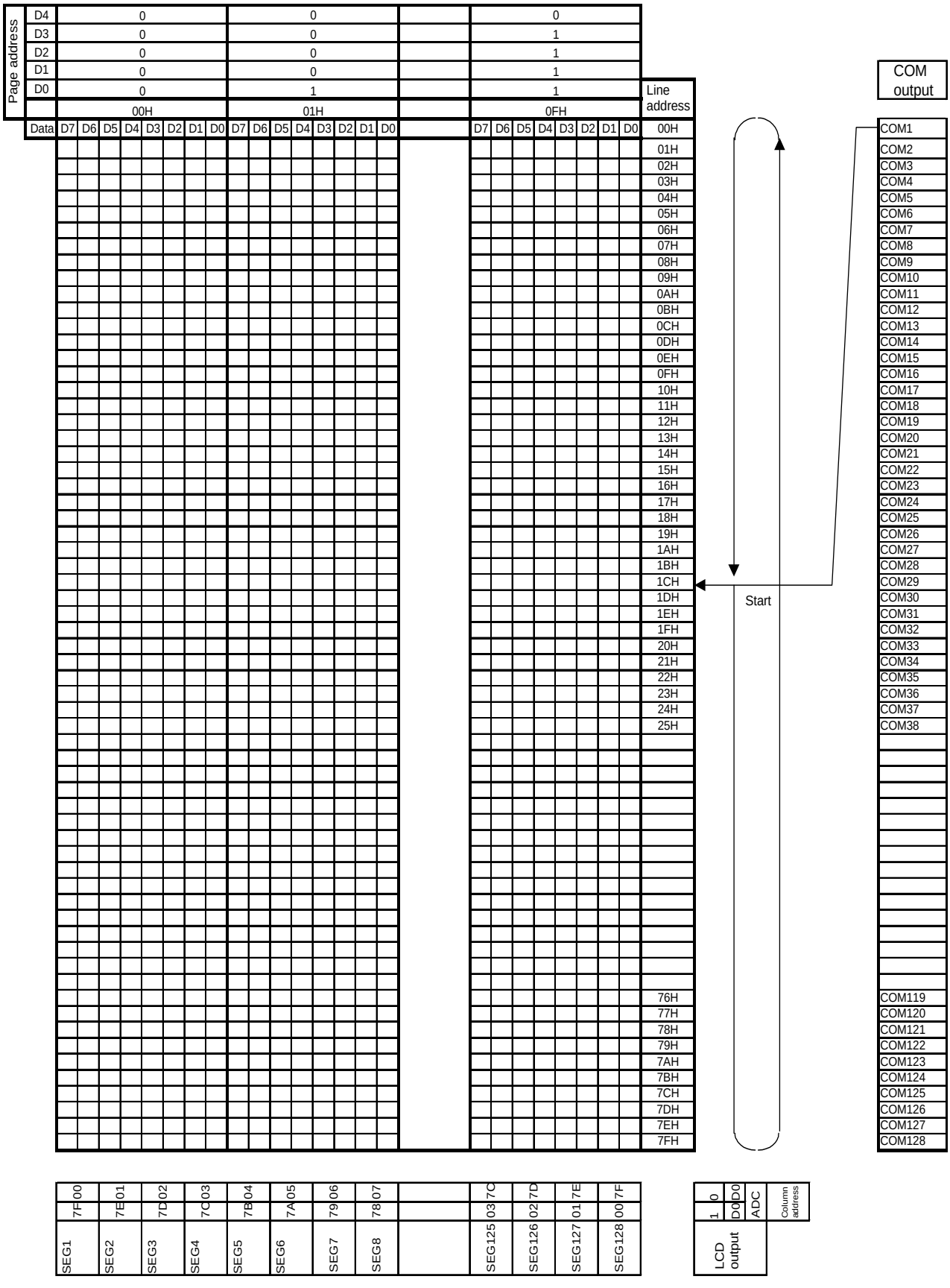


Figure 3-26. Relationship Between Display Data and LCD Display



★ **Figure 3-27. Relation Between the Display Data and Page/Column Address (in Monochrome Display Mode)**



3.8.3 Icon display

The μPD16686, 16687 include 20 segment pins and two common pins (both output the same signal) for displaying icons, independent of the pins used to display graphics. Icons are static-driven and their contrast can be adjusted at 32 levels using phase modulation.

The static icon data RAM (R41) that is used to record icon display data contains display data (DIS) and blink data (BRI) in a 20-bit x 2 configuration, as shown in Table 3-22 (where ADC = 0) and Table 3-23 (where ADC = 1).

Addresses in the static icon data RAM are specified via the static icon address register (R40) and then data is written to memory.

The icon blink function operates only when the display data setting is 1, the blink data setting is 1, and the IBL setting is also 1 (R1).

Table 3-22. Static Icon Data RAM (ADC = 0)

Address	Static Icon Output Number (PSEGn)							
	DIS	BRI	DIS	BRI	DIS	BRI	DIS	BRI
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
00H	1		2		3		4	
01H	5		6		7		8	
02H	9		10		11		12	
03H	13		14		15		16	
04H	17		18		19		20	

Table 3-23. Static Icon Data RAM (ADC = 1)

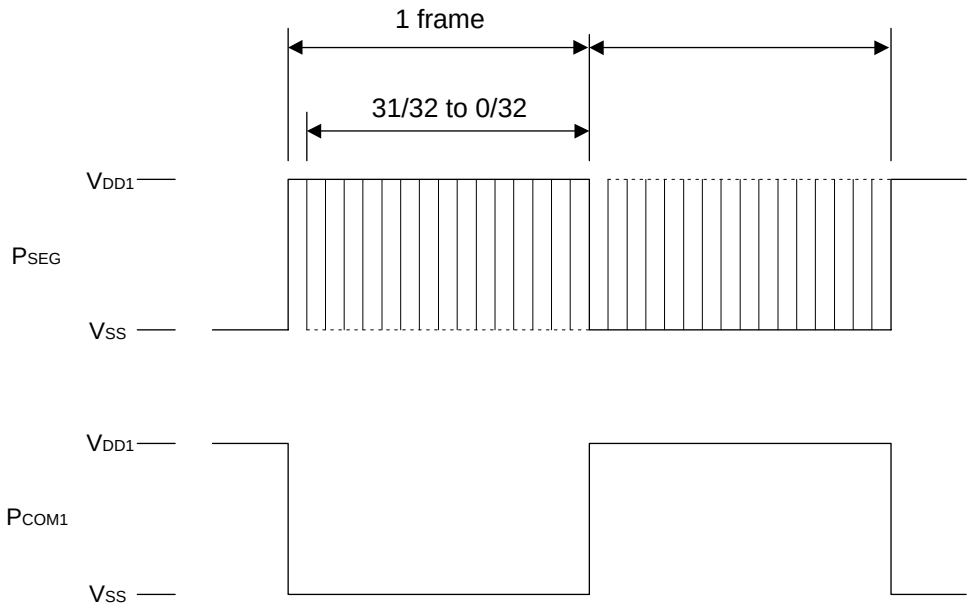
Address	Static Icon Output Number (PSEGn)							
	DIS	BRI	DIS	BRI	DIS	BRI	DIS	BRI
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
00H	20		19		18		17	
01H	16		15		14		13	
02H	12		11		10		9	
03H	8		7		6		5	
04H	4		3		2		1	

Adjustment of contrast is controlled by phase modulation set via the static icon contrast (R42). The pulse width of the ON signal that is output in static drive mode is divided into 32 levels (1/32 to 32/32 pulse width) and the dot output's timing changes during output according to the phase modulation ratio recorded in bits ICS4 to ICS0 of the static icon contrast (R42), as shown in Table 3-24.

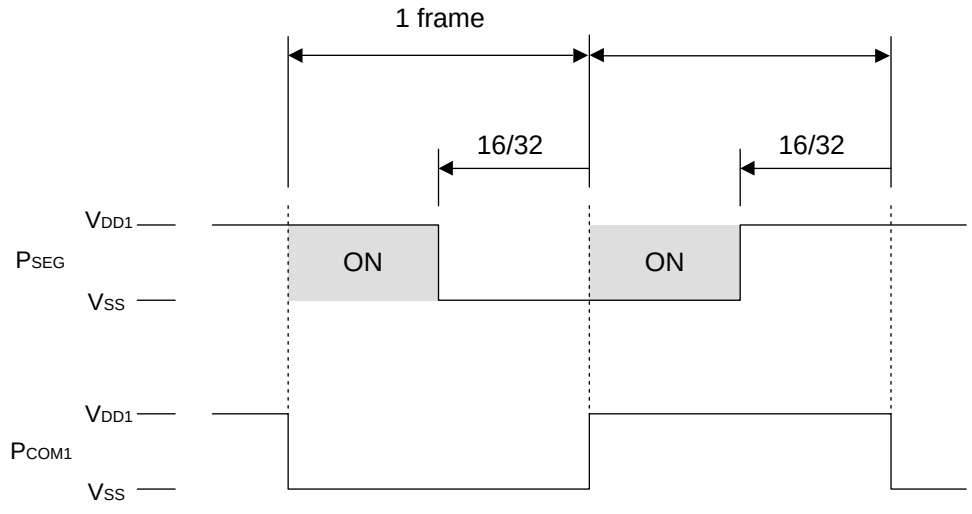
Table 3-24. Dot Output Timing Changes

ICS4	ICS3	ICS2	ICS1	ICS0	Phase Modulation Ratio
0	0	0	0	0	0/32
0	0	0	0	1	1/32
0	0	0	1	0	2/32
0	0	0	1	1	3/32
		:			:
1	1	1	0	1	29/32
1	1	1	1	0	30/32
1	1	1	1	1	31/32

Figure 3-28. Phase Modulation Driver Waveforms



Example of phase modulation amount for displaying 10H



3.9 Reset

In the μPD16686, 16687, a reset is executed when the /RES input is at low level or when a reset command is entered. The IC is reset to its default settings. These default settings are listed in the table below.

Register		/RES	Reset Command
Control register 1	R0	Enabled (DISP flag only)	Enabled
Control register 2	R1	Enabled (IDIS flag only)	
X address register	R3	Disabled	
Y address register	R4		
Duty setting register	R5		
AC driver inversion cycle register	R6		
AC driver inversion position shift register	R7		
Partial AC driver inversion cycle register	R8		
Partial AC driver inversion position shift register	R9		
Partial display mode setting	R10		
Display memory access register Note	R11		Disabled
Display start line set	R12		Enabled
Blink X address register	R13		
Blink start line address register	R14		
Blink end line address register	R15		
Blink data memory	R16		Disabled
Inverted X address register	R17		Enabled
Inversion start line address register	R18		
Inversion end line address register	R19		
Inverted data memory	R20		Disabled
Partial start line address register	R21		Enabled
Gray scale data register 1 (0, 0)	R23		
Gray scale data register 2 (0, 1)	R24		
Gray scale data register 3 (1, 0)	R25		
Gray scale data register 4 (1, 1)	R26		
Partial gray scale data register 1 (0, 0)	R27		
Partial gray scale data register 2 (0, 1)	R28		
Partial gray scale data register 3 (1, 0)	R29		
Partial gray scale data register 4 (1, 1)	R30		
Power system control 1	R32		
Power system control 2	R33		
Power system control 3	R34		
Electronic volume register	R35		
Partial electronic volume register	R36		
Boost adjustment register	R37		
Static icon address	R40		
Static icon data register	R41		Disabled
Static icon contrast	R42		Enabled
RAM test mode setting	R44		
Signature read	R45		Disabled

Enabled: Default value is input, Disabled: Default value is not input

Note When using the /RES pin to reset, the contents of memory are not retained. Use the reset command to reset if the memory contents need to be retained.

Cautions 1. Using the /RES pin to reset initializes the shift clock counter.

★ **2. Always input the reset command as the first command after power application .**

4. COMMANDS

The μPD16686, 16687 chips use a combination of RS, /RD (E), and /WR (R,/W) signals to identify data bus signals.

Command interpretation and execution is performed using internal timing that does not depend on any external clock. Therefore, processing is very fast and there is usually no need to check for a busy status.

The i80 series CPU interface activates read commands using a low pulse input to the /RD pin and activates write commands using a low pulse input to the /WR pin. The M68 series CPU interface sets read mode using a high level input to the R,/W pin and sets write mode using a low level input to the same pin. It activates both read and write commands using a high-level pulse input to the E pin. Thus, the M68 series CPU interface differs from the i80 series CPU interface in that /RD (E) is at high level during status read and display data read operations, as shown in the following command descriptions and command table.

Command descriptions using an i80 series CPU interface are shown below.

If the serial interface has been selected, data is input sequentially starting from D_7.

4.1 Control Register 1 (R0)

These commands specify the μPD16686, 16687's general operation modes.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	RMW	DISP	STBY	BLD	IVD	HALT	ADC	COMR

RMW	0: Address is incremented after both write access and read access. 1: Read/modify/write mode (Address is incremented only after write access)
DISP	0: Display OFF (All LCD output pins output the V_{SS} level and oscillator and DC/DC converter are operating) 1: Display ON
STBY	0: Normal operation 1: Internal operation and oscillation are stopped. Display is off.
BLD	The blinking dots are specified via the blink start/end line address registers and data is set to blink data RAM. 0: Stop blinking 1: Start blinking
IVD	The number of inverted dots is specified via the inversion start/end line address registers and data is set to inverted data RAM. 0: Stop inversion 1: Start inversion
HALT	0: Start internal operation 1: Stop internal operation (since different display modes are used, when switching between partial and normal display modes, the LCD output pins all output the V_{SS} level and the oscillator is operating, but the DC/DC converter is stopped)
ADC**Note**	The column address corresponding to the SEG outputs (see **Table 4-1**) for displaying the contents of the display data RAM.
COMR**Note**	This inverts (reverses) the scan direction for common outputs. (See **Table 4-2**)

Note The RESET command must be executed before changing this flag's setting.

★ **Table 4-1. Relationship Between Display RAM Column Address and SEG Outputs**

SEG Output		SEG_1				SEG_{128}
ADC	0	00H	→	Column addresses	→	7FH
(D_1)	1	7FH	←	Column addresses	←	00H

★ **Table 4-2. Relationship Between Common Scan Circuit and Scan Direction**

COM Output		Scan Direction		
COMR	0	COM_1	→	COM_{128}
(D_0)	1	COM_{128}	←	COM_1

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.2 Control Register 2 (R1)

These commands specify the μPD16686, 16687's general operation modes.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	FDM	IBL	IDIS	DSEL	BWW	GRAY	DTY	INC

FDM	Settings for full screen display mode 0: Normal operation 1: Full screen display (set entire screen to ON) (When using four-level gray scale, gray-scale level 32 is output for full screen display).
IBL	Static icon blink control, icons with "1" as blink data are blinking. 0: Static icon blink OFF 1: Static icon blink ON
IDIS	0: Static icon display OFF (All static LCD output pins output the V_{SS} level and oscillator and DC/DC converter are operating) 1: Static icon display ON
DSEL	Selects display screen during monochrome display mode. 0: Screen 1 1: Screen 2
BWW	Selects data write screen during monochrome display mode. 0: Screen 1 1: Screen 2
GRAY **Note**	0: 4-level gray scale display mode 1: Monochrome display mode
DTY **Note**	0: Normal display mode (1/1 to 1/128 duty) 1: Partial display mode (1/12, 1/25, or 1/38 duty, 1/5 or 1/6 bias)
INC	0: Increments X address at each access 1: Increments Y address at each access

Note The HALT command must be executed before changing this flag's setting.

Table 4-3. Relationship Between IC's Functions and Display Modes

Item	Normal Display Mode (DTY = 0)		Partial Display Mode (DTY = 1)
Duty	1/1 to 1/128 duty	↔	1/12, 1/25, or 1/38 duty
Booster	×4, ×5, ×6, ×7, ×8, ×9	↔	×2, ×3, ×4
Bias level	1/11, 1/12, 1/10, 1/9, 1/8, 1/7	↔	1/5, 1/6
Gray scale data	Uses levels set to gray scale data registers (R23 to R26)	↔	Uses levels set to partial gray scale data registers (R27 to R30)
(1+Rb/Ra) V_{LCD} regulator resistance factor	Uses values of VRR2, VRR1, and VRR0 in power system control register 2 (R33)	↔	Uses values of PVR2, PVR1, and PVR0 in power system control register 2 (R33)
Electronic volume	Uses value from electronic volume register (R35)	↔	Uses value from partial electronic volume register (R36)

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.3 Reset Command (R2)

When this command is input, the IC's registers (R0 to R42) are reset to their initial values.

★ Always input the reset command as the first command after power application.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0	1

4.4 X Address Register (R3)

The X address register specifies the X address in the display RAM accessed by the CPU. This address is automatically incremented each time the display RAM is accessed (INC = 0, RMW = 0).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	XA4	XA3	XA2	XA1	XA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	0	0	0	0	0

4.5 Y Address Register (R4)

The Y address register specifies the Y address in the display RAM accessed by the CPU. This address is automatically incremented each time the display RAM is accessed (INC = 1, RMW = 0).

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	YA6	YA5	YA4	YA3	YA2	YA1	YA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.6 Duty Setting Register (R5)

The display duty can be set to any duty ratio between 1/1 and 1/128, as is shown in Table 4-4.

Before modifying this register, be sure to use the HALT command (control register 1 (R0)) to stop internal operations.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	DT6	DT5	DT4	DT3	DT2	DT1	DT0

Table 4-4. Duty Setting Register (R5) Settings

DT6	DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	0	0	0	0	1/1
0	0	0	0	0	0	1	1/2
0	0	0	0	0	1	0	1/3
0	0	0	0	0	1	1	1/4
			:				:
1	1	1	1	1	0	1	1/126
1	1	1	1	1	1	0	1/127
1	1	1	1	1	1	1	1/128

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	1	1	1	1	1	1	1

4.7 AC Driver Inversion Cycle Register (R6)

The AC driver's line position for normal display mode can be set as shown in Table 4-5.

When a DTYn value is changed in the duty setting register (R5), the NIDn value is automatically overwritten by the DTYn value.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	NID6	NID5	NID4	NID3	NID2	NID1	NID0

Table 4-5. AC Driver Inversion Cycle Register (R6) Settings

NID6	NID5	NID4	NID3	NID2	NID1	NID0	Inversion Line
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
			:				:
1	1	1	1	1	0	1	126
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	1	1	1	1	1	1	1

4.8 AC Driver Inversion Position Shift Register (R7)

This shifts the inversion position for each frame in normal display mode by the shift amount shown in Table 4-6.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0

Table 4-6. AC Driver Inversion Position Shift Register (R7) Settings

MSD5	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
			:				:
1	1	1	1	1	0	1	125
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.9 Partial AC Driver Inversion Cycle Register (R8)

The AC driver's line position can be set as shown in Table 4-7.

When a PDTn value is changed in the partial display mode setting register (R10), the PIDn value is automatically overwritten by the PDTn value.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	PID5	PID4	PID3	PID2	PID1	PID0

Table 4-7. Partial AC Driver Inversion Cycle Register (R8) Settings

PID5	PID4	PID3	PID2	PID1	PID0	Inversion Line
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
			:			:
1	0	0	0	1	1	36
1	0	0	1	0	0	37
1	0	0	1	0	1	38

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	1	0	0	1	0	1

4.10 Partial AC Driver Inversion Position Shift Register (R9)

This shifts the inversion position for each frame by the shift amount shown in Table 4-8.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	PSD5	PSD4	PSD3	PSD2	PSD1	PSD0

Table 4-8. Partial AC Driver Inversion Position Shift Register (R9) Settings

PSD5	PSD4	PSD3	PSD2	PSD1	PSD0	Inversion Position Shift Amount
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
		:				:
1	0	0	0	1	1	35
1	0	0	1	0	0	36
1	0	0	1	0	1	37

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	0	0	0	0	0

4.11 Partial Display Mode Setting (R10)

This command specifies the operation mode to be used in the μPD16686, 16687's partial display mode.

Before modifying this register, be sure to use the HALT command (control register 1 (R0)) to stop internal operations.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	PBIS	-	PDT1	PDT0

PBIS	Sets bias level for partial display mode 0: 1/5 bias 1: 1/6 bias		
PDT1, PDT0	PDT1	PDT0	Duty in partial display mode
	0	0	1/38 duty
	0	1	1/25 duty
	1	0	1/12 duty
	1	1	Prohibited

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	0	-	0	0

4.12 Display Memory Access Register (R11)

The display memory access register is used when accessing the display RAM. When this register is write-accessed, data is written directly to the display RAM. When this register is read-accessed, data from the display RAM is first latched to this register before being sent to the bus during the next read operation. Accordingly, one dummy read access is required after display RAM access has been set.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	-	-	-	-

4.13 Display Start Line Set (R12)

Display start line set specifies the top line in the display.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	DSL6	DSL5	DSL4	DSL3	DSL2	DSL1	DSL0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.14 Blink X Address Register (R13)

The blink X address register specifies the X address of the blink data RAM accessed by the CPU. This address is automatically incremented each time the blink data RAM is accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	BXA3	BXA2	BXA1	BXA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	0	0	0	0

4.15 Blink Start Line Address Register (R14)

The blink start line address register specifies the start line address of the display RAM accessed when the CPU uses blink display mode. The range of blinking lines is determined based on the contents of this register and the blink end line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	-	BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.16 Blink End Line Address Register (R15)

The blink end line address register specifies the end line address of the display RAM accessed when the CPU uses blink display mode. The range of blinking lines is determined based on the contents of this register and the blink start line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	-	BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.17 Blink Data Memory (R16)

The blink data memory access register is used to access the blink data RAM. When this register is write-accessed, data is written directly to the blink data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Data	Status
0	Normal
1	Blink

Default settings (initial values set by reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.18 Inverted X Address Register (R17)

The inverted X address register specifies the X address in the inverted data RAM accessed by the CPU. This address is incremented each time the inversion RAM is accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	IXA3	IXA2	IXA1	IXA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	0	0	0	0

4.19 Inversion Start Line Address Register (R18)

The inversion start line address register specifies the start line address in the display RAM accessed by the CPU when using reverse (inverted) display mode. The range of inverted lines is determined based on the contents of this register and the inversion end line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	ISL6	ISL5	ISL4	ISL3	ISL2	ISL1	ISL0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.20 Inversion End Line Address Register (R19)

The inversion end line address register specifies the end line address in the display RAM accessed by the CPU when using reverse (inverted) display mode. The range of inverted lines is determined based on the contents of this register and the inversion start line address register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	-	IEL6	IEL5	IEL4	IEL3	IEL2	IEL1	IEL0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.21 Inverted Data Memory (R20)

The inverted data memory access register is used when accessing the inverted data RAM. When this register is accessed, the data is written directly to the inverted data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-

Data	Status
0	Normal
1	Inverted

Default settings (initial values set by reset command, all data)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.22 Partial Start Line Address Register (R21)

The partial start line address register specifies the start line address in the display RAM accessed by the CPU when using partial display mode. The partial display area is determined as the number of lines specified in the partial display mode setting register (R10), starting from this start line address.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	-	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	0	0	0	0

4.23 Gray Scale Data Registers 1 to 4 (R23, R24, R25, R26)

The gray scale data registers specify the gray scale level when using normal four-level gray scale display mode. Use of this register optimizes the gray scale display.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R23	0, 0	1	-	-	GD5	GD4	GD3	GD2	GD1	GD0	
R24	0, 1	1	-	-	GD5	GD4	GD3	GD2	GD1	GD0	
R25	1, 0	1	-	-	GD5	GD4	GD3	GD2	GD1	GD0	
R26	1, 1	1	-	-	GD5	GD4	GD3	GD2	GD1	GD0	

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Gray scale level
Disable	Disable	0	0	0	0	0	0	Level 0
Disable	Disable	0	0	0	0	0	1	Level 1
Disable	Disable	0	0	0	0	1	0	Level 2
Disable	Disable	0	0	0	0	1	1	Level 3
			:					:
Disable	Disable	0	1	1	1	1	1	Level 31
Disable	Disable	1	0	0	0	0	0	Level 32

Default settings (initial values set by reset command, for all gray scale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	0	0	0	0	0	0

4.24 Partial Gray Scale Data Registers 1 to 4 (R27, R28, R29, R30)

The partial gray scale data registers specify the gray scale level when using partial four-level gray scale display mode. Use of this register optimizes the gray scale display.

Rx	Data	RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
R23	0, 0	1	-	-	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	-
R24	0, 1	1	-	-	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	-
R25	1, 0	1	-	-	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	-
R26	1, 1	1	-	-	PGD5	PGD4	PGD3	PGD2	PGD1	PGD0	-

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Gray scale level
Disable	Disable	0	0	0	0	0	0	Level 0
Disable	Disable	0	0	0	0	0	1	Level 1
Disable	Disable	0	0	0	0	1	0	Level 2
Disable	Disable	0	0	0	0	1	1	Level 3
			:					:
Disable	Disable	0	1	1	1	1	1	Level 31
Disable	Disable	1	0	0	0	0	0	Level 32

Default settings (initial values set by reset command, for all partial gray scale data registers)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	0	0	0	0	0	0

4.25 Power System Control 1 (R32)

This command sets the μPD16686, 16687's power system mode.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	HPM1	HPM0	-	TCS2	TCS1	OP2	OP1	OP0

HPM1, HPM0	These bits set the driver mode as shown in Table 4-9.
TCS1, TCS0	These bits set the value for selecting the V_{REG} voltage's temperature curve, as shown in Table 4-10.
OP2, OP1, OP0	These bits control the booster's ON/OFF status, the voltage regulator (V regulator) and voltage follower (V/F). The functions controlled via these three bits by the power control setting command are listed in Table 4-11.

Table 4-9. Driver Mode Setting

HPM1	HPM0	Mode Setting
0	0	Normal mode
0	1	Low-power mode
1	0	High-power mode
1	1	Power activation mode

Table 4-10. Selection V_{REG} Voltage's Temperature Curve Value

TCS1	TCS0	Temperature gradient	Unit	V_{REG} (TYP.)	Unit
0	0	–0.09	%, °C	0.88	V
0	1	–0.11		0.80	
1	0	–0.12		0.75	
1	1	external inputs		-	

Table 4-11. Detailed Description of Functions Controlled by Bits of Power System Control 1

Item		Status 1	Status 0
OP2	Booster control bit	ON	OFF
OP1	V regulator control bit	ON	OFF
OP0	Voltage follower control bit	ON	OFF

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	-	0	0	1	1	1

4.26 Power System Control 2 (R33)

This command sets the μPD16686, 16687's power system mode.

RS	E /RD	R,/W /WR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	1	0	-	VRR2	VRR1	VRR0	-	PVR2	PVR1	PVR0	-

VRR2, VRR1, VRR0	When using normal display mode, power system control 2 (V_{LCD} regulator resistance factor setting command) can be used to change the resistance factor at 8 levels. The three bits in power system control 2 set the values shown in Table 4-12 as reference values for (1 + Rb/Ra).
PVR2, PVR1, PVR0	When using partial display mode, power system control 2 (V_{LCD} regulator resistance factor setting command) can be used to change the resistance factor at 8 levels. The three bits in power system control 2 set the values shown in Table 4-12 as reference values for (1 + Rb/Ra).

Table 4-12. Reference Values for V_{LCD} Internal Resistance Factor Regulator Register

Register			1+Rb/Ra
VRR2	VRR1	VRR0	
PVR2	PVR1	PVR0	
0	0	0	5
0	0	1	8
0	1	0	12
0	1	1	13
1	0	0	16
1	0	1	19
1	1	0	21
1	1	1	24

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	0	0	0	-	0	0	0

4.27 Power System Control 3 (R34)

This command sets the power system mode, including the bias setting for the μPD16686, 16687's normal display mode and the number of boost levels for partial display mode.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	BIS2	BIS1	BIS0	FBS2	FBS1	FBS0	BST1	BST0	-

BIS2, BIS1, BIS0[Note]

These three flags select the bias ratio as shown below.

BIS2	BIS1	BIS0	Boost level
0	0	0	1/12 bias
0	0	1	1/11 bias
0	1	0	1/10 bias
0	1	1	1/9 bias
1	0	0	1/8 bias
1	0	1	1/7 bias
1	1	0	Prohibited
1	1	1	Prohibited

When partial display mode is set, the bias ratio set by the partial mode setting is automatically selected.

FBS2, FBS1, FBS0[Note]

The number of boost levels in booster for normal display mode is selected as shown below.

FBS2	FBS1	FBS0	Boost level
0	0	0	x4
0	0	1	x5
0	1	0	x6
0	1	1	x7
1	0	0	x8
1	0	1	x9
1	1	0	Prohibited
1	1	1	Prohibited

BST1, BST0

The number of boost levels in the booster for partial display mode is selected as shown below.

BST1	BST0	Boost level
0	0	x2
0	1	x3
1	0	x4
1	1	Prohibited

Note Be sure to execute the HALT command before changing these flag settings.

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.28 Electronic Volume Register (R35)

The electronic volume register specifies the electronic volume value for adjusting the contrast when using normal display mode. Any value among 256 steps can be selected.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.29 Partial Electronic Volume Register (R36)

The partial electronic volume register specifies the electronic volume value for adjusting the contrast when using partial display mode. Any value among 256 steps can be selected.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0	-

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0

4.30 Boost Adjustment Register (R37)

The voltage (range: 1/8 V_{DD2} to 7/8 V_{DD2}) set to this register is applied to the boost level set for the booster.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting
1	-	-	-	-	-	DDC2	DDC1	DDC0	-

Table 4-13. Boost Adjustment Register (R37) Settings

DDC2	DDC1	DDC0	Boost Adjustment Voltage
0	0	0	Regulator Circuit Stopped
0	0	1	1/8 V_{DD2}
0	1	0	2/8 V_{DD2}
0	1	1	3/8 V_{DD2}
1	0	0	4/8 V_{DD2}
1	0	1	5/8 V_{DD2}
1	1	0	6/8 V_{DD2}
1	1	1	7/8 V_{DD2}

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	-	0	0	0

4.31 Static Icon Address (R40)

The static icon address specifies the address in the static icon data RAM accessed by the CPU.

This address is automatically incremented each time the static icon data RAM is accessed.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	-	SIA2	SIA1	SIA0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	-	0	0	0

4.32 Static Icon Data Register (R41)

The static icon data register is used when accessing the static icon data RAM. When this register is write-accessed, the data is written directly to the static icon data RAM.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	-	-	-	-

4.33 Static Icon Contrast (R42)

The static icon contrast adjusts the contrast of static icons using phase modulation.

The pulse width of the ON signal that is output in static drive mode is divided into 32 levels (1/32 to 32/32 pulse width) and the dot output's timing changes during output according to the phase modulation ratio recorded in bits ICS4 to ICS0 of the static icon contrast (R42), as is shown in Table 4-14.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	0	ICS3	ICS2	ICS1	ICS0

★

Table 4-14. Static Icon Contrast (R42) Setting

ICS4	ICS3	ICS2	ICS1	ICS0	Phase Modulation Ratio
0	0	0	0	0	0/32
0	0	0	0	1	1/32
0	0	0	1	0	2/32
0	0	0	1	1	3/32
		:			:
1	1	1	0	1	29/32
1	1	1	1	0	30/32
1	1	1	1	1	31/32

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	0	0	0	0

4.34 RAM Test Mode Setting (R44)

The RAM test mode setting register directly writes the data for each type of display mode to the display RAM, as shown in Table 4-15.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	RTS3	RTS2	RTS1	RTS0

Table 4-15. RAM Test Mode Setting (R44)

RTS3	RTS2	RTS1	RTS0	Write Data
0	0	0	0	Normal operation
0	1	0	0	Displays list of gray scales
1	0	0	0	all 00/pixel
1	0	0	1	all 11/pixel
1	0	1	0	Checker pattern: 00/11
1	0	1	1	Checker pattern: 11/00
1	1	0	0	Checker pattern: 01/10
1	1	0	1	Checker pattern: 10/01
1	1	1	0	Vertical striped pattern: 00/11
1	1	1	1	Horizontal striped pattern: 00/11

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	0	0	0	0

4.35 Signature Read (R45)

This commnad is used to read the IC signature set via the SIGIN1 and SIGIN2 pins. This is a read-only register.

RS	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	-	-	-	-	-	-	SIGIN2	SIGIN1

Default settings (initial values set by reset command)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
-	-	-	-	-	-	-	-

5. LIST OF μPD16686, 16687 REGISTERS

CS	RS	Index Register 5	4	3	2	1	0	Register Name		R/W	Data Bits 7	6	5	4	3	2	1	0
1																		
0	0							IR	Index Register	W			IR5	IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	0	R0	Control register 1	R/W	RMW	DISP	STBY	BLD	IVD	HALT	ADC	COMR
0	1	0	0	0	0	0	1	R1	Control register 2	R/W	FDM	IBL	IDIS	DSEL	BWW	GRAY	DTY	INC
0	1	0	0	0	0	1	0	R2	Reset command	W								CRES
0	1	0	0	0	0	1	1	R3	X address register	R/W				XA4	XA3	XA2	XA1	XA0
0	1	0	0	0	1	0	0	R4	Y address register	R/W		YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	0	1	0	1	R5	Duty setting register	R/W		DT6	DT5	DT4	DT3	DT2	DT1	DT0
0	1	0	0	0	1	1	0	R6	AC driver inversion cycle register	R/W		NID6	NID5	NID4	NID3	NID2	NID1	NID0
0	1	0	0	0	1	1	1	R7	AC driver inversion position shift register	W		MSD6	MSD5	MSD4	MSD3	MSD2	MSD1	MSD0
0	1	0	0	1	0	0	0	R8	Partial AC driver inversion cycle register	W				PID4	PID3	PID2	PID1	PID0
0	1	0	0	1	0	0	1	R9	Partial AC driver inversion potision shift register	W				PSD4	PSD3	PSD2	PSD1	PSD0
0	1	0	0	1	0	1	0	R10	Partial display mode setting	R/W					PBIS		PDT1	PDT0
0	1	0	0	1	0	1	1	R11	Display memory access register	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	1	0	0	R12	Display start line set	W		DSL6	DSL5	DSL4	DSL3	DSL2	DSL1	DSL0
0	1	0	0	1	1	0	1	R13	Blink X address register	R/W					BXA3	BXA2	BXA1	BXA0
0	1	0	0	1	1	1	0	R14	Blink start line address register	R/W		BSL6	BSL5	BSL4	BSL3	BSL2	BSL1	BSL0
0	1	0	0	1	1	1	1	R15	Blink end line address register	R/W		BEL6	BEL5	BEL4	BEL3	BEL2	BEL1	BEL0
0	1	0	1	0	0	0	0	R16	Blink data memory	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	0	1	R17	Inverted X address register	R/W					IXA3	IXA2	IXA1	IXA0
0	1	0	1	0	0	1	0	R18	Inversion start line address register	R/W		ISL6	ISL5	ISL4	ISL3	ISL2	ISL1	ISL0
0	1	0	1	0	0	1	1	R19	Inversion end line address register	R/W		IEL6	IEL5	IEL4	IEL3	IEL2	IEL1	IEL0
0	1	0	1	0	1	0	0	R20	Inverted data memory	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	R21	Partial start line address register	W		PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
0	1	0	1	0	1	1	0	R22										
0	1	0	1	0	1	1	1	R23	Gray scale data register 1 (0, 0)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	0	0	R24	Gray scale data register 2 (0, 1)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	0	1	R25	Gray scale data register 3 (1, 0)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	1	0	R26	Gray scale data register 4 (1, 1)	W			GD5	GD4	GD3	GD2	GD1	GD0
0	1	0	1	1	0	1	1	R27	Patial gray scale data register 1 (0, 0)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	0	0	R28	Patial gray scale data register 2 (0, 1)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	0	1	R29	Patial gray scale data register 3 (1, 0)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	1	0	R30	Patial gray scale data register 4 (1, 1)	W			PGD5	PGD4	PGD3	PGD2	PGD1	PGD0
0	1	0	1	1	1	1	1	R31										
0	1	1	0	0	0	0	0	R32	Power system control 1	W	HPM1	HPM0		TCS1	TSC0	OP2	OP1	OP0
0	1	1	0	0	0	0	1	R33	Power system control 2	W		VRR2	VRR1	VRR0		PVR2	PVR1	PVR0
0	1	1	0	0	0	1	0	R34	Power system control 3	W	BIS2	BIS1	BIS0	FBS2	FBS1	FBS0	BST1	BST0
0	1	1	0	0	0	1	1	R35	Electronic volume register	W	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0
0	1	1	0	0	1	0	0	R36	Partial electronic volume register	W	PEV7	PEV6	PEV5	PEV4	PEV3	PEV2	PEV1	PEV0
0	1	1	0	0	1	0	1	R37	Boost adjustment register	W						DDC2	DDC1	DDC0
0	1	1	0	0	1	1	0	R38										
0	1	1	0	0	1	1	1	R39										
0	1	1	0	1	0	0	0	R40	Static icon address	W						SIA2	SIA1	SIA0
0	1	1	0	1	0	0	1	R41	Static icon data register	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	1	0	1	0	R42	Static icon contrast	W				ICS4	ICS3	ICS2	ICS1	ICS0
0	1	1	0	1	0	1	1	R43										
0	1	1	0	1	1	0	0	R44	RAM test mode setting	W					RTS3	RTS2	RTS1	RTS0
0	1	1	0	1	1	0	1	R45	Signature read	R							SIG2	SIG1
0	1	1	0	1	1	1	0	R46										
0	1	1	0	1	1	1	1	R47										
0	1	1	1	0	0	0	0	R48										
0	1	1	1	0	0	0	1	R49										
0	1	1	1	0	0	1	0	R50										
0	1	1	1	0	0	1	1	R51										
0	1	1	1	0	1	0	0	R52										
0	1	1	1	0	1	0	1	R53										
0	1	1	1	0	1	1	0	R54										
0	1	1	1	0	1	1	1	R55										
0	1	1	1	1	0	0	0	R56										
0	1	1	1	1	0	0	1	R57										
0	1	1	1	1	0	1	0	R58										
0	1	1	1	1	0	1	1	R59										
0	1	1	1	1	1	0	0	R60										
0	1	1	1	1	1	0	1	R61										
0	1	1	1	1	1	1	0	R62										
0	1	1	1	1	1	1	1	R63										

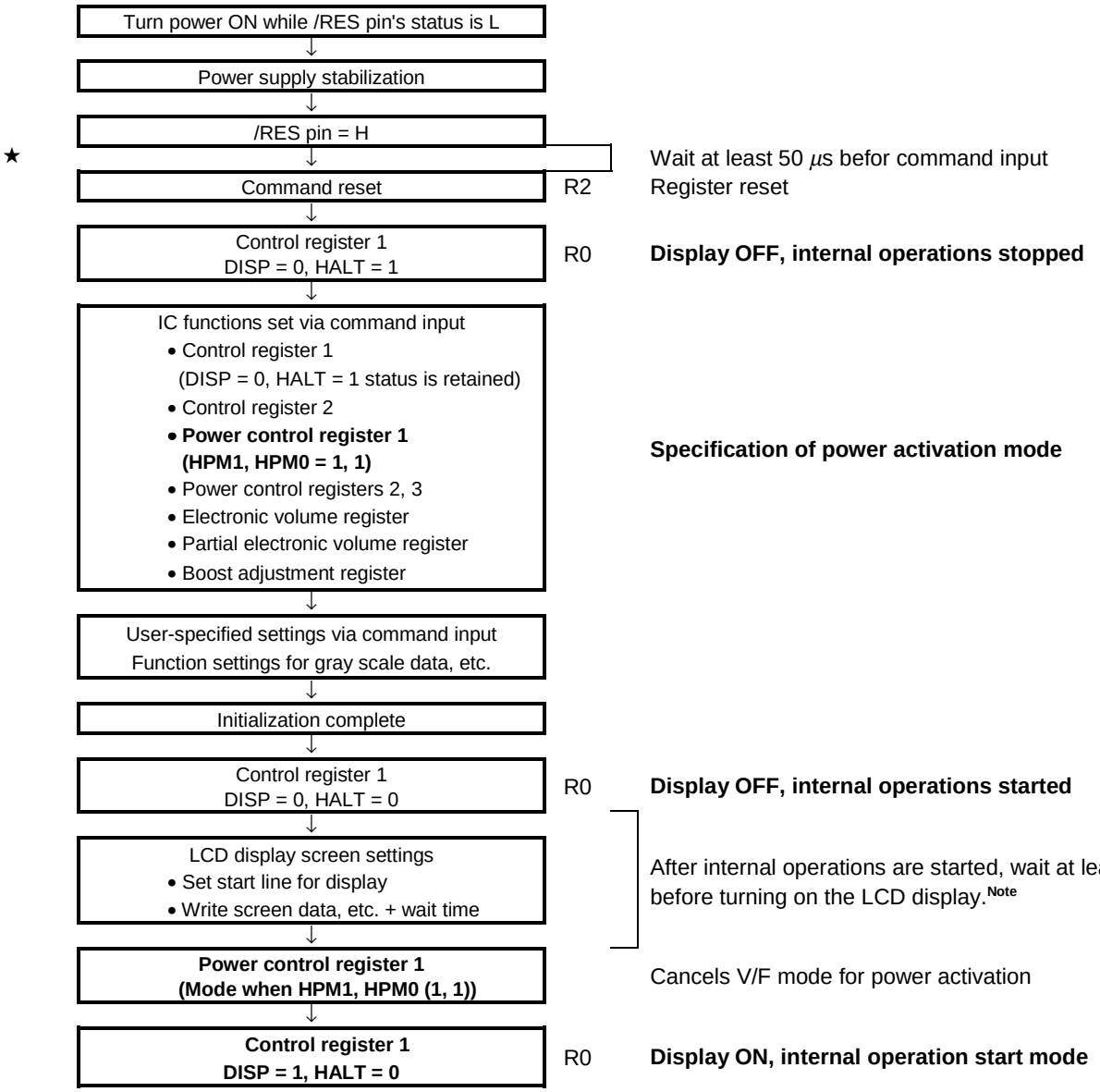
Remark : Not to use these registers.

6. POWER SUPPLY SEQUENCE

The μPD16686, 16687 includes power supply circuitry, such as a booster and a voltage follower. When a reset is performed using the /RES pin, the reset function is restricted so as to prevent operation faults that may occur due to noise effects, etc.

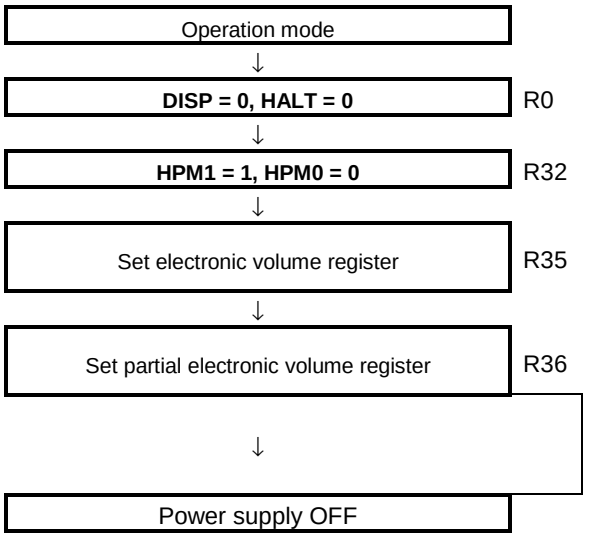
When electric charge remains in the smoothing capacitor that is connected between the V_{SS} pin and the voltage pins related to the LCD driver (V_{LCD} to V_{LC4}), abnormalities such as a brief all-black display screen may occur when the power is switched ON or OFF. The following power-on sequence is recommended as a means to avoid such abnormalities when switching the power ON or OFF.

6.1 Power ON Sequence (When Using On-Chip Power Supply, Power Supply ON → Display ON)



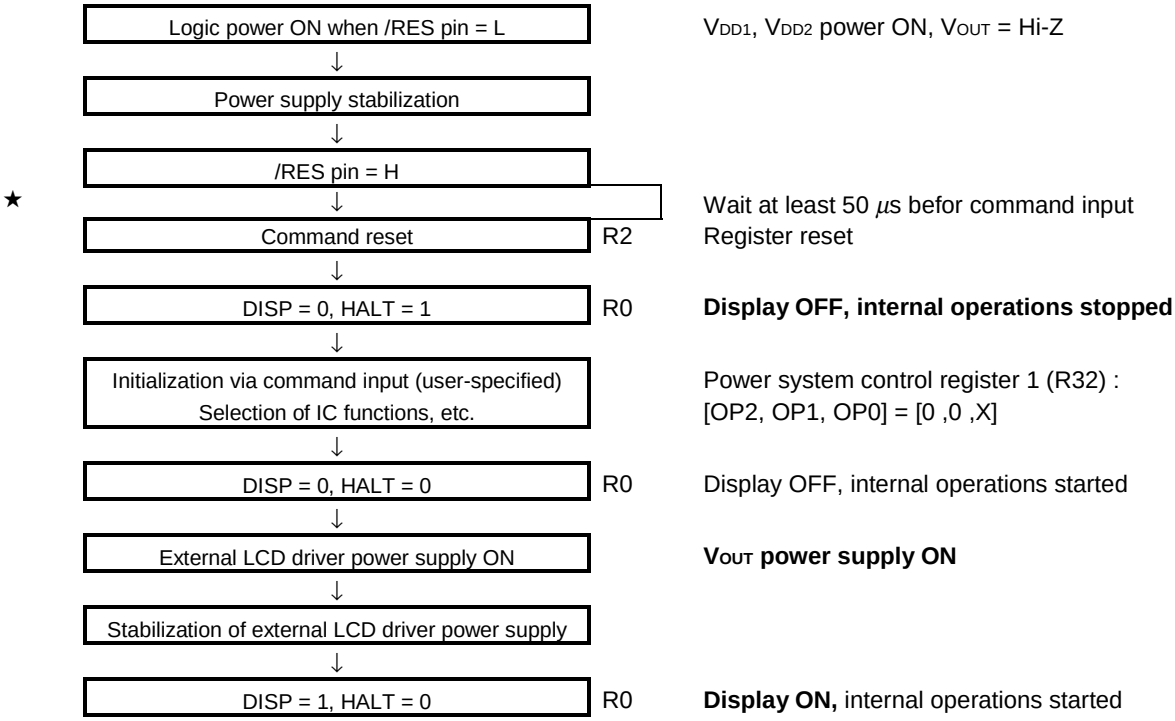
Note This 400 ms wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommend determining the wait time after making a thorough evaluation of the actual device (refer to 6.5 V_{OUT}, V_{LCD} Voltage Sequence (Power ON → Power OFF)).

6.2 Power OFF Sequence (When Using On-Chip Power Supply)

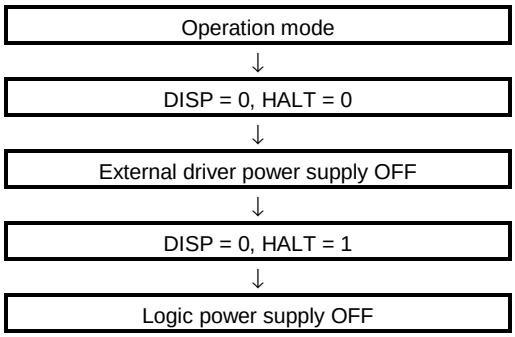


Note This 1200 ms wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. NEC recommends determining the wait time after making a thorough evaluation of the actual device (refer to 6.5 V_{OUT}, V_{LCD} Voltage Sequence (power ON → power OFF)).

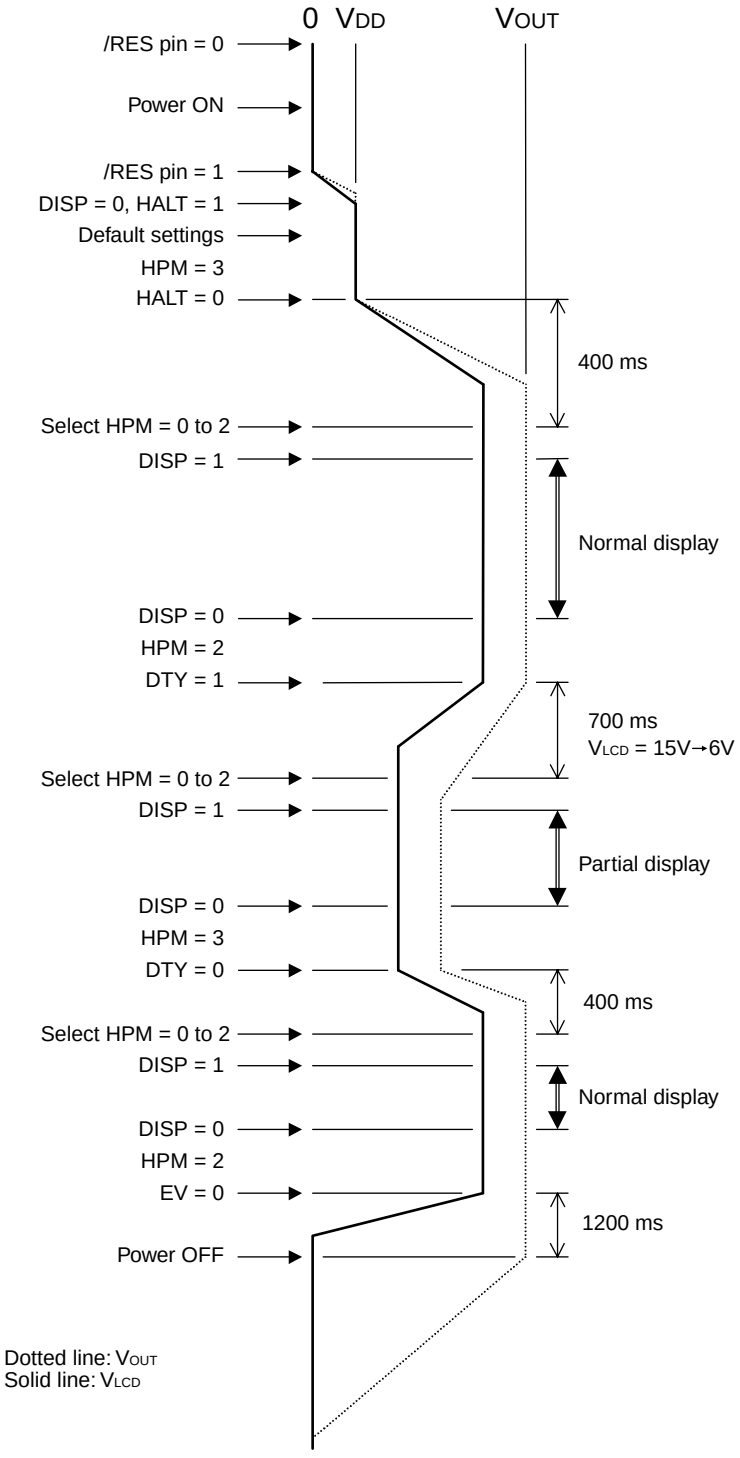
6.3 Power ON Sequence (When Using External Driver Power Supply, Power ON → Display ON)



6.4 Power Supply OFF Sequence (When Using External Driver Power Supply)



6.5 V_{OUT}, V_{LCD} Voltage Sequence (Power ON → Power OFF)



Conditions:

V_{DD}: $V_{DD1} = V_{DD2} = 3.0$ V

Boost levels: x6 (in normal display mode), x3 (in partial display mode)

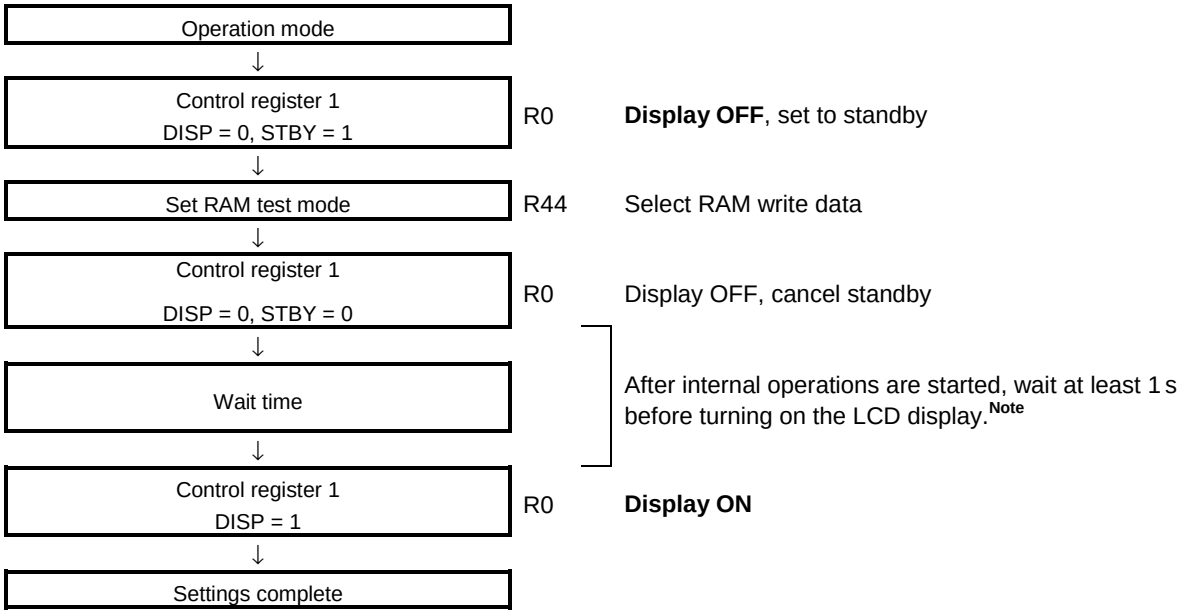
Capacitors: VLCn pin to $C^{+}/^{-}$ pin = 1 μF,

AMP_{OUT} pin, AMP_{OUTP} pin, V_{RS} pin = 0.1 μF

Caution Connect a 0.1 μF capacitor to the AMP_{OUT}, and AMP_{OUTP} pins.

7. USE OF RAM TEST MODE

The μPD16686, 16687 has a test mode for writing nine types of screen data to display RAM. When using the test mode, be sure to execute via the sequence shown below. If executing the test mode by some other sequence, abnormalities may appear in the screen display.

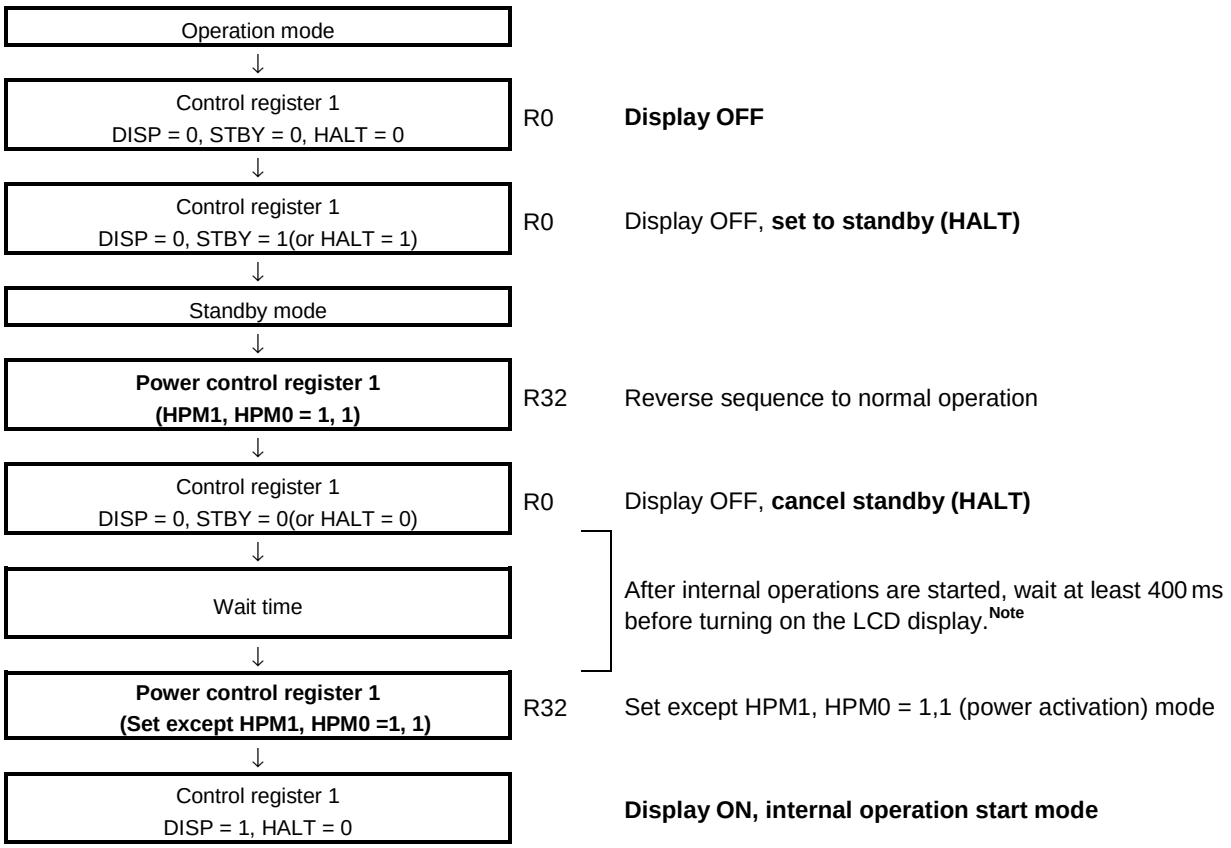


Note This 1 s wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. NEC recommends determining the wait time after making a thorough evaluation of the actual device.

8. USE OF STANDBY/HALT MODE

The μPD16686, 16687 has a standby mode for reducing current consumption, and a HALT mode for switching display mode. Electrical circuits as a DC/DC converter are stopped in standby/HALT mode.

When using the standby/HALT mode, be sure to execute via the sequence shown below. If executing the test mode by some other sequence, abnormalities may appear in the screen display.



Note This 400 ms wait time varies according to the panel characteristics and the capacitance value of the boost/smoothing capacitor. We recommends determining the wait time after making a thorough evaluation of the actual device.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic system supply voltage	V_{DD1}	–0.3 to +4.0	V
Booster supply voltage	V_{DD2}	–0.3 to +4.0	V
Driver supply voltage	V_{OUT}	–0.3 to +20.0	V
Driver reference supply input voltage	V_{LCD}, V_{LC1} to V_{LC4}	–0.3 to V_{OUT}+0.3	V
Logic system input voltage	V_{IN1}	–0.3 to V_{DD1}+0.3	V
Logic system output voltage	V_{OUT1}	–0.3 to V_{DD1}+0.3	V
Logic system input/output voltage	$V_{I/O1}$	–0.3 to V_{DD1}+0.3	V
Driver system input voltage	V_{IN2}	–0.3 to V_{OUT}+0.3	V
Driver system output voltage	V_{OUT2}	–0.3 to V_{OUT}+0.3	V
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic system supply voltage	V_{DD1}	1.7		3.6	V
Booster supply voltage	V_{DD2} **Note1**	2.4		3.6	V
Driver supply voltage	V_{OUT} **Note2**	5.5		18.0	V
Logic system input voltage	V_{IN}	0		V_{DD1}	V
Driver system supply voltage	V_{LCD}, V_{LC1} to V_{LC4} **Note2**	0		V_{OUT}	V
Maximum setting for LCD driver voltage	V_{LCD} **Note3**			V_{OUT} – 0.5	V

Notes 1. V_{DD1} must be less than or equal to V_{DD2}

2. This item is the recommended parameter when the LCD has an external driver.

3. This item is the recommended parameter when the LCD is driven by an on-chip power supply circuit.

Cautions 1. When using an external LCD driver, be sure to maintain these relations:

$V_{SS} < V_{LC4} < V_{LC3} < V_{LC2} < V_{LC1} < V_{LCD} \leq V_{OUT}$.

2. Maintain the relations shown in **6. POWER SUPPLY SEQUENCE** when turning the power on or off.

3. When using an external resister (when not using an on-chip resister for V_{LCD} adjustment), maintain supply of a voltage between 1.0 V and the V_{DD1} voltage to the V_R and V_{RS} pins.

Electrical Characteristics 1

(Unless Otherwise Specified, T_A = −40 to +85°C, V_{DD1} = 1.7 to 3.6 V, V_{DD2} = 2.4 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.[Note1]	MAX.	Unit
Input voltage, high	V_{IH}		0.8 V_{DD1}			V
Input voltage, low	V_{IL}				0.2 V_{DD1}	V
Input current, high	I_{IH1}	Except for D_7 (SI), D_6 (SCL) and D_5 to D_0			1	μA
Input current, low	I_{IL1}	Except for D_7 (SI), D_6 (SCL) and D_5 to D_0			1	μA
Output voltage, high	V_{OH}	I_{OUT} = −1 mA except OSC_{OUT}	V_{DD1}−0.5			V
Output voltage, low	V_{OL}	I_{OUT} = 1 mA except OSC_{OUT}			0.5	V
Leakage current, high	I_{LOH}	D_7 (SI), D_6 (SCL) and D_5 to D_0, $V_{IN/OUT}$ = V_{DD1}			10	μA
Leakage current, low	I_{LOL}	D_7 (SI), D_6 (SCL) and D_5 to D_0, $V_{IN/OUT}$ = V_{SS}			−10	μA
Common output ON resistance	R_{COM}	V_{LCn} → COM_n, V_{OUT} = 15 V, V_{LCD} = 13 V, 1/10 bias, $\|I_O\|$ = 50 μA			4	kΩ
Segment output ON resistance	R_{SEG}	V_{LCn} → SEG_n, V_{OUT} = 15 V, V_{LCD} = 13 V, 1/10 bias, $\|I_O\|$ = 50 μA			4	kΩ
Driver voltage (boost voltage)	V_{OUT}	In x5 boost mode, V_{DD} = 3.0 V, Checker pattern display	13.8			V
		In x6 boost mode, V_{DD} = 3.0 V, Checker pattern display	16.6			V
Oscillation frequency	f_{OSC}[Note2]	V_{DD1} = 3.0 V, T_A = 25°C, 1/38 duty, in B/W mode, R = 750 kΩ		36		kHz
		V_{DD1} = 3.0 V, T_A = 25°C, 1/38 duty, in B/W mode, R = 3 MΩ		10.6		kHz

Notes 1. TYP. values are reference values when T_A = 25°C.

2. This time varies according to the parasitic capacitance of the wiring capacitance, etc. We therefore recommend determining the oscillation resister's value after making a thorough evaluation of the actual device.

Electrical Characteristics 2

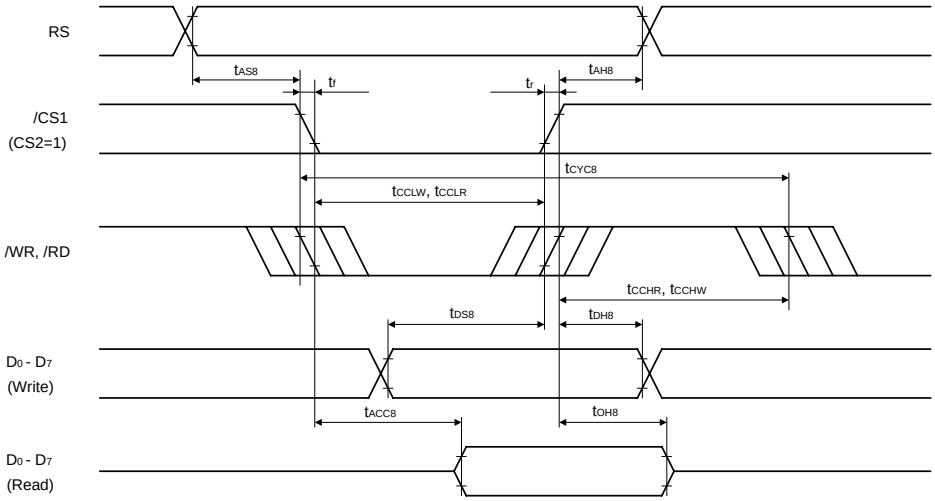
(Unless Otherwise Specified, T_A = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Current consumption (normal mode)	I_{DD11}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 13 V		180	290	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 13 V		250	390	μA
Current consumption (high-power mode)	I_{DD12}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 13 V		300	460	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode,V_{LCD} = 13 V		380	560	μA
Current consumption (low-power mode)	I_{DD13}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 13 V		135	220	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/128 duty, V_{DD1} = V_{DD2} = 3.0 V, in x5 boost mode, V_{LCD} = 13 V		210	320	μA
Current consumption (partial display mode)	I_{DD21}	Frame frequency = 70 Hz, B/W all display OFF data output, 1/38 duty, V_{DD1} = V_{DD2} = 3.0 V, in x3 boost mode, V_{LCD} = 7.0 V		95	140	μA
		Frame frequency = 70 Hz, B/W checker pattern display data output, 1/38 duty, V_{DD1} = V_{DD2} = 3.0 V, V_{LCD} = 7.0 V, in x3 boost mode		105	160	μA
Current consumption (standby mode)	I_{DD22}	V_{DD1} = V_{DD2} = 3.0 V			10	μA
Current consumption (display icon)	I_{DD23}	Icon frame frequency = 125 Hz, B/W all display OFF data output, V_{DD1} = 3.0 V		18	35	μA

Note TYP. values are reference values when T_A = 25°C.

Required Timing Conditions (Unless Otherwise Specified, T_A = −30 to +85°C)

(1) i80 CPU interface



When V_{DD1} = 1.7 V to 2.0 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		1000			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	160			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	430			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	160			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	160			ns
Data setup time	t_{DS8}	D_0 to D_7	160			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.0 to 2.5 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		600			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	240			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	120			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	120			ns
Data setup time	t_{DS8}	D_0 to D_7	120			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

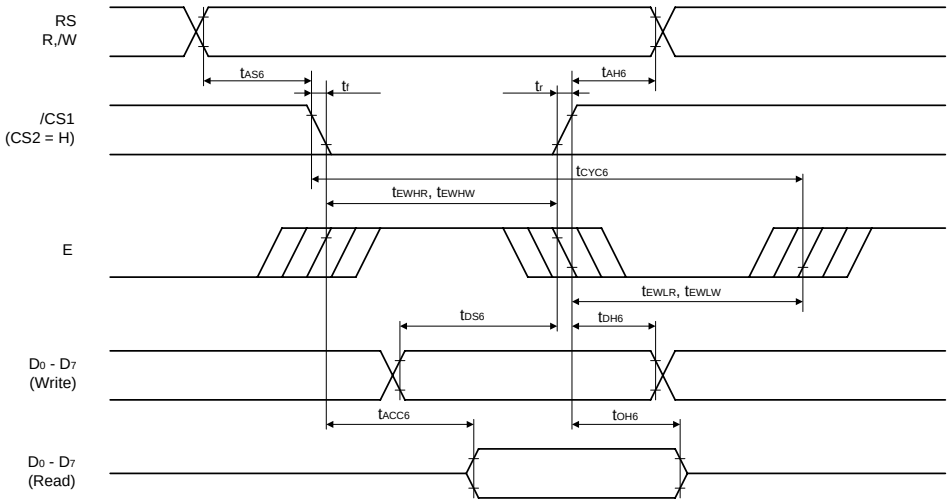
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	120			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	60			ns
Data setup time	t_{DS8}	D_0 to D_7	60			ns
Data hold time	t_{DH8}	D_0 to D_7	0			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100 pF	0		140	ns
Output disable time	t_{OH8}	D_0 to D_5, C_L = 5 pF, R = 3 kΩ	0		70	ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(2) M68 CPU interface



When V_{DD1} = 1.7 to 2.0 V

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		1000			ns
Data setup time		t_{DS6}	D_0 to D_7	160			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		470	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable high pulse width	Read	t_{EWHR}	E	430			ns
	Write	t_{EWHW}	E	160			ns
Enable low pulse width	Read	t_{EWLR}	E	160			ns
	Write	t_{EWLW}	E	160			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.0 to 2.5 V

Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		600			ns
Data setup time		t_{DS6}	D_0 to D_7	120			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		280	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		170	ns
Enable high pulse width	Read	t_{EWHR}	E	240			ns
	Write	t_{EWHW}	E	120			ns
Enable low pulse width	Read	t_{EWLR}	E	120			ns
	Write	t_{EWLW}	E	120			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

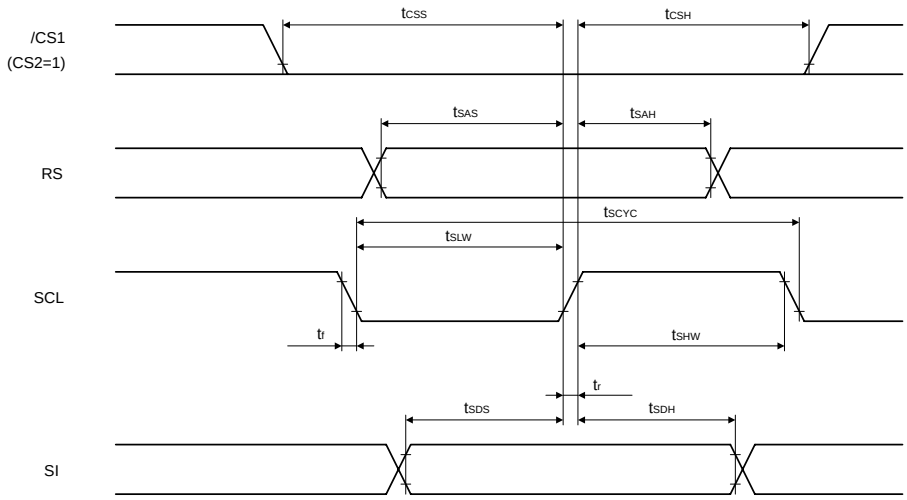
Parameter		Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		250			ns
Data setup time		t_{DS6}	D_0 to D_7	60			ns
Data hold time		t_{DH6}	D_0 to D_7	0			ns
Access time		t_{ACC6}	D_0 to D_7, C_L = 100 pF	0		140	ns
Output disable time		t_{OH6}	D_0 to D_7, C_L = 5 pF, R = 3 kΩ	0		70	ns
Enable high pulse width	Read	t_{EWHR}	E	120			ns
	Write	t_{EWHW}	E	60			ns
Enable low pulse width	Read	t_{EWLR}	E	60			ns
	Write	t_{EWLW}	E	60			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signals (t_r and t_f) are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) or ($t_r + t_f$) ≤ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$).

2. All timing is rated based on 20% or 80% of V_{DD1}.

(3) Serial interface



When V_{DD1} = 1.7 to 2.5 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	250			ns
SCL high-level pulse width	t_{SHW}	SCL	100			ns
SCL low-level pulse width	t_{SLW}	SCL	100			ns
Address hold time	t_{SAH}	RS	150			ns
Address setup time	t_{SAS}	RS	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS - SCL time	t_{CSS}	CS	150			ns
	t_{CSH}	CS	150			ns

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high-level pulse width	t_{SHW}	SCL	60			ns
SCL low-level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address setup time	t_{SAS}	RS	90			ns
Data setup time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	CS	90			ns
	t_{CSH}	CS	90			ns

Note TYP. values are reference values when T_A = 25°C.

Cautions 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(4) Common

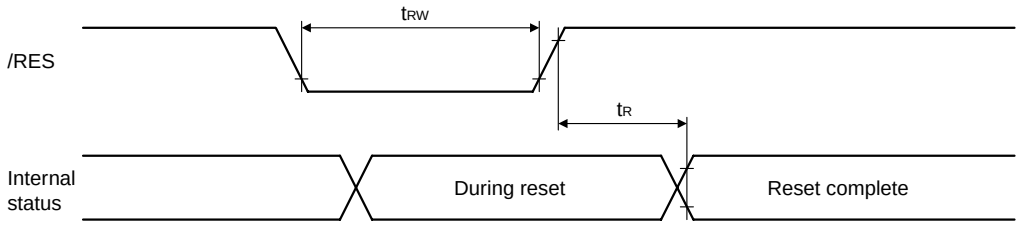
Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Clock input 1	f_N	When using OSC_{IN1}, external clock, and on-chip divider, 1/128 duty, B/W mode		36	150	kHz
		When using OSC_{IN1}, external clock, and on-chip divider, 1/128 duty, four-level gray scale mode		72	150	kHz
Clock input 2	f_P	When using OSC_{IN2}, external clock for partial display mode, but not using on-chip divider, B/W mode		10.6	50	kHz
		When using OSC_{IN2}, external clock for partial display mode, but not using on-chip divider, four-level gray scale mode		21.3	50	kHz

Note TYP. values are reference values when frame frequency = 70 Hz.

Cautions 1. The rise and fall times of input signal (tr and tf) are rated as 15 ns or less.

2. All timing is rated based on 20% or 80% of V_{DD1}.

(a) Reset timing



When V_{DD1} = 1.7 to 2.5 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset low pulse width	t_{RW}	/RES	50			μs

Note TYP. values are reference values when T_A = 25°C.

When V_{DD1} = 2.5 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.[Note]	MAX.	Unit
Reset time	t_R				50	μs
Reset low pulse width	t_{RW}	/RES	50			μs

Note TYP. values are reference values when T_A = 25°C.

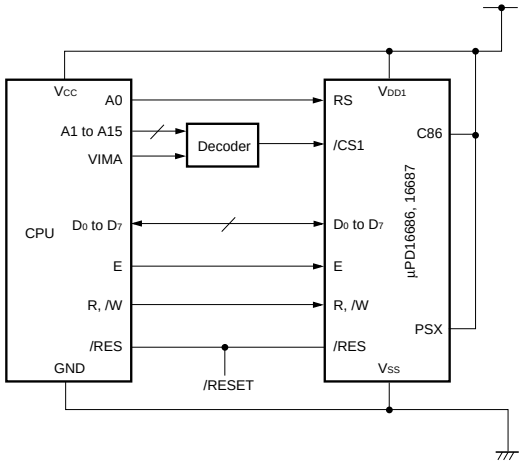
Caution All timing is rated based on 20% or 80% of V_{DD1}.

10. CPU INTERFACE (REFERENCE EXAMPLE)

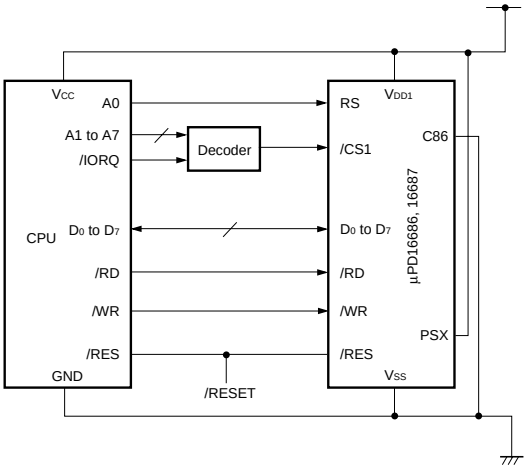
The μPD16686, 16687 can be connected to either an i80 series CPU or an M68 series CPU. Also, if a serial interface connection is used, the number of signal lines can be reduced.

If several μPD16686, 16687 chips are used, the display area can be enlarged. When using this method, use the chip select signal to select and access the ICs.

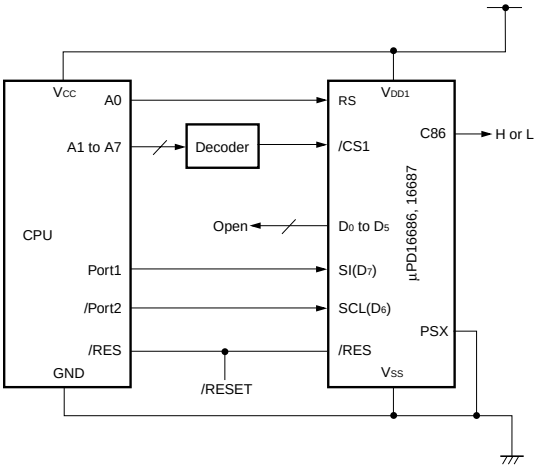
(1) M68 series CPU



(2) i80 series CPU



(3) When using serial interface



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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