DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD16675A

1/34, 1/36 DUTY LCD CONTROLLER/DRIVER

The μPD16675A is a driver containing a RAM capable of full-dot LCD display. A single μPD16675A IC chip can operate a full-dot (up to 128-by-32 dots) LCD and two-line (upper & lower) pictograph display.

This IC is ideal for Kanji character or Chinese character pagers, displaying 16-by-16 dots per character.

FEATURES

- LCD driver with built-in display RAM
- Can operate on a single 3-V power supply
- Booster circuit incorporated: Switchable between 2X & 3X
- Dot display RAM: 128 × 32 bits
- Pictographic display RAM (portion of two lines): 128 × 2 bits
- Pictographic display RAM duty changeable: 1/34 and 2/36 duties
- Output: 128 segments & 34 commons
- Data input based on serial & 4-/8-bit parallel switchover
- Split resistor incorporated
- Oscillation circuit incorporated

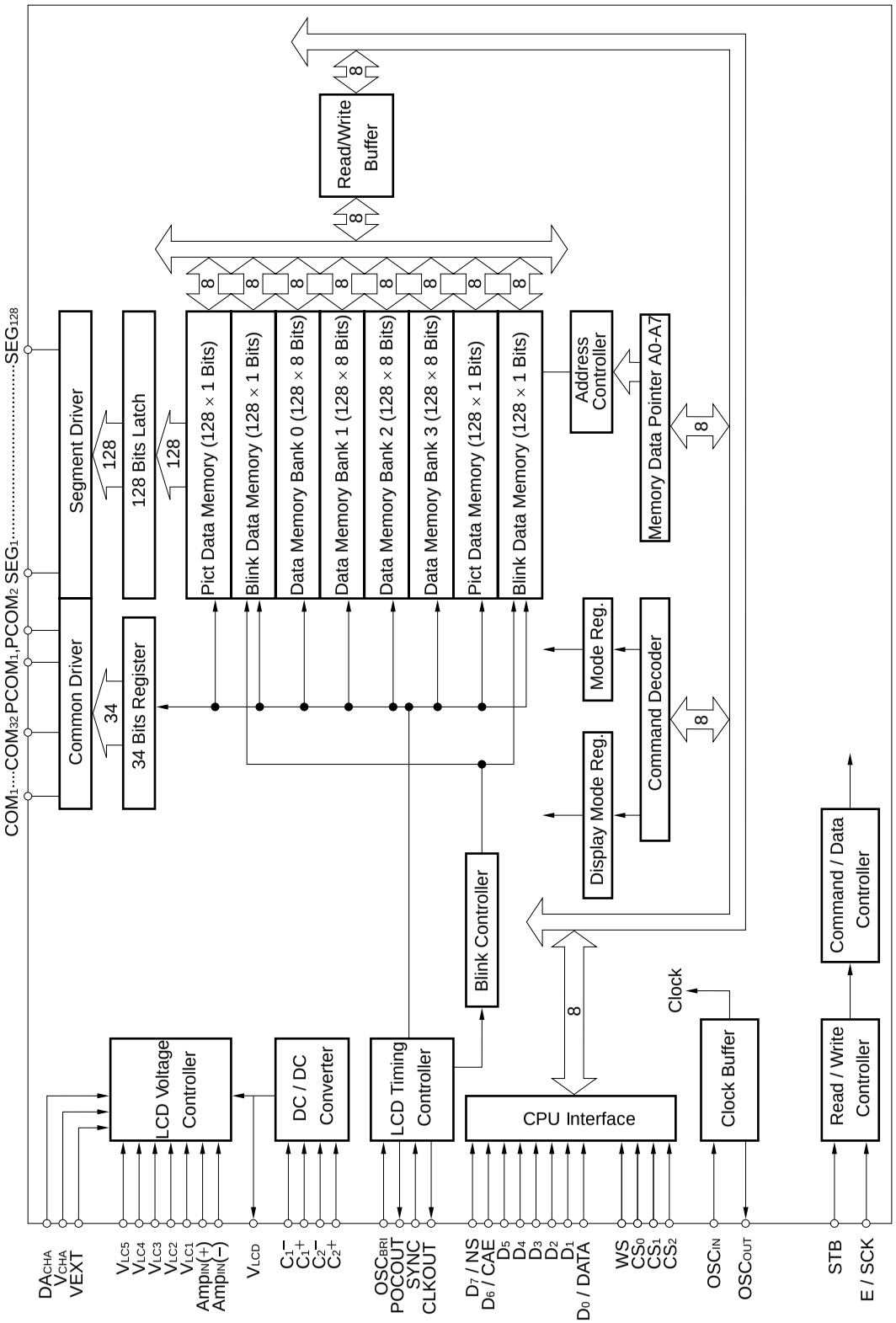
ORDERING INFORMATION

Part Number	Package
μPD16675AP/W	Chips/wafer (Matched COG mounting)
μPD16675AN-051	2-side standard TCP (Output OLB: 0.25 mm pitch)
μPD16675AN-xxx	TCP (TAB)

Purchasing the above products in terms of chips per wafer requires an exchange of other documents as well, including a memorandum on the product quality. Therefore, those who are interested in this regard are advised to contact an NEC sales representative for further details.

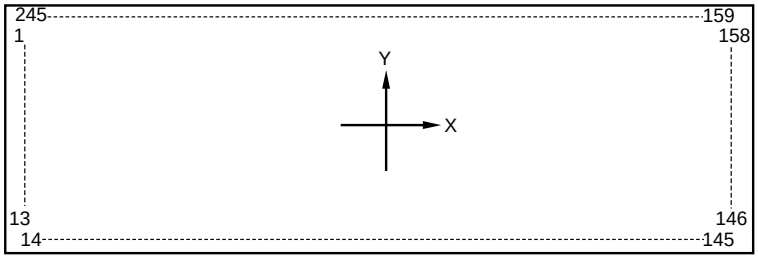
Document No. S11195EJ1V0DS00 (1st edition)
Date Published July 1998 NS CP (K)
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION (PAD LAYOUT)

(Chip size: 12.68 × 1.81 mm²)



No.	PIN	X (μm)	Y (μm)
1	DUMMY	-6094.8	516.6
2	DUMMY	-6094.8	426.6
3	COM_{22}	-6094.8	336.6
4	COM_{21}	-6094.8	246.6
5	COM_{20}	-6094.8	156.6
6	COM_{19}	-6094.8	66.6
7	COM_{18}	-6094.8	-23.4
8	COM_{17}	-6094.8	-113.4
9	DUMMY	-6094.8	-203.4
10	DUMMY	-6094.8	-293.4
11	DUMMY	-6094.8	-383.4
12	DUMMY	-6094.8	-473.4
13	DUMMY	-6094.8	-563.4
14	DUMMY	-5893.8	-661.6
15	DUMMY	-5803.8	-661.6
16	SEG_{128}	-5713.8	-661.6
17	SEG_{127}	-5623.8	-661.6
18	SEG_{126}	-5533.8	-661.6
19	SEG_{125}	-5443.8	-661.6
20	SEG_{124}	-5353.8	-661.6
21	SEG_{123}	-5263.8	-661.6
22	SEG_{122}	-5173.8	-661.6
23	SEG_{121}	-5083.8	-661.6
24	SEG_{120}	-4993.8	-661.6
25	SEG_{119}	-4903.8	-661.6
26	SEG_{118}	-4813.8	-661.6
27	SEG_{117}	-4723.8	-661.6
28	SEG_{116}	-4633.8	-661.6
29	SEG_{115}	-4543.8	-661.6
30	SEG_{114}	-4453.8	-661.6
31	SEG_{113}	-4363.8	-661.6
32	SEG_{112}	-4273.8	-661.6
33	SEG_{111}	-4183.8	-661.6
34	SEG_{110}	-4093.8	-661.6
35	SEG_{109}	-4003.8	-661.6
36	SEG_{108}	-3913.8	-661.6
37	SEG_{107}	-3823.8	-661.6
38	SEG_{106}	-3733.8	-661.6
39	SEG_{105}	-3643.8	-661.6
40	SEG_{104}	-3553.8	-661.6
41	SEG_{103}	-3463.8	-661.6
42	SEG_{102}	-3373.8	-661.6
43	SEG_{101}	-3283.8	-661.6
44	SEG_{100}	-3193.8	-661.6
45	SEG_{99}	-3103.8	-661.6
46	SEG_{98}	-3013.8	-661.6
47	SEG_{97}	-2923.8	-661.6
48	SEG_{96}	-2833.8	-661.6
49	SEG_{95}	-2743.8	-661.6
50	SEG_{94}	-2653.8	-661.6
51	SEG_{93}	-2563.8	-661.6
52	SEG_{92}	-2473.8	-661.6
53	SEG_{91}	-2383.8	-661.6
54	SEG_{90}	-2293.8	-661.6
55	SEG_{89}	-2203.8	-661.6
56	SEG_{88}	-2113.8	-661.6
57	SEG_{87}	-2023.8	-661.6
58	SEG_{86}	-1933.8	-661.6
59	SEG_{85}	-1843.8	-661.6
60	SEG_{84}	-1753.8	-661.6
61	SEG_{83}	-1663.8	-661.6
62	SEG_{82}	-1573.8	-661.6
63	SEG_{81}	-1483.8	-661.6

No.	PIN	X (μm)	Y (μm)
64	SEG_{80}	-1393.8	-661.6
65	SEG_{79}	-1303.8	-661.6
66	SEG_{78}	-1213.8	-661.6
67	SEG_{77}	-1123.8	-661.6
68	SEG_{76}	-1033.8	-661.6
69	SEG_{75}	-943.8	-661.6
70	SEG_{74}	-853.8	-661.6
71	SEG_{73}	-763.8	-661.6
72	SEG_{72}	-673.8	-661.6
73	SEG_{71}	-583.8	-661.6
74	SEG_{70}	-493.8	-661.6
75	SEG_{69}	-403.8	-661.6
76	SEG_{68}	-313.8	-661.6
77	SEG_{67}	-223.8	-661.6
78	SEG_{66}	-133.8	-661.6
79	SEG_{65}	-43.8	-661.6
80	SEG_{64}	46.2	-661.6
81	SEG_{63}	136.2	-661.6
82	SEG_{62}	226.2	-661.6
83	SEG_{61}	316.2	-661.6
84	SEG_{60}	406.2	-661.6
85	SEG_{59}	496.2	-661.6
86	SEG_{58}	586.2	-661.6
87	SEG_{57}	676.2	-661.6
88	SEG_{56}	766.2	-661.6
89	SEG_{55}	856.2	-661.6
90	SEG_{54}	946.2	-661.6
91	SEG_{53}	1036.2	-661.6
92	SEG_{52}	1126.2	-661.6
93	SEG_{51}	1216.2	-661.6
94	SEG_{50}	1306.2	-661.6
95	SEG_{49}	1396.2	-661.6
96	SEG_{48}	1486.2	-661.6
97	SEG_{47}	1576.2	-661.6
98	SEG_{46}	1666.2	-661.6
99	SEG_{45}	1756.2	-661.6
100	SEG_{44}	1846.2	-661.6
101	SEG_{43}	1936.2	-661.6
102	SEG_{42}	2026.2	-661.6
103	SEG_{41}	2116.2	-661.6
104	SEG_{40}	2206.2	-661.6
105	SEG_{39}	2296.2	-661.6
106	SEG_{38}	2386.2	-661.6
107	SEG_{37}	2476.2	-661.6
108	SEG_{36}	2566.2	-661.6
109	SEG_{35}	2656.2	-661.6
110	SEG_{34}	2746.2	-661.6
111	SEG_{33}	2836.2	-661.6
112	SEG_{32}	2926.2	-661.6
113	SEG_{31}	3016.2	-661.6
114	SEG_{30}	3106.2	-661.6
115	SEG_{29}	3196.2	-661.6
116	SEG_{28}	3286.2	-661.6
117	SEG_{27}	3376.2	-661.6
118	SEG_{26}	3466.2	-661.6
119	SEG_{25}	3556.2	-661.6
120	SEG_{24}	3646.2	-661.6
121	SEG_{23}	3736.2	-661.6
122	SEG_{22}	3826.2	-661.6
123	SEG_{21}	3916.2	-661.6
124	SEG_{20}	4006.2	-661.6
125	SEG_{19}	4096.2	-661.6
126	SEG_{18}	4186.2	-661.6

No.	PIN	X (μm)	Y (μm)
127	SEG_{17}	4276.2	-661.6
128	SEG_{16}	4366.2	-661.6
129	SEG_{15}	4456.2	-661.6
130	SEG_{14}	4546.2	-661.6
131	SEG_{13}	4636.2	-661.6
132	SEG_{12}	4726.2	-661.6
133	SEG_{11}	4816.2	-661.6
134	SEG_{10}	4906.2	-661.6
135	SEG_{9}	4996.2	-661.6
136	SEG_{8}	5086.2	-661.6
137	SEG_{7}	5176.2	-661.6
138	SEG_{6}	5266.2	-661.6
139	SEG_{5}	5356.2	-661.6
140	SEG_{4}	5446.2	-661.6
141	SEG_{3}	5536.2	-661.6
142	SEG_{2}	5626.2	-661.6
143	SEG_{1}	5716.2	-661.6
144	DUMMY	5806.2	-661.6
145	DUMMY	5896.2	-661.6
146	DUMMY	6094.8	-563.4
147	DUMMY	6094.8	-473.4
148	DUMMY	6094.8	-383.4
149	DUMMY	6094.8	-293.4
150	DUMMY	6094.8	-203.4
151	$PCOM_{1}$	6094.8	-113.4
152	COM_{1}	6094.8	-23.4
153	COM_{2}	6094.8	66.6
154	COM_{3}	6094.8	156.6
155	COM_{4}	6094.8	246.6
156	COM_{5}	6094.8	336.6
157	DUMMY	6094.8	426.6
158	DUMMY	6094.8	516.6
159	DUMMY	5870.6	760
160	DUMMY	5780.6	760
161	DUMMY	5690.6	760
162	DUMMY	5600.6	760
163	COM_{6}	5510.6	760
164	COM_{7}	5420.6	760
165	COM_{8}	5330.6	760
166	COM_{9}	5240.6	760
167	COM_{10}	5150.6	760
168	COM_{11}	5060.6	760
169	COM_{12}	4970.6	760
170	COM_{13}	4880.6	760
171	COM_{14}	4790.6	760
172	COM_{15}	4700.6	760
173	COM_{16}	4610.6	760
174	DUMMY	4520.6	760
175	V_{LC5}	4400.8	760
176	V_{LC4}	4224.8	760
177	V_{LC3}	4048.8	760
178	V_{LC2}	3872.8	760
179	V_{LC1}	3696.8	760
180	V_{LCD}	3520.8	760
181	V_{LCD}	3344.8	760
182	$Amp_{IN}(-)$	3168.8	760
183	$Amp_{IN}(+)$	2992.8	760
184	Amp_{OUT}	2816.8	760
185	C_1^-	2640.8	760
186	C_1^-	2550.8	760
187	C_1^-	2460.8	760
188	C_1^+	2284.8	760
189	C_1^+	2194.8	760

No.	PIN	X (μm)	Y (μm)
190	C_1^+	2104.8	760
191	C_2^-	1928.8	760
192	C_2^-	1838.8	760
193	C_2^-	1748.8	760
194	C_2^+	1572.8	760
195	C_2^+	1482.8	760
196	C_2^+	1392.8	760
197	V_{DD2}	1232.8	760
198	VEXT	1056.8	760
199	OSC_{BRI}	880.8	760
200	OSC_{IN}	704.8	760
201	OSC_{OUT}	528.8	760
202	DA_{CHA}	352.8	760
203	V_{DD1}	176.8	760
204	V_{DD1}	0.8	760
205	V_{CHA}	-175.2	760
206	V_{SS}	-351.2	760
207	CS_0	-527.2	760
208	CS_1	-703.2	760
209	CS_2	-879.2	760
210	$\overline{RESET}$	-1055.2	760
211	D_7/NS	-1231.2	760
212	D_6/CAE	-1407.2	760
213	D_5	-1583.2	760
214	D_4	-1759.2	760
215	D_3	-1935.2	760
216	D_2	-2111.2	760
217	D_1	-2287.2	760
218	D_0/DATA	-2463.2	760
219	E/SCK	-2639.2	760
220	STB	-2815.2	760
221	V_{SS}	-2991.2	760
222	V_{SS}	-3167.2	760
223	WS	-3343.2	760
224	V_{DD1}	-3519.2	760
225	POCOUT	-3695.2	760
226	CLKOUT	-3871.2	760
227	SYNC	-4047.2	760
228	V_{EE}	-4223.2	760
229	V_{EE}	-4399.2	760
230	DUMMY	-4520.6	760
231	$PCOM_{2}$	-4610.6	760
232	COM_{32}	-4700.6	760
233	COM_{31}	-4790.6	760
234	COM_{30}	-4880.6	760
235	COM_{29}	-4970.6	760
236	COM_{28}	-5060.6	760
237	COM_{27}	-5150.6	760
238	COM_{26}	-5240.6	760
239	COM_{25}	-5330.6	760
240	COM_{24}	-5420.6	760
241	COM_{23}	-5510.6	760
242	DUMMY	-5600.6	760
243	DUMMY	-5690.6	760
244	DUMMY	-5780.6	760
245	DUMMY	-5870.6	760

CONTENTS

1. PIN FUNCTIONS

1.1 Power System

Pin Symbol	Pin Name	Pin No.	I/O	Description
V_{DD1}	Logic power supply pin	203, 204, 224	---	Power supply pin for logic
V_{DD2}	Power supply pin for booster circuit	197	---	Power supply pin for booster circuit. Set the pin to $V_{DD1} \leq V_{DD2}$.
V_{SS}	Logic ground pin	206, 221, 222	---	Ground pin for logic
V_{LCD}	Driver power supply pin	180, 181	---	Driver power supply pin. Output pin of internal booster circuit. Connect with a 1-μF booster capacitor to the V_{DD2} pin. When not using the internal booster circuit, the driver power can be turned on directly.
V_{LC1} to V_{LC5}	Driver reference power supply	179 to 175	---	Reference power supply pin for LCD drive. When the internal bias is selected, be sure to leave it open.
C_1^+, C_1^-, C_2^+, C_2^-	Capacitor connection pins	185 to 196	---	Capacitor connection pins for booster circuit. Connect a 1 μF capacitor.
V_{EE}	Driver ground pin	228, 229	---	Ground pin for driver

1.2 Logic System

Pin Symbol	Pin Name	Pin No.	I/O	Description
WS	Word length selection	223	I	This pin selects the word length. At High level, it becomes an 8-bit parallel interface. At Low level, it becomes a 4-bit parallel interface if D_7/NS is High; and a serial interface if D_7/NS is Low. When the word length is 4 bits, data is transferred in the upper-to-lower sequence by means of data buses D_0 to D_3. The word length cannot be changed after power-on.
STB	Strobe	220	I	Data can be input/output at Low level either in parallel interface or serial interface mode.
E/SCK	Enable/shift clock	219	I	In parallel interface mode, this becomes the data enable input pin. During read-in, data is fetched into the interface buffer at the rising edge. During read-out, data is fetched from the interface buffer at the falling edge. In serial interface mode, this pin becomes the data shift clock. During read-in, data is fetched into the shift register at the rising edge. During read-out, data is fetched from the shift register at the falling edge.
CLKOUT	Clock for slave IC output	226	O	This pin outputs an inverted oscillation clock. It connects to slave IC's OSC_{IN} directly.
POCOUT	Power-on reset monitor	225	O	Monitor pin for internal power-on reset. At Low level, power-on reset is set internally. At Low level, power-on reset is released. The pin is for IC testing. Normally leave it open.

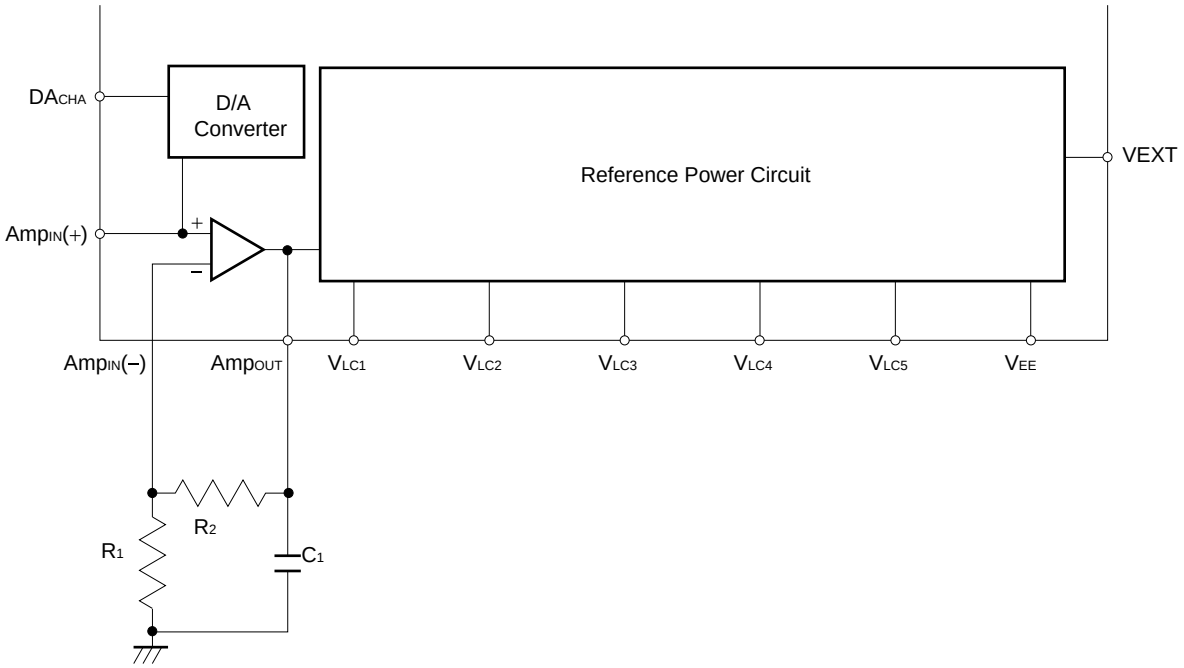
1.2 Logic System (Continued)

Pin Symbol	Pin Name	Pin No.	I/O	Description
D_0/DATA	Data bus/data	218	I/O	In parallel interface mode, this pin becomes the D_0 bit of the data bus. In serial interface mode, it becomes the input/output pin of the command and display data (3 states).
D_1 to D_5	Data bus	217 to 213	I/O	In parallel interface mode, these pins become the D_1 to D_5 bits of the data bus. In serial interface mode, leave them open.
D_6/CAE	Data bus/chip address enable	212	I/O	In 8-bit parallel interface mode, this pin becomes the D_6 bit of the data bus. In 4-bit parallel interface and serial interface modes, it becomes chip address enable. Also, at High level, it becomes chip address valid; at Low level, chip address invalid. In 8-bit parallel interface, it becomes chip address valid.
D_7/NS	Data bus/nibble select	211	I/O	When the word select (WS) is High level, this bit becomes the D_7 bit of the data bus. When WS is Low level, it becomes the nibble select (NS). When NS is High level, it becomes 4-bit parallel interface. When NS is Low level, it becomes serial interface. In 4-bit parallel interface mode, data cannot be read out.
$\overline{\text{RESET}}$	Reset	210	I	At Low level, internal initialization is performed.
V_{CHA}	Boosting magnitude switching	205	I	The boosting magnitude of the internal booster circuit is switched over. At High level, it is switched to 3X, while, at Low level, 2X.
DA_{CHA}	D/A converter switching	202	I	Select whether to use the internal D/A converter for temperature correction or not. At High level, this circuit is used, at Low level, unused.
VEXT	Reference supply switching	198	I	Selects the method for supplying the reference power circuit. At High level, the circuit is supplied externally; and, at Low level, internally.
SYNC	Synchronization	227	I/O	Input/output pin for synchronization. Master mode: Output Slave mode: Input
CS_0 to CS_2	Chip select	207 to 209	I	When used for multiple chips, these pins are used to specify their addresses. They can be accessed only when coinciding with b2 to b4 bits of the interface control register.
OSC_{IN}	Oscillation pin	200	I	These pins are connected with the 1 MΩ resistor. When using external oscillation, input it into the OSC_{IN}, leaving the OSC_{OUT} open.
OSC_{OUT}		201	O	
OSC_{BRI}	External clock for blinks	199	I	Input pin of the 2-Hz external clock. It internally divides this clock by 2 to generate 1 Hz and make it the synchronizing signal for blinks.

1.3 Driver System

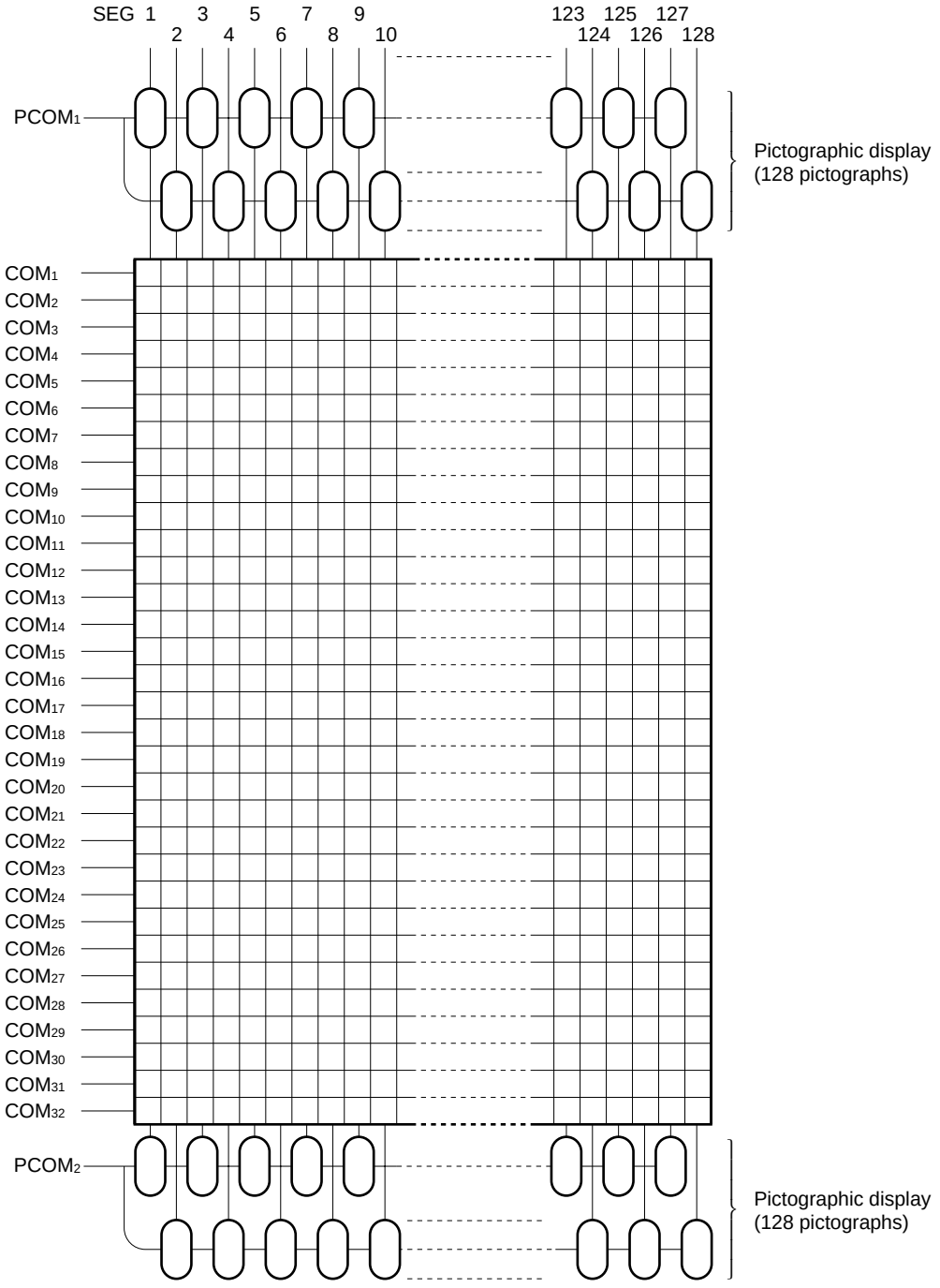
Pin Symbol	Pin Name	Pin No.	I/O	Description
SEG_1 to SEG_{128}	Segment	143 to 16	O	Segment output pins
COM_1 to COM_{32}	Commons	3 to 8, 152 to 156, 163 to 173, 232 to 241	O	Common output pins
$PCOM_1$, $PCOM_2$	Pictographic commons	151, 231	O	Common output pins for pictograph
$Amp_{IN}(+)$, $Amp_{IN}(-)$	Operational amplifier input	183, 182	I	These are the input pins of the operational amplifier for LCD drive voltage adjustment. Leave $Amp_{IN}(+)$ open when using the internal D/A converter. When not using the D/A converter, it is necessary to input the reference voltage. Connect $Amp_{IN}(-)$ to the LCD voltage adjustment resistor (see the diagram below).
Amp_{OUT}	Operational amplifier output	184	O	This is the input pin of the operational amplifier for LCD drive voltage adjustment. It is normal to connect this pin to the LCD voltage adjustment resistor (see the diagram below). It is recommended to connect approx. 0.1 to 1 μF capacitor to this pin to stabilize the internal amplifier's output.

2. VOLTAGE CONTROL CIRCUIT EXAMPLE



3. LCD DISPLAY

The μPD16675A's LCD can display 128 by 32 dots (called full-dot display) as well as 128 by 2 pictographs on a single screen.

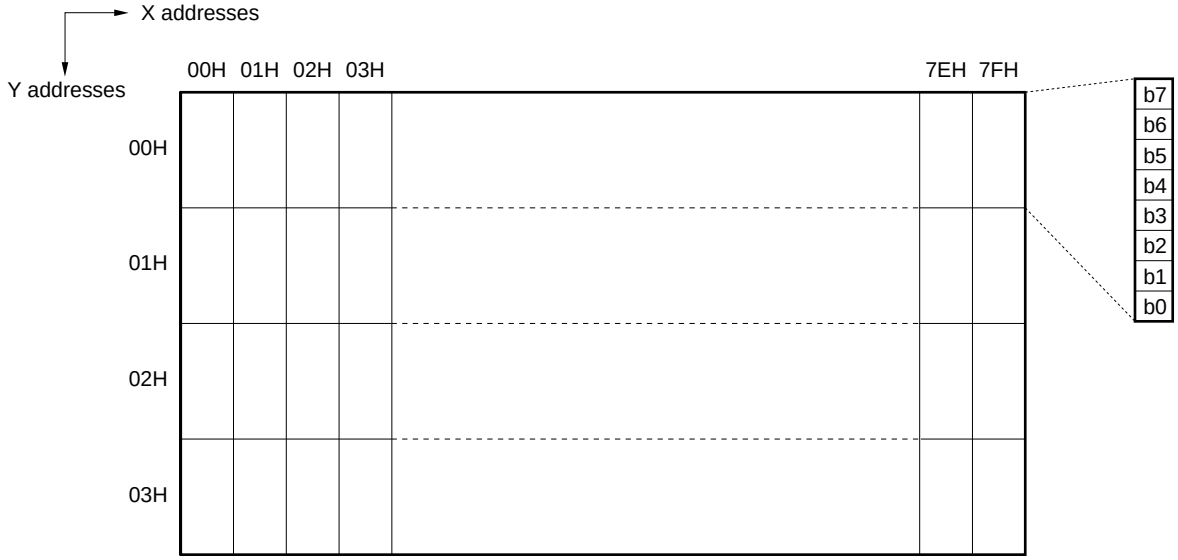


4. GROUP ADDRESSES

4.1 Dot Display

The group addresses of dot display are assigned as follows.

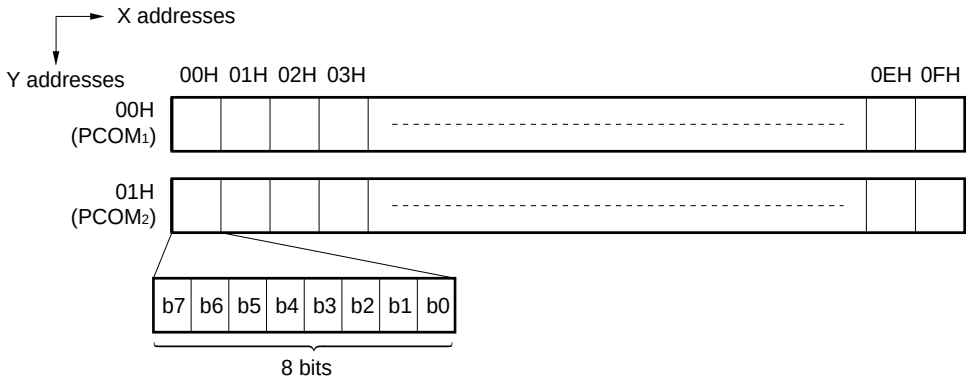
If address increment is set, when the X address goes to 7FH, the next address is 00H. At this time, the Y address changes to the next address. Also, when the Y address goes to 03H, the next address is 00H.



4.2 Pictographic Display

The group addresses of pictograph display are assigned as follows.

If address increment is set, when the X address goes to 0FH, the next address is 00H. At this time, the Y address changes to the next address. Also, when the Y address goes to 01H, the next address is 00H.



(1) PCOM1 (Y Address = 00H)

X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	101	102	103	104
0DH	105	106	107	108	109	110	111	112
0EH	113	114	115	116	117	118	119	120
0FH	121	122	123	124	125	126	127	128

(2) PCOM2 (Y Address = 01H)

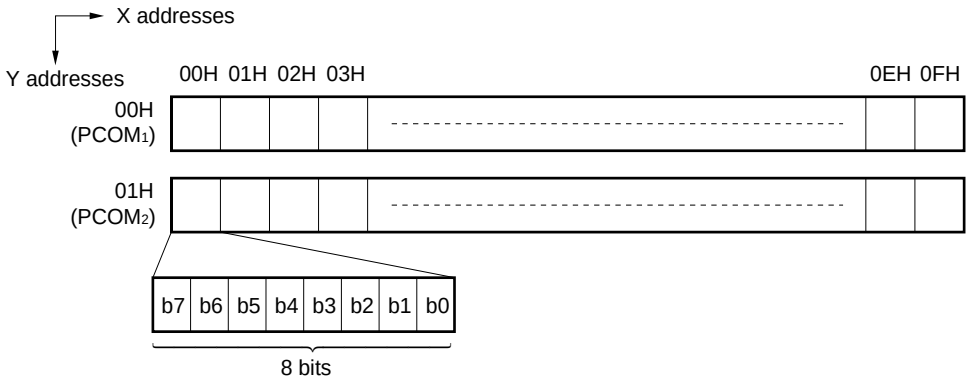
X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	101	102	103	104
0DH	105	106	107	108	109	110	111	112
0EH	113	114	115	116	117	118	119	120
0FH	121	122	123	124	125	126	127	128

4.3 Blink Data

The group addresses of pictographic blink data are assigned as follows.

Write “1” in the address of the pictographic to be blinked.

If address increment is set, when the X address goes to 0FH, the next address is 00H. At this time, the Y address changes to the next address. Also, when the Y address goes to 01H, the next address is 00H.



(1) PCOM1 (Y Address = 00H)

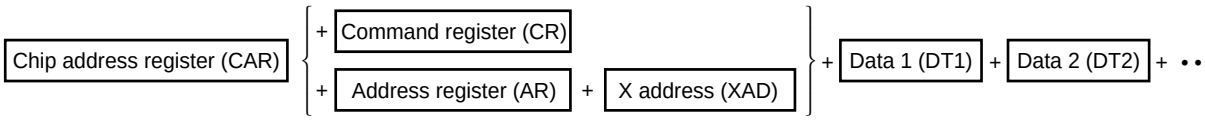
X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	101	102	103	104
0DH	105	106	107	108	109	110	111	112
0EH	113	114	115	116	117	118	119	120
0FH	121	122	123	124	125	126	127	128

(2) PCOM2 (Y Address = 01H)

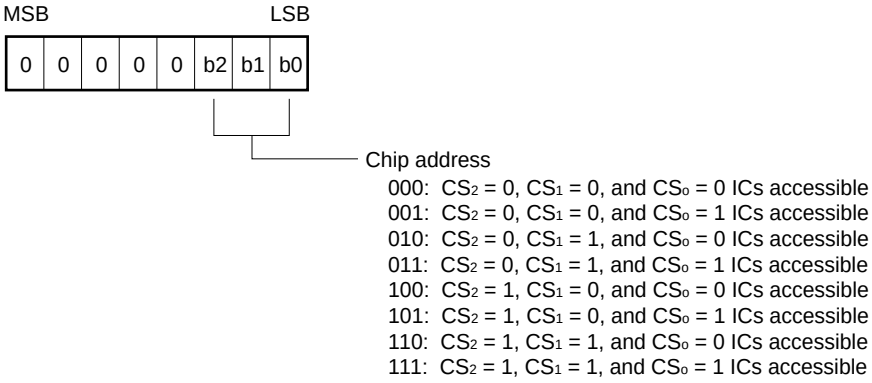
X address	Segment output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64
08H	65	66	67	68	69	70	71	72
09H	73	74	75	76	77	78	79	80
0AH	81	82	83	84	85	86	87	88
0BH	89	90	91	92	93	94	95	96
0CH	97	98	99	100	101	102	103	104
0DH	105	106	107	108	109	110	111	112
0EH	113	114	115	116	117	118	119	120
0FH	121	122	123	124	125	126	127	128

5. COMMAND

5.1 Basic Form



5.2 Chip Address Register (CAR)



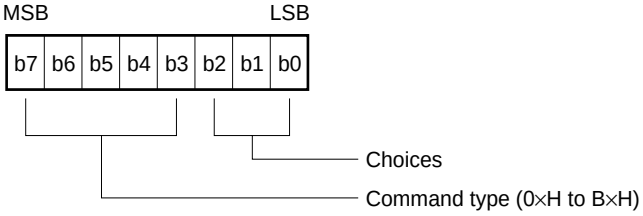
The register is made valid in the following states.

Interface	CAE	
	High level	Low level
Serial	Valid	Invalid
4-bit parallel	Valid	Invalid
8-bit parallel	Valid (CAE: Used as the D_6 bit)	

It is unnecessary to transmit the register that is invalid.

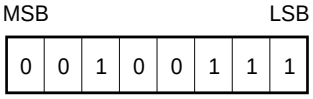
5.3 Command Register

The command register's basic configuration is as follows.



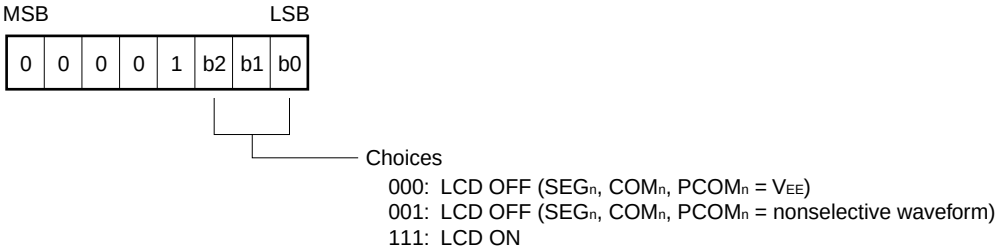
5.3.1 Reset

All the IC's commands are initialized. Resetting takes effect only during the internally predetermined time (one shot).



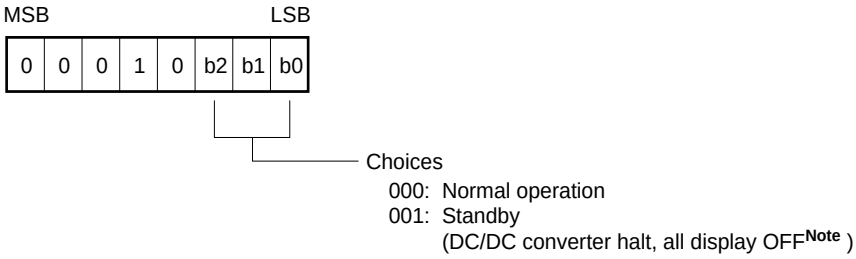
5.3.2 Display ON/OFF

ON/OFF of the display is controlled.



5.3.3 Standby

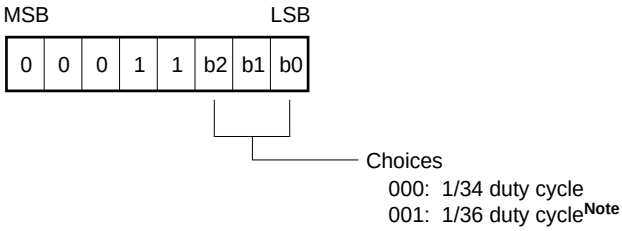
The DC/DC converter is stopped, thus reducing the supply current. The display is placed in the OFF state (SEG_n, $COM_n = V_{EE}$).



Note SEG_n, COM_n, $PCOM_n = V_{EE}$

5.3.4 Duty setting

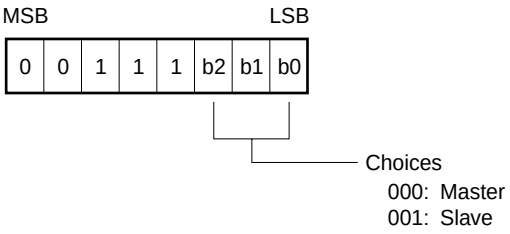
The duty is set.



Note If the duty cycle is 1/36, $PCOM_1$ and $PCOM_2$ are respectively selected for twice the period of the duty (2/36).

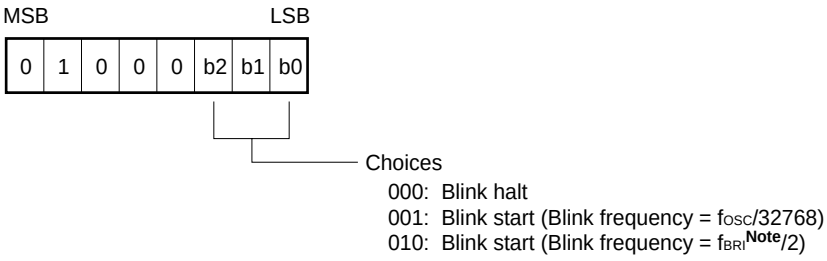
5.3.5 Master/slave setting

The master/slaves are set.



5.3.6 Blink setting

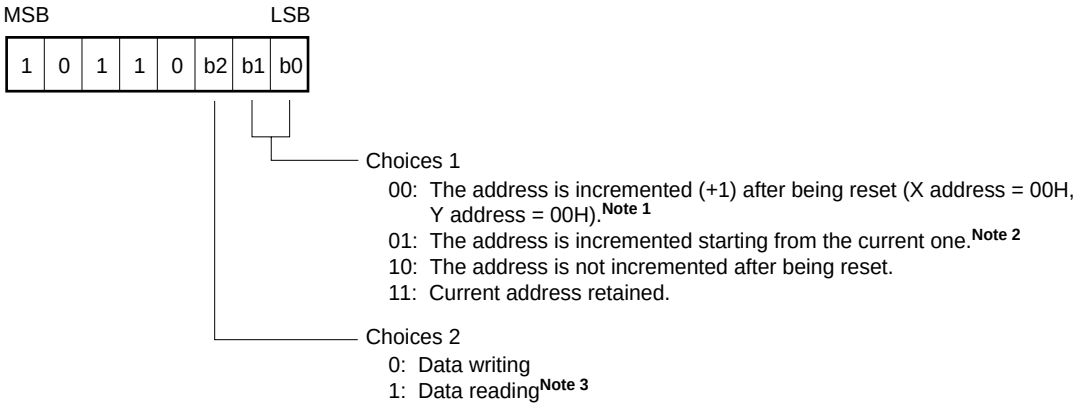
The blinks of the pictograph of the address whose blink data is “1” are controlled.



Note This refers to the frequency of the external clock which is input from the OSC_{BRI} pin.

5.3.7 Data R/W mode

Data Read/Write (R/W), increment, address counter resetting, etc. are set in this mode.



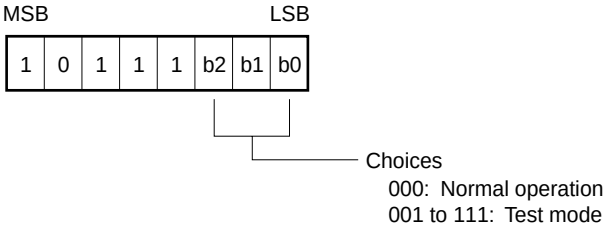
Notes 1. When the X address goes to the last address, the next address is 00H.

2. The data Read mode is cancelled at STB's rising edge (switched to data Write mode).

3. In 4-bit parallel interface mode, data cannot be read out.

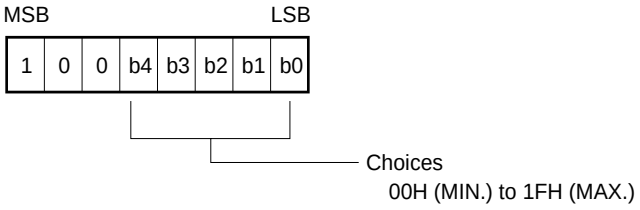
5.3.8 Test mode

The test mode is set. The test mode is for checking IC operation, and no assurance is made for its regular use or continued operation.



5.3.9 D/A converter setting

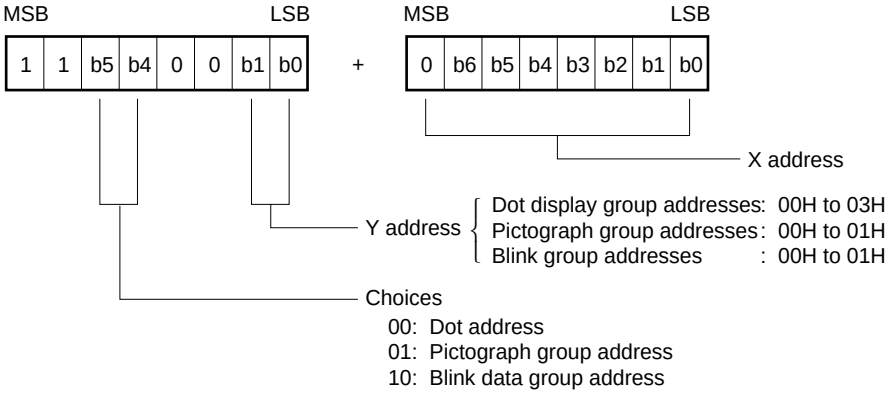
D/A converter output is set in 32 steps from V_{DD2} to 2/3 V_{DD2}.



10H is set after reset.

5.4 Address Register

Selects the address type and specifies the address.



Caution If unspecified addresses have been set, the operation is not assured.

6. RESETTING

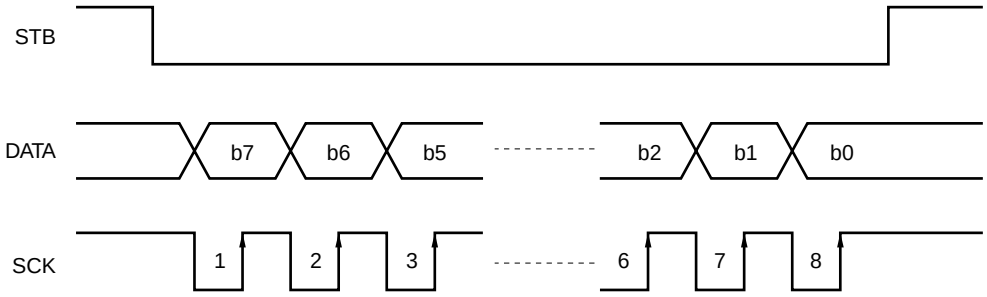
When reset (power-ON reset, command reset, hardware (terminal) reset), the contents of each register are as follows:

Register name	Register contents								Status
	b7	b6	b5	b4	b3	b2	b1	b0	
Chip address register	0	0	0	0	0	0	0	0	The ICs of CS_2 = 0, CS_1 = 0, CS_0 = 0 can be accessed.
Display ON/OFF	0	0	0	0	1	0	0	0	LCD OFF (SEG_n, COM_n, $PCOM_n$ = V_{LC5})
Standby	0	0	0	1	0	0	0	0	Normal operation
Duty setting	0	0	0	1	1	0	0	0	1/34 duty cycle
Blink setting	0	1	0	0	0	0	0	0	Blink halt
D/A converter setting	1	0	0	0	0	0	0	0	LCD drive voltage: Set to 2/3 V_{DD2}
Data R/W mode	1	0	1	1	0	0	0	0	Data write/address reset/increment (+1)
Test mode	1	0	1	1	1	0	0	0	Normal operation

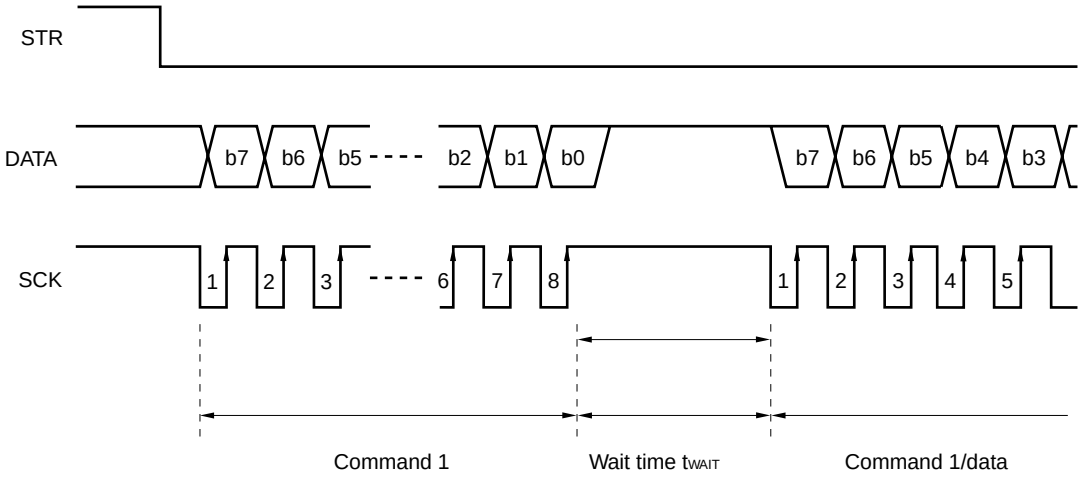
7. COMMUNICATION FORMAT

7.1 Serial

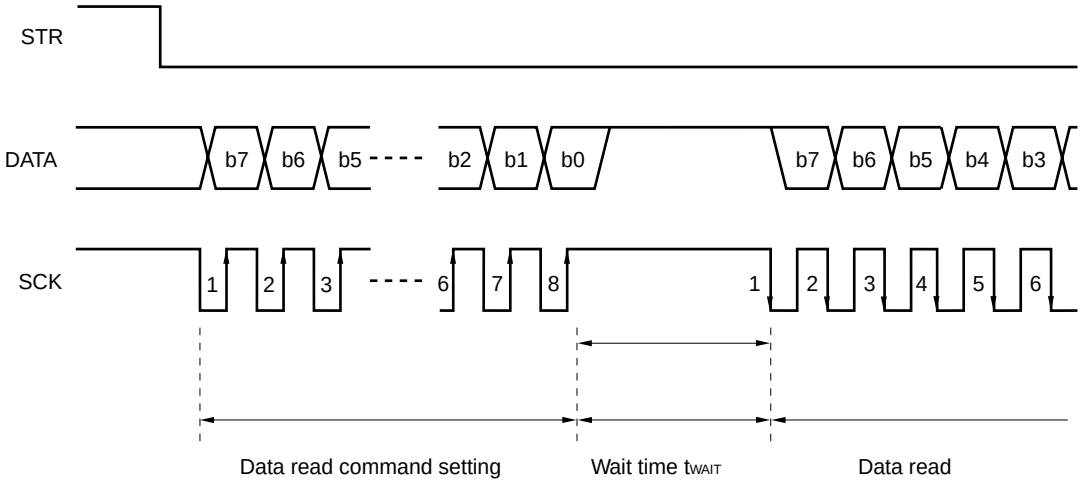
7.1.1 Reception 1 (Command/data write: 1 byte)



7.1.2 Reception 2 (Command/data write: 2 bytes or more)

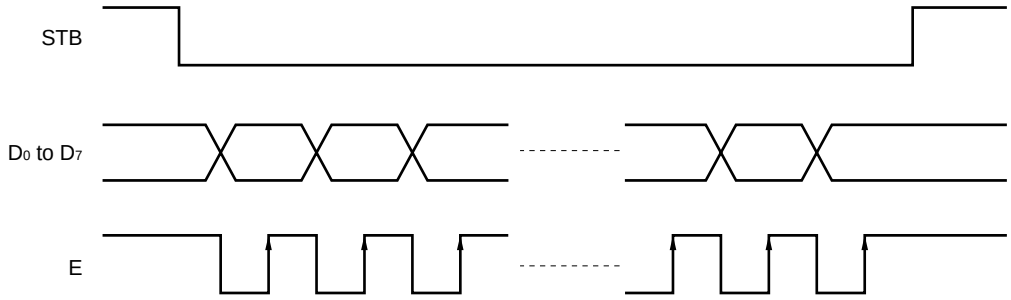


7.1.3 Transmission (Command/data read)

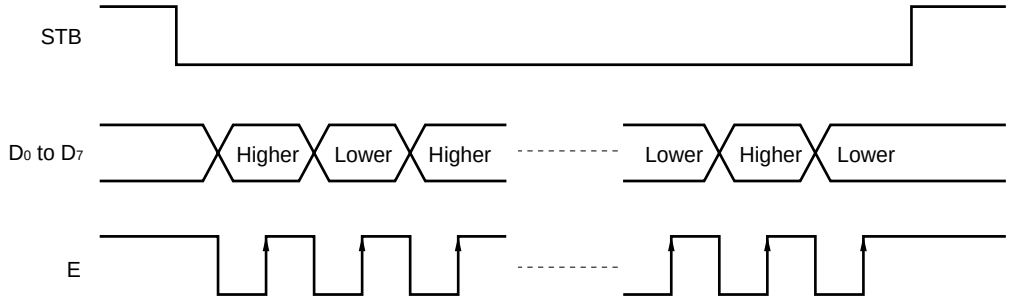


7.2 Parallel

7.2.1 8-bit parallel interface



7.2.2 4-bit parallel interface



8. CPU ACCESS EXAMPLES

Examples of access procedure are shown below. In serial or 4-bit parallel interface mode, the Chip Address Register (CAR) is not transmitted when the CAR is invalid (CAE = L, see page 13).

8.1 Initialize and Data Write

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	(Power-on reset is released 200 μs after power supply is started)
Chip Address Register (CAR)	L	0	0	0	0	0	0	0	0	Chip address = 000
Duty setting	L	0	0	0	1	1	0	0	0	1/34 duty
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
D/A converter setting	L	1	0	0	1	0	0	0	0	D/A converter output = 10000H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	0	0	0	0	0	Dot address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	0	0	1	Data write, the address is incremented starting from the current one.
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 00H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 01H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 02H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 03H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	1	0	0	0	0	Pictograph group address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000

Remark X = Don't Care, D = Data

8.1 Initialize and Data Write (Continued)

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Data R/W mode	L	1	0	1	1	0	0	0	1	Data write, the address is incremented starting from the current one.
Pict display data 1 | Pict display data 16	L | L	D D	D D	D D	D D	D D	D D	D D	D D	Data of Y address = 00H (16 bytes)
Pict display data 1 | Pict display data 16	L | L	D D	D D	D D	D D	D D	D D	D D	D D	Data of Y address = 01H (16 bytes)
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Display ON/OFF	L	0	0	0	0	1	1	1	1	LCD ON
End	H	X	X	X	X	X	X	X	X	

Remark X = Don't Care, D = Data

8.2 Change Display Data and Pictographic Data (All Data are Changed)

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Chip Address Register (CAR)	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	0	0	0	0	0	Dot address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	0	0	1	Data write, the address is incremented starting from the current one.
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 00H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 01H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 02H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 03H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	1	0	0	0	0	Pictograph group address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	0	0	1	Data write, the address is incremented starting from the current one.
Pict display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 00H (16 bytes)
|	|									
Pict display data 16	L	D	D	D	D	D	D	D	D	
Pict display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 01H (16 bytes)
|	|									
Pict display data 16	L	D	D	D	D	D	D	D	D	
End	H	X	X	X	X	X	X	X	X	

Remark X = Don't Care, D = Data

8.3 Read Display Data and Pictograph Data

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Chip Address Register (CAR)	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	0	0	0	0	0	Dot address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	1	0	1	Data write, the address is incremented starting from the current one.
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 00H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 01H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 02H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
Dot display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 03H (128 bytes)
|	|									
Dot display data 128	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	0	1	0	0	0	0	Pictograph group address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	1	0	1	Data write, the address is incremented starting from the current one.
Pict display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 00H (16 bytes)
|	|									
Pict display data 16	L	D	D	D	D	D	D	D	D	
	H	X	X	X	X	X	X	X	X	
Pict display data 1	L	D	D	D	D	D	D	D	D	Data of Y address = 01H (16 bytes)
|	|									
Pict display data 16	L	D	D	D	D	D	D	D	D	
End	H	X	X	X	X	X	X	X	X	

Remark X = Don't Care, D = Data

8.4 Blink Data Setting

Parameter	STB	Command/data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Start	H	X	X	X	X	X	X	X	X	
Chip Address Register (CAR)	L	0	0	0	0	0	0	0	0	Chip address = 000
Address register 1	L	1	1	1	0	0	0	0	0	Blink data group address, Y address = 00H
Address register 2	L	0	0	0	0	0	0	0	0	X address = 00H
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Data R/W mode	L	1	0	1	1	0	0	0	1	Data write, the address is incremented starting from the current one.
Blink display data 1 | Blink display data 16	L | L	D D	D D	D D	D D	D D	D D	D D	D D	} Data of Y address = 00H (16 bytes)
Blink display data 1 | Blink display data 16	L | L	D D	D D	D D	D D	D D	D D	D D	D D	} Data of Y address = 01H (16 bytes)
	H	X	X	X	X	X	X	X	X	
CAR	L	0	0	0	0	0	0	0	0	Chip address = 000
Blink setting	L	0	1	0	0	0	0	1	0	Start blinking, blink frequency = $f_{BRI}/2$
End	H	X	X	X	X	X	X	X	X	

Remark X = Don't Care, D = Data

9. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = +25°C, V_{SS} = V_{EE} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD1}	–0.3 to +7.0	V
Booster circuit supply voltage (V_{CHA} = H)	V_{DD2}	–0.3 to +5.0, $V_{DD1} \leq V_{DD2}$	V
Booster circuit supply voltage (V_{CHA} = L)	V_{DD2}	–0.3 to +7.0, $V_{DD1} \leq V_{DD2}$	V
Driver supply voltage	V_{LCD}	–0.3 to +15.0, $V_{DD2} \leq V_{LCD}$	V
Driver reference supply input voltage	V_{LC1} to V_{LC5}	–0.3 to V_{LCD} +0.3	V
Logic system input voltage	V_{IN1}	–0.3 to V_{DD1} +0.3	V
Logic system output voltage	V_{OUT1}	–0.3 to V_{DD1} +0.3	V
Logic system input/output voltage	$V_{I/O1}$	–0.3 to V_{DD1} +0.3	V
Driver system input voltage	V_{IN2}	–0.3 to V_{LCD} +0.3	V
Driver system output voltage	V_{OUT2}	–0.3 to +V_{LCD} +0.3	V
Operating temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1} Note 1	2.7		3.3	V
Booster circuit supply voltage (V_{CHA} = H)	V_{DD2} Note 1	2.7	3.0	3.6	V
Booster circuit supply voltage (V_{CHA} = L)	V_{DD2} Note 1	2.7	5.0	5.5	V
Driver supply voltage	V_{LCD} Note 2	V_{DD2}	10	12	V
Logic system input voltage	V_{IN}	0		V_{DD1}	V
Driver system input voltage	V_{LC1} to V_{LC5}	0		V_{LCD}	V

Notes 1. Set this to $V_{DD1} \leq V_{DD2}$.

2. If use external LCD voltage as V_{LCD}, cannot use standby. Also, maintain $V_{DD1} = V_{DD2}$.

Caution At power on and power off, keep $V_{DD1} \leq V_{DD2} \leq V_{LCD}$.

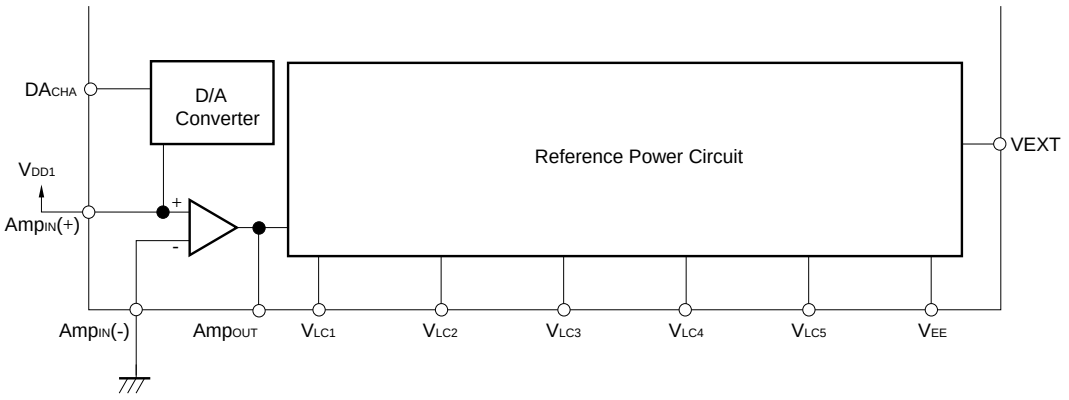
Electrical Specifications

(Unless otherwise specified, T_A = –40 to +85°C, V_{DD1} = 2.7 to 3.3 V, V_{CHA} = H: V_{DD2} = 2.7 to 3.6 V or V_{CHA} = L: V_{DD2} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		0.8 V_{DD1}			V
Low level input voltage	V_{IL}				0.2 V_{DD1}	V
High level input current	I_{IH1}	Except D_0/DATA, D_1 to D_7/NS, DA_{CHA}			1	μA
Low level input current	I_{IL1}	Except D_0/DATA, D_1 to D_7/NS, DA_{CHA}			–1	μA
High level output voltage	V_{OH}	I_{OUT} = –1.5 mA, except OSC_{OUT}	V_{DD1} –0.5			V
Low level output voltage	V_{OL}	I_{OUT} = 4 mA, except OSC_{OUT}			0.5	V
High level leakage current	I_{LOH}	D_0/DATA, D_1 to D_7/NS $V_{IN/OUT}$ = V_{DD1}			10	μA
Low level leakage current	I_{LOL}	D_0/DATA, D_1 to D_7/NS $V_{IN/OUT}$ = V_{SS}			–10	μA
Common output ON resistance	R_{COM}	V_{LCn}→COM_n, V_{LCD} ≥ 2 V_{DD2} $\|I_O\|$ = 50 μA			2	kΩ
Segment output ON resistance	R_{SEG}	V_{LCn}→SEG_n, V_{LCD} ≥ 2 V_{DD2} $\|I_O\|$ = 50 μA			4	kΩ
Driver supply voltage (Booster voltage)	V_{LCD}	V_{CHA} = L, **Note**	1.8 V_{DD2}		2.0 V_{DD2}	V
		V_{CHA} = H, **Note**	2.7 V_{DD2}		3.0 V_{DD2}	V
Logic system current consumption (V_{DD1})	I_{DD11}	f_{OSC} = 30 kHz, no load V_{DD1} = V_{DD2} = 3.0 V, Not to access RAM			30	μA
		f_{OSC} = 30 kHz, no load V_{DD1} = V_{DD2} = 3.0 V, To access RAM			60	μA
Driver system current consumption (V_{DD2})	I_{DD21}	f_{OSC} = 30 kHz, All display OFF data output, V_{DD1} = V_{DD2} = 3.0 V, VCHA = H, **Note**			150	μA

Remark The TYP. value is a reference value when T_A = 25°C.

Note Measurement circuit



Switching Characteristics

(Unless otherwise specified, T_A = –40 to +85°C, V_{DD1} = 2.7 to 3.3 V, V_{CHA} = H: V_{DD2} = 2.7 to 3.6 V or V_{CHA} = L: V_{DD2} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	Self-oscillation	21	30	50	kHz
Transfer delay time	t_{PHL}	SCK↓→DATA↓			100	ns
	t_{PLH}	SCK↓→DATA↑			300	ns

Remark The TYP. value is a reference value when T_A = 25°C.

The time for one frame is obtained with the following formula.

1 frame = 1/f_{OSC} × 8 × number of duties

If f_{OSC} = 30 kHz and 1/34 duty, then the result is:

1 frame = 33 μs × 8 × 34 = 9.1 ms

Required Conditions for Timing

(Unless otherwise specified, T_A = –40 to +85°C, V_{DD1} = 2.7 to 3.3 V, V_{CHA} = H: V_{DD2} = 2.7 to 3.6 V or V_{CHA} = L: V_{DD2} = 2.7 to 5.5 V)

(1) Common

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{OSC}	OSC_{IN} external clock	20	30	50	kHz
High level clock pulse width	t_{WHC1}	OSC_{IN} external clock	10		25	μs
Low level clock pulse width	t_{WLC1}	OSC_{IN} external clock	10		25	μs
High level clock pulse width	t_{WHC2}	OSC_{BRI} external clock	400			ns
Low level clock pulse width	t_{WLC2}	OSC_{BRI} external clock	400			ns
Rise/fall time	t_r, t_f	OSC_{BRI} external clock			100	ns
Reset pulse width	t_{WRE}	Reset pin	1.0			μs

Remark The TYP. value is a reference value when T_A = 25°C.

(2) Serial interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Shift clock cycle	t_{CYK}	SCK	900			ns
High level shift clock pulse width	t_{WHK}	SCK	400			ns
Low level shift clock pulse width	t_{WLK}	SCK	400			ns
Shift clock hold time	t_{HSTBK}	STB↓→SCK↓	1.5			μs
Data setup time	t_{DS1}	DATA→SCK↑	100			ns
Data hold time	t_{DH1}	SCK↑→DATA	400			ns
STB hold time	t_{HKSTB}	SCK↑→STB↑	1			μs
STB pulse width	t_{WSTB}		1			μs
Wait time	t_{WAIT}	8th CLK↑→1st CLK↓	1			μs

Remark The TYP. value is a reference value when T_A = 25°C.

(3) Parallel interface (8-bit/4-bit)

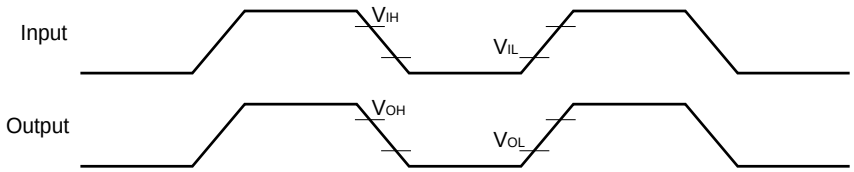
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Enable cycle time	t_{CYCE}	E↑→E↑	900			ns
High level enable pulse width	t_{WHE}	E	400			ns
Low level enable pulse width	t_{WLE}	E	400			ns
STB pulse width	t_{WSTB}		1			μs
STB hold time	t_{HKSTB}		1			μs
Enable hold time	t_{HSTBK}		1.5			μs
Data setup time	t_{DS2}	D_0 to D_7→E↑	100			ns
Data hold time	t_{DH2}	D_0 to D_7→E↓	300			ns

Remarks 1. The TYP. value is a reference value when T_A = 25°C.

2. In 4-bit parallel mode, D_0 to D_3 = “L”.

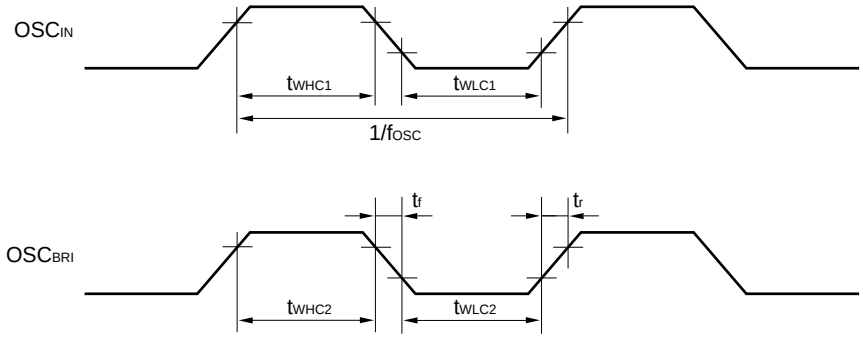
Switching Characteristics Waveforms

AC Measurement Point

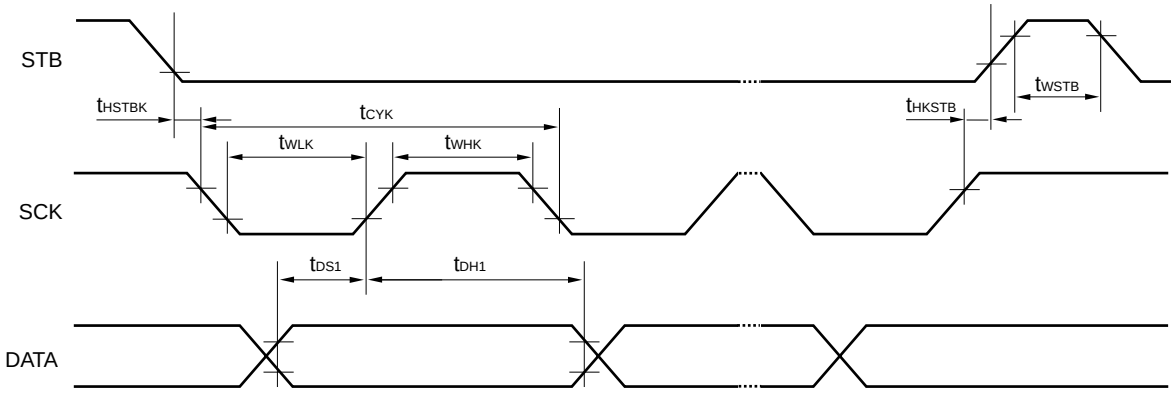


AC Characteristics Waveform

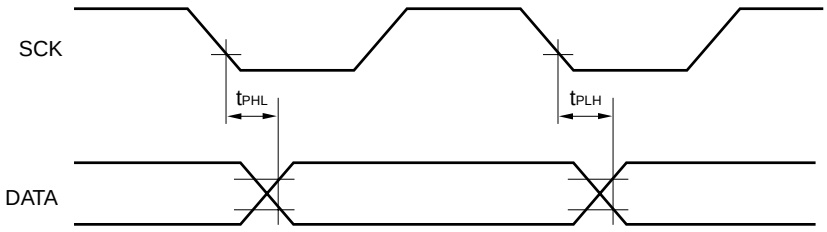
OSC



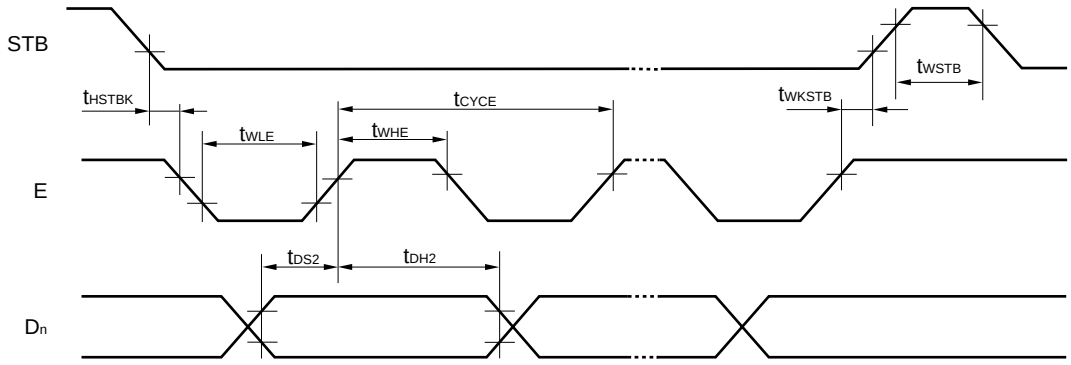
Serial interface (input)



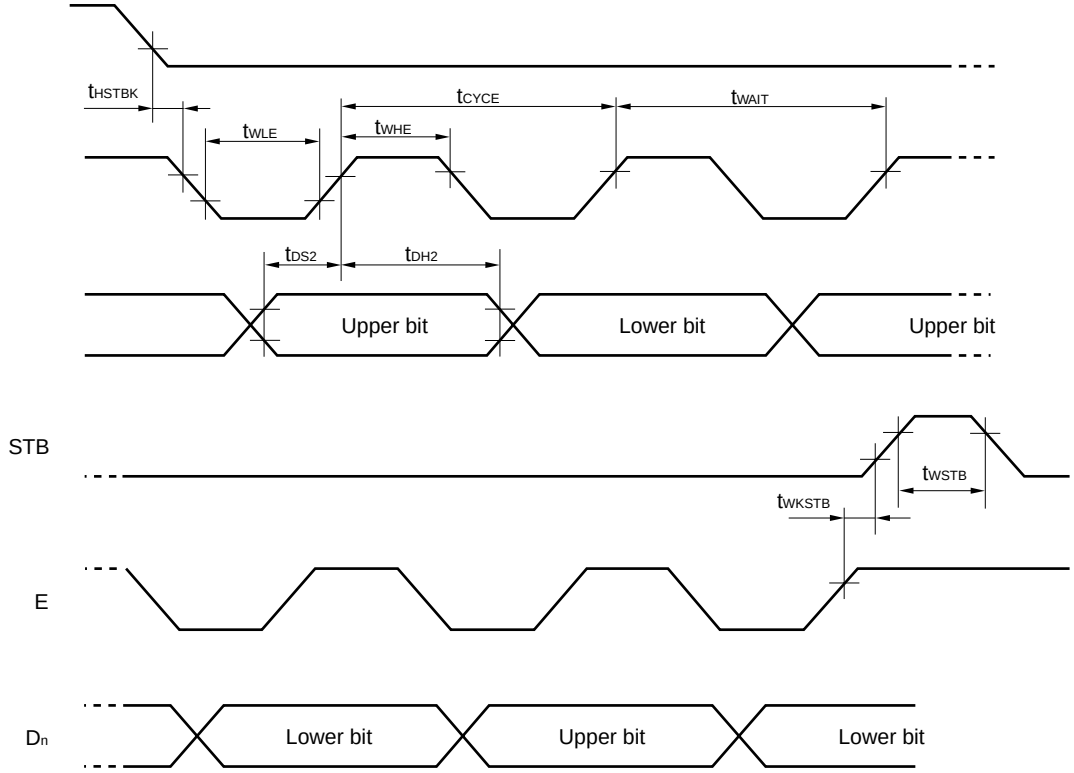
Serial interface (output)



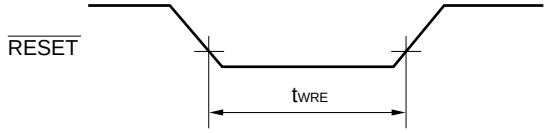
8-bit parallel interface



4-bit parallel interface

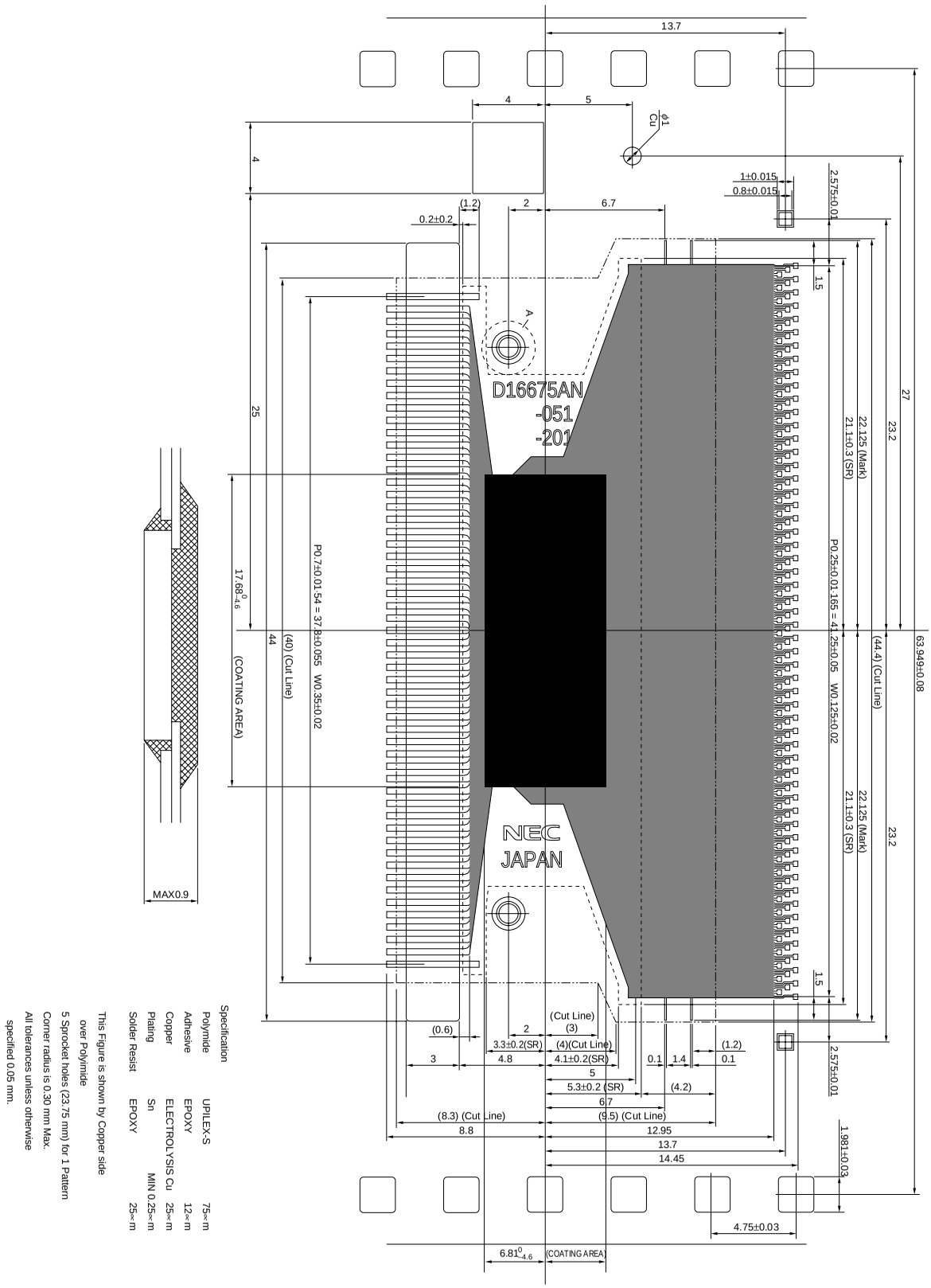


Reset



10. PACKAGE DRAWING

Standard TCP Drawing (μPD16675AN-051)



Specification

Polymide	UPILEX-S	75∝m
Adhesive	EPOXY	12∝m
Copper	ELECTROLYSIS Cu	25∝m
Plating	Sn	MIN 0.25∝m
Solder Resist	EPOXY	25∝m

This Figure is shown by Copper side over Polymide

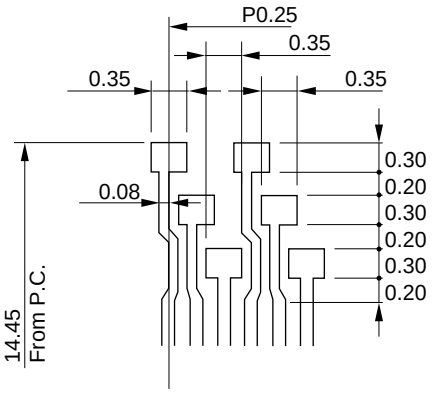
5 Sprocket holes (23.75 mm) for 1 Pattern

Corner radius is 0.30 mm Max.

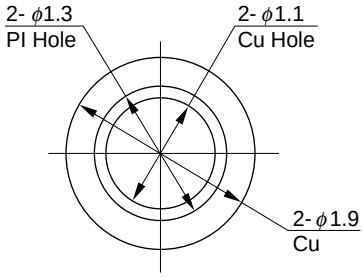
All tolerances unless otherwise specified 0.05 mm.

Standard TCP Drawing (μPD16675AN-051)

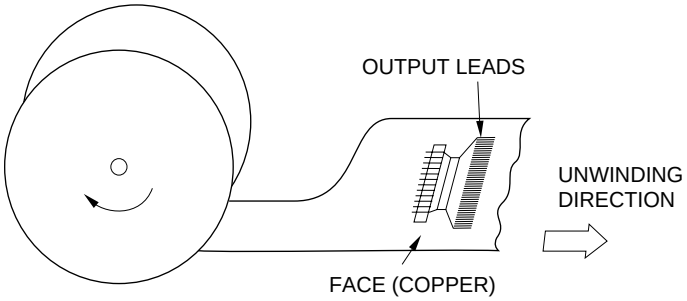
Detail of test pad



Detail of "A" part

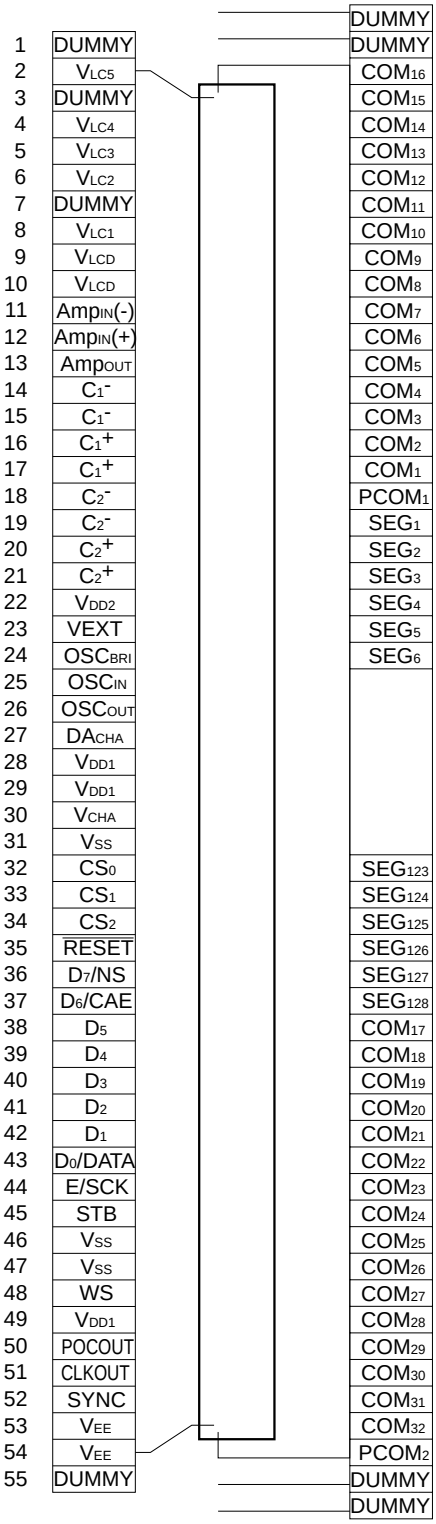


Tape unwinding direction



Standard TCP Drawing (μPD16675AN-051)

Pin configuration



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference

Document	Number
Quality Grades on NEC's Semiconductor Devices	C11531E
Semiconductor Device Mounting Technology Manual	C10535E

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5