NEC

MOS INTEGRATED CIRCUIT

μPD16432B

1/8, 1/15 DUTY LCD CONTROLLER/DRIVER

DESCRIPTION

The μPD16432B is a controller/driver with 1/8 and 1/15 duty dot matrix LCD display capability. It has 60 segment outputs, 10 common outputs, and 5 dual segment/common outputs, giving a maximum display capability of 12 columns × 2 lines (at 1/15 duty).

LED drive outputs, key scanning key source outputs, and key data inputs are also provided, making it ideal for use in a car stereo front panel, etc.

FEATURES

- Dot matrix LCD controller/driver
- Pictograph display segment drive capability (MAX. 64)
- LCD driver unit power supply V_{LCD} independently settable (MAX. 10 V)
- On-chip key scan circuit (8 × 4 matrix)
- Alphanumeric character and symbol display capability provided by on-chip ROM (5 × 7 dots)
  240 characters + 16 user-defined characters
- Display contents
  1/8 duty: 13 columns × 1 line, 64 pictograph displays, 4 LEDs
  1/15 duty: 12 columns × 2 lines, 60 pictograph displays, 4 LEDs
- Serial data input/output (SCK, $\overline{STB}$, DATA)
- On-chip oscillator
- Reduced power consumption possible using standby mode

ORDERING INFORMATION

Part Number	Package
μPD16432BGC-001-9EU	100-PIN PLASTIC TQFP (FINE PITCH, 14 × 14), Standard ROM code

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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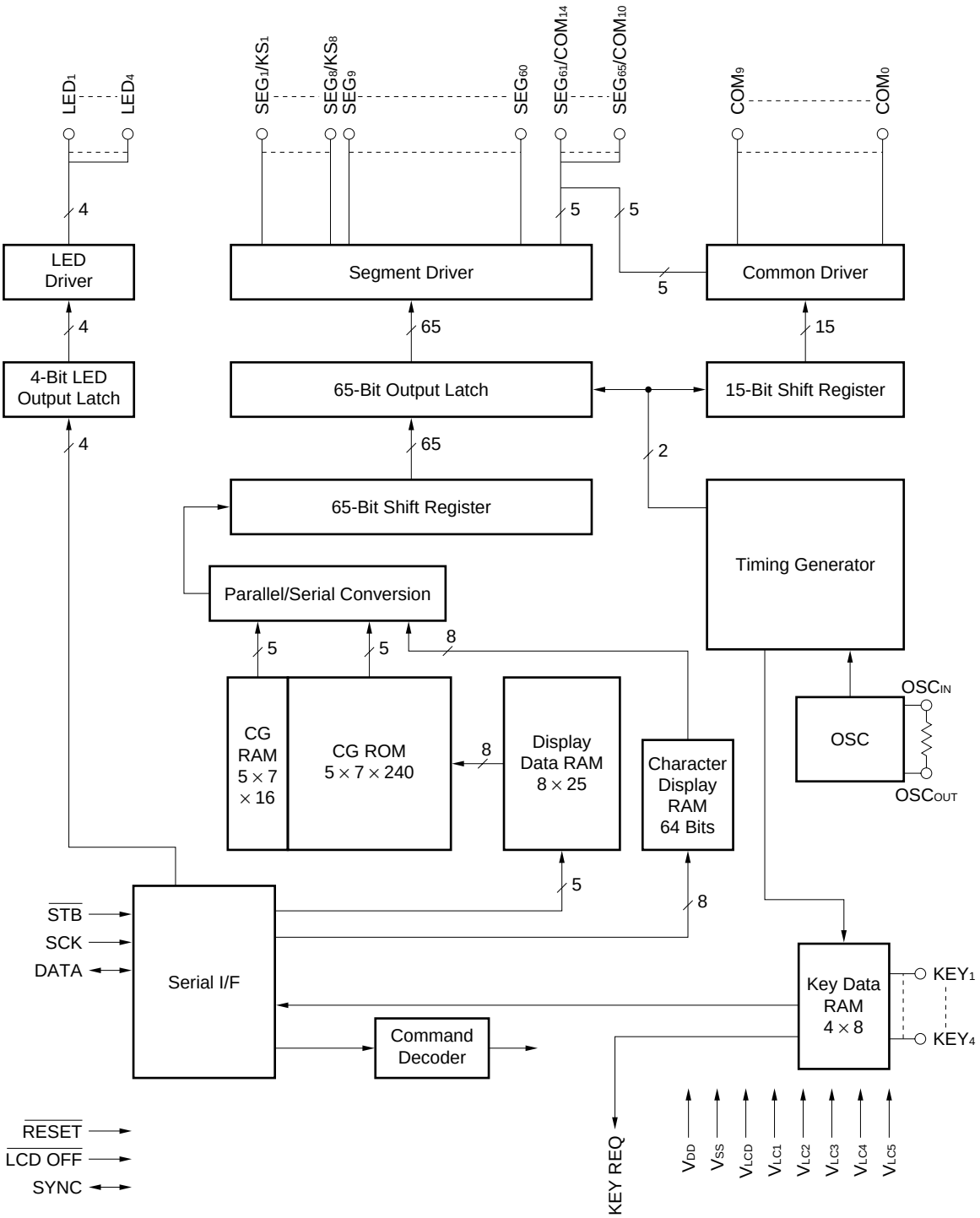
The mark ★ shows major revised points.

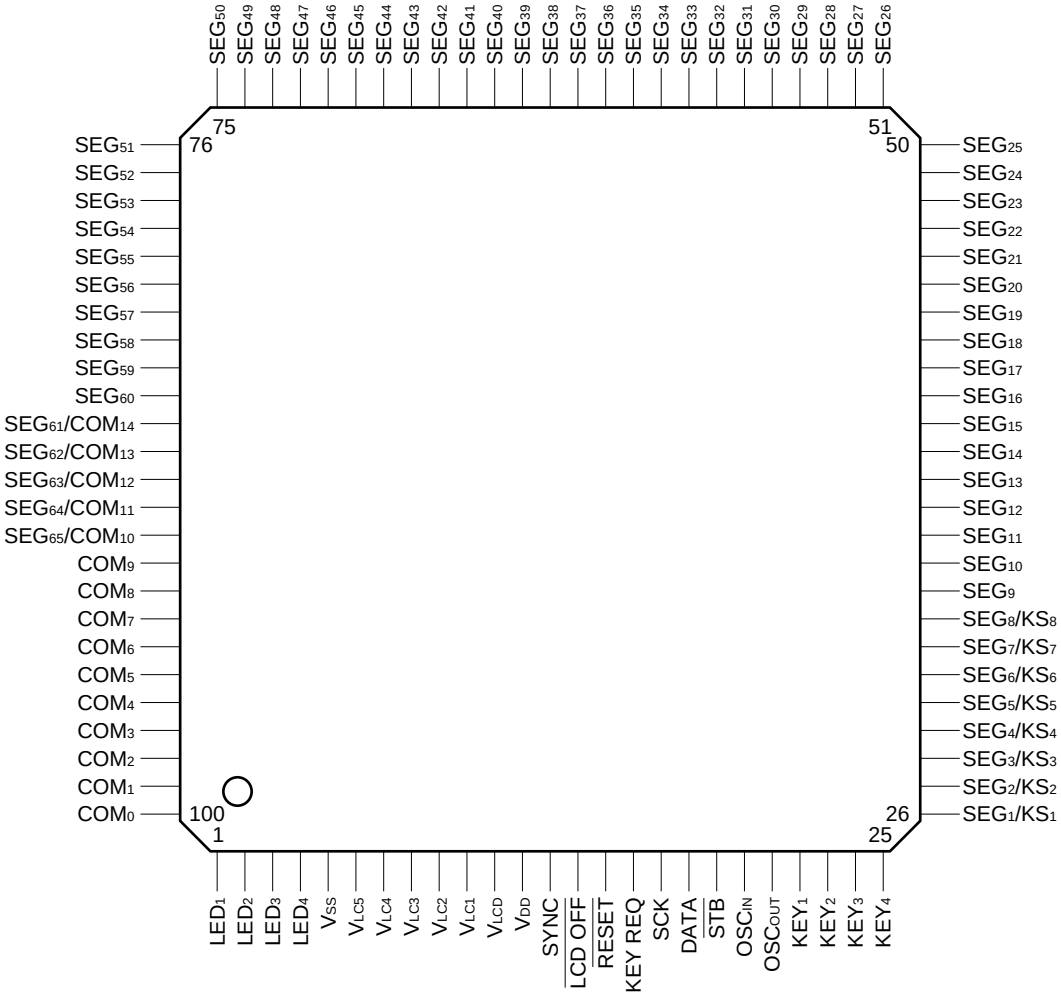
CONTENT

1. BLOCK DIAGRAM



2. PIN CONFIGURATION (Top view)

- **μPD16432BGC-001-9EU**



3. PIN DESCRIPTIONS

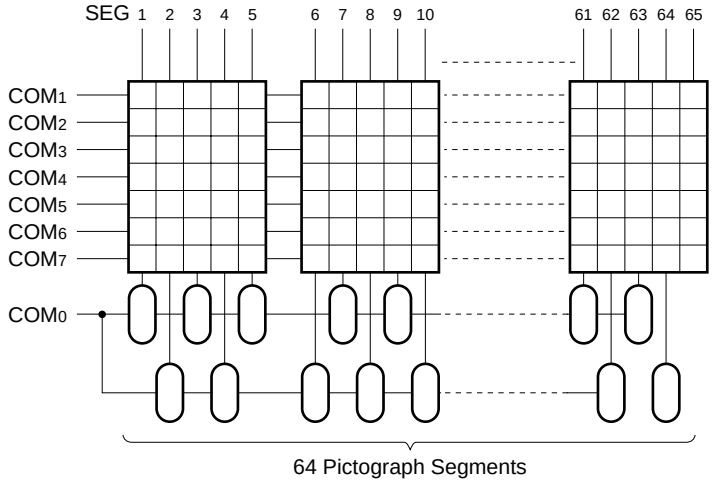
Symbol	Pin Name	Pin No.	I/O	Function
SEG_1/KS_1 to SEG_8/KS_8	Segment /key source dual-function	26 to 33	O	Pins with dual function as dot matrix LCD segment outputs and key scanning key source outputs
SEG_9 to SEG_{60}	Segment	34 to 85	O	Dot matrix LCD segment outputs
SEG_{61}/COM_{14} to SEG_{85}/COM_{10}	Segment /common dual-function	86 to 90	O	Switchable to either dot matrix LCD segment outputs or common outputs
COM_0 to COM_9	Common	91 to 100	O	Dot matrix LCD common outputs
LED_1 to LED_4	LED	1 to 4	O	LED outputs are Nch open-drain
SCK	Shift clock	17	I	Data shift clock. Data is read on rising edge, and output on falling edge.
DATA	Data	18	I/O	Performs input of commands, key data, etc., and key data output. Input is performed from the MSB on the rise of the shift clock, and the first 8 bits are recognized as a command. Output is performed from the MSB on the fall of the shift clock. Output is Nch open-drain.
$\overline{STB}$	Strobe	19	I	Data input is enabled when “H”. Command processing is performed on a fall.
KEY REQ	Key request	16	O	“H” if there is key data, “L” if there is none. Key data can be read irrespective of the state of this pin. Output is CMOS output.
$\overline{RESET}$	Reset	15	I	Initial state is set when “L”.
$\overline{LCD\ OFF}$	LCD off	14	I	When “L”, a forced LCD off operation is performed, and SEG_n & COM_n output the unselected waveform.
SYNC	Synchronization	13	I/O	Synchronization signal input/output pin. When 2 or more chips are used, wired-OR connection is made to each chip. A pull-up resistor is also required when one chip is used.
OSC_{IN}	Oscillation	20	I	Connect oscillator resistor. When an external oscillator is used, input a clock signal to the OSC_{IN} pin and leave the OSC_{OUT} pin open, depending on the setting status of the CLS pin.
★ OSC_{OUT}		21	O	
KEY_1 to KEY_4	Key data	22 to 25	I	Key scanning key data inputs
V_{DD}	Logic power supply	12	–	Internal logic power supply pin
V_{SS}	GND	5	–	GND pin
V_{LCD}	LCD drive voltage	11	–	LCD drive power supply pin
★ V_{LC1} to V_{LC5}	LCD drive power supply	10 to 6	–	Dot matrix LCD drive power supply. Connect V_{LC5} to ground when an internal oscillator is used.

4. PIN FUNCTION

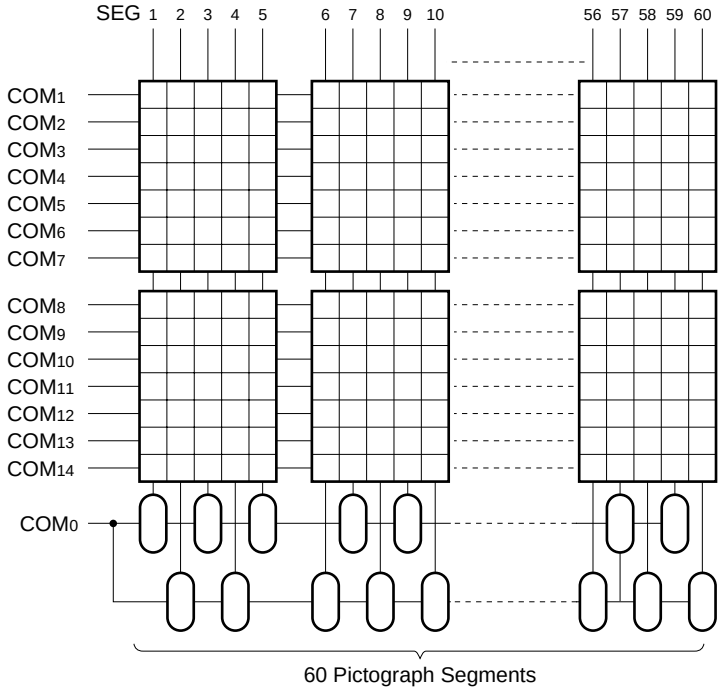
4.1 LCD Display

In the μPD16432B LCD display, a 5 × 7-segment display and pictograph display segments can be driven. The pictograph display segment common output is allocated to COM_0, and up to 64 can be driven.

(1) Example of 1/8 duty connections



(2) Example of 1/15 duty connections



4.2 Character Codes and Character Patterns

The relation between character codes and character patterns is shown below. Character codes 00H to 0FH are allocated to CGRAM.

Character codes 10H to 1FH and E0H to FFH are undefined.

Higher Bits / Lower Bits	0XH	1XH	2XH	3XH	4XH	5XH	6XH	7XH	8XH	9XH	AXH	BXH	CXH	DXH	EXH	FXH
X0HRAM	CG (1)															
X1HRAM	CG (2)															
X2HRAM	CG (3)															
X3HRAM	CG (4)															
X4HRAM	CG (5)															
X5HRAM	CG (6)															
X6HRAM	CG (7)															
X7HRAM	CG (8)															
X8HRAM	CG (9)															
X9HRAM	CG (10)															
XAHRAM	CG (11)															
XBHRAM	CG (12)															
XCHRAM	CG (13)															
XDHRAM	CG (14)															
XEHRAM	CG (15)															
XFHRAM	CG (16)															

4.3 Display RAM Addresses

Display RAM addresses are allocated as shown below irrespective of the display mode.

Column No.	1	2	3	4	5	6	7	8	9	10	11	12	13
Line 1	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH
Line 2	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	

4.4 Pictograph Display RAM Addresses

Pictograph display RAM addresses are allocated as shown below.

Address	Segment Output No.							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	1	2	3	4	5	6	7	8
01H	9	10	11	12	13	14	15	16
02H	17	18	19	20	21	22	23	24
03H	25	26	27	28	29	30	31	32
04H	33	34	35	36	37	38	39	40
05H	41	42	43	44	45	46	47	48
06H	49	50	51	52	53	54	55	56
07H	57	58	59	60	61	62	63	64

Remark When 1/15 duty is used (12 columns × 2 lines), 61 to 64 are disabled.

4.5 CGRAM Column Addresses

A maximum of any sixteen 5 × 7-dot characters can be written in CGRAM. The row address within one character is allocated as shown below, and is specified by bits b7 to b5.

The character code for which a write is to be performed must be specified beforehand with an address setting command.

Row Address	Dot Data							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	0	0	0	*	*	*	*	*
01H	0	0	1	*	*	*	*	*
02H	0	1	0	*	*	*	*	*
03H	0	1	1	*	*	*	*	*
04H	1	0	0	*	*	*	*	*
05H	1	0	1	*	*	*	*	*
06H	1	1	0	*	*	*	*	*

Row Address　　Font Data (5 × 7 Dots)

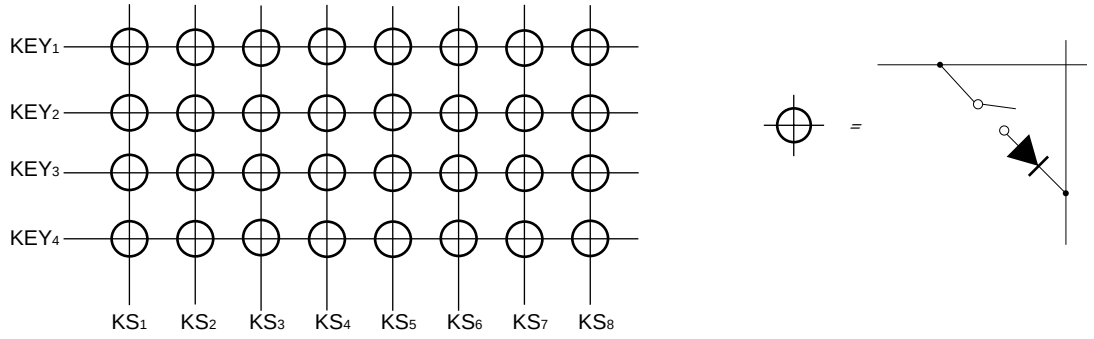
Remark * : Font data (1: ON, 0: OFF)

★ 4.6 Configuring a Key Matrix

Examples of key matrix configurations are shown below.

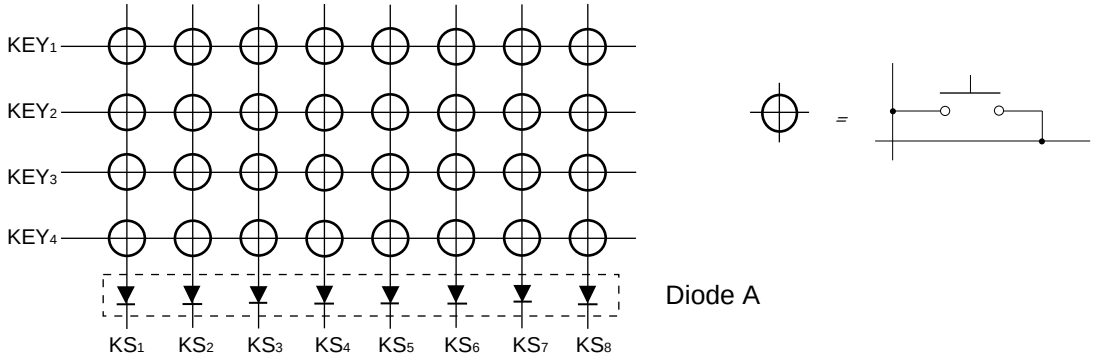
(1) Assumed case when 3 or more keys simultaneously pressed

A configuration example is shown below. In this kind of configuration, between 0 and 32 switches in the ON state can be identified.



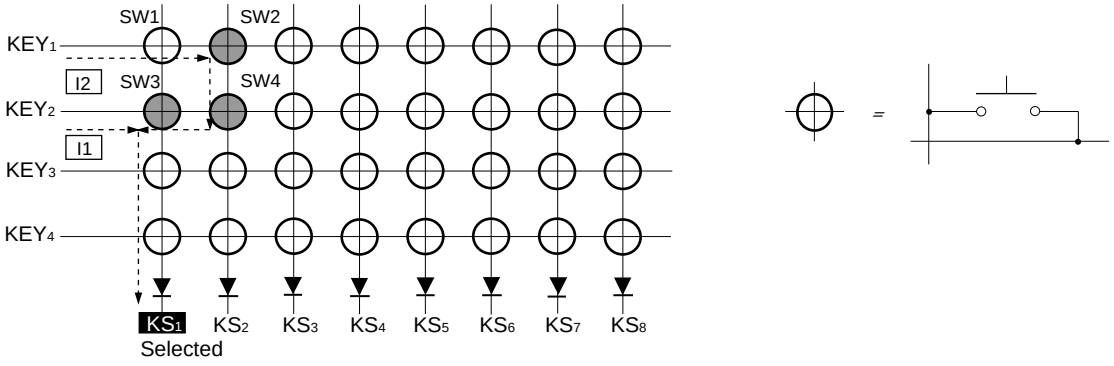
(2) Assumed case when 2 or fewer keys simultaneously pressed

A configuration example is shown below. In this kind of configuration, between 0 and 2 switches in the ON state can be identified.



In this example, if 3 or more keys are simultaneously pressed, switches in the OFF state may be inadvertently judged as being ON.

Take, for example, the case shown below where SW2 to SW4 are ON and KS_1 is selected (low level). Normally, the I1 current would flow and SW3 would be detected as being in the ON state. However, because SW2 and SW4 are ON, the I2 current flows, and SW1 is mistakenly identified as being ON.



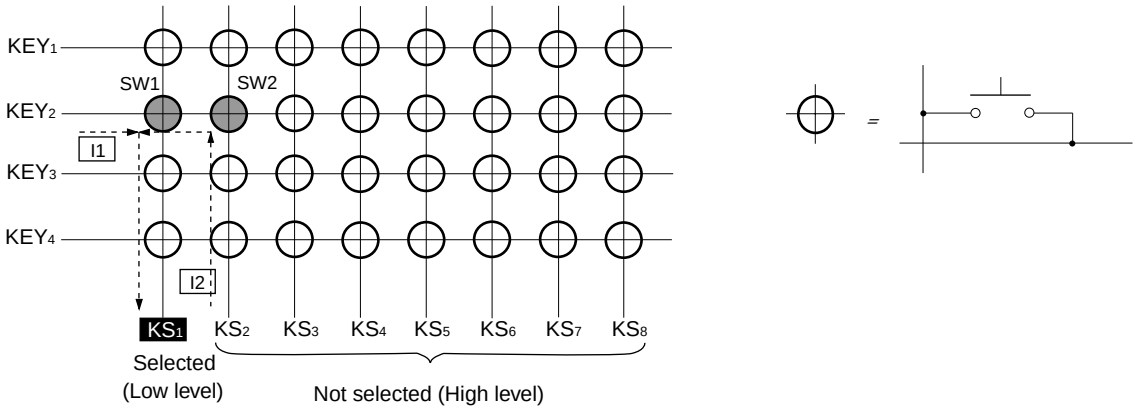
Also, if diode A is not connected, not only will the key data be unable to be read correctly, but the LCD may also be affected and the IC damaged or its characteristics degraded.

Take, for example, the case shown below where SW1 and SW2 are ON, and KS_1 is selected (low level). In this case, in addition to I1, which is the current that normally flows, the short current between KS_1 and KS_2 (I2) also flows, potentially causing the following three problems.

<1> Incorrect transmission of the level to KEY_2 will prevent the key data from being latched properly.

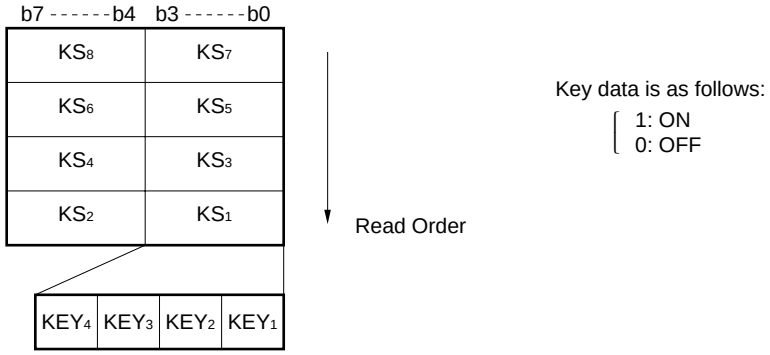
<2> Because KS_1 and KS_2 have alternate functions as SEG outputs, the LCD will not display correctly.

<3> The flowing of the short current between KS_2 (high level) and KS_1 (low level) (I2) will damage or degrade the IC.

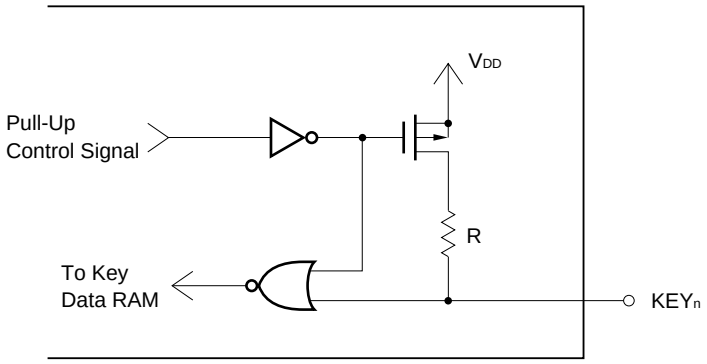


4.7 Construction of Key Data RAM

Key data is stored as shown below, and is read in MSB-first order by a read command.



4.8 Key Input Equivalent Circuit



Remark In the event of key source output, the pull-up control signal becomes “H”, and the pull-up transistor is turned on.

4.9 Key Request (KEY REQ)

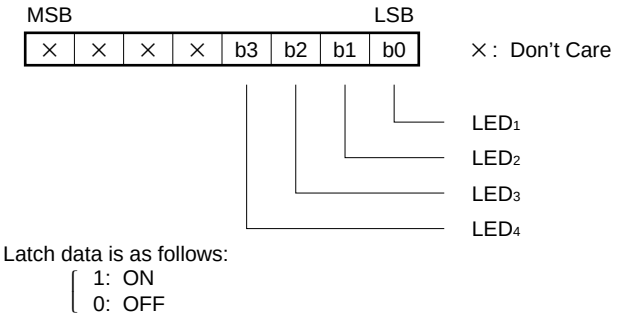
A key request is output as shown below according to the state.

State	KEY REQ[Note]	Key Scan Internal Pull-Up Resistor
In key scan operation	High level is output while any key data is "1".[Note]	During key scan : ON During display : OFF
In standby mode or when SEG_n & COM_n are fixed at V_{LC5}	High level is output in case of key input only.	Always ON
When key scanning is stopped	Fixed at low level	Always OFF

Note KEY REQ does not become low until the key data is all "0" (It is not synchronized with the key data reads).

4.10 LED Output Latch Configuration

The low-order 4 bits of the LED output latch are enabled, and the high-order 4 bits disabled, as shown below.



4.11 Commands

Commands set the display mode and status.

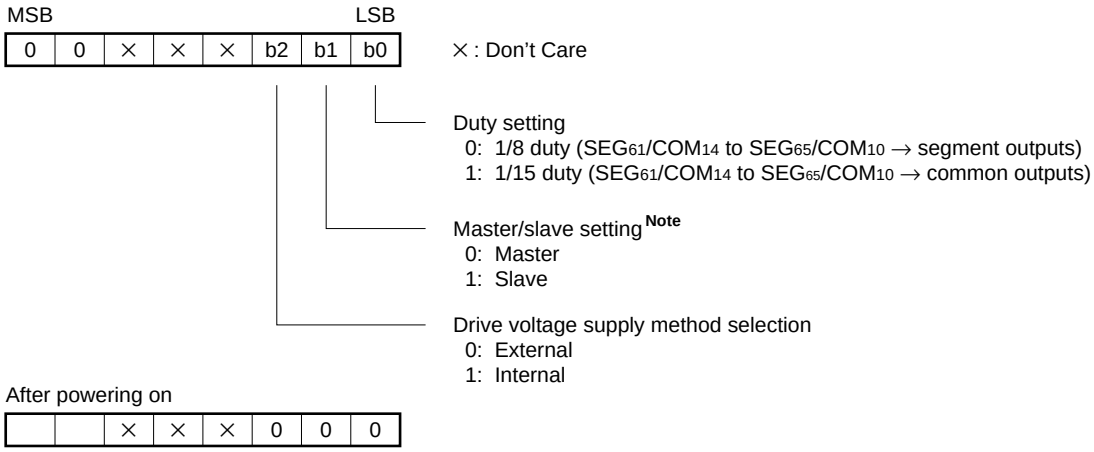
The first byte after a rise edge on the $\overline{STB}$ pin is regarded as a command.

If $\overline{STB}$ is driven low during command/data transfer, serial communication is initialized and the command/data being transferred is invalidated (However, a command or data that has already been transferred is valid).

(1) Display Setting Command

This command initializes the μPD16432B, and sets the duty, number of segments, number of commons, master/slave operation, and the drive voltage supply method. When multiple chips are used, only the chip that sent the command is enabled. If initialization is performed during display, the display may be affected (especially when multiple chips are used).

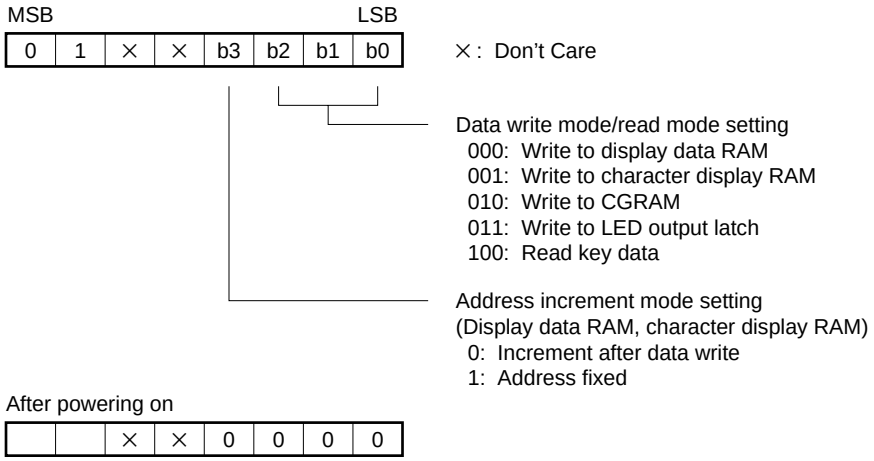
The state set when this command is executed is: LCD off, LED on, key scanning stopped. To restart the display, it is necessary to execute "status command" normal operation. However, nothing is done if the same mode is selected.



★ **Note** Please set only one μPD16432B to master, and the other to slave when in multi-chip mode. And please set to master, when in single chip mode.

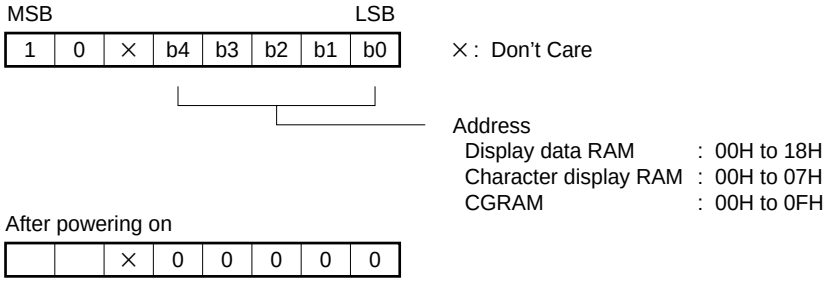
(2) Data Setting Command

Sets the data write mode, read mode, and address increment mode.



(3) Address Setting Command

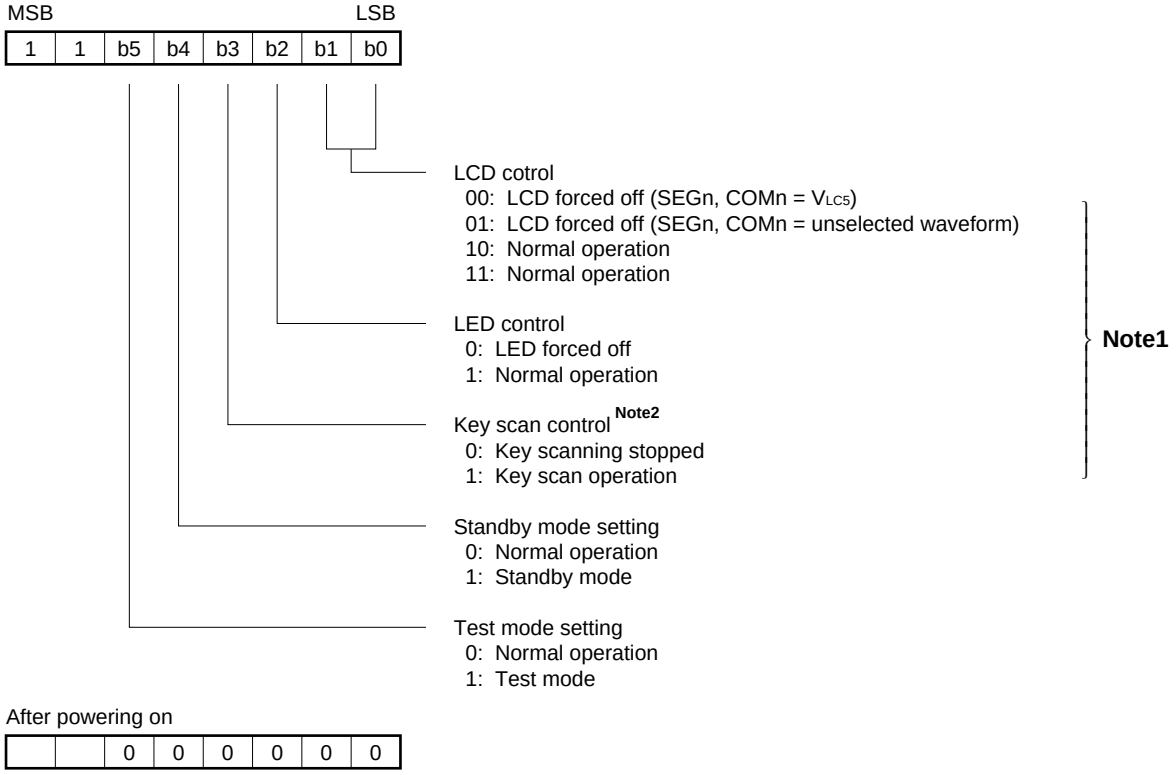
Sets the display data RAM or character display RAM address.



Caution If an unspecified address is set, data cannot be written until a correct address is next set. The address is not incremented even in increment mode.

(4) Status Command

Controls the status of the μPD16432.



Notes 1. The following states are use prohibited modes, and key scanning does not operate if these states are set.

		0	0	1	0	0	0

		0	0	1	1	0	0

★ **2.** The key data input operation is stopped. The key source signals from SEGn pin are output even in this state.

4.12 Standby Mode

If standby mode is selected with bit b4 of the status command, the following state is set irrespective of bits b3 to b0 of the status command.

(1) LCD forced off (SEG_n, $COM_n = V_{LC5}$)
(2) LED forced off
(3) Key scanning stopped (but KEY_n = key input wait)
(4) OSC stopped

There are two ways of releasing standby mode, as follows:

(a) Using Status Command
(b) Using KEY_n

(a) Using Status Command

Select normal operation with bit b4 of the status command.

Table 4-1 Example of Use of Status Command

Item	$\overline{STB}$	Command/Data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Standby mode	L									
Status command	H	1	1	0	0	0	0	0	0	Standby release (OSC oscillation start), LCD control off (SEG_n, $COM_n = V_{LC5}$), LED forced off, key scanning stopped
Standby transition time	L									10 μs[Note]
Status command	H	1	1	0	0	1	1	1	0	Normal operation
End	L									

Note If LCD normal operation or key scan operation is initiated within the standby transition time, the LCD may flicker.

(b) Using KEY$_n$

If any key is set to the ON state, the standby mode is released and OSC oscillation starts. Also, KEY REQ is set to “H”, informing the microcomputer that a key has been pressed and standby mode has been released. In this state, the key data is not memorized, and therefore it is necessary to set key scanning to the normal state after the standby transition time, and fetch the key data.

Table 4-2 Example of Use of KEY$_n$

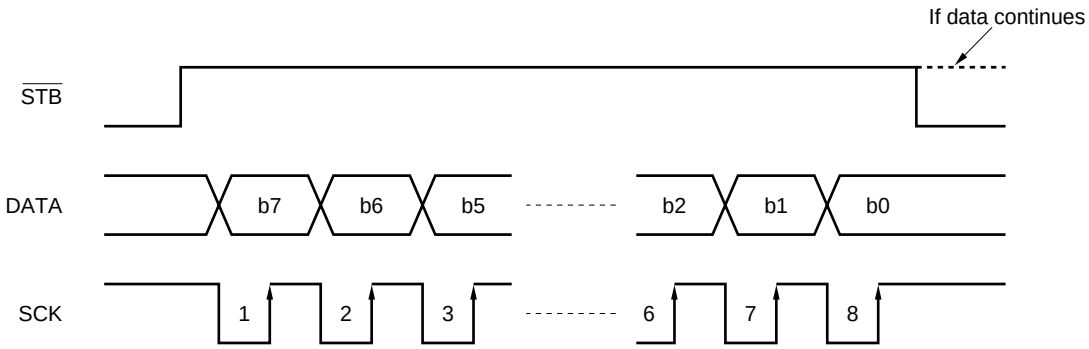
Item	$\overline{STB}$	Command/Data								Description
		b7	b6	b5	b4	b3	b2	b1	b0	
Standby mode	L									
Key data present	L									Standby release (KEY REQ = H, OSC oscillation start)
Standby transition time	L									10 μs[Note]
Status command	H	1	1	0	0	1	0	0	1	LCD forced off (unselected waveform), LED forced off, key scan operation
Key scan	L									1 frame or more
Data setting command	H	0	1	0	0	0	1	0	0	Key data read, address increment
Key data	H	*	*	*	*	*	*	*	*	For KS$_8$, KS$_7$
Key data	H	*	*	*	*	*	*	*	*	For KS$_6$, KS$_5$
Key data	H	*	*	*	*	*	*	*	*	For KS$_4$, KS$_3$
Key data	H	*	*	*	*	*	*	*	*	For KS$_2$, KS$_1$
End	L									Key distinction

Note If LCD normal operation or key scan operation is initiated within the standby transition time, the LCD may flicker.

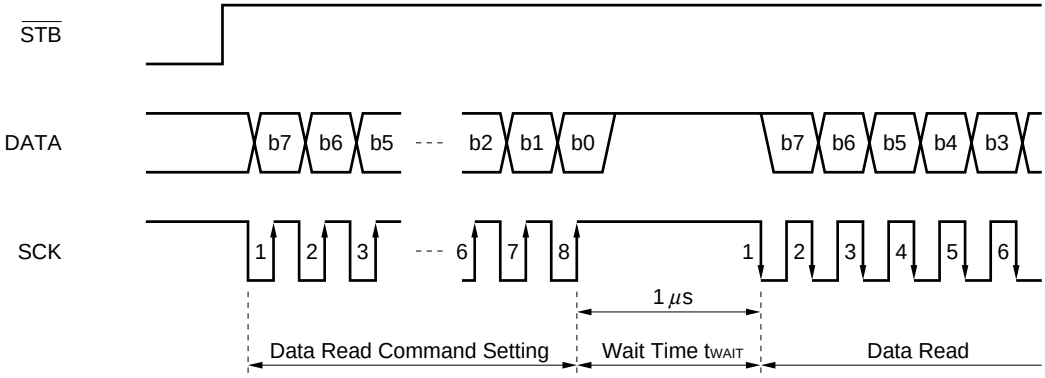
Remark * : key data (1:ON, 0 : OFF)

4.13 Serial Communication Formats

(1) Reception (Command/Data Write)



(2) Transmission (Command/Data Read)



Caution As the DATA pin is an Nch open-drain output, a pull-up resistor must be connected externally (1 kΩ to 10 kΩ).

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25℃, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	–0.3 to +7.0	V
Logic input voltage	V_{IN}	–0.3 to +V_{DD} + 0.3	V
Logic output voltage (D_{OUT}, LEDn)	V_{OUT}	–0.3 to +7.0	V
LCD drive supply voltage	V_{LCD}	–0.3 to +12.0	V
LCD drive power supply input voltage	V_{LC1} to V_{LC5}	–0.3 to +V_{LCD} + 0.3	V
Driver output voltage (Segment, Common)	V_{OUT2}	–0.3 to +V_{LCD} + 0.3	V
LED drive current	I_{OL1}	20	mA
Package allowable dissipation	P_T	1000	mW
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature range	T_{stg}	–55 to +150	°C

★ **Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Recommended Operating Ranges

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD}		2.7	5.0	5.5	V
LCD drive supply voltage	V_{LCD}		V_{DD}	8.0	10.0	V
Logic input voltage	V_{IN}		0		V_{DD}	V
Driver input voltage	V_{LCD1} to V_{LCD5}		0		V_{LCD}	V
LED drive current	I_{OL1}				15	mA

Electrical Characteristics (Unless specified otherwise, T_A = -40 to +85℃, V_{DD} = 5 V ±10%, V_{LCD} = 8 V ±10%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.3 V_{DD}	V
High-level input current	I_{IH}	SCK, $\overline{STB}$, $\overline{LCDOFF}$, $\overline{RESET}$, KEY_1 to KEY_4			1	μA
Low-level input current	I_{IL}	SCK, $\overline{STB}$, $\overline{LCD\ OFF}$, $\overline{RESET}$, KEY_1 to KEY_4			–1	μA
Low-level output voltage	V_{OL1}	LED_1 to LED_4, I_{OL1} = 15 mA			1.0	V
High-level output voltage	V_{OH2}	OSC_{OUT}, KEY REQ, I_{OH2} = –1 mA	0.9 V_{DD}			V
Low-level output voltage	V_{OL2}	DATA, OSC_{OUT}, SYNC, I_{OL2} = 4 mA			0.1 V_{DD}	V
High-level leak current	I_{LOH2}	DATA, SYNC, $V_{IN/OUT}$ = V_{DD}			1	μA
Low-level leak current	I_{LOL2}	DATA, SYNC, $V_{IN/OUT}$ = V_{SS}			–1	μA
Common output ON-resistance	R_{COM}	V_{LCD} to V_{LC5} → COM_0 to COM_{14}, | I_O | = 100 μA			2.4	kΩ
Segment output ON-resistance	R_{SEG}	V_{LCD} to V_{LC5} → SEG_1 to SEG_{60}, | I_O | = 100 μA			4.0	kΩ
Current consumption (Logic)	I_{DD1}	Normal operation[Note], V_I = V_{DD} or V_{SS}, f_{OSC} = 250 kHz			500	μA
	I_{DD2}	Standby mode, V_I = V_{DD} or V_{SS}, f_{OSC} stopped			5	μA
Current consumption (Driver)	I_{LCD1}	Normal operation, internal bias selected, no load			1000	μA
	I_{LCD2}	Standby mode, internal bias used, no load			5	μA

Note Normal operation: V_{DD} = 5 V, V_{LCD} = 8 V

Switching Characreristics (Unless Specified Otherwise, T_A = -40 to +85℃, V_{DD} = V_{LCD} = 5 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{OSC}	R = 100 kΩ	175	250	325	kHz
Output data delay time	t_{PZL}	SCK ↓ → DATA ↓			100	ns
Output data delay time	t_{PLZ}	SCK ↓ → DATA ↑			300	ns
SYNC delay time	t_{DSYNC}				1.5	μs

Remarks 1. The time for one frame is found as follows.

1 frame = 1/f_{OSC} × 128 clocks × duty number + 1/f_{OSC} × 64 clocks

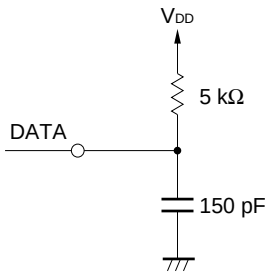
If f_{OSC} = 250 kHz and duty = 1/15, 1 frame = 4 μs × 128 × 15 + 4 μs × 64 = 7.94 ms

2. TYP. values are reference values for T_A = 25°C.

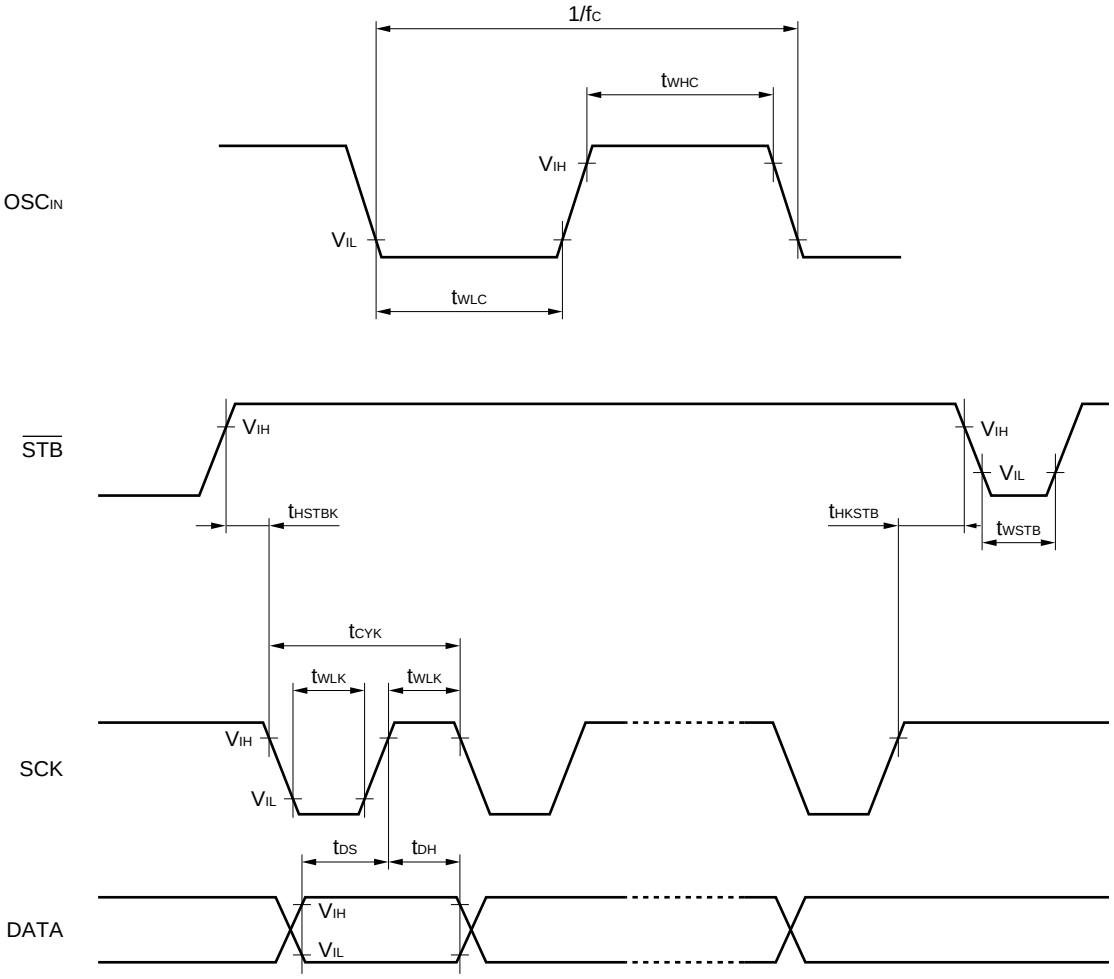
Required Timing Conditions (Unless Specified Otherwise, T_A = -40 to +85℃, V_{DD} = 5 V ±10%, V_{LCD} = 8 V ±10%, R_L = 5 kΩ, C_L = 150 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{OSC}	OSC_{IN} external clock	100		500	kHz
High-level clock pulse width	t_{WHC}	OSC_{IN} external clock	1		5	μs
Low-level clock pulse width	t_{WLC}	OSC_{IN} external clock	1		5	μs
Shift-clock cycle	t_{CYK}	SCK	900			ns
High-level shift clock pulse width	t_{WHK}	SCK	400			ns
Low-level shift clock pulse width	t_{WLK}	SCK	400			ns
Shift clock hold time	t_{HSTBK}	$\overline{STB}$ ↑ → SCK ↓	1.5			μs
Data setup time	t_{DS}	DATA → SCK ↑	100			ns
Data hold time	t_{DH}	SCK ↑ → DATA	200			ns
STB hold time	t_{HKSTB}	SCK ↑ → $\overline{STB}$ ↓	1			μs
STB hold time	t_{WSTB}		1			μs
Wait time	t_{WAIT}	8th SCK ↑ → 9th SCK ↓, in data read	1			μs
SYNC removal time	t_{SREM}		250			ns
Standby transition time	t_{PSTB}		10			μs
Reset pulse width	t_{WRS}	RESET	0.1			μs
Power-ON reset time	t_{PON}	From Power-ON	4			CLK

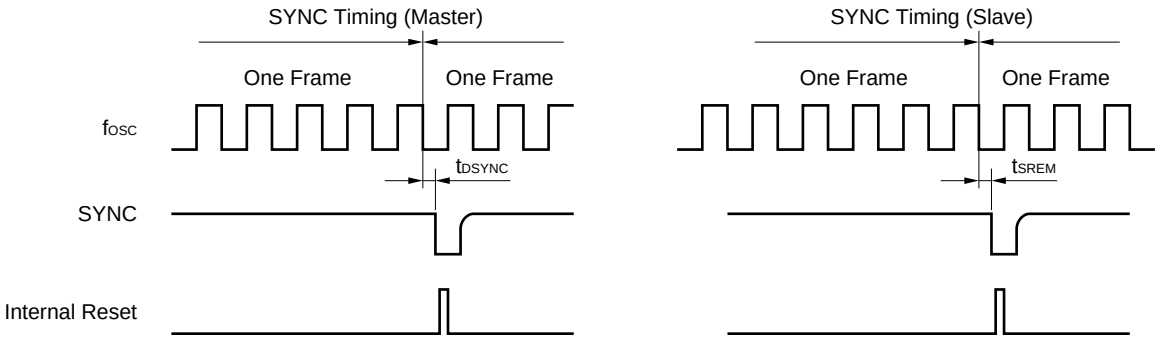
Output Load Circuit

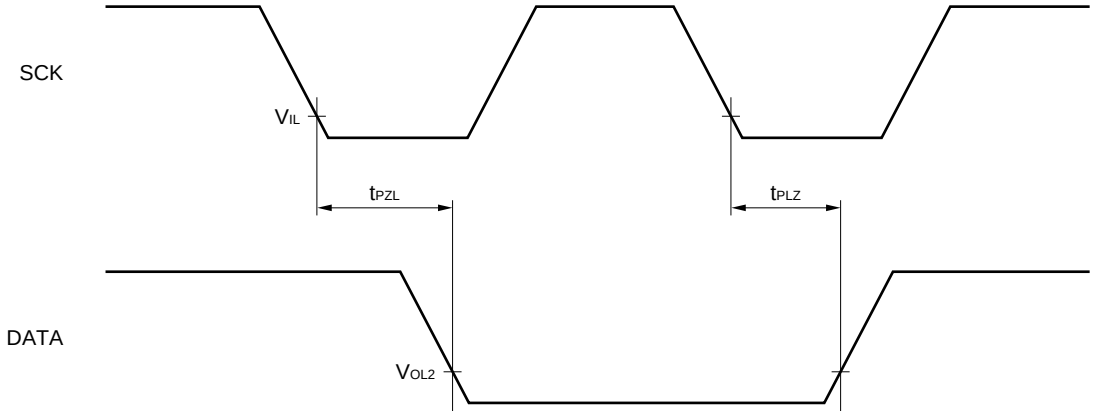


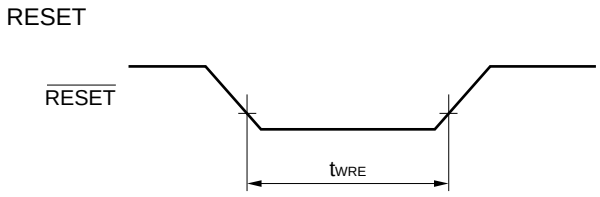
Switching Specifications Waveform Diagrams (1/2)



Switching Specification Waveform Diagrams (2/2)



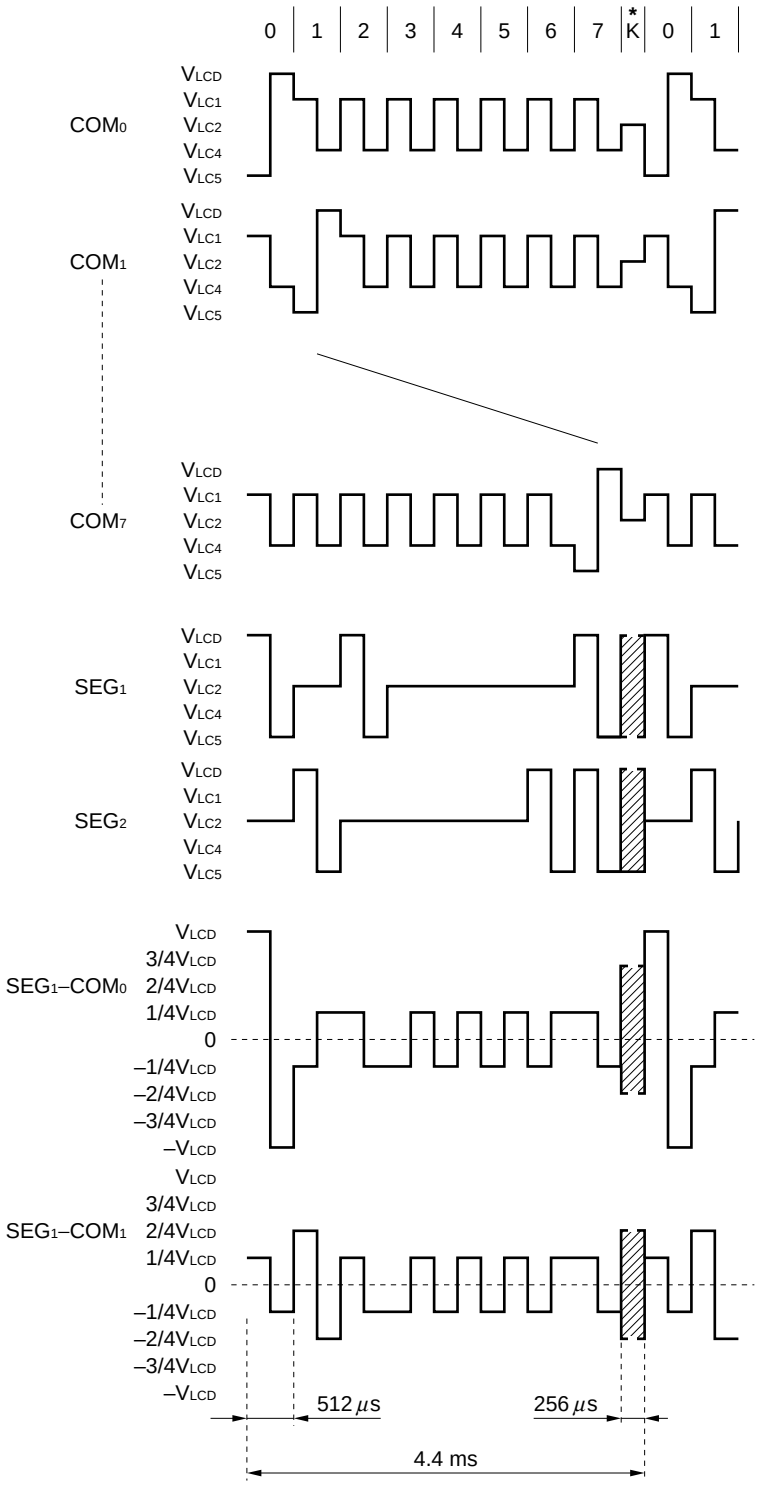




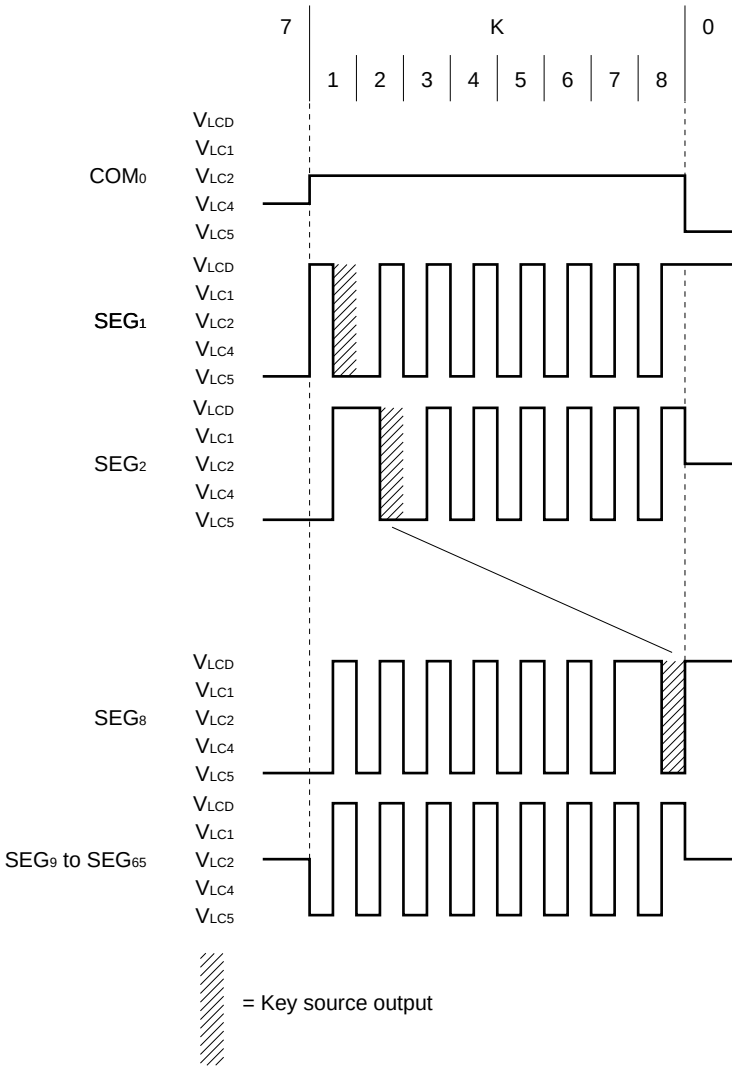
Output Waveforms

(1) 1/8 Duty (1/4 Bias: V_{LC2}: V_{LC3})

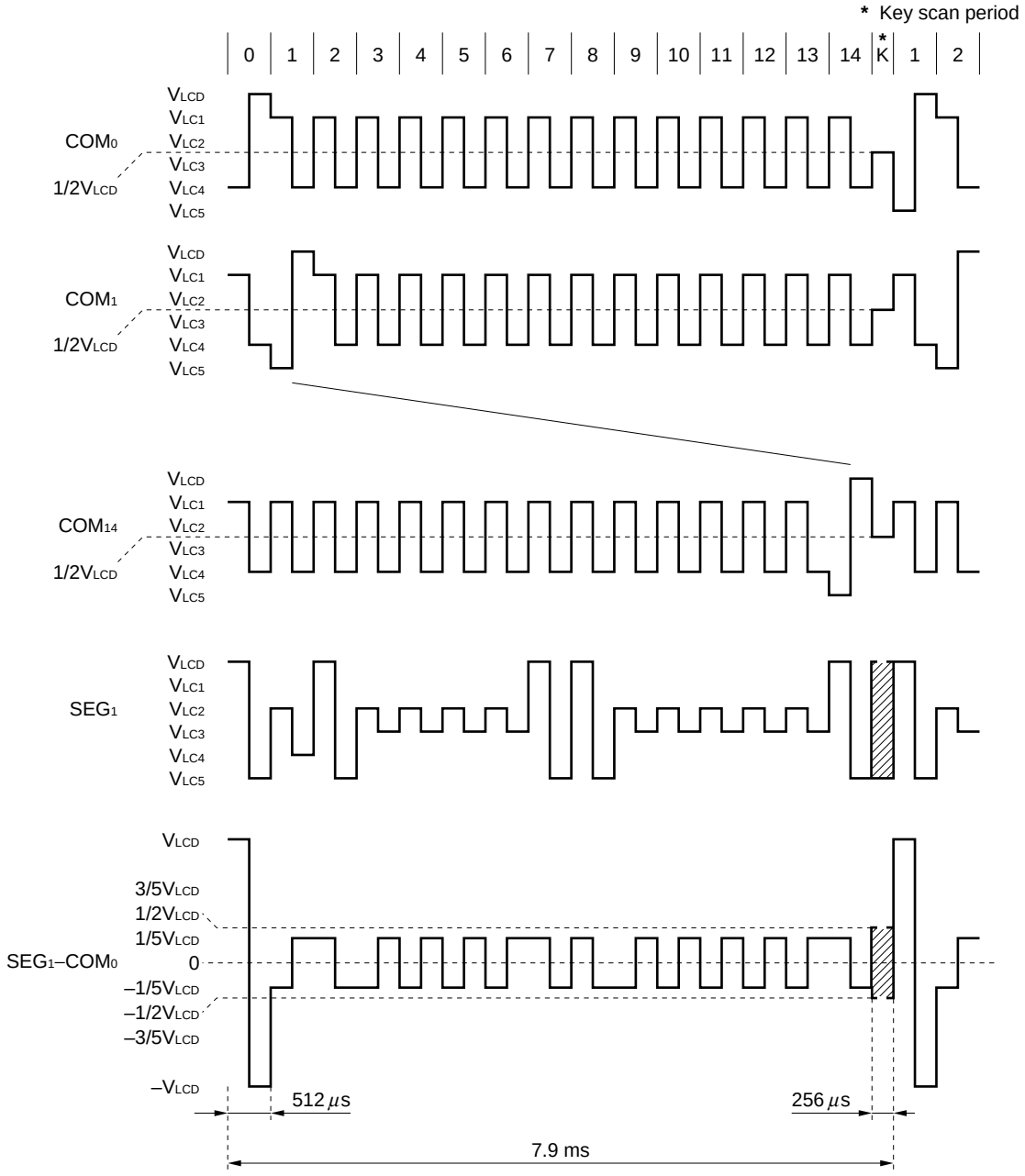
* Key scan period



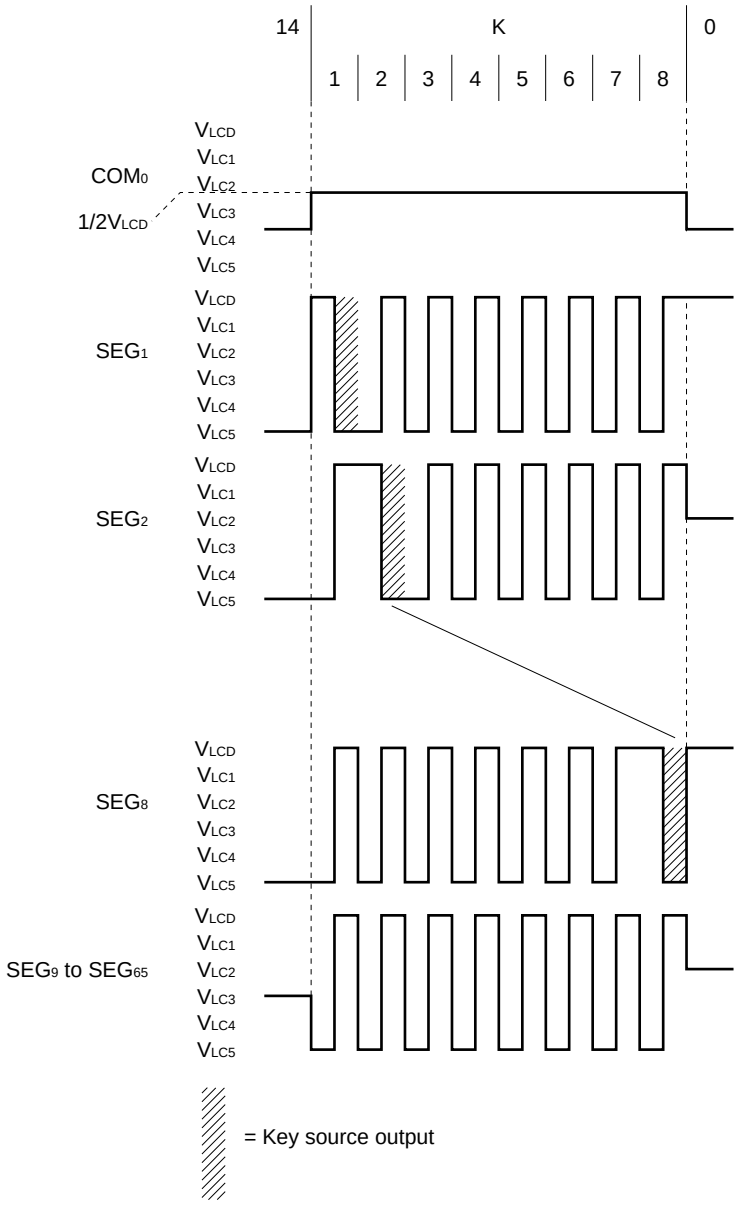
Enlargement of Key Scan Period



(2) 1/15 Duty (1/5 Bias)



Enlargement of Key Scan Period

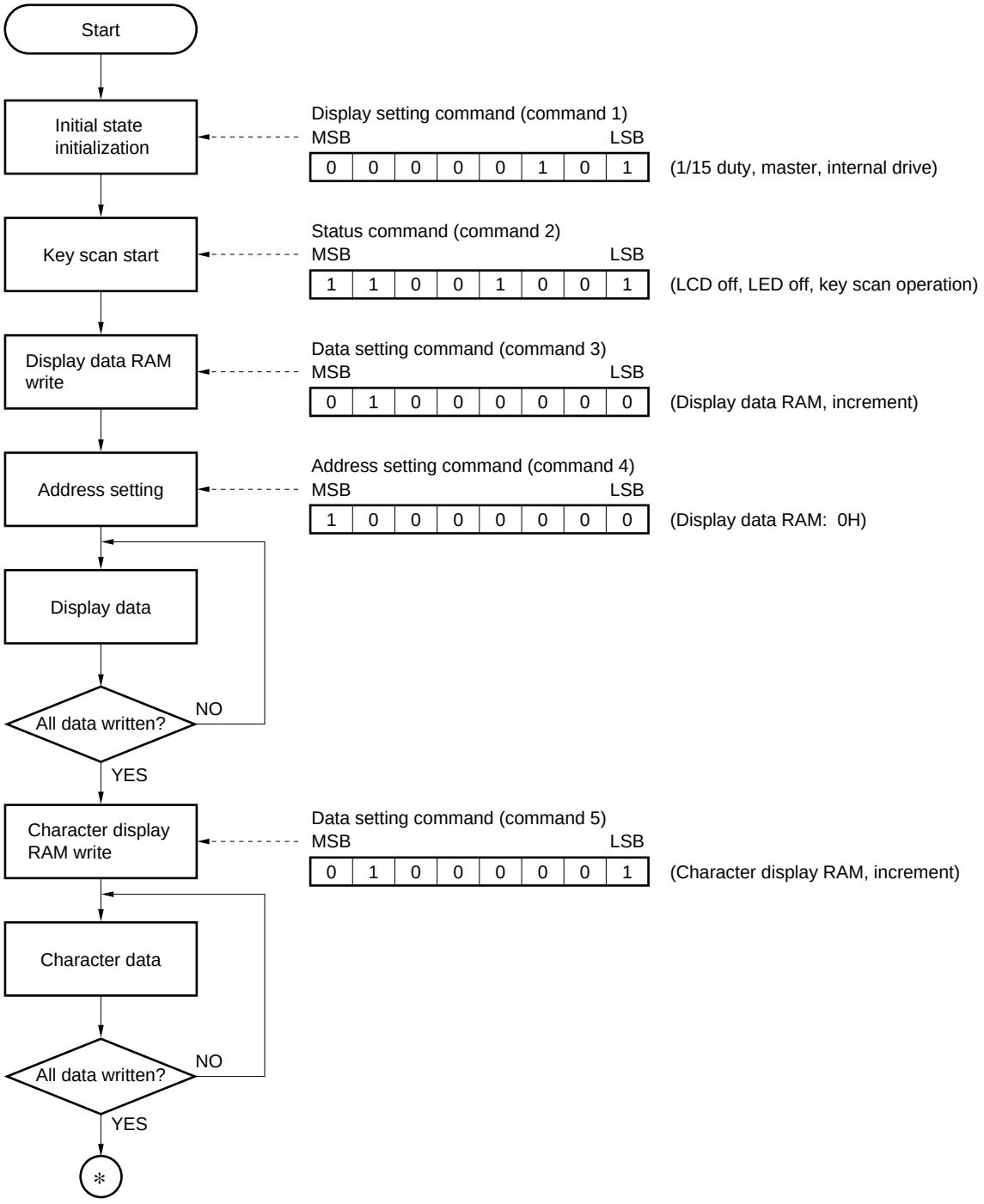


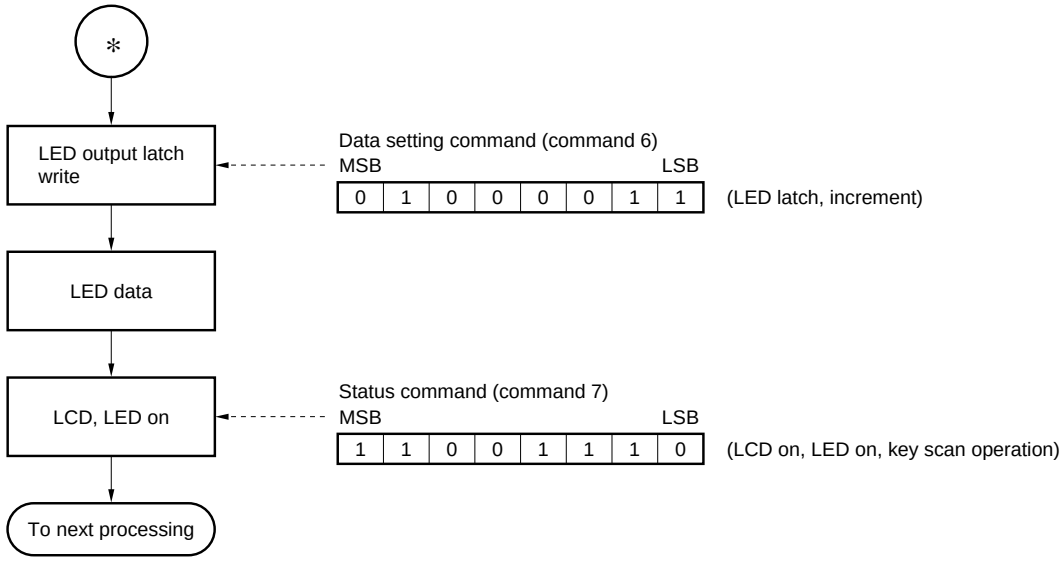
6. ACCESS PROCEDURES

Access procedures are illustrated below by means of flowcharts and timing charts.

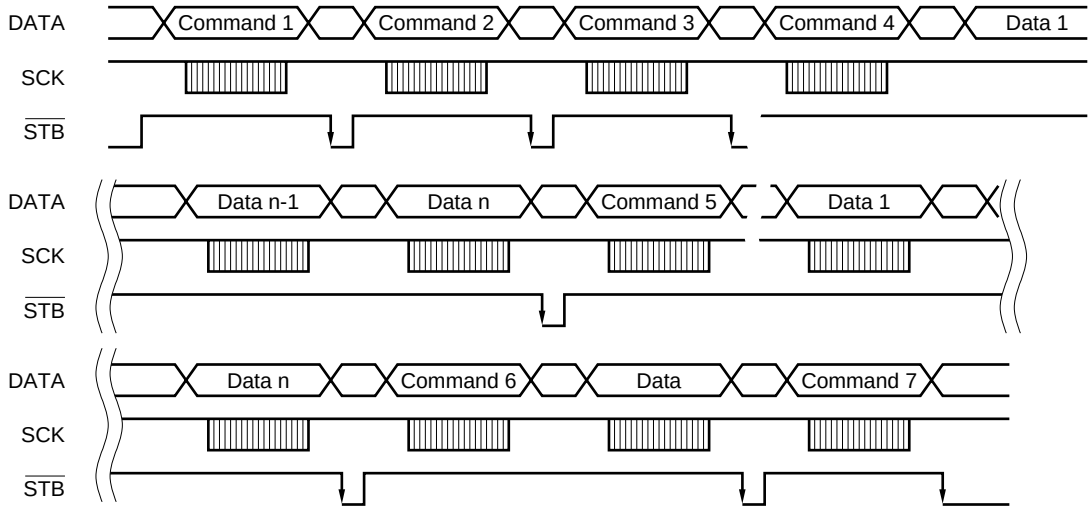
6.1 Initialization

(1) Flowchart



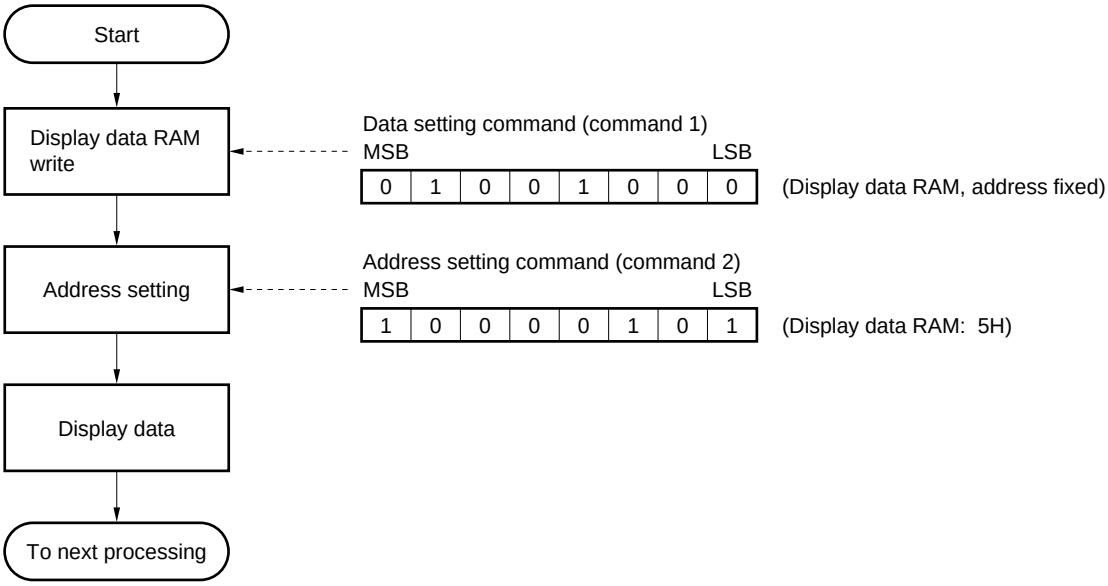


(2) Timing chart

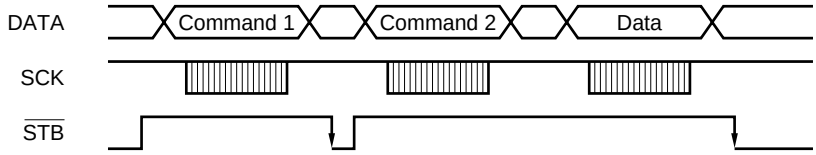


6.2 Display Data Rewrite (Address Setting)

(1) Flowchart

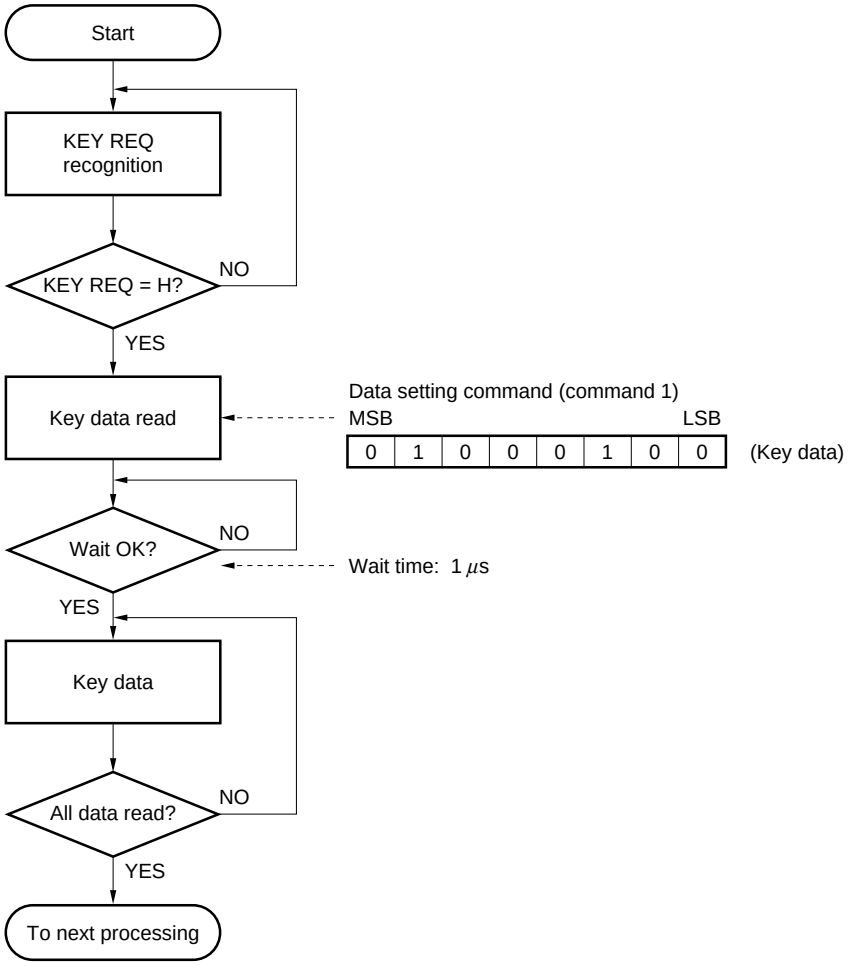


(2) Timing chart

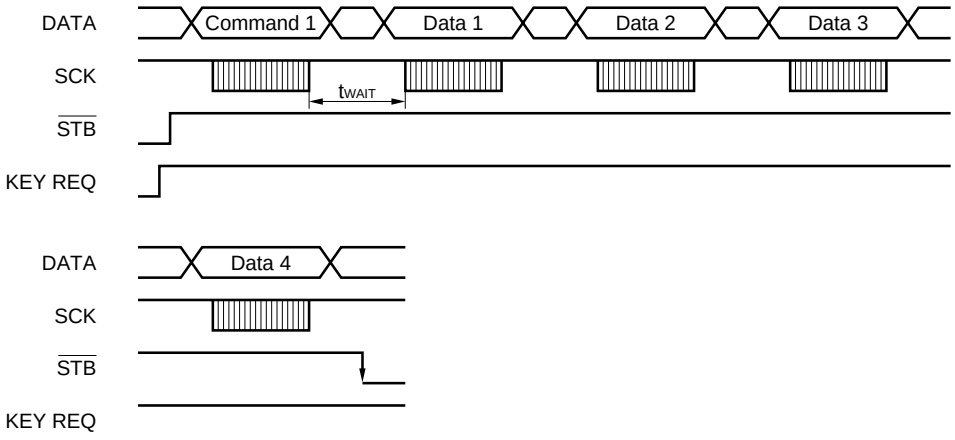


6.3 Key Data Read

(1) Flowchart



(2) Timing chart

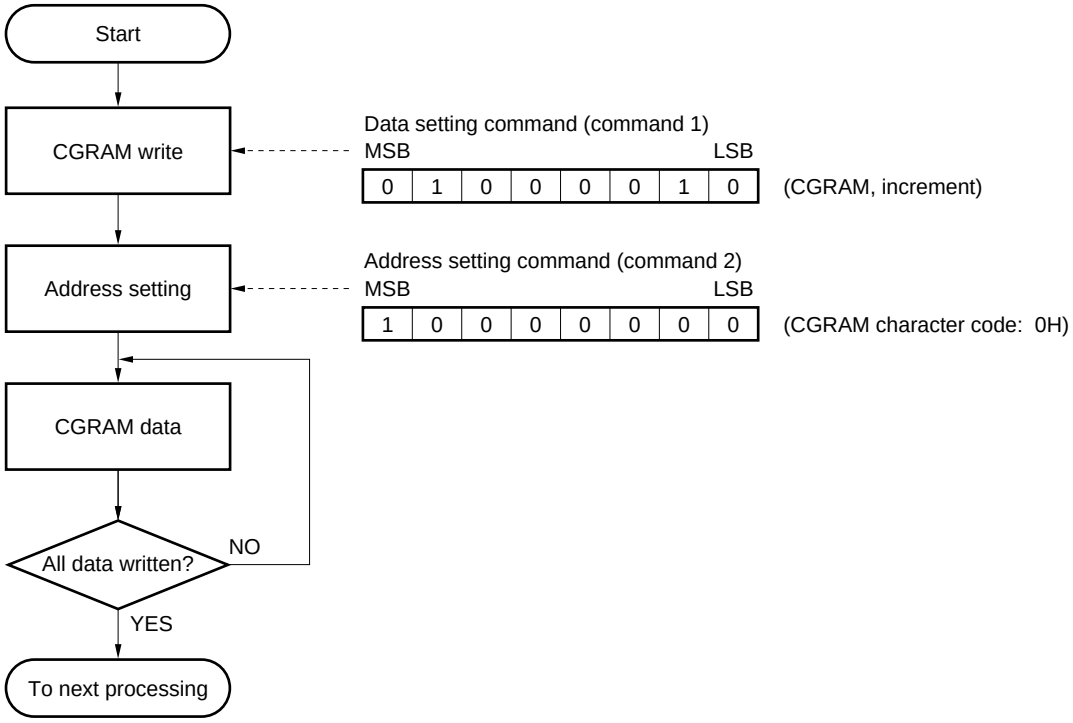


Cautions 1. Wait time t_{WAIT} (1 μs) is necessary from the rise of the 8th shift clock of command 1 until the fall of the 1st shift clock of data 1.

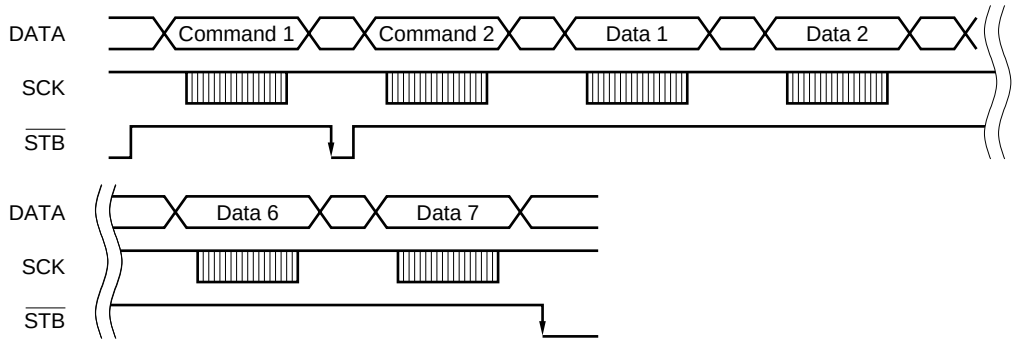
2. KEY REQ does not become low until the key data is all "0".
(It is not synchronized with the key data reads.)

6.4 CGRAM Write

(1) Flowchart

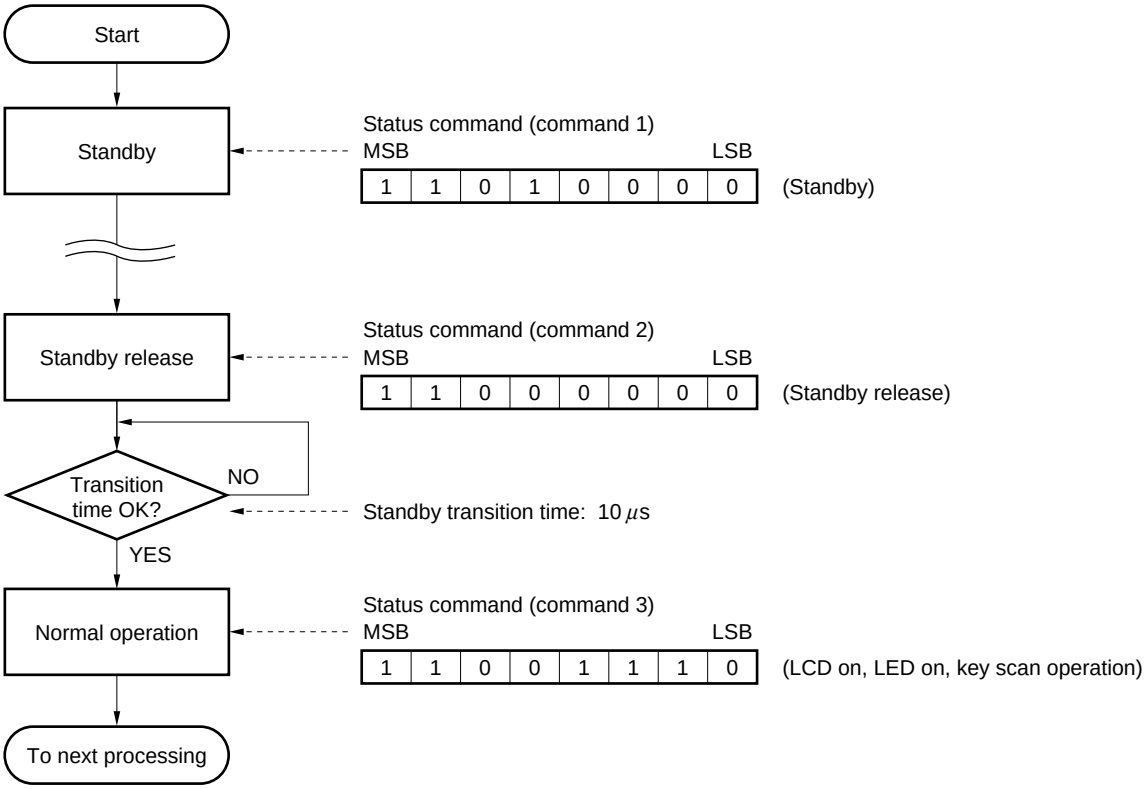


(2) Timing chart

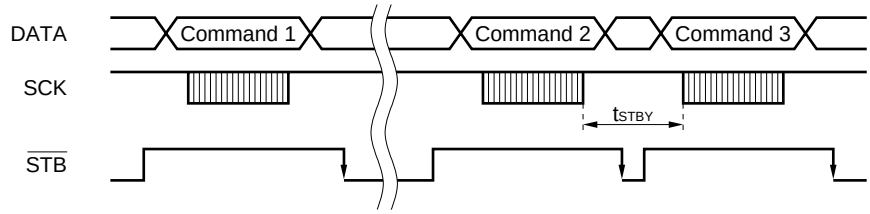


6.5 Standby (Released by Status Command)

(1) Flowchart

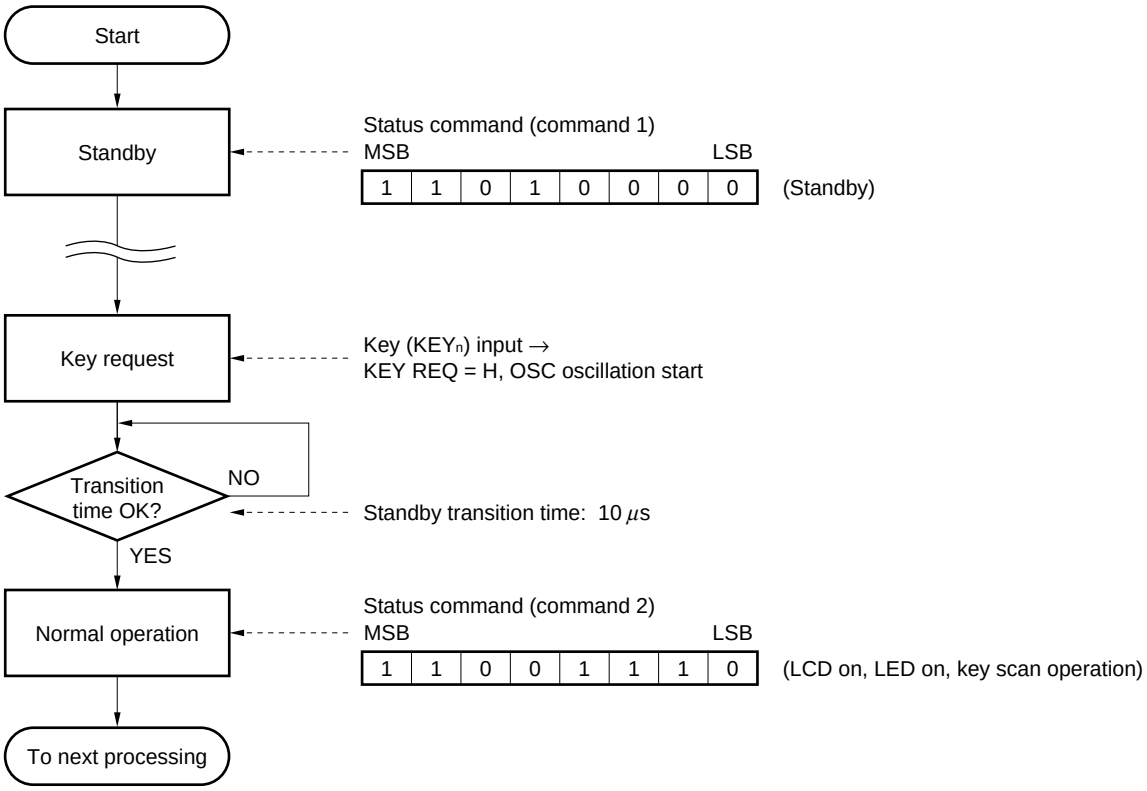


(2) Timing chart

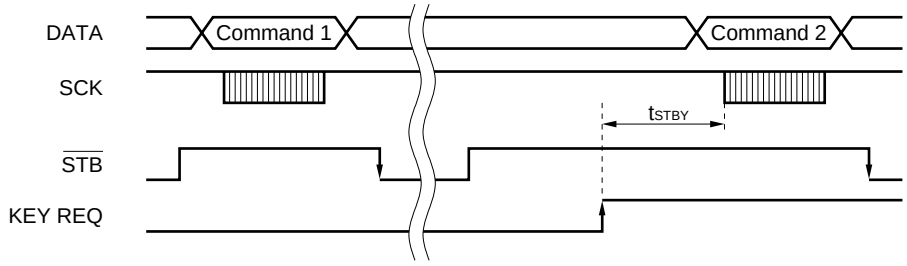


6.6 Standby (Released by KEY$_n$)

(1) Flowchart



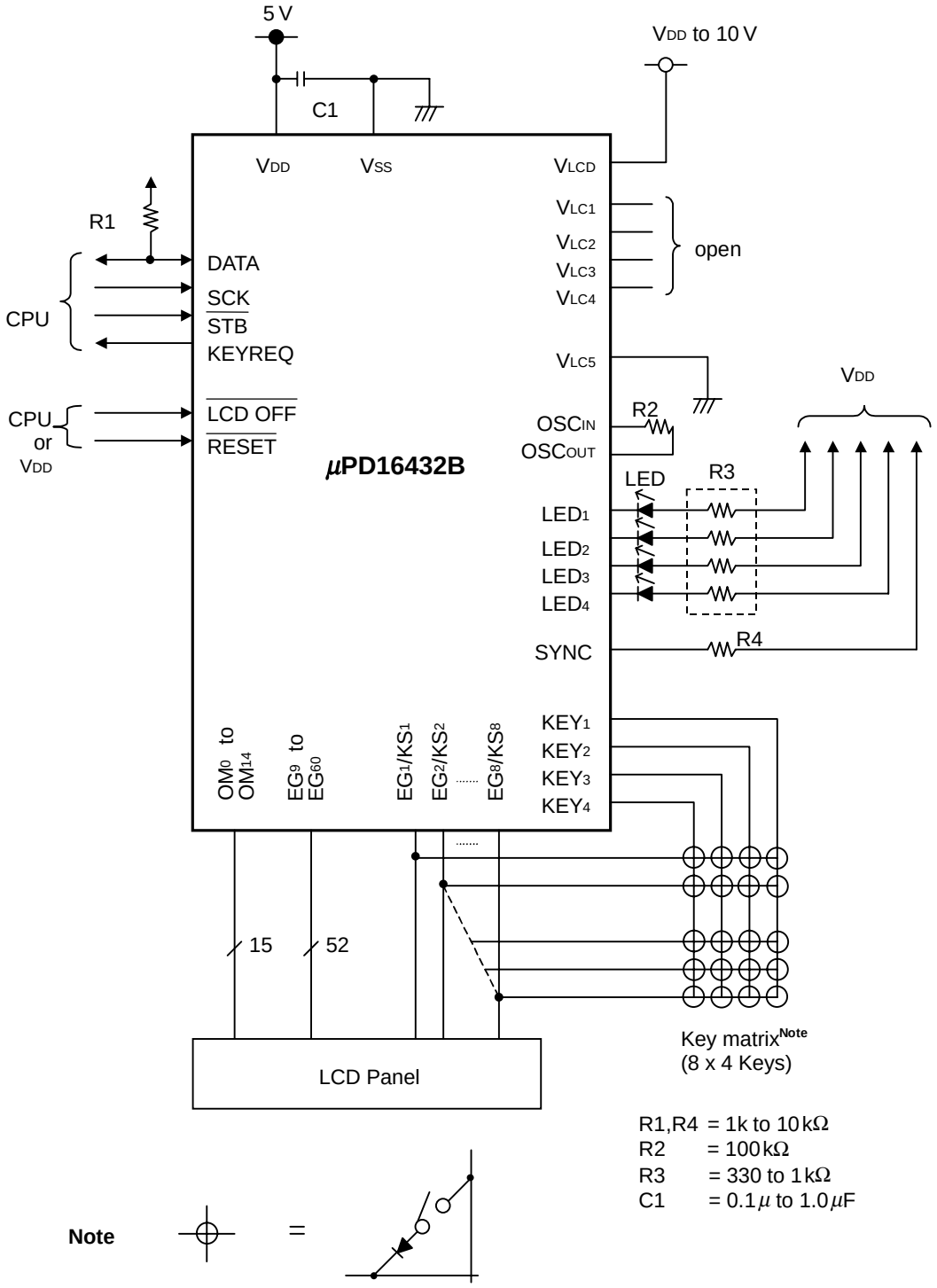
(2) Timing chart



★ 7. μPD16432B APPLICATION CIRCUITS

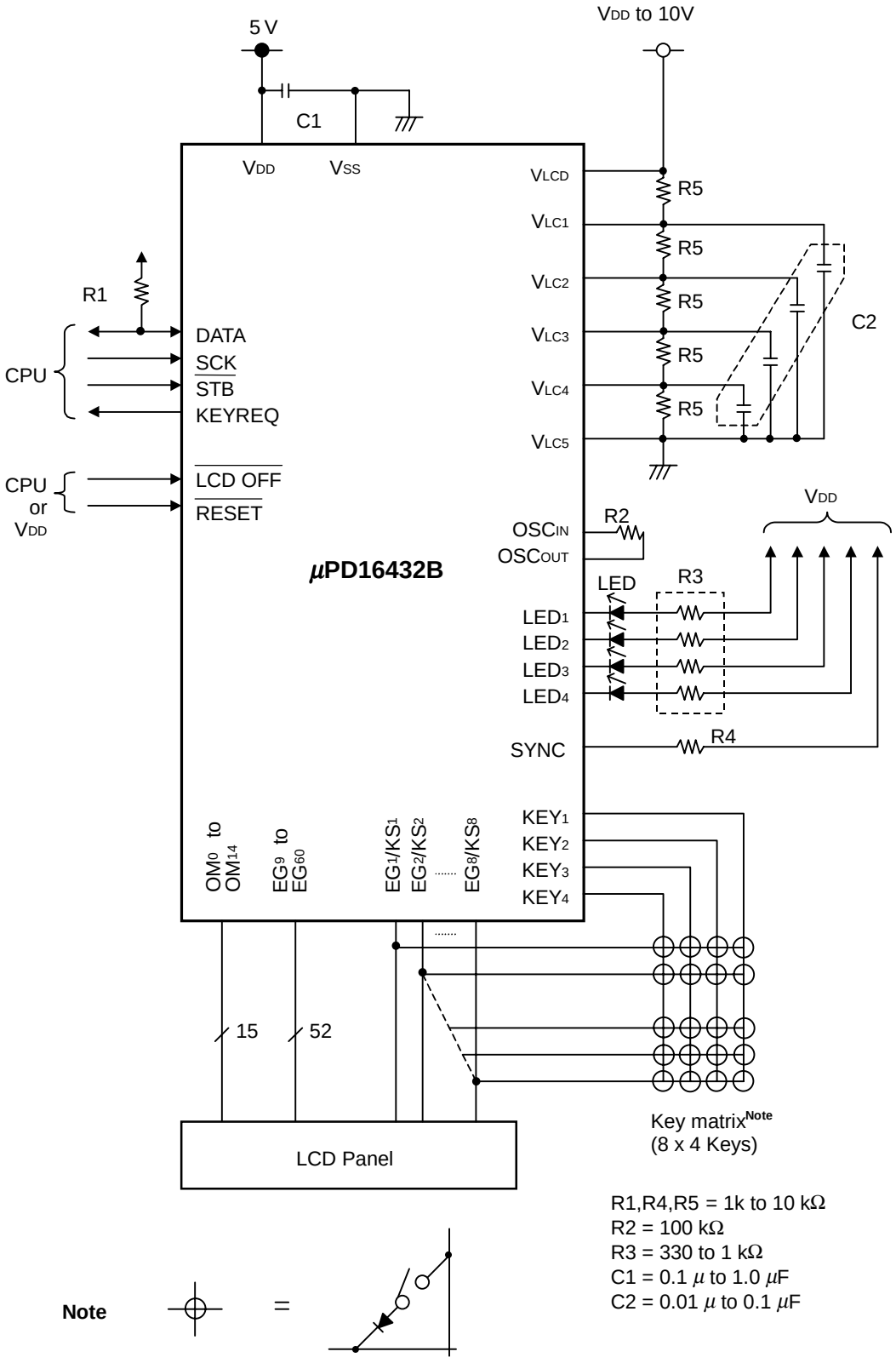
7.1 Example 1 of μPD16432B application circuit

(With internal power supply circuit, 1/15 duty)



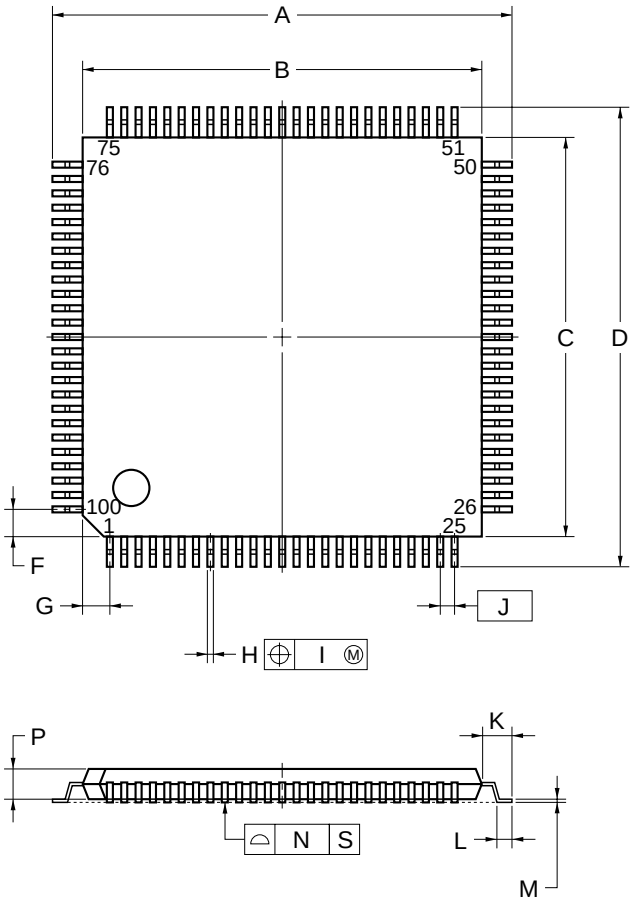
7.2 Example 2 of μPD16432B application circuit

(With external drive circuit, 1/15 duty)

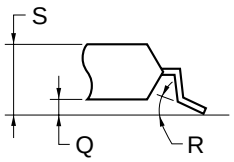


8. PACKAGE DRAWING

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S100GC-50-9EU-2

9. RECOMMENDED SOLDERING CONDITIONS

The μPD16432B should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document Semiconductor Device Mounting Technology Manual(C10535E).

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPD16432BGC-001-9EU : 100-PIN PLASTIC TQFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Soldering Condition Symbol
Infrared reflow	Package peak temperature : 235°C, Time : 30 sec. MAX. (at 210 or higher), Count : 3 times or less. Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature : 235°C, Time : 40 sec. MAX. (at 210 or higher), Count : 3 times or less. Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours).	VP15-107-3
Partial heating	Pin temperature: 300°C MAX., Time: 3 seconds MAX. (per side of device)	–

Note After opening the dry pack, store it at 25°C ro less and 65% RH or less for the allowable storeage period.

Caution Do not use different soldering methods together (except the partial heating).

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

REFERENCE DOCUMENTS

NEC Semiconductor Device Reliability/Quality Control System	(IEI-1212)
Semiconductor Device Mounting Technology Manual	(C10535E)