

64-BIT AC-PDP DRIVER
DESCRIPTION

The μ PD16344 is a row driver for an AC plasma display panel (PDP) using high breakdown voltage CMOS process. The μ PD16344 consists of a 64-bit bi-directional shift register, latch circuit and high breakdown voltage CMOS driver section. The logic section operates on a 5-V power supply so that it can be connected directly to a gate array and microcomputer (CMOS level input). The driver section provides high breakdown voltage output of 120 V and +400 mA, -150 mA. Both the logic and driver sections are constructed by CMOS, which allows operation with low power consumption.

FEATURES

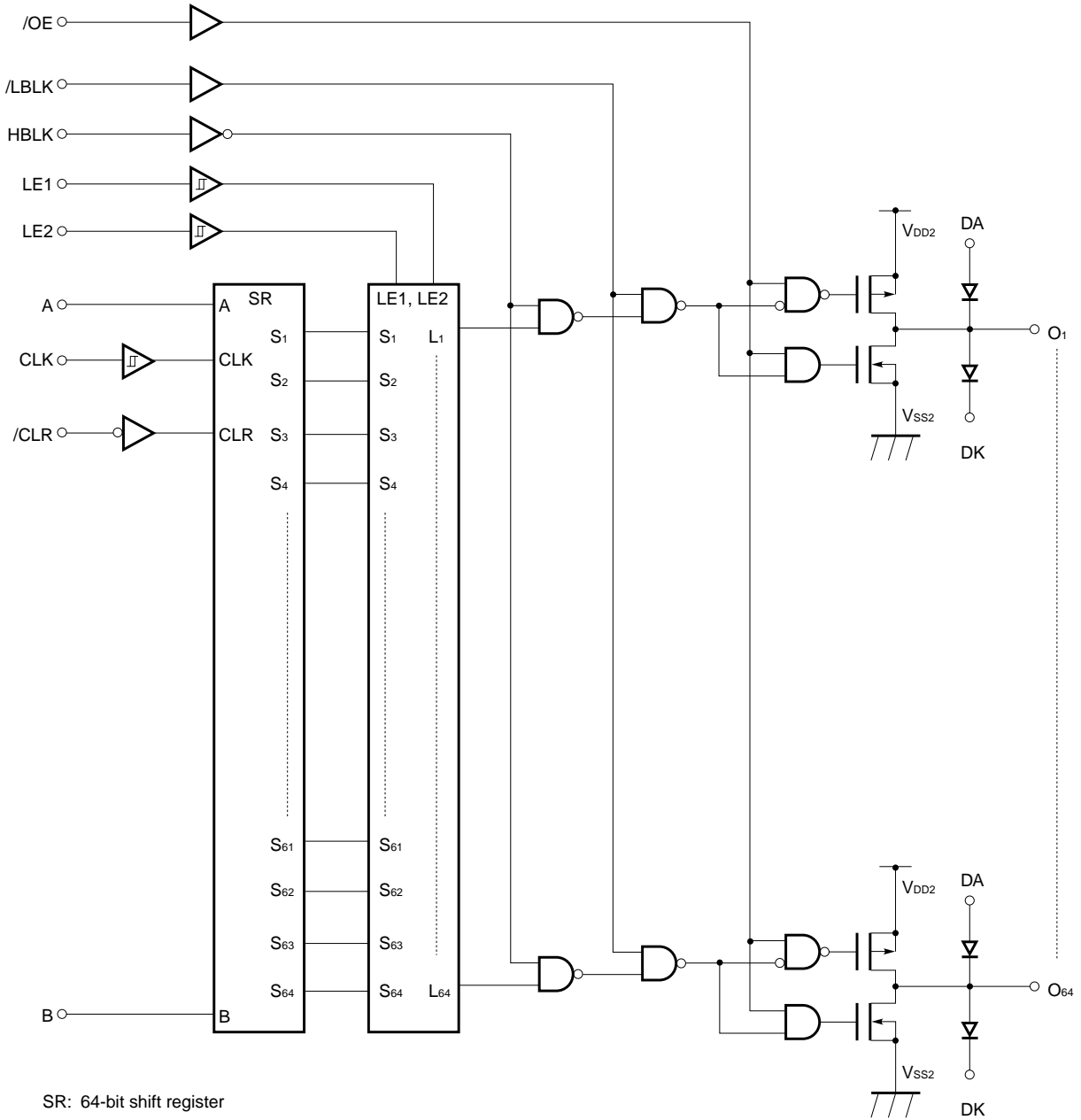
- High voltage full CMOS process
- High breakdown voltage, high current output (Maximum rating: 120 V, +400 mA, -150 mA)
- 64-bit bi-directional shift register on chip
- Data control by transfer clock (external) and latch
- High-speed data transfer capability ($f_{CLK} = 12$ MHz MAX.: when cascaded)
- Wider operating ambient temperature ($T_A = -40^\circ\text{C}$ to 85°C)

ORDERING INFORMATION

Part number	Package
μ PD16344GF-3BA	100-pin plastic QFP(14 x 20)

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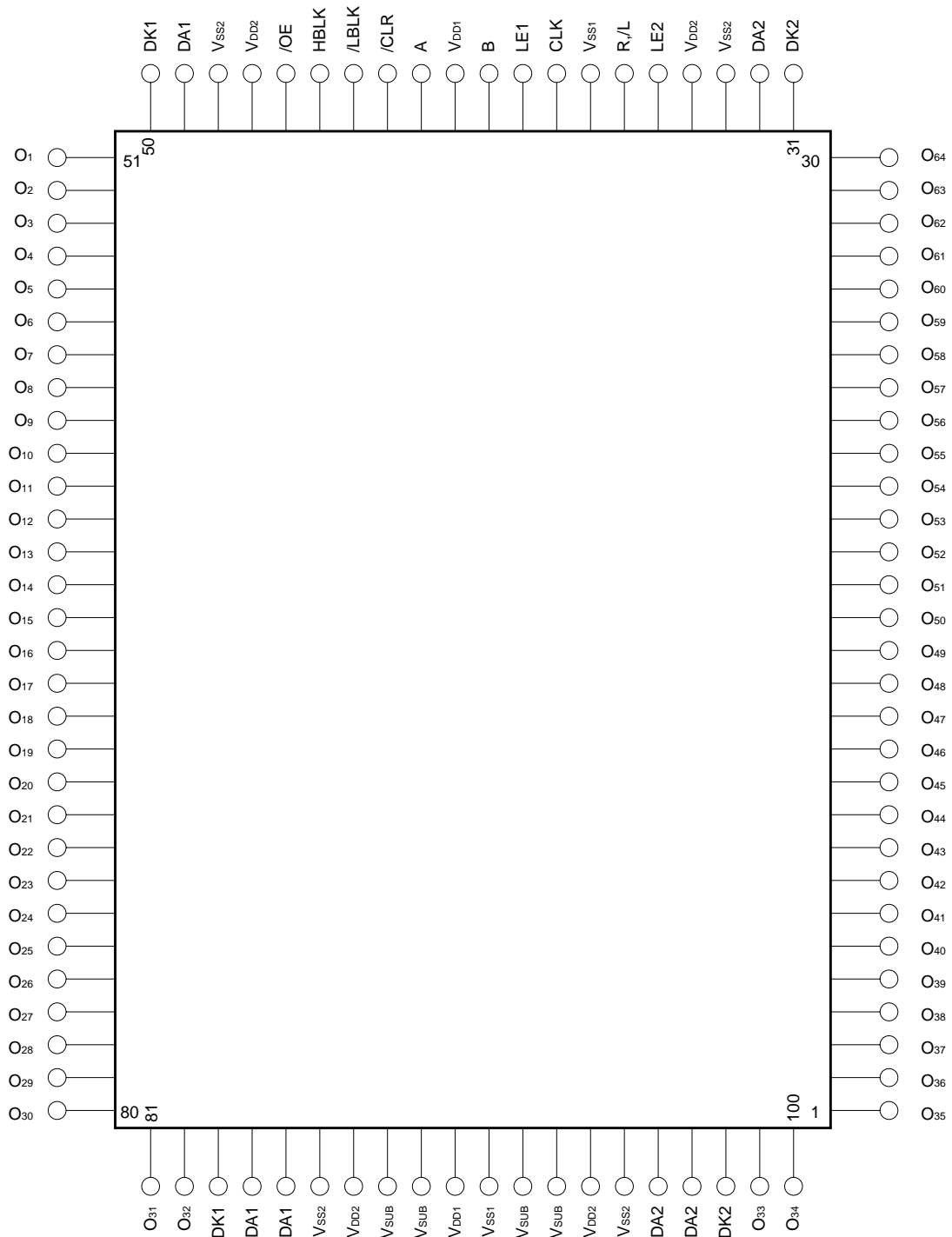
1. BLOCK DIAGRAM (Shift register: 64-bit)



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Top view)

μ PD16344GF-3BA



Caution Be sure to use all of the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Use V_{SS1}, V_{SS2}, and V_{SUB} at the same potential.

3. PIN FUNCTIONS

Pin Symbol	Pin Name	Pin Number	Description
HBLK	High blanking input	45	All output = H, when HBLK = H
LE1, LE2	Latch strobe input	35, 39	L = Through, H = Data preservation LE1: Latch of odd register LE2: Latch of even register
A	Left data input	42	When R,/L = L: A: Input B: Output When R,/L = H: A: Output B: Input
B	Right data input	40	
CLK	Clock input	38	Shift performed on a rising edge
/OE	Enable input	46	L = All output, high-impedance
/LBLK	Low blanking input	44	All output = L, when /LBLK = L
R,/L	Shift control input	36	L = Left shift mode A → O ₁ ... O ₆₄ → B H = Right shift mode B → O ₆₄ ... O ₁ → A
/CLR	Register clear	43	L = All shift register data cleared (L level clear)
O ₁ to O ₆₄	High withstand voltage output	1 to 30, 51 to 82, 99, 100,	110 V, +300 mA, -100 mA
DA1	Diode source 1	49, 84, 85	Diode source pin for O ₁ to O ₃₂
DK1	Diode sink 1	50, 83	Diode sink pin for O ₁ to O ₃₂
DA2	Diode source 2	32, 96, 97	Diode source pin for O ₃₃ to O ₆₄
DK2	Diode sink 2	31, 98	Diode sink pin for O ₃₃ to O ₆₄
V _{DD1}	Logic section power supply	41, 90	5 V ± 10 %
V _{DD2}	Driver section power supply	34, 47, 87, 94	30 to 110 V
V _{SS1}	Logic ground	37, 91	Connected to system GND
V _{SS2}	Driver ground	33, 48, 86, 95	Connected to system GND
V _{SUB}	Substrate ground	88, 89, 92, 93	Connected to system GND

4. TRUTH TABLE

Shift Register Section

Input		Output		/CLR	Shift Register
R,/L	CLK	A	B		
L	↑	Input	Output ^{Note1}	H	Left shift operation performed
L	H or L		Output	H	Hold
H	↑	Output ^{Note2}	Input	H	Right shift operation performed
H	H or L	Output		H	Hold
×	×	×	×	L	All registers = L

- Notes**
1. On the rising edge of the clock, the data of S₆₃ is shifted to S₆₄, and data is output from B.
 2. On the rising edge of the clock, the data of S₂ is shifted to S₁, and data is output from A.

Latch Section

LE	Operation (L _n)
H	Holds and outputs data immediately before LE becomes H.
L	Outputs shift register data.

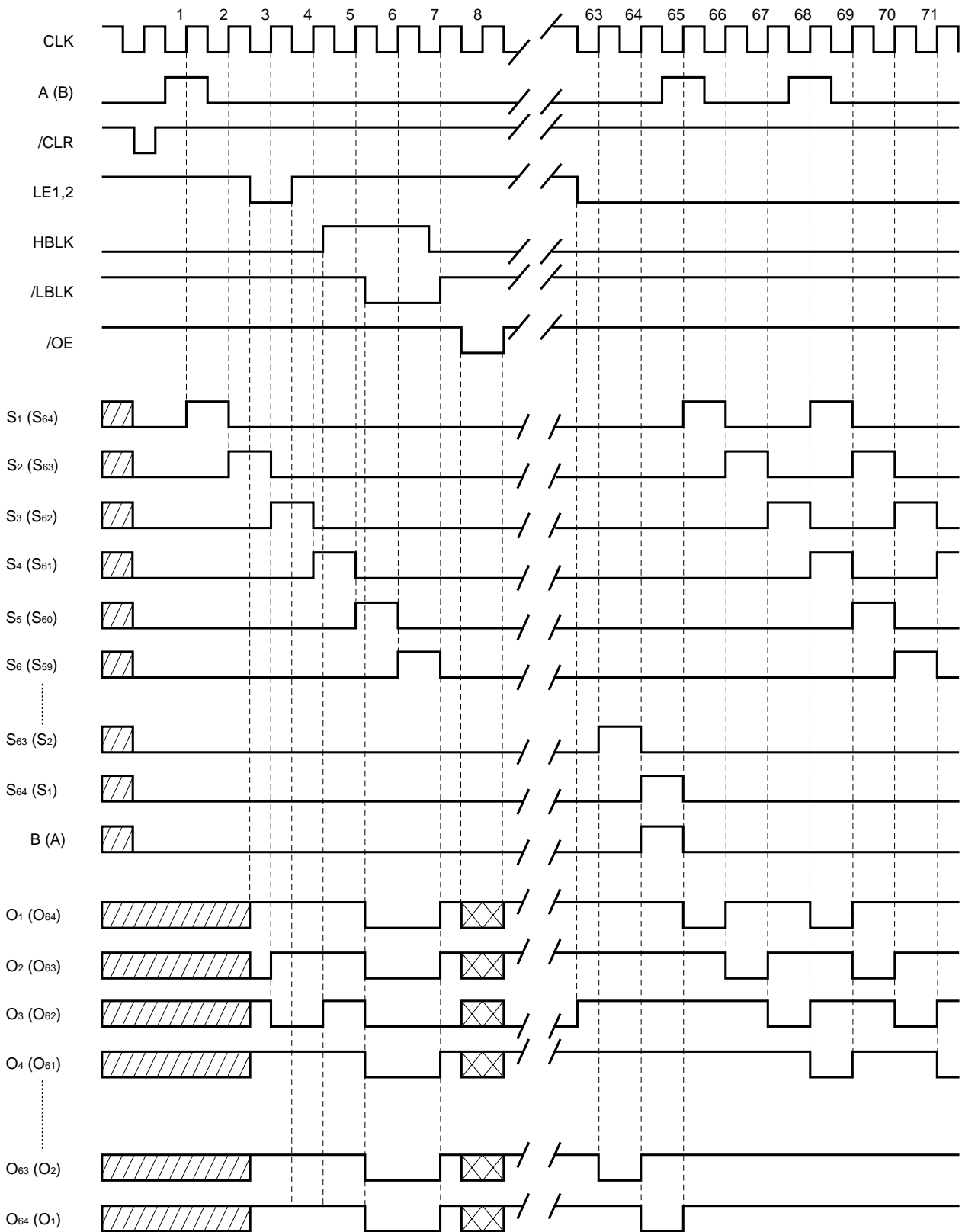
Driver Section

A (B)	HBLK	/LCLK	/OE	/CLR	Driver Output State
×	H	H	H	×	All driver output: H
×	×	L	H	×	All driver output: L ^{Note}
×	×	×	L	×	All driver output: High impedance
L	L	H	H	H	H
H	L	H	H	H	L
×	L	H	H	L	H

Note The capacity of the Nch transistor decreases to about 1/4 of the normal state for a certain period of time at the falling edge of /LCLK. Refer to **Switching Characteristics Waveform on 8. ELECTRICAL SPECIFICATIONS.**

Remark ×: H or L, H: High level, L: Low level

5. TIMING CHART (R,/L = "L", when left shift mode)



Remark In the parentheses: when R,/L=H

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic section supply voltage	V _{DD1}	-0.5 to +6.0	V
Driver section supply voltage	V _{DD2}	-0.5 to +120	V
Logic section input voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Driver section output current	I _O	+400, -150 ^{Note}	mA
Diode peak forward current	I _{FM}	±450	mA
Allowed package loss	P _D	1000	mW
Operating ambient temperature	T _A	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C

Note Simultaneous operation can be performed with up to 4 outputs.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operation Ranges (T_A = -40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic section supply voltage	V _{DD1}		4.5	5.0	5.5	V
Driver section supply voltage	V _{DD2}		30		110	V
High-level input voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low-level input voltage	V _{IL}		0		0.2 V _{DD1}	V
Driver output current	I _{OH}				-100	mA
	I _{OL1}				+300	mA
	I _{OL2}	Low capacity ^{Note}			(+75)	mA
Diode forward current	I _{FOH}				-400	mA
	I _{FOL}				+400	mA

Note The period of 560 ns MAX. from the falling edge of /BLK. The value enclosed in parentheses is a reference value.

Electrical Characteristics (T_A = 25°C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 110 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V _{OH1}	Logic, I _{OH} = -1.0 mA	0.9 V _{DD1}		V _{DD1}	V
Low-level output voltage	V _{OL1}	Logic, I _{OL} = 1.0 mA	0		0.1 V _{DD1}	V
High-level output voltage	V _{OH2}	O ₁ to O ₆₄ , I _{OH} = -60 mA	90	100		V
Low-level output voltage	V _{OL21}	O ₁ to O ₆₄ , I _{OL} = 200 mA		4	8	V
	V _{OL22}	Low capacity ^{Note1} , I _{OL} = 50 mA		(4)	(8)	V
High-level output voltage	V _{OHd}	O ₁ to O ₆₄ , I _{OH} = -400 mA ^{Note2} , DA = 110 V	103	105		V
Low-level output voltage	V _{OLd}	O ₁ to O ₆₄ , I _{OL} = 400 mA ^{Note2} , DK = 0 V		5	7	V
Input leakage current	I _{IL}	V _i = V _{DD1} or V _{SS1}			±1.0	μA
High-level input voltage	V _{IH}		0.7 V _{DD1}			V
Low-level input voltage	V _{IL}				0.2 V _{DD1}	V
Static current consumption	I _{DD11}	Logic, T _A = -40 to +85°C			500	μA
	I _{DD11}	Logic, T _A = 25°C			300	μA
	I _{DD21}	Driver, T _A = -40 to +85°C			1000	μA
	I _{DD21}	Driver, T _A = 25°C			100	μA

Notes 1. The period of 560 ns MAX. from the falling edge of /LCLK. The value enclosed in parentheses is a reference value.

2. The current characteristic of the diode built into the output section is indicated.

Switching Characteristics (T_A = 25°C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 110 V, Logic C_L = 15 pF, Driver C_L = 50 pF)

★

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Propagation delay time	t _{PHL1}	CLK → A, B			70	ns
	t _{PLH1}				70	ns
	t _{PHL2}	/CLR → A, B			70	ns
	t _{PHL3}	CLK → O ₁ to O ₆₄			160	ns
	t _{PLH3}				160	ns
	t _{PHL4}	LE → O ₁ to O ₆₄			160	ns
	t _{PLH4}				160	ns
	t _{PHL5}	HBLK → O ₁ to O ₆₄			160	ns
	t _{PLH5}				160	ns
	t _{PHL6}	/LBLK → O ₁ to O ₆₄			200	ns
	t _{PLH6}				200	ns
	t _{PHZ}	/OE → O ₁ to O ₆₄ R _L = 20 kΩ			300	ns
	t _{PZH}				160	ns
	t _{PZL}				160	ns
t _{PLZ}				300	ns	
Output rising time	t _{TLH}	O ₁ to O ₆₄			150	ns
Output falling time	t _{THL1}	O ₁ to O ₆₄			100	ns
	t _{THL2}	Low capacity ^{Note1}			400	ns
Output Nch low-driver capability period	t _{LA}	from the falling edge of /LBLK		(280) ^{Note2}	(560) ^{Note2}	ns
Clock frequency	f _{CLK}	Data intake, Duty = 50%			15	MHz
		Cascade connection, Duty = 50%			12	MHz
Input capacity	C _I				15	pF

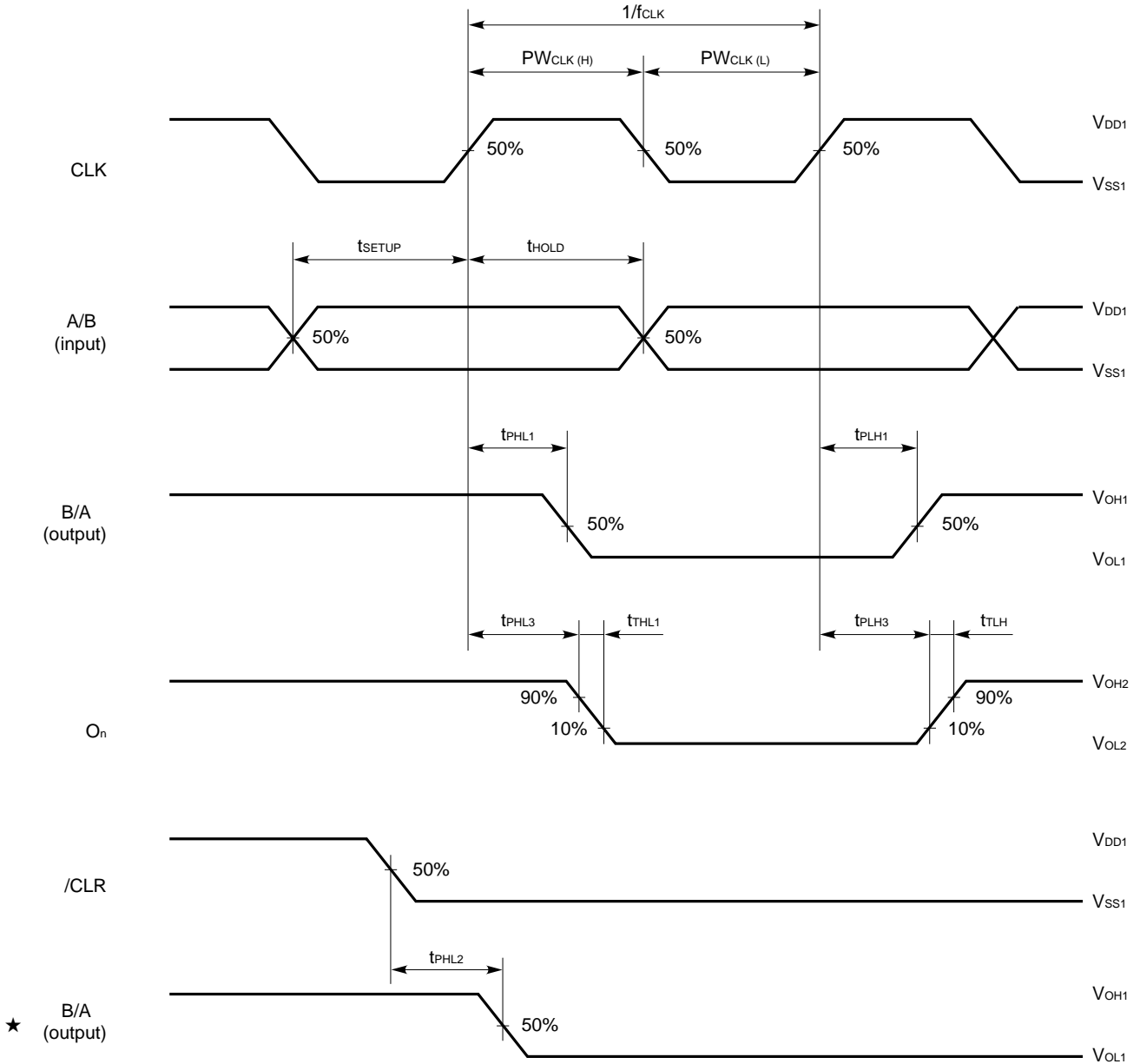
Notes 1. The period of 560 ns MAX. from the falling edge of /LBLK.

2. The value enclosed in parentheses is a reference value.

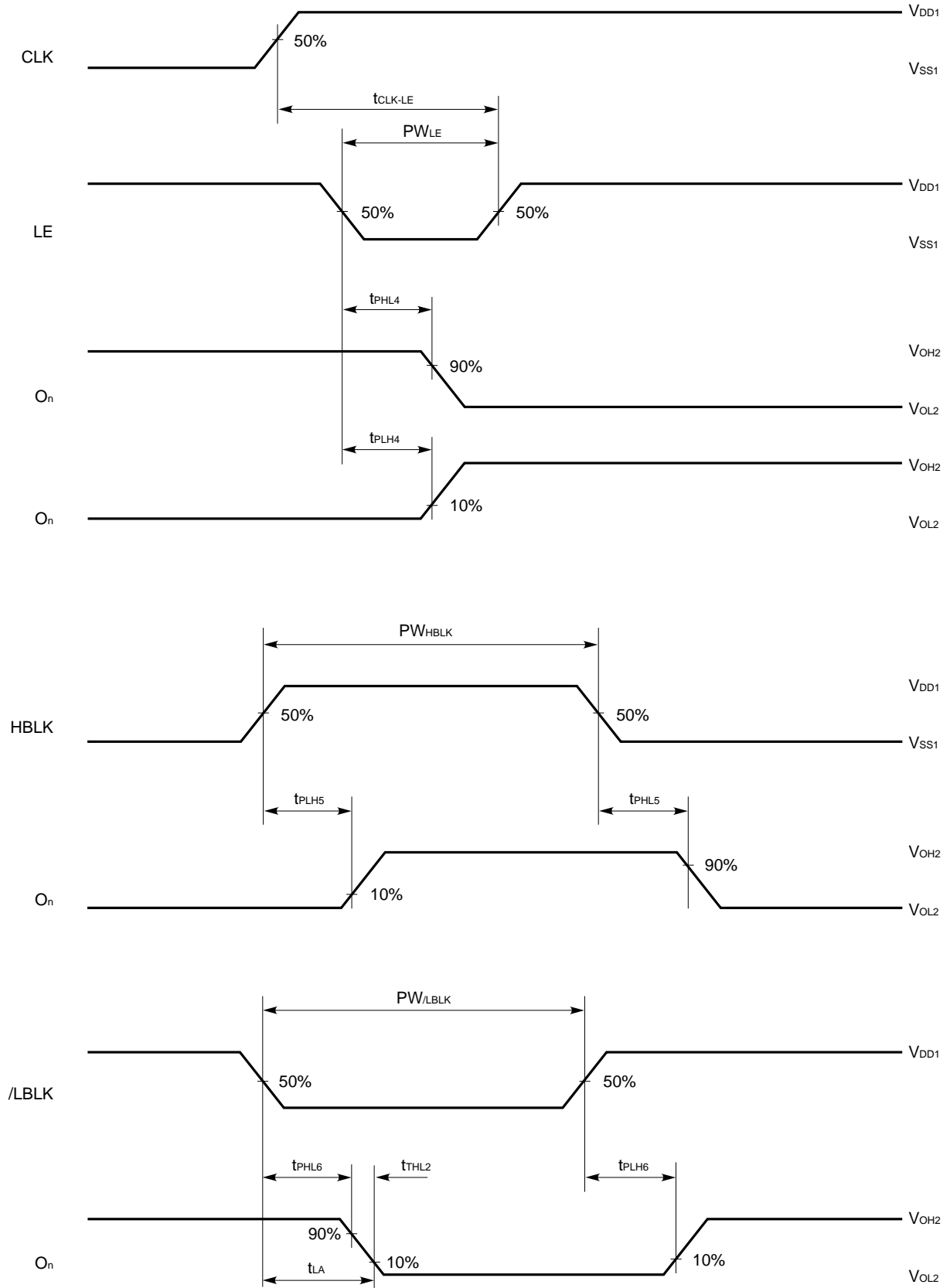
Timing Requirements (T_A = -40 to +85°C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW _{CLK(H)} ,		30			ns
	PW _{CLK(L)}					
Latch enable pulse width	PW _{LE}		30			ns
Blank pulse width	PW _{HBLK}		300			ns
	PW _{LBLK}		600			ns
Clear pulse width	PW _{CLR}		30			ns
Data setup time	t _{setup}		10			ns
Data hold time	t _{hold}		10			ns
Clock latch time	t _{CLK-LE}	CLK ↑ → LE ↑	30			ns

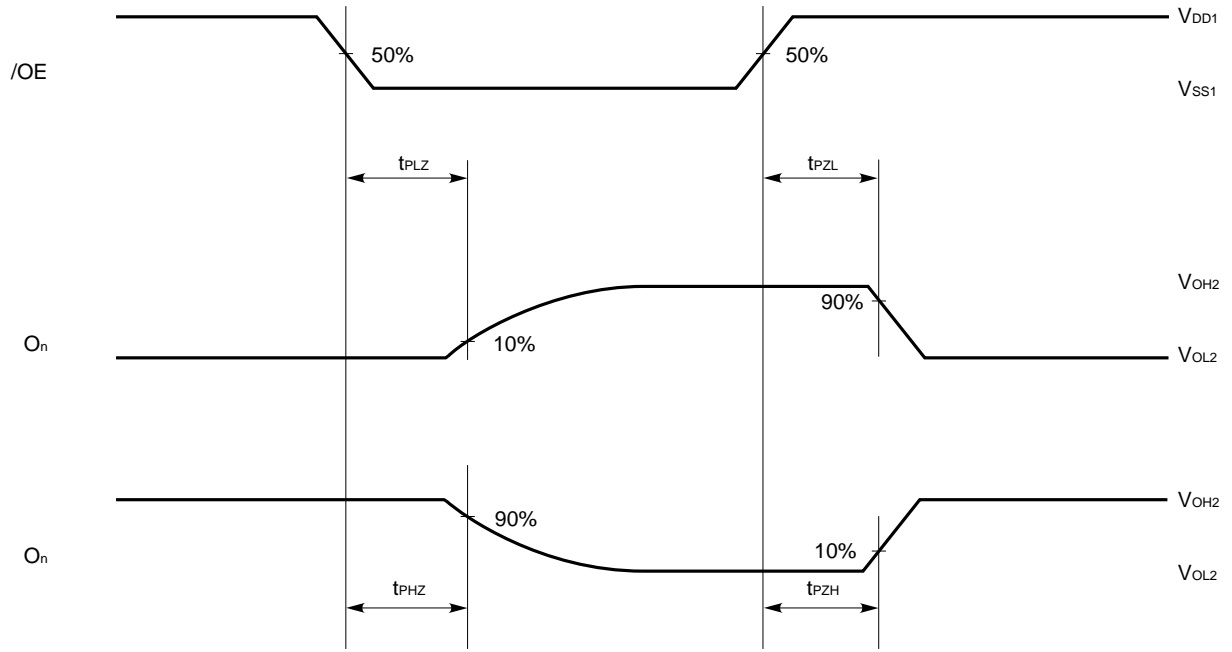
Switching Characteristics Waveform (1/3)



Switching Characteristics Waveform (2/3)

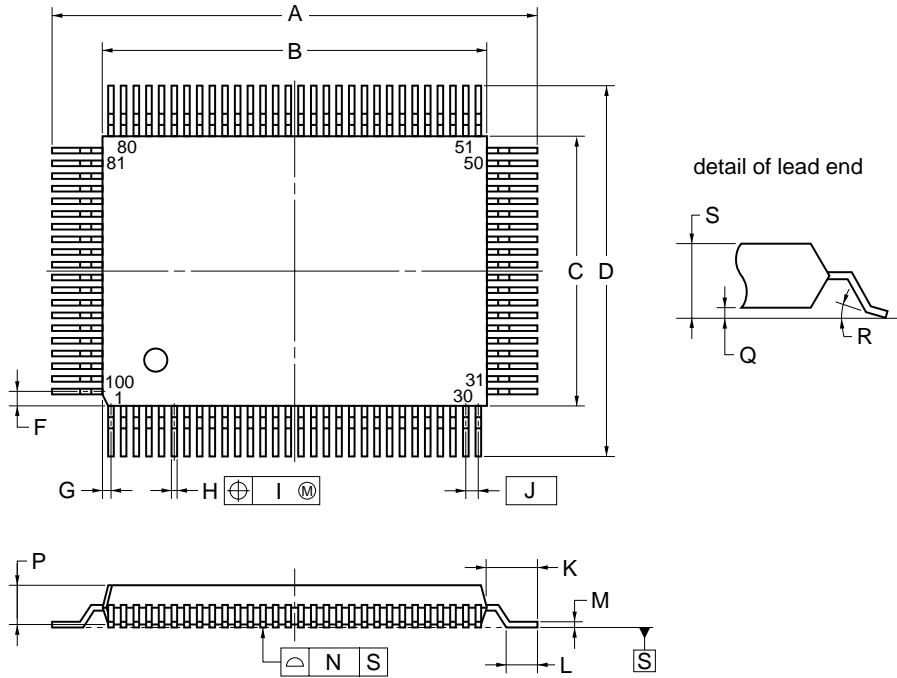


Switching Characteristics Waveform (3/3)



8. PACKAGE DRAWING

100 PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.2±0.2
B	20.0±0.2
C	14.0±0.2
D	17.2±0.2
F	0.8
G	0.6
H	0.32±0.08
I	0.15
J	0.65 (T.P.)
K	1.6±0.2
L	0.8±0.2
M	0.17 ^{+0.08} _{-0.07}
N	0.10
P	2.7
Q	0.125±0.075
R	5°±5°
S	2.825±0.175
S100GF-65-3BA-4	

★ 9. SOLDERING CONDITIONS

Solder the product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and soldering conditions other than those recommended, please contact one of our sales representatives.

Surface Mount Type

μ PD16344GF-3BA: 100-pin plastic QFP(14 x 20)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds MAX. (210°C MIN.), Number of times: 3 MAX., Max day: 7 days (need 10 hours with 125°C pre- beak after limited day) <Precaution> Products other than in hear-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR35-207-3
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX. (200°C MIN.), Number of times: 3 MAX., Max day: 7 days (need 10 hours with 125°C pre- beak after limited day) <Precaution> Products other than in hear-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	VP15-207-3
Partial heating	Pin temperature: 300°C MAX., Time: 3seconds MAX. (per side of device)	—

Caution Do not use two or more soldering methods in combination (except the partial heating method).

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents**NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades to NEC's Semiconductor Devices (C11531E)**

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