NEC

MOS INTEGRATED CIRCUIT

μPD16331

40-BIT AC-PDP DRIVER

The μPD16331 is a column driver for an AC plasma display panel (PDP) using high breakdown voltage CMOS process. It consists of 40-bit bidirectional shift register, latch circuit and high breakdown voltage CMOS driver blocks. The logic block operates on a 5 V power supply so that it can be connected directly to a microcontroller (CMOS level input). The driver block has high breakdown voltage output of 100 V and ±150 mA MAX. Both the logic block and driver block are constructed by CMOS, which allows operation with low power consumption.

FEATURES

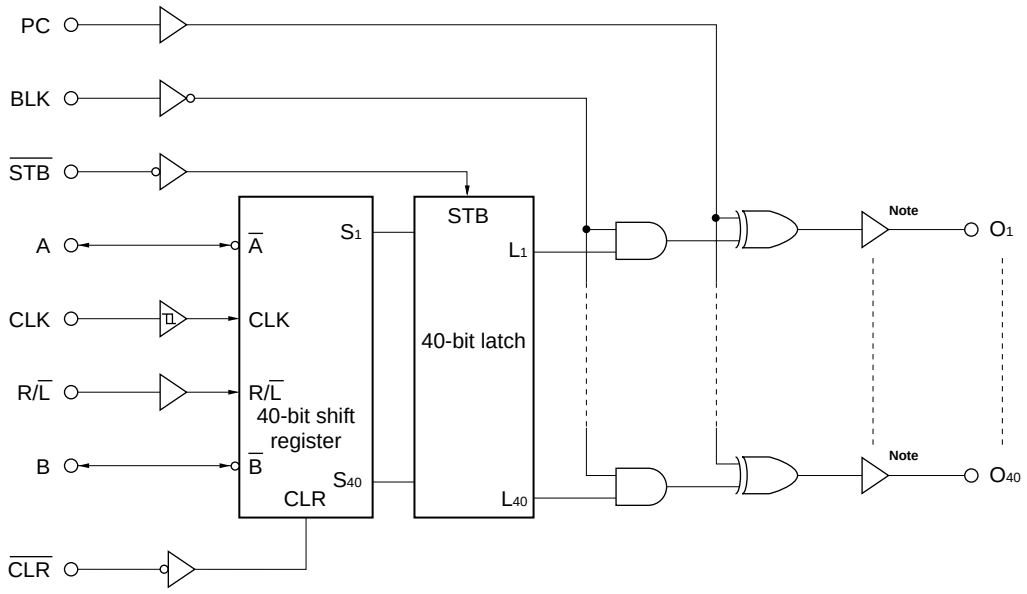
- High voltage full CMOS process
- High breakdown voltage, high current output (100 V, ±150 mA MAX.)
- 40-bit bidirectional shift register on chip
- Data control by transfer clock (external) and latch
- High speed data transfer capability ($f_{max.}$ = 16 MHz $_{MIN.}$; when cascaded)
- Wide operating temperature range (T_A = –20 to 85 °C)
- Polarity of all driver outputs can be inverted by PC pins.

ORDERING INFORMATION

Part Number	Package
μPD16331GF-3B9	80-pin plastic QFP (copper lead frame)

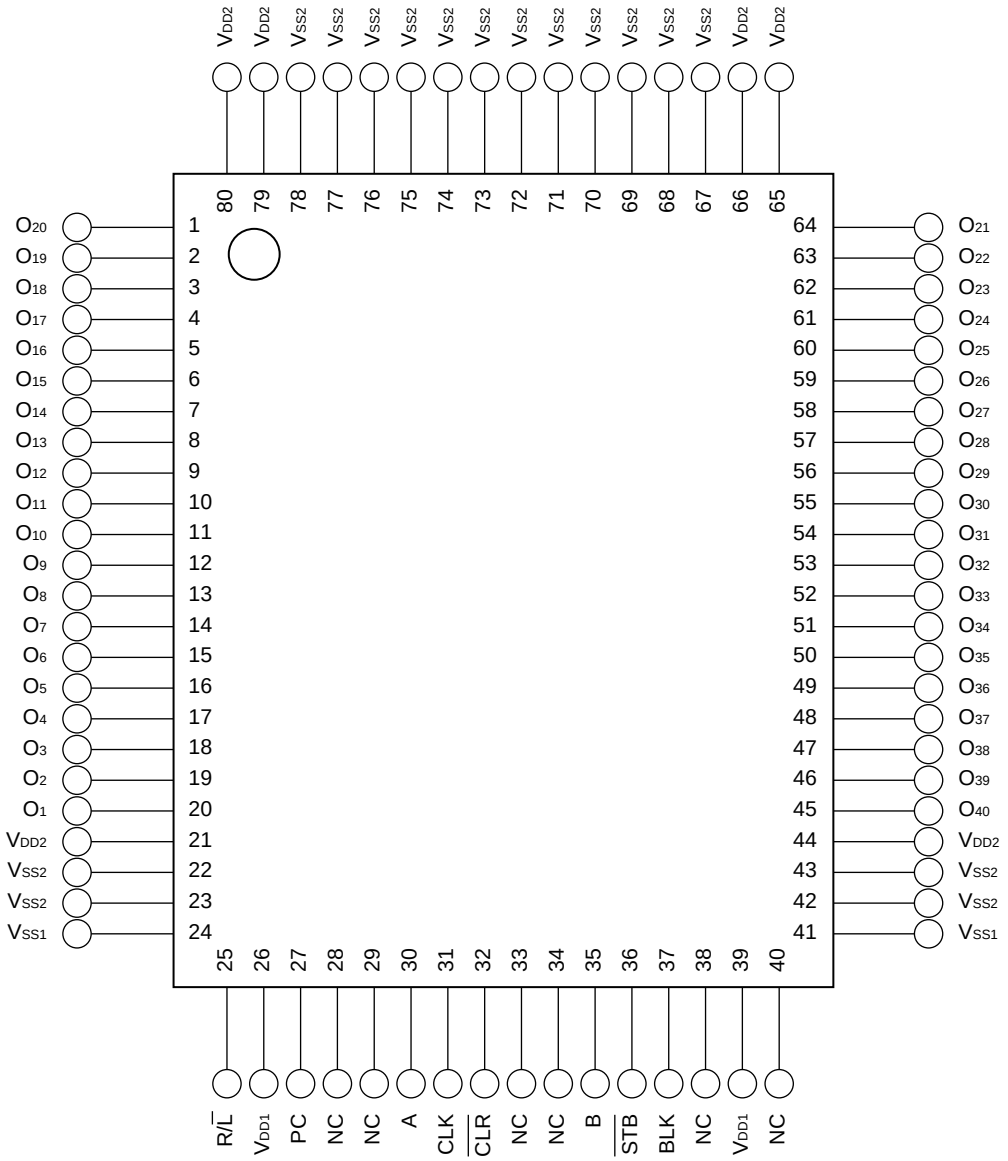
Document No. S11502EJ1V0DS00 (1st edition)
Date Published December 1996 N
Printed in Japan

BLOCK DIAGRAM



Note High breakdown voltage CMOS driver

PIN CONFIGURATION (Top View)



Be sure to use all of the V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2} pins. Use V_{SS1} and V_{SS2} at the same potential. The power should be turned on for V_{DD1}, logic input, and V_{DD2}, in that order and should be turned off in the reverse order.

PIN DESCRIPTION

Pin Symbol	Pin Name	Pin No.	Description
PC	Inverted polarity input	27	PC = H: Polarity of all outputs inverted
BLK	Blanking input	37	BLK = H: All outputs = H or L
$\overline{STB}$	Latch strobe input	36	L: Through H: Data retained
A[Note]	RIGHT data input	30	When R/$\overline{L}$ = H, A: Input B: Output
B[Note]	LEFT data input	35	When R/$\overline{L}$ = L, A: Output B: Input
CLK	Clock input	31	Shift executed on rise
$\overline{CLR}$	Clear input	32	L: All shift registers set to "L"
R/$\overline{L}$	Shift control input	25	H: Right shift mode $A \rightarrow O_1 \cdots O_{40} \rightarrow B$ L: Left shift mode $B \rightarrow O_{40} \cdots O_1 \rightarrow A$
O_1 to O_{40}	High breakdown voltage output	1 to 20, 45 to 64	100 V, 150 mA MAX.
V_{DD1}	Logic block power supply	26, 39	5 V ± 10 %
V_{DD2}	Driver block power supply	21, 44, 65, 66, 79, 80	30 to 90 V
V_{SS1}	Logic ground	24, 41,	Connected to system GND
V_{SS2}	Driver ground	22, 23, 42, 43, 67 to 78	Connected to system GND
NC	Non-connection pins	28, 29, 33, 34, 38, 40	Non-connection

Note Data which is input to the shift registers is always inverted input data A (B) and data in the shift registers is always inverted when it is output. (Refer to the truth tables and timing chart.)

TRUTH TABLE 1 (Shift Register Block)

Input		Output		Shift Register
R/$\overline{L}$	CLK	A	B	
H	↑	Input	Output[Notes 1]	Right shift executed
H	H or L		Output	Retained
L	↑	Output[Notes 2]	Input	Left shift executed
L	H or L	Output		Retained

Notes 1. The data of internal shift register S_{39} is shifted to S_{40} on a rise of CLK and inverted data of S_{40} is output from B. (Refer to the timing chart.)

2. The data of internal shift register S_2 is shifted to S_1 on a rise of CLK and inverted data of S_1 is output from A. (Refer to the timing chart.)

TRUTH TABLE 2 (Latch Block)

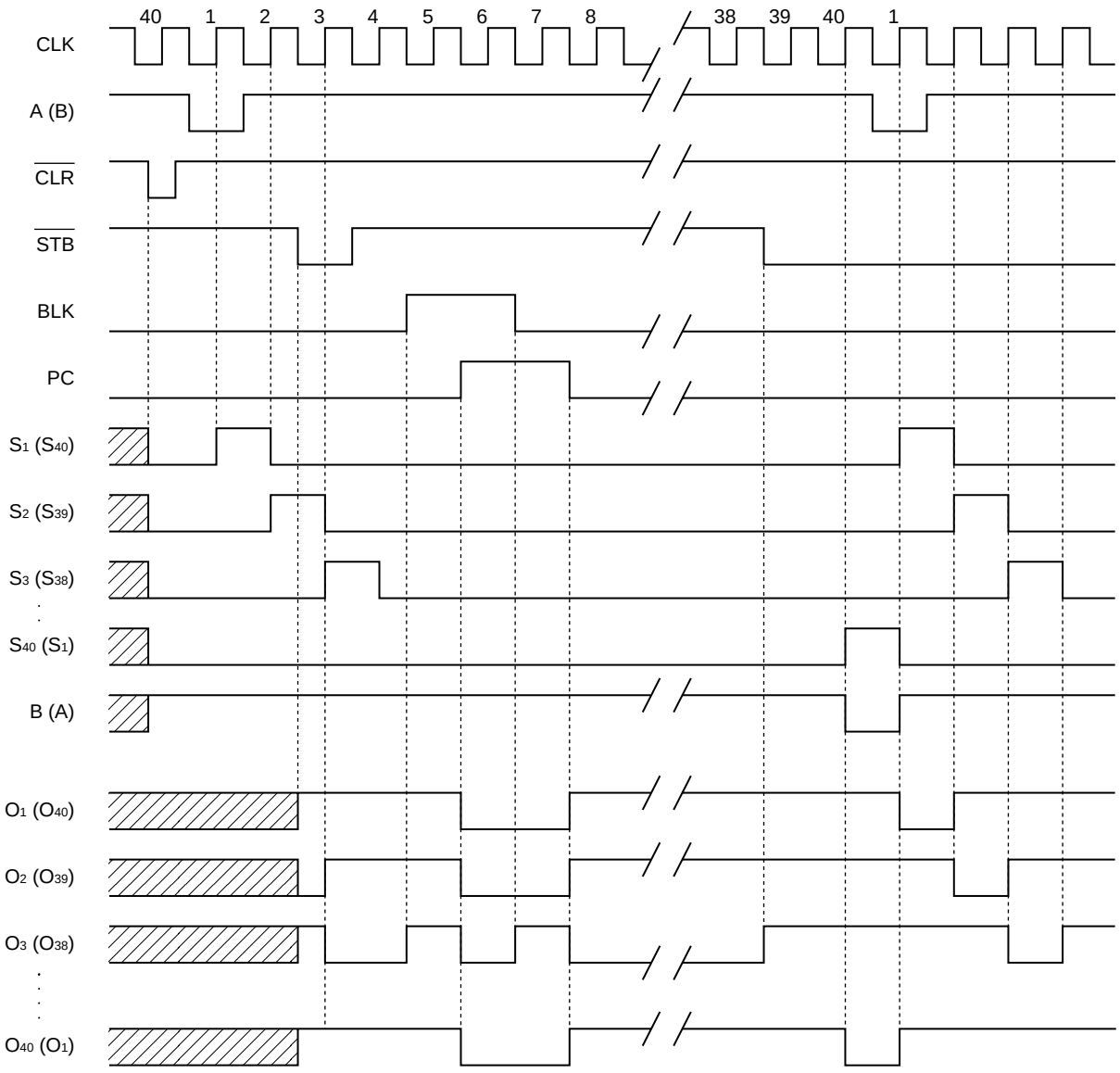
$\overline{STB}$	Operation
H	Retains data immediately before $\overline{STB}$ becomes H.
L	Outputs data of shift register.

TRUTH TABLE 3 (Driver Block)

Input				State of Driver Output
A (B)	$\overline{STB}$	BLK	PC	
×	×	H	H	L (all driver outputs: L)
×	×	H	L	H (all driver outputs: H)
L	L	L	H	H
L	L	L	L	L
H	L	L	H	L
H	L	L	L	H
×	H	L	H	Outputs data of S_n on $\overline{STB}$ rise.
×	H	L	L	Inverts and outputs data of S_n on $\overline{STB}$ rise.

×: H or L, H: High level L: Low level

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Rating	Unit
Logic block supply voltage	V_{DD1}	– 0.5 to + 7.0	V
Driver block supply voltage	V_{DD2}	– 0.5 to + 100	V
Logic block input voltage	V_{I1}	– 0.5 to V_{DD1} + 0.5	V
Logic block output voltage	V_{O1}	– 0.5 to V_{DD1} + 0.5	V
Driver block output voltage	V_{O2}	– 0.5 to V_{DD2} + 0.5	V
Driver output current	I_{O2}	± 150 Notes 1	mA
Package power dissipation	P_D	1300 Notes 2	mW
Operating ambient temperature	T_A	– 20 to + 85	°C
Storage temperature	$T_{stg.}$	– 65 to + 150	°C

Notes 1. A period of driver peak output current is less than 1 μs pulse width.

2. T_A = 25 °C (however, values after the chip is soldered to PWB will be TBD.)
When $T_A \geq$ 25 °C, load should be reduced to –13 mW/ °C.

RECOMMENDED OPERATING RANGE (T_A = –20 to +85 °C, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V_{DD2}	30		90	V
Input voltage, high	V_{IH}	0.7V_{DD1}		V_{DD1}	V
Input voltage, low	V_{IL}	0		0.2V_{DD1}	V
Driver output current	I_O			±100	mA

ELECTRICAL SPECIFICATIONS (T_A = 25 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 90 V, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	A (B), I_{OH} = –1.0 mA	0.9 V_{DD1}		V_{DD1}	V
Output voltage, low	V_{OL1}	A (B), I_{OL} = 1.0 mA	0		0.1V_{DD1}	V
Output voltage, high	V_{OH21}	O_1 to O_{40}, I_{OH2} = –100 mA	70	80		V
	V_{OH22}	O_1 to O_{40}, I_{OH2} = –60 mA	78	84		V
Output voltage, low	V_{OL21}	O_1 to O_{40}, I_{OL2} = 100 mA		10	20	V
	V_{OL22}	O_1 to O_{40}, I_{OL2} = 60 mA		6	12	V
Input leakage current	I_I	V_I = V_{DD1} or V_{SS1}			±1.0	V
Static consumption current	I_{DD11}	Logic, T_A = –20 to +85 °C			100	μA
	I_{DD12}	Logic, T_A = +25 °C			10	μA
	I_{DD21}	Driver, T_A = –20 to +85 °C			1	mA
	I_{DD22}	Driver, T_A = +25 °C			100	μA

SWITCHING CHARACTERISTICS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 90 V, Logic C_L = 15 pF, Driver C_L = 150 pF)

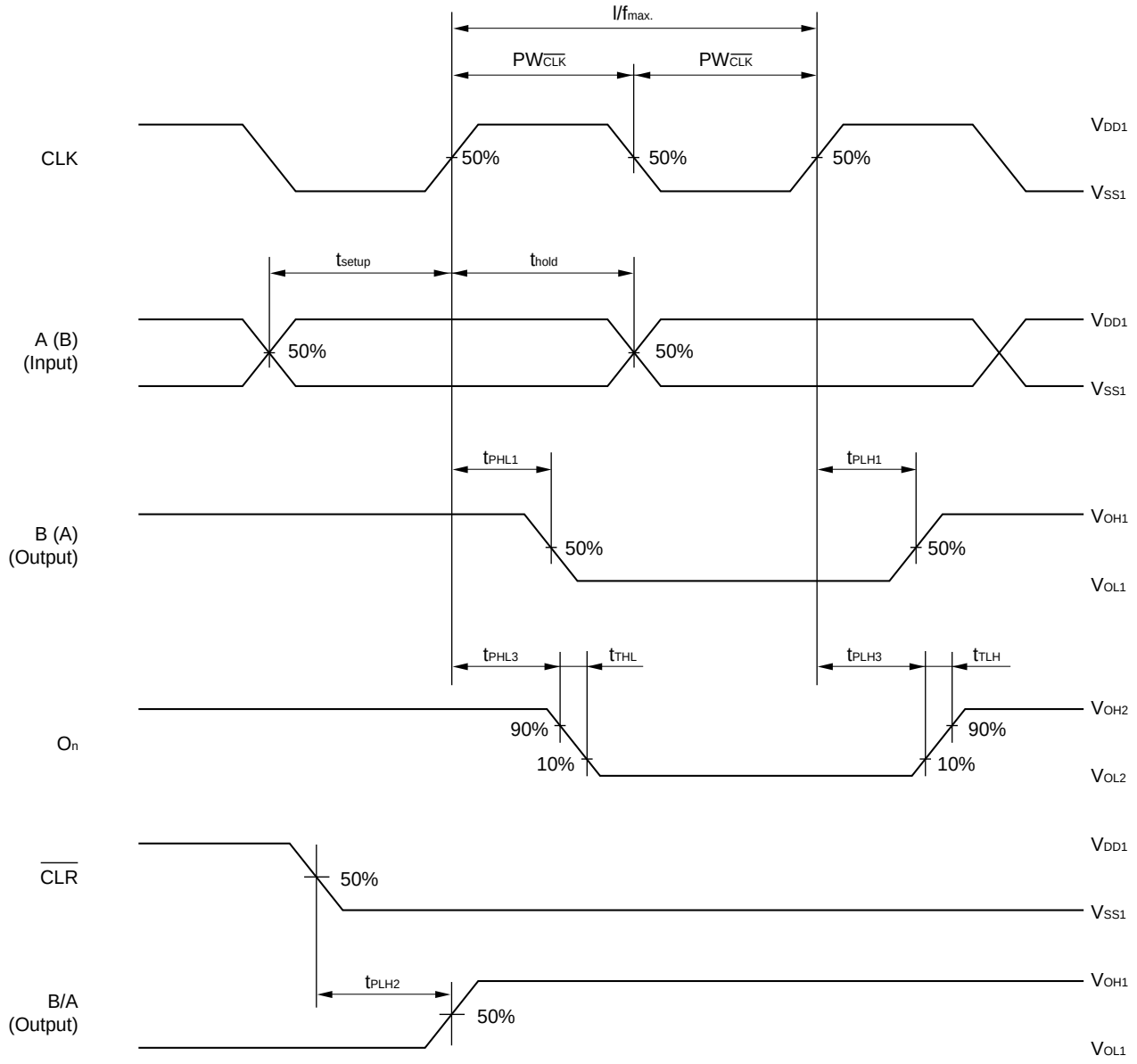
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transmission delay time	t_{PHL1}	CLK → A/B			50	ns
	t_{PLH1}				50	ns
	t_{PLH2}	$\overline{CLR}$ → A/B			60	ns
	t_{PHL3}	CLK → O_1 to O_{40}			200	ns
	t_{PLH3}				200	ns
	t_{PHL4}	$\overline{STB}$ → O_1 to O_{40}			180	ns
	t_{PLH4}				180	ns
	t_{PHL5}	BLK → O_1 to O_{40}			175	ns
	t_{PLH5}				175	ns
	t_{PHL6}	PC → O_1 to O_{40}			170	ns
	t_{PLH6}				170	ns
Rise time O_1 to O_{40}	t_{TLH}	C_L = 150 pF			150	ns
Fall time O_1 to O_{40}	t_{THL}	C_L = 150 pF			150	ns
Maximum clock frequency	$f_{max.}$	Data fetch, duty = 50%	20			MHz
		With cascading, duty = 50%	16			MHz
Input capacitance	C_I				15	pF

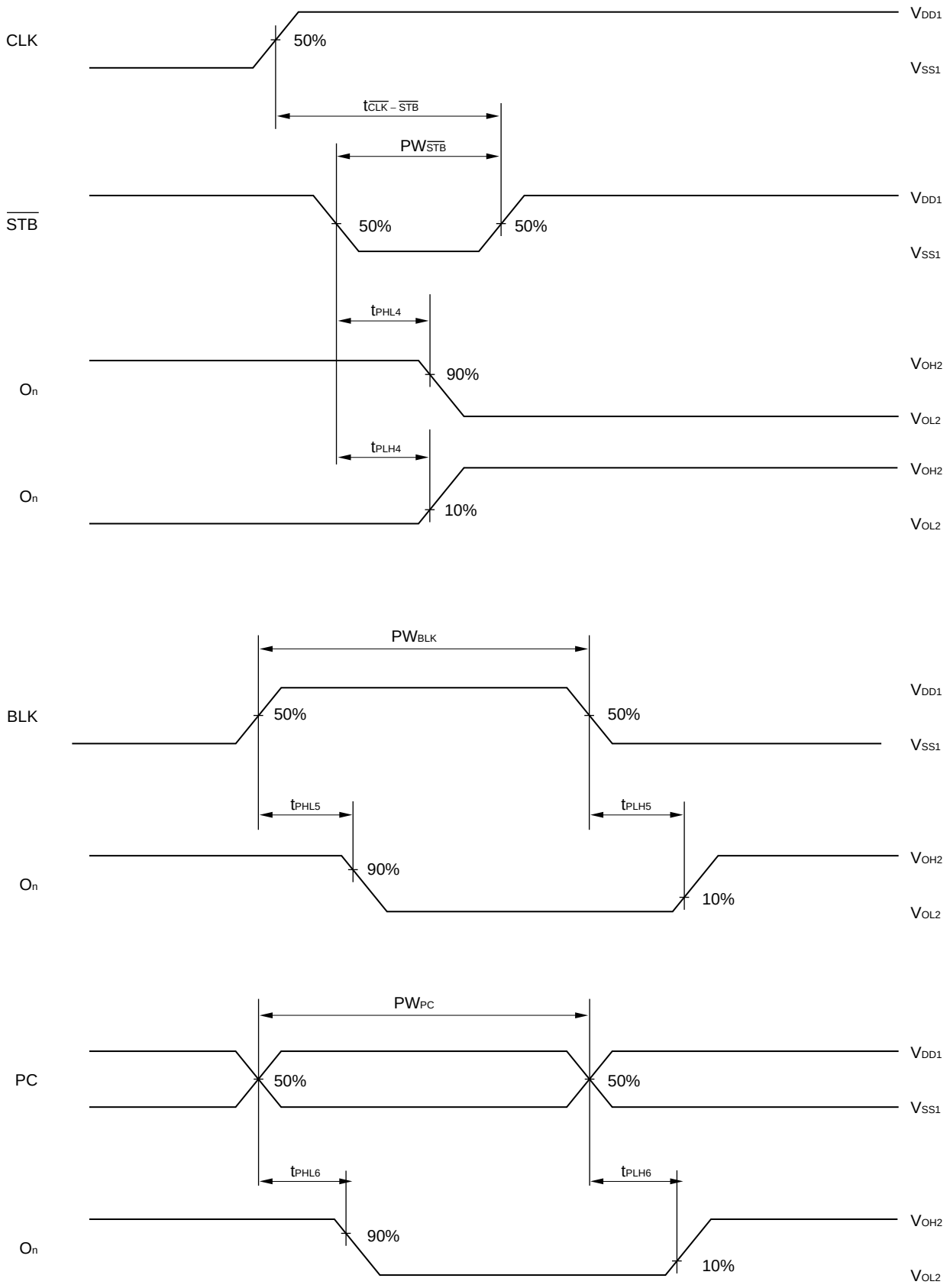
TIMING REQUIREMENTS (T_A = –20 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		25			ns
Strobe pulse width	$PW_{\overline{STB}}$		60			ns
Blank pulse width	PW_{BLK}		400			ns
Inverted polarity pulse width	PW_{PC}		400			ns
Clear pulse width	$PW_{\overline{CLR}}$		120			ns
Data setup time	t_{setup}		10			ns
Data hold time	t_{hold}		10			ns
Clock-strobe time	$t_{CLK\text{-}\overline{STB}}$	CLK ↑ → $\overline{STB}$ ↑	60			ns

SWITCHING CHARACTERISTIC WAVEFORMS (R/$\overline{L}$ = H)

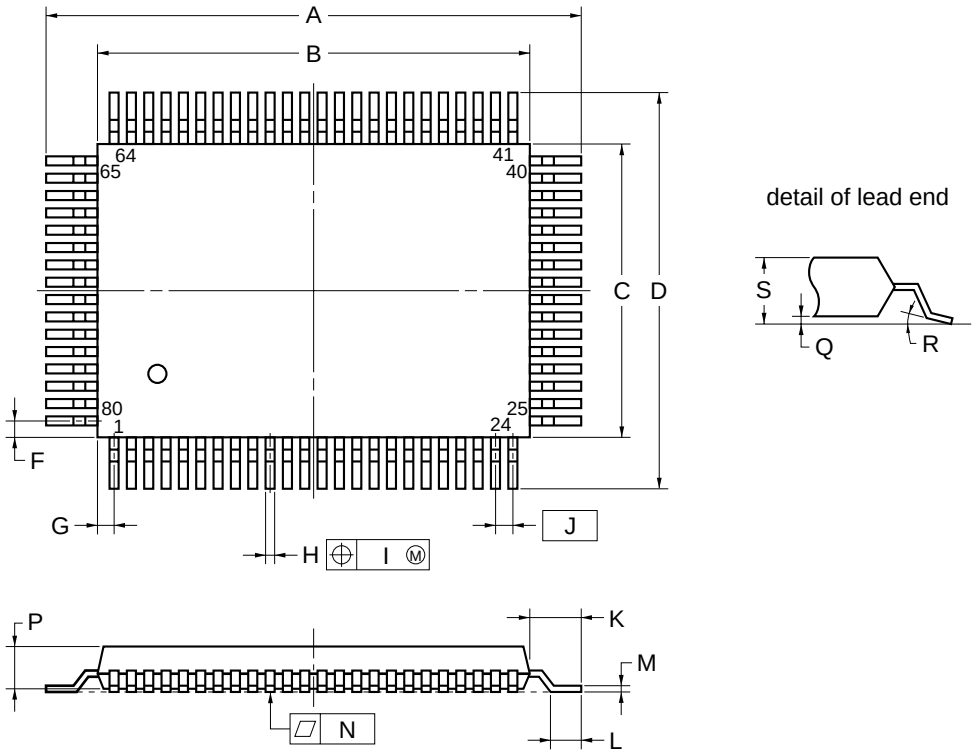
Figures in parentheses apply when R/$\overline{L}$ = H.




CLK
50%
VDD1
VSS1
tCLK – STB
PWSTB
STB
50%
50%
VDD1
VSS1
tPHL4
On
90%
VOH2
VOL2
tPLH4
On
10%
VOH2
VOL2
PWBLK
BLK
50%
50%
VDD1
VSS1
tPHL5
tPLH5
On
90%
10%
VOH2
VOL2
PWPC
PC
50%
50%
VDD1
VSS1
tPHL6
tPLH6
On
90%
10%
VOH2
VOL2

PACKAGE DRAWING

80 PIN PLASTIC QFP (14×20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

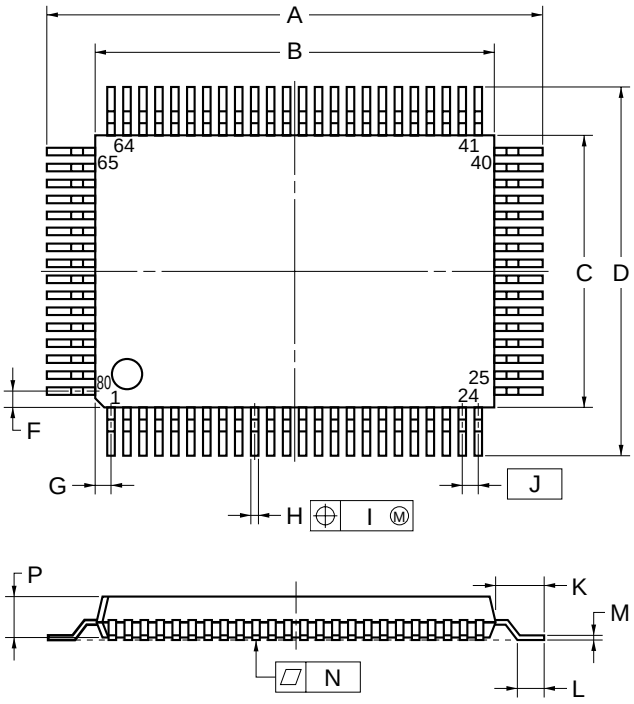
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

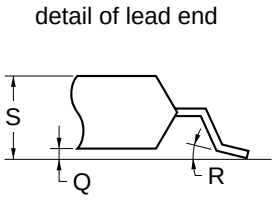
P80GF-80-3B9-3

Caution Since there are two type packages which lead length is different, need designing to be able to use two packages. (note: page 10, 11)

PACKAGE DRAWING

80 PIN PLASTIC QFP (14×20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.2±0.2	$0.913^{+0.009}_{-0.008}$
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.2	0.677±0.008
F	1.0	0.039
G	1.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GF-80-3B9-3

RECOMMENDED SOLDERING CONDITIONS

Please perform the soldered mounting of this product under the following recommended conditions.

For soldering methods and conditions other than those recommended here, please contact your NEC sales representative.

Surface Mount Type

For details on recommended soldering conditions, please refer to the **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

μPD16306AGF-3BA

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared Reflow	Package peak temperature: 235 °C, time: up to 30 sec. (no less than 210 °C), count: twice, restricted number of days: less than 7 days[Note]	IR-35-207-2
VPS	Package peak temperature: 215 °C, time: up to 40 sec. (no less than 200 °C), count: once, restricted number of days: less than 7 days[Note]	VP15-207-1
Pin Part Heating	Pin part temperature: no more than 300 °C, time: up to 10 sec., restricted number of days: none[Note]	

Note This refers to the restricted number of days for storage after decapsulating the dry pack. The storage conditions are no more than 25 °C and 65 % RH.

Caution Please avoid mixing use of soldering methods (except for pin part heating methods).

References

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)
Quality Grades of NEC Semiconductor Devices (C11531E)
Semiconductor Device Mounting Technology Manual (C10535E)

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