NEC

MOS INTEGRATED CIRCUIT

μPD161622

396 OUTPUT TFT-LCD SOURCE DRIVER WITH RAM

DESCRIPTION

The μPD161622 is a TFT-LCD source driver that includes display RAM.

This driver has 396 outputs, a display RAM capacity of 371,712 bits (132 pixels x 16 bits x 176 lines) and, can provide a 65,536-color display.

FEATURES

- TFT-LCD driver with on-chip display RAM
- Logic power supply voltage: 2.5 to 3.6 V
- Driver power supply voltage: 4.3 to 5.5 V
- Display RAM: 132 x 16 x 176 bits
- Driver outputs: 396 output
- CPU interface: Serial, 8-bit/16-bit parallel interface selectable
- Colors: 65,536 colors/pixel
- On-chip VCOM generator
- On-chip timing generator
- On-chip oscillator

ORDERING INFORMATION

Part Number	Package
μPD161622P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

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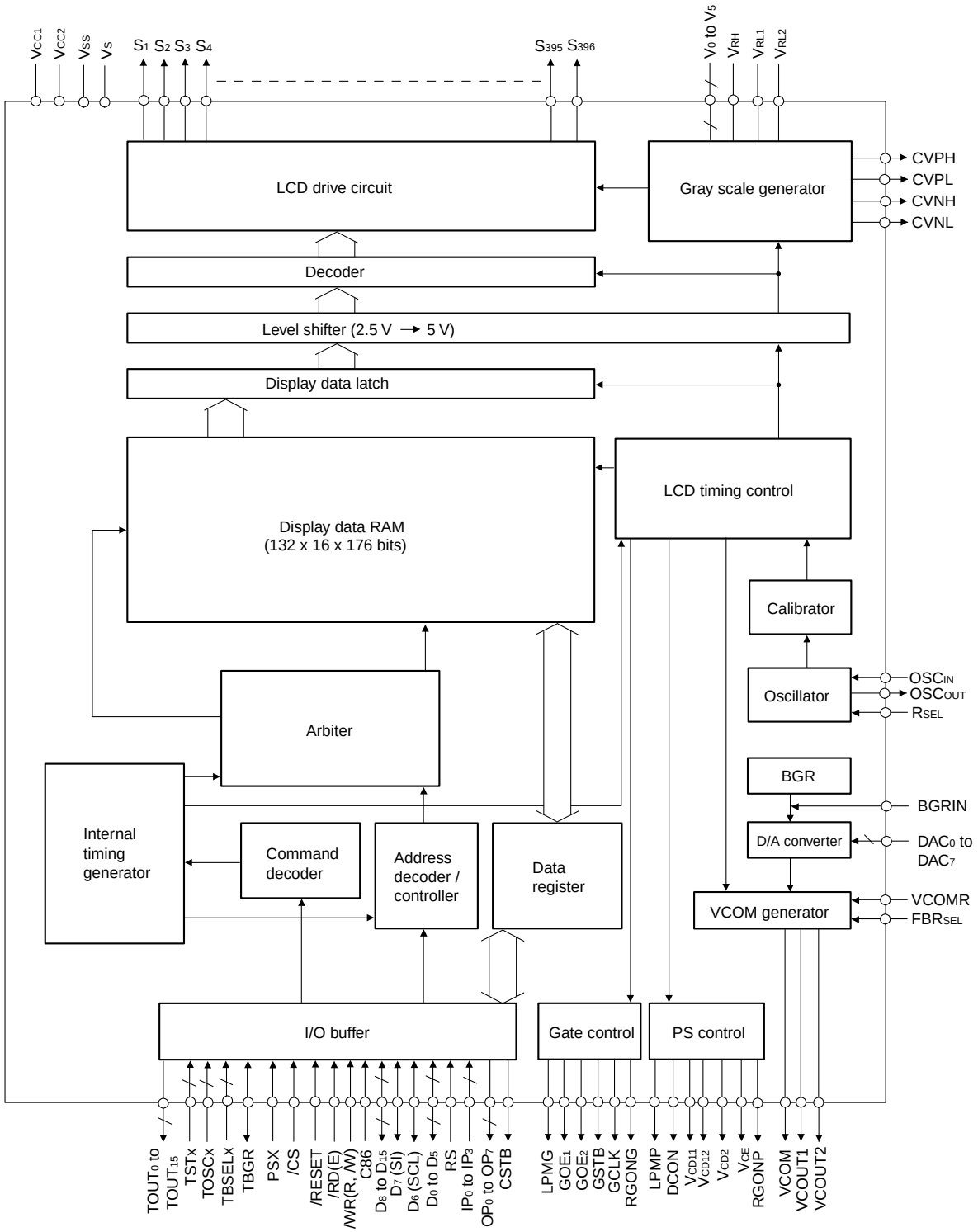
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (Pad Layout)

Chip size: 3.60 x 17.80 mm^2 TYP.

Bump size (output type A): 35 x 94 μm^2 TYP.

Bump size (input & dummy): 80 x 86 μm^2 TYP.

Alignment mark (mark center, unit: μm)

	X	Y
M1	–1615	8715
M2	–1615	–8715
M3	1435	–8715

Alignment mark reference (unit: μm)

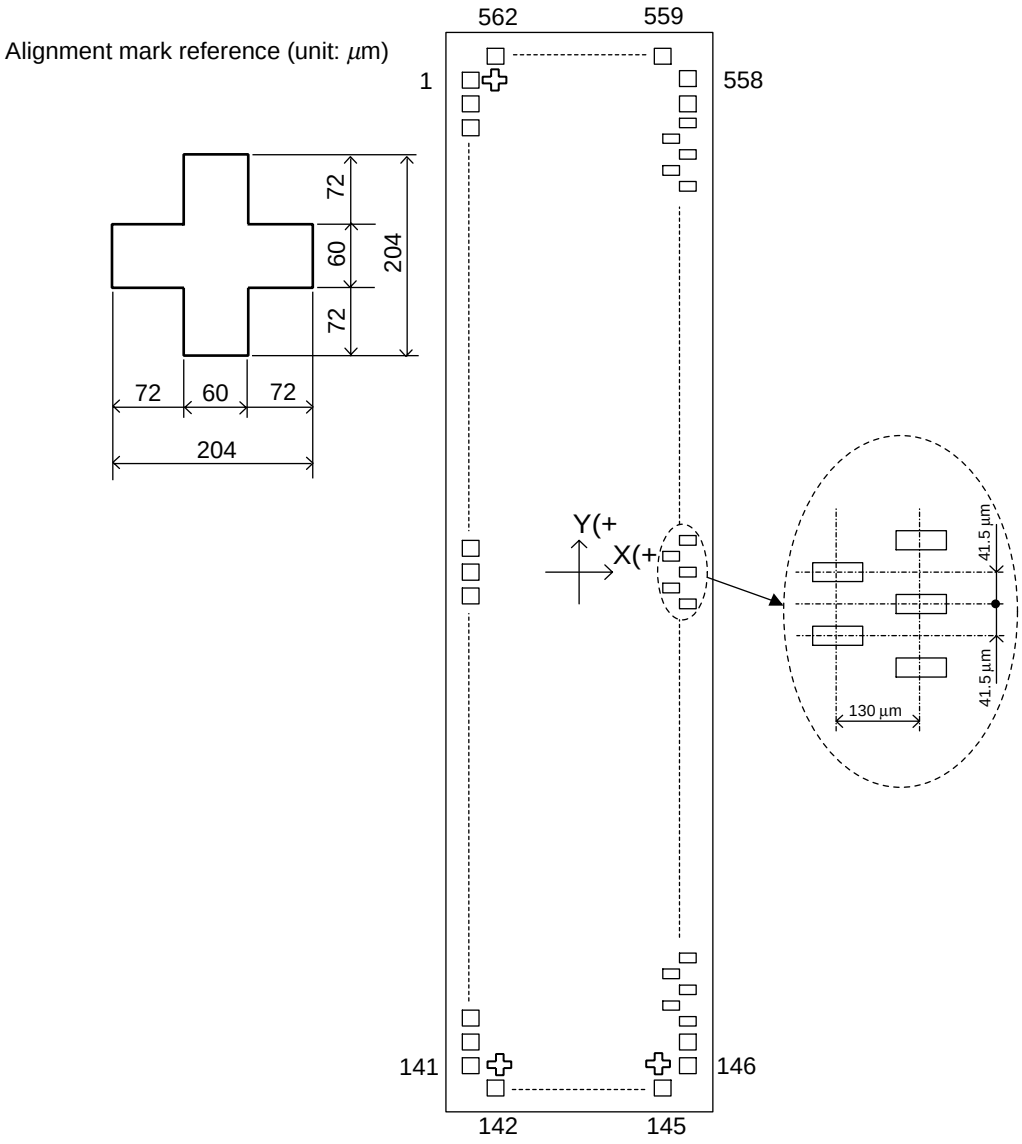


Table 2–1. Pad Layout (1/4)

Pin No.	Pin Name	Pad Type	X [μm]	Y [μm]
1	DUMMY	B	-1674.00	839.00
2	DUMMY	B	-1674.00	827.00
3	DUMMY	B	-1674.00	815.00
4	TOUT15	B	-1674.00	803.00
5	TOUT14	B	-1674.00	791.00
6	TOUT13	B	-1674.00	779.00
7	TOUT12	B	-1674.00	767.00
8	TOUT11	B	-1674.00	755.00
9	TOUT10	B	-1674.00	743.00
10	TOUT9	B	-1674.00	731.00
11	TOUT8	B	-1674.00	719.00
12	TOUT7	B	-1674.00	707.00
13	TOUT6	B	-1674.00	695.00
14	TOUT5	B	-1674.00	683.00
15	TOUT4	B	-1674.00	671.00
16	TOUT3	B	-1674.00	659.00
17	TOUT2	B	-1674.00	647.00
18	TOUT1	B	-1674.00	635.00
19	TOUT0	B	-1674.00	623.00
20	VSS(MODE)	B	-1674.00	611.00
21	TSTMHL	B	-1674.00	599.00
22	TSTRTST	B	-1674.00	587.00
23	TOSCSELO	B	-1674.00	575.00
24	TOSCSELI	B	-1674.00	563.00
25	TOSCI	B	-1674.00	551.00
26	TOSCO	B	-1674.00	539.00
27	VCC1(MODE)	B	-1674.00	527.00
28	RSEL	B	-1674.00	515.00
29	VSS(MODE)	B	-1674.00	503.00
30	OSCOUT	B	-1674.00	491.00
31	VSS(MODE)	B	-1674.00	479.00
32	OSCIN	B	-1674.00	467.00
33	VSS(MODE)	B	-1674.00	455.00
34	CSTB	B	-1674.00	443.00
35	D15	B	-1674.00	431.00
36	D14	B	-1674.00	419.00
37	D13	B	-1674.00	407.00
38	D12	B	-1674.00	395.00
39	D11	B	-1674.00	383.00
40	D10	B	-1674.00	371.00
41	D9	B	-1674.00	359.00
42	D8	B	-1674.00	347.00
43	D7 (SI)	B	-1674.00	335.00
44	D6 (SCL)	B	-1674.00	323.00
45	D5	B	-1674.00	311.00
46	D4	B	-1674.00	299.00
47	D3	B	-1674.00	287.00
48	D2	B	-1674.00	275.00
49	D1	B	-1674.00	263.00
50	D0	B	-1674.00	251.00
51	VSS(MODE)	B	-1674.00	239.00
52	/CS	B	-1674.00	227.00
53	/RESET	B	-1674.00	215.00
54	RS	B	-1674.00	203.00
55	/WR(R/W)	B	-1674.00	191.00
56	/RD(E)	B	-1674.00	179.00
57	VCC2	B	-1674.00	167.00
58	PSX	B	-1674.00	155.00
59	C86	B	-1674.00	143.00
60	VSS(MODE)	B	-1674.00	131.00
61	VCE	B	-1674.00	119.00
62	VCD2	B	-1674.00	107.00
63	VCD12	B	-1674.00	95.00
64	VCD11	B	-1674.00	83.00
65	LPMP	B	-1674.00	71.00
66	RGONP	B	-1674.00	59.00
67	DCON	B	-1674.00	47.00
68	VCOUT2	B	-1674.00	35.00
69	VSS	B	-1674.00	23.00
70	VCC2	B	-1674.00	11.00
71	VCC1	B	-1674.00	-1.00
72	VSS	B	-1674.00	-13.00
73	VSS	B	-1674.00	-25.00
74	CVNL	B	-1674.00	-37.00
75	CVNH	B	-1674.00	-49.00
76	CVPL	B	-1674.00	-61.00
77	CVPH	B	-1674.00	-73.00
78	VS	B	-1674.00	-85.00
79	VS	B	-1674.00	-97.00
80	VSS	B	-1674.00	-109.00
81	VCOUT1	B	-1674.00	-121.00
82	VCOUT1	B	-1674.00	-133.00
83	VCC1	B	-1674.00	-145.00
84	VCC1	B	-1674.00	-157.00
85	VCOM	B	-1674.00	-169.00
86	DUMMY	B	-1674.00	-181.00
87	DUMMY	B	-1674.00	-193.00
88	VSS(MODE)	B	-1674.00	-205.00
89	VCOMR	B	-1674.00	-217.00
90	BGRIN	B	-1674.00	-229.00
91	VCC1(MODE)	B	-1674.00	-241.00
92	FBRSEL	B	-1674.00	-253.00
93	VSS(MODE)	B	-1674.00	-265.00
94	VRH	B	-1674.00	-277.00
95	V0	B	-1674.00	-289.00
96	V1	B	-1674.00	-301.00
97	V2	B	-1674.00	-313.00
98	V3	B	-1674.00	-325.00
99	V4	B	-1674.00	-337.00
100	V5	B	-1674.00	-349.00
101	VRL1	B	-1674.00	-361.00
102	VRL2	B	-1674.00	-373.00
103	VSS(MODE)	B	-1674.00	-385.00
104	TBSEL1	B	-1674.00	-397.00
105	TBSEL2	B	-1674.00	-409.00
106	TBGR	B	-1674.00	-421.00
107	DAC7	B	-1674.00	-433.00
108	DAC6	B	-1674.00	-445.00
109	DAC5	B	-1674.00	-457.00
110	DAC4	B	-1674.00	-469.00
111	DAC3	B	-1674.00	-481.00
112	DAC2	B	-1674.00	-493.00
113	DAC1	B	-1674.00	-505.00
114	DAC0	B	-1674.00	-517.00
115	VSS(MODE)	B	-1674.00	-529.00
116	OP0	B	-1674.00	-541.00
117	OP1	B	-1674.00	-553.00
118	OP2	B	-1674.00	-565.00
119	OP3	B	-1674.00	-577.00
120	OP4	B	-1674.00	-589.00
121	OP5	B	-1674.00	-601.00
122	OP6	B	-1674.00	-613.00
123	OP7	B	-1674.00	-625.00
124	VCC1(MODE)	B	-1674.00	-637.00
125	IP0	B	-1674.00	-649.00
126	VSS(MODE)	B	-1674.00	-661.00
127	IP1	B	-1674.00	-673.00
128	VCC1(MODE)	B	-1674.00	-685.00
129	IP2	B	-1674.00	-697.00
130	VSS(MODE)	B	-1674.00	-709.00
131	IP3	B	-1674.00	-721.00
132	VCC1(MODE)	B	-1674.00	-733.00
133	GSTB	B	-1674.00	-745.00
134	GCLK	B	-1674.00	-757.00
135	GOE1	B	-1674.00	-769.00
136	GOE2	B	-1674.00	-781.00
137	RGONG	B	-1674.00	-793.00
138	LPMG	B	-1674.00	-805.00
139	DUMMY	B	-1674.00	-817.00
140	DUMMY	B	-1674.00	-829.00
141	DUMMY	B	-1674.00	-841.00
142	DUMMY	B	-1350.00	-874.00
143	DUMMY	B	-510.00	-874.00
144	DUMMY	B	330.00	-874.00
145	DUMMY	B	1170.00	-874.00
146	DUMMY	B	1670.00	-860.00
147	DUMMY	A	1670.00	-852.00
148	DUMMY	A	1540.00	-847.50
149	S396	A	1670.00	-843.00
150	S395	A	1540.00	-838.50
151	S394	A	1670.00	-834.00
152	S393	A	1540.00	-829.50
153	S392	A	1670.00	-825.00
154	S391	A	1540.00	-820.50
155	S390	A	1670.00	-816.00
156	S389	A	1540.00	-811.50
157	S388	A	1670.00	-807.00
158	S387	A	1540.00	-802.50
159	S386	A	1670.00	-798.00
160	S385	A	1540.00	-793.50
161	S384	A	1670.00	-789.00
162	S383	A	1540.00	-784.50
163	S382	A	1670.00	-780.00
164	S381	A	1540.00	-775.50
165	S380	A	1670.00	-771.00
166	S379	A	1540.00	-766.50
167	S378	A	1670.00	-762.00
168	S377	A	1540.00	-757.50
169	S376	A	1670.00	-753.00
170	S375	A	1540.00	-748.50
171	S374	A	1670.00	-744.00
172	S373	A	1540.00	-739.50
173	S372	A	1670.00	-735.00
174	S371	A	1540.00	-730.50
175	S370	A	1670.00	-726.00
176	S369	A	1540.00	-721.50
177	S368	A	1670.00	-717.00
178	S367	A	1540.00	-712.50
179	S366	A	1670.00	-708.00
180	S365	A	1540.00	-703.50

Table 2–1. Pad Layout (2/4)

Pin No.	Pin Name	Pad Type	X [μm]	Y [μm]
181	S364	A	167.00	-7109.00
182	S363	A	154.00	-7067.50
183	S362	A	167.00	-7026.00
184	S361	A	154.00	-6984.50
185	S360	A	167.00	-6943.00
186	S359	A	154.00	-6901.50
187	S358	A	167.00	-6860.00
188	S357	A	154.00	-6818.50
189	S356	A	167.00	-6777.00
190	S355	A	154.00	-6735.50
191	S354	A	167.00	-6694.00
192	S353	A	154.00	-6652.50
193	S352	A	167.00	-6611.00
194	S351	A	154.00	-6569.50
195	S350	A	167.00	-6528.00
196	S349	A	154.00	-6486.50
197	S348	A	167.00	-6445.00
198	S347	A	154.00	-6403.50
199	S346	A	167.00	-6362.00
200	S345	A	154.00	-6320.50
201	S344	A	167.00	-6279.00
202	S343	A	154.00	-6237.50
203	S342	A	167.00	-6196.00
204	S341	A	154.00	-6154.50
205	S340	A	167.00	-6113.00
206	S339	A	154.00	-6071.50
207	S338	A	167.00	-6030.00
208	S337	A	154.00	-5988.50
209	S336	A	167.00	-5947.00
210	S335	A	154.00	-5905.50
211	S334	A	167.00	-5864.00
212	S333	A	154.00	-5822.50
213	S332	A	167.00	-5781.00
214	S331	A	154.00	-5739.50
215	S330	A	167.00	-5698.00
216	S329	A	154.00	-5656.50
217	S328	A	167.00	-5615.00
218	S327	A	154.00	-5573.50
219	S326	A	167.00	-5532.00
220	S325	A	154.00	-5490.50
221	S324	A	167.00	-5449.00
222	S323	A	154.00	-5407.50
223	S322	A	167.00	-5366.00
224	S321	A	154.00	-5324.50
225	S320	A	167.00	-5283.00
226	S319	A	154.00	-5241.50
227	S318	A	167.00	-5200.00
228	S317	A	154.00	-5158.50
229	S316	A	167.00	-5117.00
230	S315	A	154.00	-5075.50
231	S314	A	167.00	-5034.00
232	S313	A	154.00	-4992.50
233	S312	A	167.00	-4951.00
234	S311	A	154.00	-4909.50
235	S310	A	167.00	-4868.00
236	S309	A	154.00	-4826.50
237	S308	A	167.00	-4785.00
238	S307	A	154.00	-4743.50
239	S306	A	167.00	-4702.00
240	S305	A	154.00	-4660.50
241	S304	A	167.00	-4619.00
242	S303	A	154.00	-4577.50
243	S302	A	167.00	-4536.00
244	S301	A	154.00	-4494.50
245	S300	A	167.00	-4453.00
246	S299	A	154.00	-4411.50
247	S298	A	167.00	-4370.00
248	S297	A	154.00	-4328.50
249	S296	A	167.00	-4287.00
250	S295	A	154.00	-4245.50
251	S294	A	167.00	-4204.00
252	S293	A	154.00	-4162.50
253	S292	A	167.00	-4121.00
254	S291	A	154.00	-4079.50
255	S290	A	167.00	-4038.00
256	S289	A	154.00	-3996.50
257	S288	A	167.00	-3955.00
258	S287	A	154.00	-3913.50
259	S286	A	167.00	-3872.00
260	S285	A	154.00	-3830.50
261	S284	A	167.00	-3789.00
262	S283	A	154.00	-3747.50
263	S282	A	167.00	-3706.00
264	S281	A	154.00	-3664.50
265	S280	A	167.00	-3623.00
266	S279	A	154.00	-3581.50
267	S278	A	167.00	-3540.00
268	S277	A	154.00	-3498.50
269	S276	A	167.00	-3457.00
270	S275	A	154.00	-3415.50
271	S274	A	167.00	-3374.00
272	S273	A	154.00	-3332.50
273	S272	A	167.00	-3291.00
274	S271	A	154.00	-3249.50
275	S270	A	167.00	-3208.00
276	S269	A	154.00	-3166.50
277	S268	A	167.00	-3125.00
278	S267	A	154.00	-3083.50
279	S266	A	167.00	-3042.00
280	S265	A	154.00	-3000.50
281	S264	A	167.00	-2959.00
282	S263	A	154.00	-2917.50
283	S262	A	167.00	-2876.00
284	S261	A	154.00	-2834.50
285	S260	A	167.00	-2793.00
286	S259	A	154.00	-2751.50
287	S258	A	167.00	-2710.00
288	S257	A	154.00	-2668.50
289	S256	A	167.00	-2627.00
290	S255	A	154.00	-2585.50
291	S254	A	167.00	-2544.00
292	S253	A	154.00	-2502.50
293	S252	A	167.00	-2461.00
294	S251	A	154.00	-2419.50
295	S250	A	167.00	-2378.00
296	S249	A	154.00	-2336.50
297	S248	A	167.00	-2295.00
298	S247	A	154.00	-2253.50
299	S246	A	167.00	-2212.00
300	S245	A	154.00	-2170.50
301	S244	A	167.00	-2129.00
302	S243	A	154.00	-2087.50
303	S242	A	167.00	-2046.00
304	S241	A	154.00	-2004.50
305	S240	A	167.00	-1963.00
306	S239	A	154.00	-1921.50
307	S238	A	167.00	-1880.00
308	S237	A	154.00	-1838.50
309	S236	A	167.00	-1797.00
310	S235	A	154.00	-1755.50
311	S234	A	167.00	-1714.00
312	S233	A	154.00	-1672.50
313	S232	A	167.00	-1631.00
314	S231	A	154.00	-1589.50
315	S230	A	167.00	-1548.00
316	S229	A	154.00	-1506.50
317	S228	A	167.00	-1465.00
318	S227	A	154.00	-1423.50
319	S226	A	167.00	-1382.00
320	S225	A	154.00	-1340.50
321	S224	A	167.00	-1299.00
322	S223	A	154.00	-1257.50
323	S222	A	167.00	-1216.00
324	S221	A	154.00	-1174.50
325	S220	A	167.00	-1133.00
326	S219	A	154.00	-1091.50
327	S218	A	167.00	-1050.00
328	S217	A	154.00	-1008.50
329	S216	A	167.00	-967.00
330	S215	A	154.00	-925.50
331	S214	A	167.00	-884.00
332	S213	A	154.00	-842.50
333	S212	A	167.00	-801.00
334	S211	A	154.00	-759.50
335	S210	A	167.00	-718.00
336	S209	A	154.00	-676.50
337	S208	A	167.00	-635.00
338	S207	A	154.00	-593.50
339	S206	A	167.00	-552.00
340	S205	A	154.00	-510.50
341	S204	A	167.00	-469.00
342	S203	A	154.00	-427.50
343	S202	A	167.00	-386.00
344	S201	A	154.00	-344.50
345	S200	A	167.00	-303.00
346	S199	A	154.00	-261.50
347	S198	A	167.00	-220.00
348	S197	A	154.00	-178.50
349	S196	A	167.00	-137.00
350	S195	A	154.00	-95.50
351	S194	A	167.00	-54.00
352	S193	A	154.00	-12.50
353	DUMMY	A	167.00	29.00
354	DUMMY	A	154.00	70.50
355	DUMMY	A	167.00	112.00
356	DUMMY	A	154.00	153.50
357	DUMMY	A	167.00	195.00
358	DUMMY	A	154.00	236.50
359	DUMMY	A	167.00	278.00
360	DUMMY	A	154.00	319.50

Table 2–1. Pad Layout (3/4)

Pin No.	Pin Name	Pad Type	X [μm]	Y [μm]
361	DUMMY	A	167.00	361.00
362	DUMMY	A	154.00	402.50
363	DUMMY	A	167.00	444.00
364	DUMMY	A	154.00	485.50
365	S192	A	167.00	527.00
366	S191	A	154.00	568.50
367	S190	A	167.00	610.00
368	S189	A	154.00	651.50
369	S188	A	167.00	693.00
370	S187	A	154.00	734.50
371	S186	A	167.00	776.00
372	S185	A	154.00	817.50
373	S184	A	167.00	859.00
374	S183	A	154.00	900.50
375	S182	A	167.00	942.00
376	S181	A	154.00	983.50
377	S180	A	167.00	1025.00
378	S179	A	154.00	1066.50
379	S178	A	167.00	1108.00
380	S177	A	154.00	1149.50
381	S176	A	167.00	1191.00
382	S175	A	154.00	1232.50
383	S174	A	167.00	1274.00
384	S173	A	154.00	1315.50
385	S172	A	167.00	1357.00
386	S171	A	154.00	1398.50
387	S170	A	167.00	1440.00
388	S169	A	154.00	1481.50
389	S168	A	167.00	1523.00
390	S167	A	154.00	1564.50
391	S166	A	167.00	1606.00
392	S165	A	154.00	1647.50
393	S164	A	167.00	1689.00
394	S163	A	154.00	1730.50
395	S162	A	167.00	1772.00
396	S161	A	154.00	1813.50
397	S160	A	167.00	1855.00
398	S159	A	154.00	1896.50
399	S158	A	167.00	1938.00
400	S157	A	154.00	1979.50
401	S156	A	167.00	2021.00
402	S155	A	154.00	2062.50
403	S154	A	167.00	2104.00
404	S153	A	154.00	2145.50
405	S152	A	167.00	2187.00
406	S151	A	154.00	2228.50
407	S150	A	167.00	2270.00
408	S149	A	154.00	2311.50
409	S148	A	167.00	2353.00
410	S147	A	154.00	2394.50
411	S146	A	167.00	2436.00
412	S145	A	154.00	2477.50
413	S144	A	167.00	2519.00
414	S143	A	154.00	2560.50
415	S142	A	167.00	2602.00
416	S141	A	154.00	2643.50
417	S140	A	167.00	2685.00
418	S139	A	154.00	2726.50
419	S138	A	167.00	2768.00
420	S137	A	154.00	2809.50
421	S136	A	167.00	2851.00
422	S135	A	154.00	2892.50
423	S134	A	167.00	2934.00
424	S133	A	154.00	2975.50
425	S132	A	167.00	3017.00
426	S131	A	154.00	3058.50
427	S130	A	167.00	3100.00
428	S129	A	154.00	3141.50
429	S128	A	167.00	3183.00
430	S127	A	154.00	3224.50
431	S126	A	167.00	3266.00
432	S125	A	154.00	3307.50
433	S124	A	167.00	3349.00
434	S123	A	154.00	3390.50
435	S122	A	167.00	3432.00
436	S121	A	154.00	3473.50
437	S120	A	167.00	3515.00
438	S119	A	154.00	3556.50
439	S118	A	167.00	3598.00
440	S117	A	154.00	3639.50
441	S116	A	167.00	3681.00
442	S115	A	154.00	3722.50
443	S114	A	167.00	3764.00
444	S113	A	154.00	3805.50
445	S112	A	167.00	3847.00
446	S111	A	154.00	3888.50
447	S110	A	167.00	3930.00
448	S109	A	154.00	3971.50
449	S108	A	167.00	4013.00
450	S107	A	154.00	4054.50
451	S106	A	167.00	4096.00
452	S105	A	154.00	4137.50
453	S104	A	167.00	4179.00
454	S103	A	154.00	4220.50
455	S102	A	167.00	4262.00
456	S101	A	154.00	4303.50
457	S100	A	167.00	4345.00
458	S99	A	154.00	4386.50
459	S98	A	167.00	4428.00
460	S97	A	154.00	4469.50
461	S96	A	167.00	4511.00
462	S95	A	154.00	4552.50
463	S94	A	167.00	4594.00
464	S93	A	154.00	4635.50
465	S92	A	167.00	4677.00
466	S91	A	154.00	4718.50
467	S90	A	167.00	4760.00
468	S89	A	154.00	4801.50
469	S88	A	167.00	4843.00
470	S87	A	154.00	4884.50
471	S86	A	167.00	4926.00
472	S85	A	154.00	4967.50
473	S84	A	167.00	5009.00
474	S83	A	154.00	5050.50
475	S82	A	167.00	5092.00
476	S81	A	154.00	5133.50
477	S80	A	167.00	5175.00
478	S79	A	154.00	5216.50
479	S78	A	167.00	5258.00
480	S77	A	154.00	5299.50
481	S76	A	167.00	5341.00
482	S75	A	154.00	5382.50
483	S74	A	167.00	5424.00
484	S73	A	154.00	5465.50
485	S72	A	167.00	5507.00
486	S71	A	154.00	5548.50
487	S70	A	167.00	5590.00
488	S69	A	154.00	5631.50
489	S68	A	167.00	5673.00
490	S67	A	154.00	5714.50
491	S66	A	167.00	5756.00
492	S65	A	154.00	5797.50
493	S64	A	167.00	5839.00
494	S63	A	154.00	5880.50
495	S62	A	167.00	5922.00
496	S61	A	154.00	5963.50
497	S60	A	167.00	6005.00
498	S59	A	154.00	6046.50
499	S58	A	167.00	6088.00
500	S57	A	154.00	6129.50
501	S56	A	167.00	6171.00
502	S55	A	154.00	6212.50
503	S54	A	167.00	6254.00
504	S53	A	154.00	6295.50
505	S52	A	167.00	6337.00
506	S51	A	154.00	6378.50
507	S50	A	167.00	6420.00
508	S49	A	154.00	6461.50
509	S48	A	167.00	6503.00
510	S47	A	154.00	6544.50
511	S46	A	167.00	6586.00
512	S45	A	154.00	6627.50
513	S44	A	167.00	6669.00
514	S43	A	154.00	6710.50
515	S42	A	167.00	6752.00
516	S41	A	154.00	6793.50
517	S40	A	167.00	6835.00
518	S39	A	154.00	6876.50
519	S38	A	167.00	6918.00
520	S37	A	154.00	6959.50
521	S36	A	167.00	7001.00
522	S35	A	154.00	7042.50
523	S34	A	167.00	7084.00
524	S33	A	154.00	7125.50
525	S32	A	167.00	7167.00
526	S31	A	154.00	7208.50
527	S30	A	167.00	7250.00
528	S29	A	154.00	7291.50
529	S28	A	167.00	7333.00
530	S27	A	154.00	7374.50
531	S26	A	167.00	7416.00
532	S25	A	154.00	7457.50
533	S24	A	167.00	7499.00
534	S23	A	154.00	7540.50
535	S22	A	167.00	7582.00
536	S21	A	154.00	7623.50
537	S20	A	167.00	7665.00
538	S19	A	154.00	7706.50
539	S18	A	167.00	7748.00
540	S17	A	154.00	7789.50

Table 2–1. Pad Layout (4/4)

Pin No.	Pin Name	Pad Type	X [μm]	Y [μm]
541	S16	A	1670.00	7831.00
542	S15	A	1540.00	7872.50
543	S14	A	1670.00	7914.00
544	S13	A	1540.00	7955.50
545	S12	A	1670.00	7997.00
546	S11	A	1540.00	8038.50
547	S10	A	1670.00	8080.00
548	S9	A	1540.00	8121.50
549	S8	A	1670.00	8163.00
550	S7	A	1540.00	8204.50
551	S6	A	1670.00	8246.00
552	S5	A	1540.00	8287.50
553	S4	A	1670.00	8329.00
554	S3	A	1540.00	8370.50
555	S2	A	1670.00	8412.00
556	S1	A	1540.00	8453.50
557	DUMMY	A	1670.00	8495.00
558	DUMMY	B	1670.00	8575.00
559	DUMMY	B	1220.00	8774.00
560	DUMMY	B	380.00	8774.00
561	DUMMY	B	-460.00	8774.00
562	DUMMY	B	-1300.00	8774.00

3. PIN FUNCTIONS

3.1 Power Supply System Pins

Symbol	Pin Name	Pad No.	I/O	Function
V_{CC1}	Logic power supply	71, 83, 84	–	Power supply pin for logic circuit
V_{CC2}	I/O power supply	57, 70	–	Power supply pin for I/O buffer
V_S	Driver power supply	78, 79	–	Power supply pin for driver circuit
V_{SS}	Ground	69, 72, 72, 80	–	Ground pin for logic and driver circuits
V_0 to V_5 V_{RH} V_{RL1}, V_{RL2}	Power supply for γ-curve correction	95 to 100, 94, 101, 102	–	The μPD161622 includes power supplies and resistors for the γ-curve, so if the characteristics of the γ-curve and LCD panel in the μPD161622 match, leave V_0 to V_5, V_{RH}, V_{RL1}, V_{RL2} open. If some kind of correction is required, adjust the γ-curve by connecting resistors between the V_0 to V_5, V_{RH}, V_{RL1}, V_{RL2} pins (see **5.9 γ-Curve Correction Power Supply Circuit for Cases of Unbalanced Driving**).
$V_{CC1(MODE)}$	Mode setting pull-up power-supply	27, 91, 124, 128, 132	–	Pull-up power-supply pin for mode setting
$V_{SS(MODE)}$	Mode setting pull-down power-supply	20, 29, 31, 33, 51, 60, 88, 93, 103, 115, 126, 130	–	Pull-down power-supply pin for mode setting

3.2 Logic System Pins (1/2)

Symbol	Pin Name	Pad No.	I/O	Function
PSX	CPU interface selection	58	Input	These pins are used to select the CPU interface mode. PSX = H: Parallel interface PSX = L: Serial interface When the parallel interface is selected, this data but width can be changed between 8 bits and 16 bits by using BMD of index register 5 (R5).
★ /CS	Chip select	52	Input	This pin is used for chip select signals. When /CS = L, the chip is active and can perform data input/output operations including command and data I/O.
/RESET	Reset	53	Input	When /RESET is low, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.
/RD (E)	Read (enable)	56	Input	When i80 series parallel data transfer (/RD) has been selected, the signal at this pin is used to enable read operations. Data is output to the data bus only when this pin is low. When M68 series parallel data transfer (E) has been selected, the signal at this pin is used to enable read/write operations.
/WR (R, /W)	Write (read/write)	55	Input	When i80 series parallel data transfer (/WR) has been selected, the signal at this pin is used to enable write operations. Data is written at the rising edge of this signal. When M68 series parallel data transfer (R, /W) and serial data has been selected, this pin is used to determine the direction of data transfer. L: Write H: Read
C86	Select interface	59	Input	This pin is used to switch between interface modes (i80 series CPU or M68 series CPU). L: Selects i80 series CPU mode H: Selects M68 series CPU mode

(2/2)

	Symbol	Pin Name	Pad No.	I/O	Function
★ ★	D_0 to D_5, D_8 to D_{15}, D_6 (SCL), D_7 (SI)	Data bus (serial clock) (serial data input)	50 to 35	I/O	These pins comprise 16-bit bi-directional data. When the serial interface has been selected (PSX = L), D_7 functions as a serial data input pin (SI), D_6 functions as a serial clock input pin (SCL). In either case, pins D_0 to D_7 and D_8 to D_{15} are in high impedance mode. When the chip is not selected, D_0 to D_{15} are in high impedance mode.
	RS	Index register/, data/command selection	54	Input	When parallel data transfer has been selected, this pin is usually connected to the least significant bit of the standard CPU address bus and is used to distinguish between data from index registers and data/commands. RS = H: Indicates that data from D_0 to D_{15} is data/command RS = L: Indicates that data from D_0 to D_7 is index register contents Also, when serial data transfer is selected, the level of the RS pin is fetched at the rising edge of the eighth clock of the serial clock and whether the data is index register contents or data/command is distinguished. RS = H: Indicates that the data input to SI is data/command. RS = L: Indicates that the data input to SI is index register contents.
	IP_0 to IP_3	Input port	125, 127, 129, 131	Input	This is a general-purpose input port. The status of these pins (H or L) can be read via a command. Because this is a CMOS input, do not leave open.
	OP_0 to OP_7	Output port	116 to 123	Output	This is a general-purpose output port. The status of these pins (H or L) can be write via a command. Leave open when in unused.
	R_{SEL}	Oscillation signal select	28	Input	This pin is for oscillation signal selection. When in used external resistance connection oscillator circuit, this pin set H. When in used internal oscillator circuit, this pin set L. R_{SEL} = H: External resistance connection oscillator circuit select R_{SEL} = L: CR internal oscillator circuit select
★	OSC_{IN}	Oscillation signal	32	Input	This pin is for oscillation signal input. R_{SEL} = H: Connect 51 kΩ resistance between OSC_{IN} and OSC_{OUT}. R_{SEL} = L: Leave open
★	OSC_{OUT}	Oscillation signal	30	Output	This pin is for oscillation signal input. R_{SEL} = H: Connect 51 kΩ resistance between OSC_{IN} and OSC_{OUT}. R_{SEL} = L: Leave open
	CSTB	GSTB logic signal	34	Output	This pin outputs STB signal for gate driver leveled by interface power supply voltage (V_{CC2}). This output signal is reverse signal of GSTB.

Remark T.B.D. (To be determined.)

3.3 Gate Driver IC Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
LPMG	Low power mode signal	138	Output	This is an output pin for low power mode (for the gate driver). Connect to the LPM pin of the gate driver.
GOE_1	OE_1 output for gate driver	135	Output	This pin is an output pin for the low power mode (for the OE_1). Connect to the OE_1 pin of the gate driver. Timing signal for output, refer to **5.4 Display timing generator.**
GOE_2	OE_2 output for gate driver	136	Output	This pin is the OE_2 output for the gate driver. Connect to the OE_2 pin of the gate driver. Timing signal for output, refer to **5.4 Display timing generator.**
GSTB	STB output for gate driver	133	Output	This pin is the STB output for the gate driver. Connect to the STVR or STVL pin of the gate driver. Timing signal for output, refer to **5.4 Display timing generator.**
GCLK	CLK output for gate driver	134	Output	This pin is the CLK output for the gate driver. Connect to the CLK pin of the gate driver.
RGONG	Regulator control	137	Output	Regulator ON/OFF control of gate driver IC Connect to the RGONG pin of the gate driver.

3.4 Power Supply Control Pins

Symbol	Pin Name	Pad No.	I/O	Function
LPMP	Low power mode signal	65	Output	Low power mode control signal output pin (for power-supply IC). This pin connects to LPM pin of power-supply IC.
DCON	DC/DC converter control	67	Output	DC/DC converter ON/OFF signal pin for power-supply IC. This pin connects DCON pin of power-supply IC.
RGONP	Regulator control	66	Output	Regulator ON/OFF control signal pin for power-supply IC. This pin connects to RGONP pin of power-supply IC.
V_{CD11}, V_{CD12}	V_{DD1} booster selection	64, 63	Output	Control signal to select x4/x5/x6/x7 booster of power-supply IC for V_{CC1}. Connect to the V_{CD11} and V_{CD12} pins of the power-supply IC.
V_{CD2}	V_{DD2} booster selection	62	Output	Control signal to select x2/x3 booster of power-supply IC for V_{CC2}. Connect to the V_{CD2} pin of the power-supply IC.
V_{CE}	V_O level selection	61	Output	Signal for selecting the level of the power-supply IC booster voltage, to be used for the maximum voltage of V_O. Selects that the booster voltage level is either the same level as V_{DD1} or a multiple of minus 1. Connect to the V_{CE} pin of the power-supply IC.

3.5 Driver-Related Pins

Symbol	Pin Name	Pad No.	I/O	Function
S_1 to S_{396}	Source output	556 to 365, 352 to 149	Output	Source output pins
VCOM	COM adjustment	85	Output	This pin is the common adjustment output.
VCOUT1	Center rectangle signal output	81, 82	Output	This pin is the center rectangle signal output (V_{p-p}) for common modulation between 0 V to V_S.
VCOUT2	Center rectangle signal output	68	Output	This pin is the center rectangle signal output (V_{p-p}) for common modulation between 0 V to V_{CC1}.
BGRIN	External-power-supply connect	90	Input	This is an external-power-supply connect pin for VCOM. This pin is valid when BGRS (power supply control register 1: R25) = 1. In this case, the reference voltage of the amplifier for setting the common waveform center value is input from outside the μPD161622 When BGRS = 0, power supply with built-in the μPD161622 is set up as a standard voltage for common waveform center value setup. In this case, leave it open. For more detail, refer to **5.5 Common Adjustment.**
VCOMR	VCOM setting resistor connection	89	Input	Connects an external feedback resistor for VCOM setting. This pin is valid when FBR_{SEL} = L. In this case, connect a feedback resistor between the VCOM pin and GND. When FBR_{SEL} = H, the amplifier for setting the common waveform center value operates as a voltage follower. In this case, leave it open. For more detail, refer to **5.5 Common Adjustment.**
FBR_{SEL}	VCOM setting external circuit select	92	Input	This pin is used to select the method of adjusting the amplifier for setting the common waveform center value used to set the COMMON drive waveform center level. FBR_{SEL} = H: Voltage follower circuit used (VCOMR connected to VCOM internally) FBR_{SEL} = L: External feedback resistor used
CVPH, CVPL, CVNH, CVNL	Basis power supply for γ-corrected power supplies	77, 76, 75, 74	–	This is operational amplifier output pin for the γ-corrected power supplies. Normally, this pin connects capacitor of T.B.D. μF
DAC_0 to DAC_7	D/A converter value setting	114 to 107	Input	These pins set the reference voltage of the amplifier for setting the VCOM value used to set the COMMON drive waveform center level. These pins are valid when the VCOM output center value setting register (R29) = 00H and BGRS (R25: D_6) = 0. This pin is pulled up to the inside IC, therefore, connect to only V_{SS} when in low level setting pin. For more details, refer to **5.5 Common Adjustment Circuit.**

3.6 Test or Other Pins

Symbol	Pin Name	Pad No.	I/O	Function
$TOUT_0$ to $TOUT_{15}$, TOSCO	Source output	19 to 4, 26	Output	This is output pin when μPD161622 is in test mode. Normally, leave it open.
★ TSTRTST, TSTVIHL, TOSCI, TOSCSELI, TOSCSELO, $TBSEL_1$, $TBSEL_2$	COM adjustment	22, 21, 25, 24, 23, 104, 105	Output	These pins are to set up test mode of μPD161622. Normally, fixed it to V_{SS}.
TBGR	Test input/output	106	I/O	This is output pin when μPD161622 is in test mode. Normally, leave it open.
DUMMY	Dummy pin	1 to 3, 86, 87, 139 to 148, 353 to 364, 557 to 562	–	Dummy pin The dummy pins of pads No. 1, 2, 557, and 558 are wired using aluminum inside the μPD161622. The dummy pins of pads No. 140, 141, 146, and 147 are wired using aluminum inside the μPD161622.

4. PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The I/O circuit types of each pin and recommended connection of unused pins are described below.

Pin Name	Input Type	I/O	Power supply	Recommended Connection of Unused Pins		Notes
				Parallel Interface	Serial Interface	
PSX	Schmitt trigger	Input	V_{CC2}	Mode setting pin		1
/RESET	Schmitt trigger	Input	V_{CC2}	Always reset on power application		–
/RD (E)	Schmitt trigger	Input	V_{CC2}	Connect to V_{CC2} (when i80 series interface)	Connect to V_{CC2} or V_{SS}.	–
★ C86	Schmitt trigger	Input	V_{CC2}	Mode setting pin	Connect to V_{CC1} or V_{SS}.	1
D_0 to D_5	Schmitt trigger	I/O	V_{CC2}	–	Leave open	–
D_6 (SCL)	Schmitt trigger	I/O	V_{CC2}	–		–
D_7 (SI)	Schmitt trigger	I/O	V_{CC2}	–		–
D_8 to D_{15}	Schmitt trigger	I/O	V_{CC2}	–	Leave open	–
RS	Schmitt trigger	Input	V_{CC2}	Register setting pin		2
IP_0 to IP_3	Schmitt trigger	Input	V_{CC1}	Connect to V_{CC1} or V_{SS}.		–
OP_0 to OP_7	–	Output	V_{CC1}	Leave open		–
★ OSC_{IN}	CMOS	Input	V_{CC2}	Input external clock (R_{SEL} = H) Leave open (R_{SEL} = L)		–
★ OSC_{OUT}	CMOS	Input	V_{CC2}	Leave open (R_{SEL} = H/L)		–
CSTB	–	Output	V_{CC2}	Leave open		–
R_{SEL}	Schmitt trigger	Input	V_{CC1}	Mode setting pin		3
LPMG	–	Output	V_{CC1}	Leave open		–
GOE_1	–	Output	V_{CC1}	Always connect to the gate driver		–
GOE_2	–	Output	V_{CC1}	Always connect to the gate driver		–
GSTB	–	Output	V_{CC1}	Always connect to the gate driver		–
GCLK	–	Output	V_{CC1}	Always connect to the gate driver		–
RGONG	–	Output	V_{CC1}	Always connect to the gate driver		–
LPMP	–	Output	V_{CC1}	Leave open		–
DCON	–	Output	V_{CC1}	Always connect to the power IC		–
RGONP	–	Output	V_{CC1}	Always connect to the power IC		–
V_{CD11}, V_{CD12}	–	Output	V_{CC1}	Always connect to the power IC		–
V_{CD2}	–	Output	V_{CC1}	Always connect to the power IC		–
V_{CE}	–	Output	V_{CC1}	Always connect to the power IC		–
VCOUT1	–	Output	V_S	Leave open		–
VCOUT2	–	Output	V_{CC1}	Leave open		–
BGRIN	–	Input	V_S	Leave open (BGRS = L [R25])		–
V_{COM}	–	Output	V_S	Leave open (FRB_{SEL} = H)		–
VCOMR	–	Input	V_S	Leave open (FRB_{SEL} = H)		–
$TOUT_0$ to $TOUT_{15}$	–	Output	V_{CC1}	Leave open		–
TOSCO	–	Output	V_{CC1}	Leave open		–
TSTRTST	–	Input	V_{CC1}	Connect to V_{SS}.		–
TSTVIHL	–	Input	V_{CC1}	Connect to V_{SS}.		–
TOSCI	–	Input	V_{CC1}	Connect to V_{SS}.		–
TOSCSELI	–	Input	V_{CC1}	Connect to V_{SS}.		–
TOSCSELO	–	Input	V_{CC1}	Connect to V_{SS}.		–
TBSEL1	–	Input	V_{CC1}	Connect to V_{SS}.		–
TBSEL2	–	Input	V_{CC1}	Connect to V_{SS}.		–
TBGR	–	I/O	V_{CC1}	Leave open		–

Notes 1. Connect to V_{CC2} or V_{SS}, depending on the mode selected.

2. Input either H or L by CPU, depending on the register selected

3. Connect to V_{CC1} or V_{SS}, depending on the mode selected.

5. DESCRIPTION OF FUNCTIONS

5.1 CPU Interface

5.1.1 Selection of interface type

The μPD161622 chip transfers data using a 16-bit bi-directional data bus (D_{15} to D_0), 8-bit bi-directional data bus (D_7 to D_0) or a serial data input (SI). Setting the polarity of the PSX pin as either H or L enables the selections shown in table 5–1 below.

★ **Table 5–1.**

PSX	BMD	Mode	/CS	RS	/RD (E)	/WR (R,/W)	C86	D_{15} to D_8	D_7	D_6	D_5 to D_0
H	0	16-bit parallel	/CS	RS	/RD (E)	/WR (R,/W)	C86	D_{15} to D_8	D_7	D_6	D_5 to D_0
H	1	8-bit parallel	/CS	RS	/RD (E)	/WR (R,/W)	C86	Hi-Z Note1	D_7	D_6	D_5 to D_0
L	X Note2	Serial Note3	/CS	RS	**Note2**	**Note2**	**Note2**	Hi-Z Note1	SI	SCL	Hi-Z Note1

Notes 1. Hi-Z: High impedance

2. X: Don't care (1 or 0)

3. In serial mode, read function is not available.

5.1.2 Parallel interface

When the parallel interface has been selected (PSX = H), setting the C86 pin as either H or L enables a direct connection to an i80 series or M68 series CPU (see table 5–2 below).

Table 5–2.

C86	Mode	/RD (E)	/WR (R,/W)
H	M68 series CPU	E	R, /W
L	i80 series CPU	/RD	/WR

The data bus signal is identified according to the combination of the RS, /RD (E), and /WR (R, /W) signals, as shown in the following table 5–3.

Table 5–3.

Common	M68 series CPU	i80 series CPU		Function
RS	R, /W	/RD	/WR	
H	H	L	H	Read display data and registers
H	L	H	L	Write display data and registers
L	H	L	H	Prohibited
L	L	H	L	Write to control index register

Moreover, when using the parallel interface, it is possible to use the BMD flag (D_7 of the data access control register (R5) to select the length of the data to be transmitted as either 16 bits (BMD = 0) or 8 bits (BMD = 1). This setting is valid for the display data written as DR data to the display memory register (R12).

The relationship between the command input and the data bus length is as follows.

- Commands other than those of the display memory register (R12) are executed in 1-byte units regardless of the value of BMD (bus length setting flag in data access control register (R5)).
- Display memory register (R12) commands are executed in 1-byte units when BMD = 1, and in 1-word units when BMD = 0.

(1) Commands other than those of the display memory register (R12)

BMD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Data	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note 0 or 1

(2) Display memory register (R12)

BMD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Data	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Relationship data bus and display RAM (16-bit parallel interface: BMD = 0)

Data bus side

16 bit															
DB_{15}	DB_{14}	DB_{13}	DB_{12}	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1					Dot 2						Dot 3				
1 pixel (= 1X address)															

Display RAM side

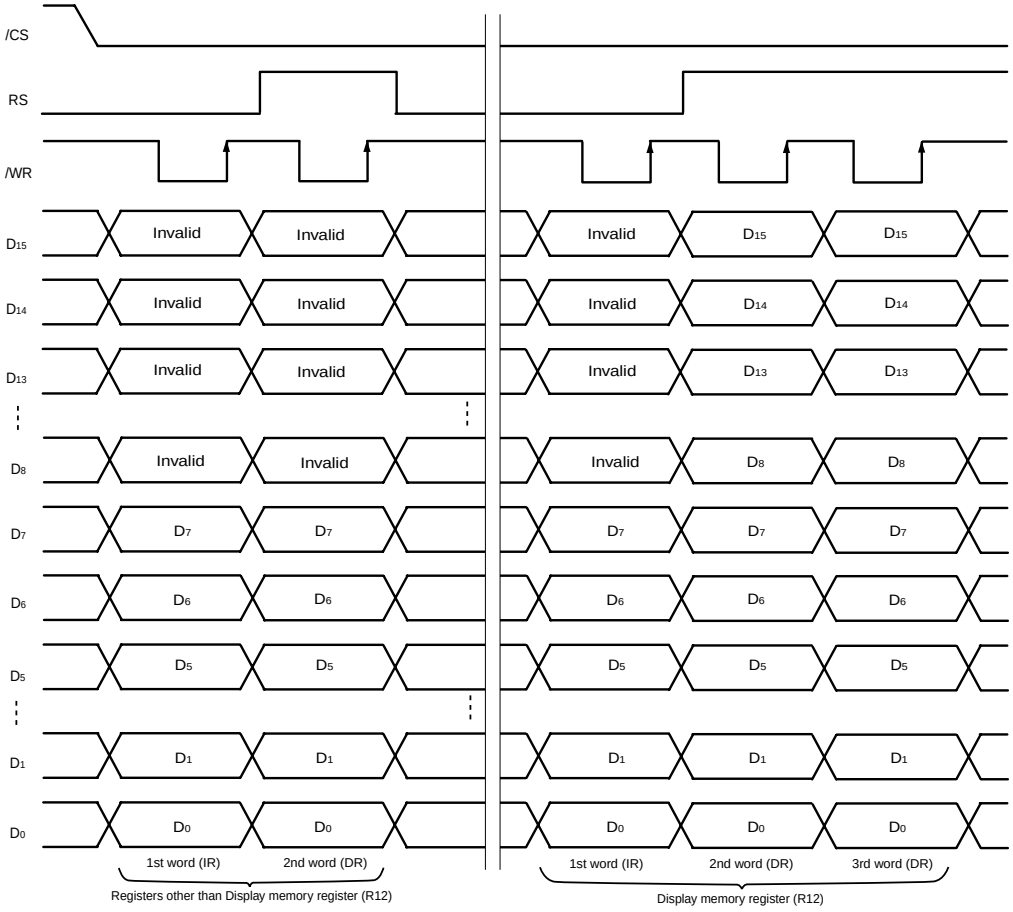
Relationship data bus and display RAM (18-bit parallel interface: BMD = 1)

Data bus side

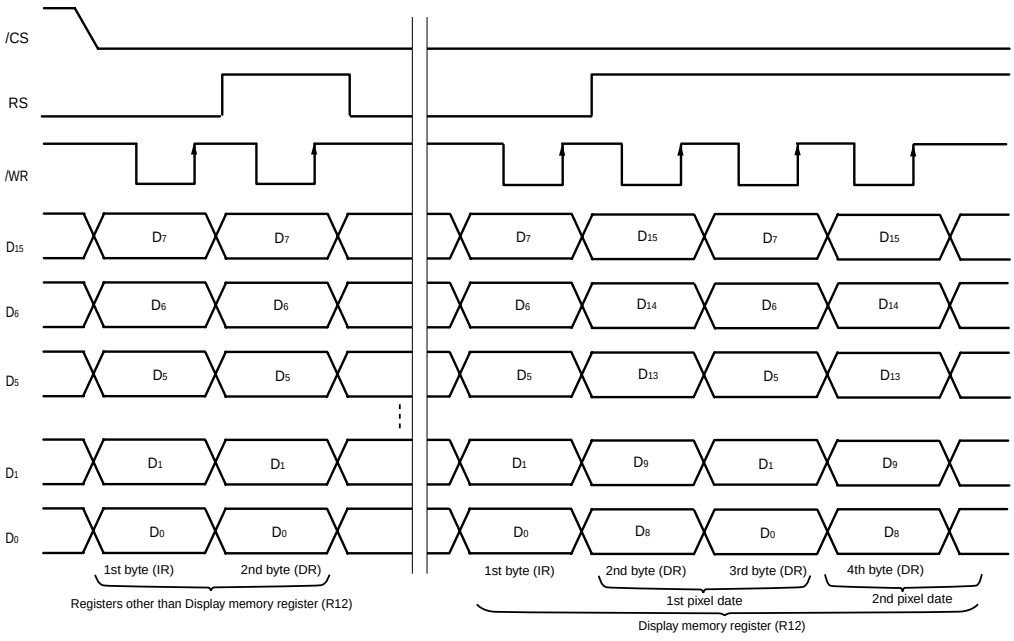
8 bit (1st byte)								8 bit (2nd byte)							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1					Dot 2						Dot 3				
1 pixel (= 1X address)															

Display RAM side

Figure 5–1. Example of 16-bit Data Access (i80 series interface, BMD = 0)



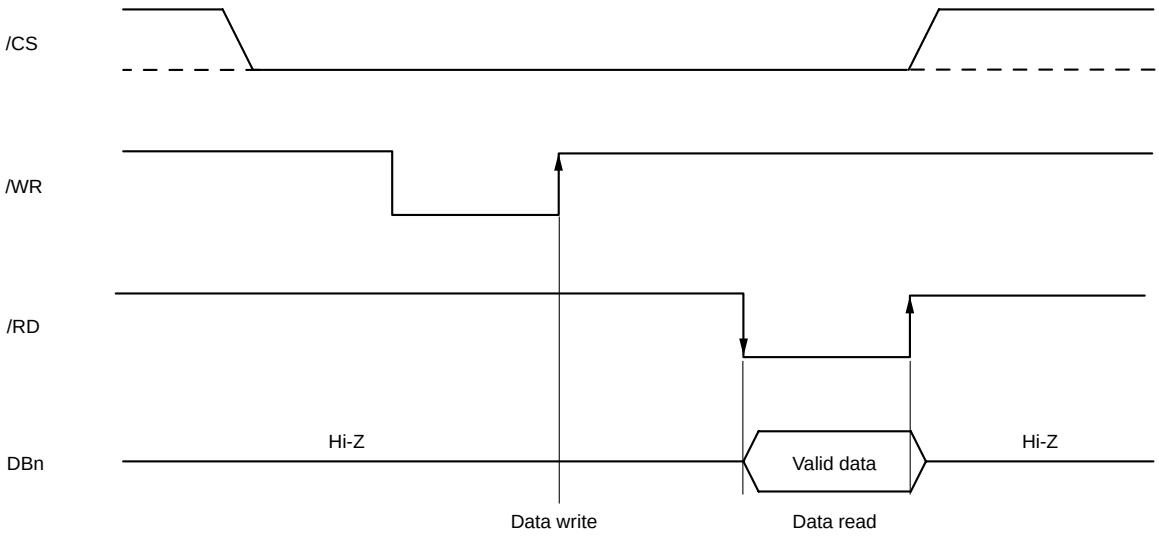
★ **Figure 5–2. Example of 8-bit Data Access (i80 series interface, BMD = 1)**



(1) i80 Series Parallel Interface

When i80 series parallel data transfer has been selected, data is written to the μPD161622 at the rising edge of the /WR signal. The data is output to the data bus when the /RD signal is L.

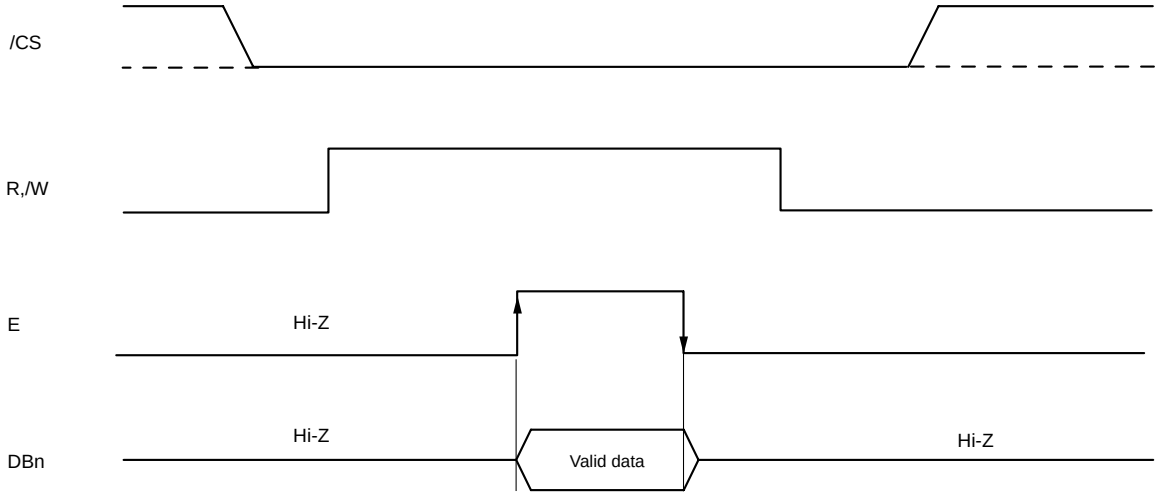
Figure 5–3. i80 Series Interface Data Bus Status



(2) M68 Series Parallel Interface

When M68 series parallel data transfer has been selected, data is written at the falling edge of the E signal when the R,/W signal is L. In a data read operation, data is output at the rising edge of the E signal in a period when the R,/W signal is H. The data bus is released (Hi-Z) at the falling edge of the E signal.

Figure 5–4. M68 Series Interface Data Bus Status (when data read)

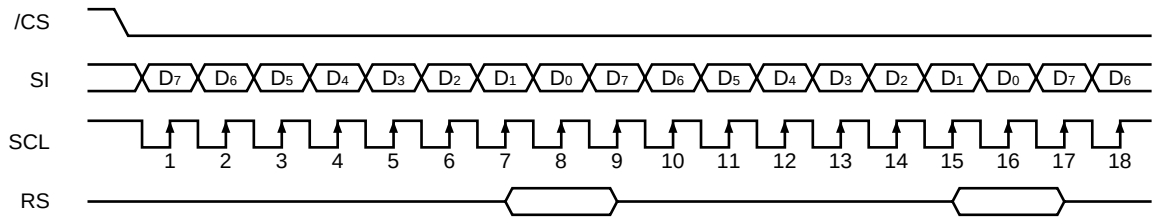


5.1.3 Serial interface

When the serial interface has been selected (PSX = L), if the chip is active (/CS = L), serial data input (SI) and serial clock input (SCL) can be received. Serial data is read from D_7 and then from D_6 to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing.

RS input is used to judge serial input data as display data or command data when RS = H the data is display data and when RS = L the data is command data. When the chip enters active mode, RS input is read at the rising edge after every eighth serial clock and is then used to judge the serial input data. The serial interface signal chart is shown below.

Figure 5–5. Serial Interface Signal Chart



Remarks 1. If the chip is not active, the shift register and counter are reset to their initial settings.

2. The data read function is disabled during serial interface mode.

3. When using SCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. Our recommends checking operation with the actual device.

5.1.4 Chip select

The μPD161622 has two chip select pins (/CS). The CPU parallel and serial interfaces can be used only when /CS = L. When the chip select pin is inactive, D_0 to D_{15} are set to high impedance (invalid) and input of RS, /RD, or /WR is not active. If a serial interface mode has been set, the shift register and counter are both initialized.

5.1.5 Access to display data RAM and internal registers

When the CPU accessed the μPD161622, the CPU only has to satisfy the requirement of the cycle time (t_{CYC}) and can transfer data at high speeds. Usually, it is not necessary for the CPU to take wait time into consideration.

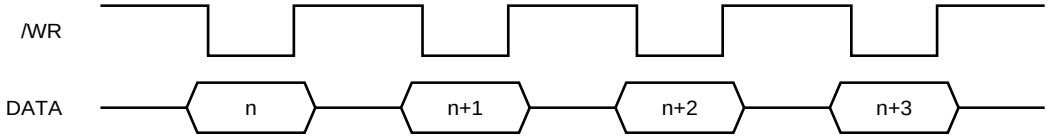
A high-speed RAM write function, as well as the ordinary RAM write function, is provided for writing data to the display data RAM. By using the high-speed write function, data can be written to the display RAM at an access speed four times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported. For details, refer to **5.2.5 High-speed RAM write mode**

Dummy data is not required when either reading or writing data. In the μPD161622, data of the display memory register (R12) cannot be read. This relationship is shown in Figure 5–6.

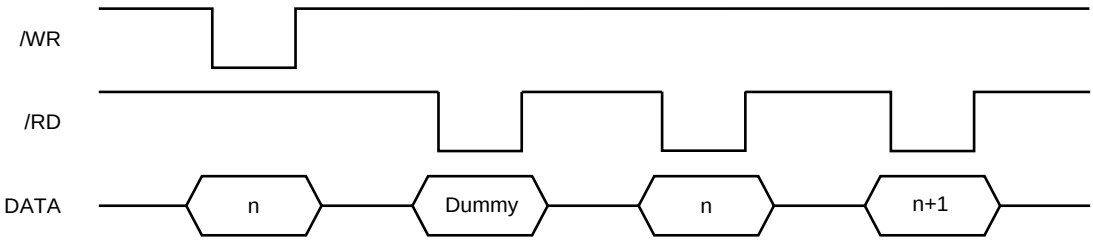
Note that when in write mode of data at high speed for data read mode of read cycle time, this mode equals to normal mode.

Figure 5–6. Image of internal access to display RAM

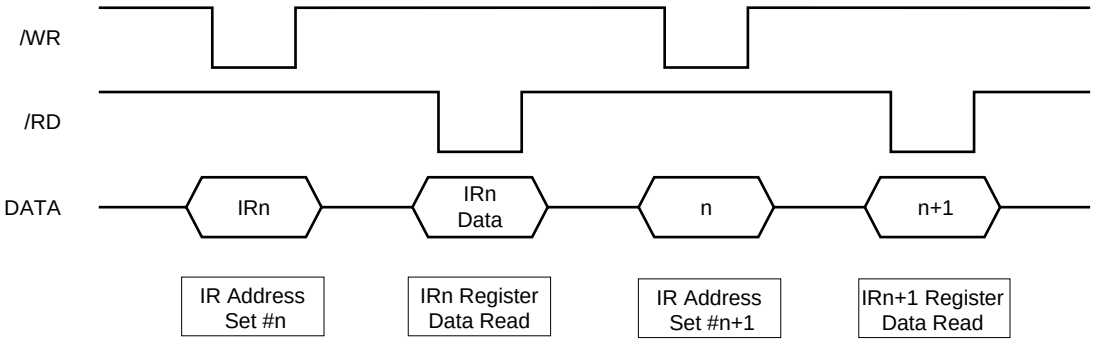
Writing



Reading (display memory register)



Reading (registers other than display memory register)



5.2 Display Data RAM

This RAM stores dot data for display and consists of 2,112 bits (132 x 16) x 176 bits. Any address of this RAM can be accessed by specifying an X address and an Y address.

Display data D_0 to D_{15} transmitted from the CPU corresponds to the pixels on the LCD (refer to Table 5–5).

Table 5–5. Display Data RAM

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Dot 1					Dot 2						Dot 3				
Pixel 1 (= 1 x address)															

5.2.1 X address circuit

An X address of the display data RAM is specified by using the X address register as shown in Figure 5–8. If the X address increment mode (INC = 0: data access control register: R5) is used, the specified X address is incremented or decremented by one each time display data is written. Whether the address is incremented or decremented is specified by the XDIR flag of data access control register (R5) as shown in Table 5–6.

In the increment mode, the X address is incremented up to 83H. If more display data is written, the Y address is incremented (YDIR = 0) or decremented (YDIR = 1), and the X address returns to 00H.

In the decrement mode, the X address is decremented to 00H. If more display data is written, the Y address is incremented (YDIR = 0) or decremented (YDIR = 1), and the X address returns to 83H.

5.2.2 Y address circuit

A Y address of the display data RAM is specified by using the Y address register as shown in Figure 5–8. If the Y address increment mode (INC = 1: data access control register: R5) is used, the specified Y address is incremented or decremented by one each time display is written. Whether the address is incremented or decremented is specified by the YDIR flag of data access control register (R5) as shown in Table 5–6.

In the increment mode, the Y address is incremented up to AFH. If more display data is written, the X address is incremented (XDIR = 0) or decremented (XDIR = 1), and the Y address returns to 00H.

In the decrement mode, the Y address is decremented to 00H. If more display data is written, the X address is incremented (XDIR = 0) or decremented (XDIR = 1), and the Y address returns to AFH.

The relationship between the setting of INC, XDIR, and YDIR of data access control register (R5) and the address is as follows:

Table 5–6. Data Access Control Register (R5) Setting

INC	Setting
0	The address is successively incremented or decremented in the X direction when data is accessed.
1	The address is successively incremented or decremented in the Y direction when data is accessed.

XDIR	Setting
0	Increments the X address (+1) when data is accessed.
1	Decrements the X address (–1) when data is accessed.

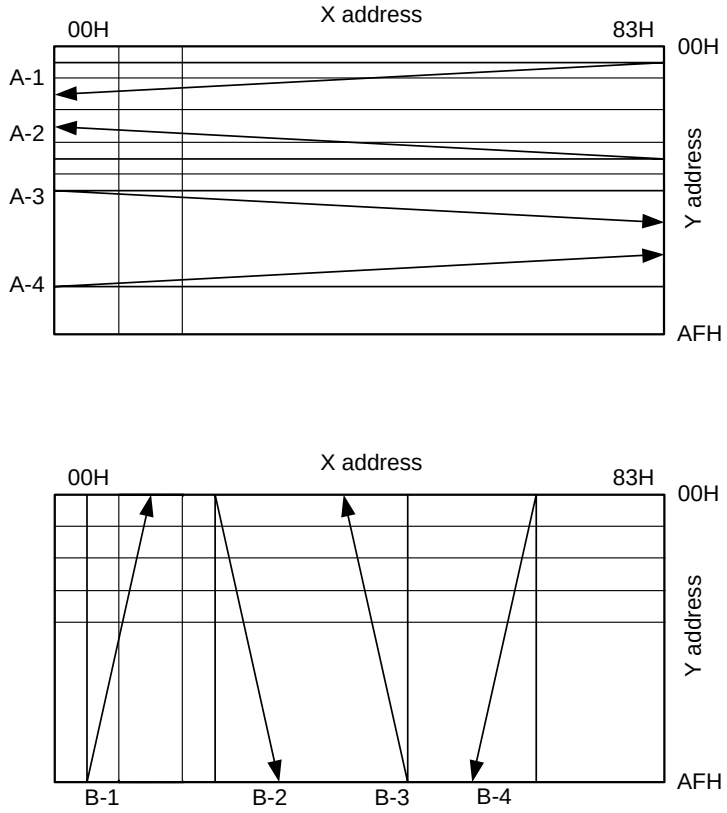
YDIR	Setting
0	Increments the Y address (+1) when data is accessed.
1	Decrements the Y address (–1) when data is accessed.

Table 5–7. Combination of INC, XDIR, and YDIR, and Address Direction

INC	XDIR	YDIR	Image of Address Scanning
0	0	0	A-1
	0	1	A-2
	1	0	A-3
	1	1	A-4
1	0	0	B-1
	0	1	B-2
	1	0	B-3
	1	1	B-4

Caution If the access direction is changed by using INC, XDIR, or YDIR, be sure to set the X address register (R6) and Y address register (R7) before accessing the display RAM.

Figure 5–7. Combination of INC, XDIR, and YDIR, and Address Scanning Image



5.2.3 Column address circuit

When the contents of the display data RAM are displayed, column addresses are output to the SEG output pins as shown in Figure 5–8.

The correspondence relationship between the column addresses of the display RAM and segment outputs can be reversed by the ADC flag (segment driver direction select flag) of control register 1 (R0) as shown in Table 5–8. This reduces the restrictions on chip layout when the LCD module is assembled.

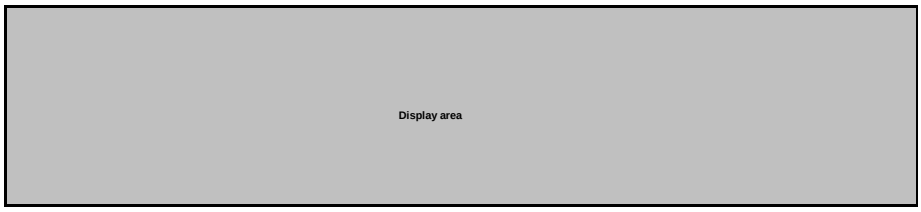
Table 5–8. Relationship between Column Address of Display RAM and Segment Output

SEG Output		SEG_1	SEG_2	→			SEG_{385}	SEG_{386}
ADC	0	000H	000H	→	Column address	→	18AH	18BH
	1	18BH	18AH	←	Column address	←	001H	000H

Figure 5–8. μPD161622 RAM Addressing

Source output														
	ADC=0	S1	S2	S3	S4	S5	Y6	---	---	S391	S392	S393	S394	S395	S396
	ADC=1	S396	S395	S394	S393	S392	S391	---	---	S6	S5	S4	S3	S2	S1
	X-address	000H			001H			---	---	08EH			08FH		
	Column addres	000H	001H	002H	003H	004H	005H	---	---	186H	187H	188H	189H	18AH	18BH
		D15---D11	D10---D5	D4---D0	D15---D11	D10---D5	D4---D0			D15---D11	D10---D5	D4---D0	D15---D11	D10---D5	D4---D0

Gate output		Y-address
R,/L=H	R,/L=L	
O1	O176	00H
O2	O175	01H
|	|	|
|	|	|
O87	O90	56H
O88	O89	57H
O89	O88	58H
O90	O87	59H
|	|	|
|	|	|
O175	O2	AEH
O176	O1	AFH



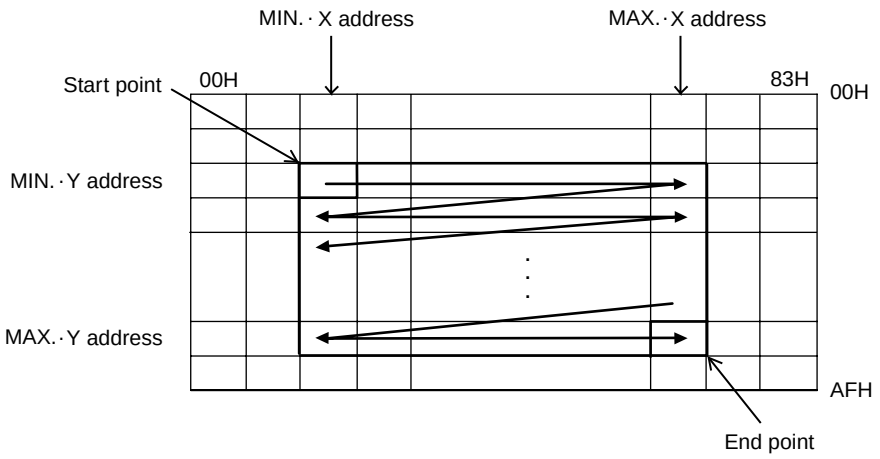
5.2.4 Arbitrary address area access (window access mode (WAS))

With the μPD161622, any area of the display RAM selected by the MIN.··X/Y address registers (R8 and R10) and MAX.· X/Y address registers (R9 and R11) can be accessed.

First, select the area to be accessed by using the MIN.·X/Y address registers and MAX.·X/Y address registers. When WAS of control register 1 is set to 1, the window access mode is then selected. The address scanning setting by INC, XDIR, and YDIR of data access control register (R5) is also valid in this mode, in the same manner as when data is normally written to the display RAM. In addition, data can be written from any address by specifying the X address register (R6) and Y address register (R7).

Note that the display RAM must be accessed after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register or MAX.· X/Y address register.

Figure 5–9. Example of Incrementing Address When INC = 0, XDIR = 0, and YDIR = 0



Cautions 1. When using the window access mode, the relationship between the start point and end point shown in the table below must be established.

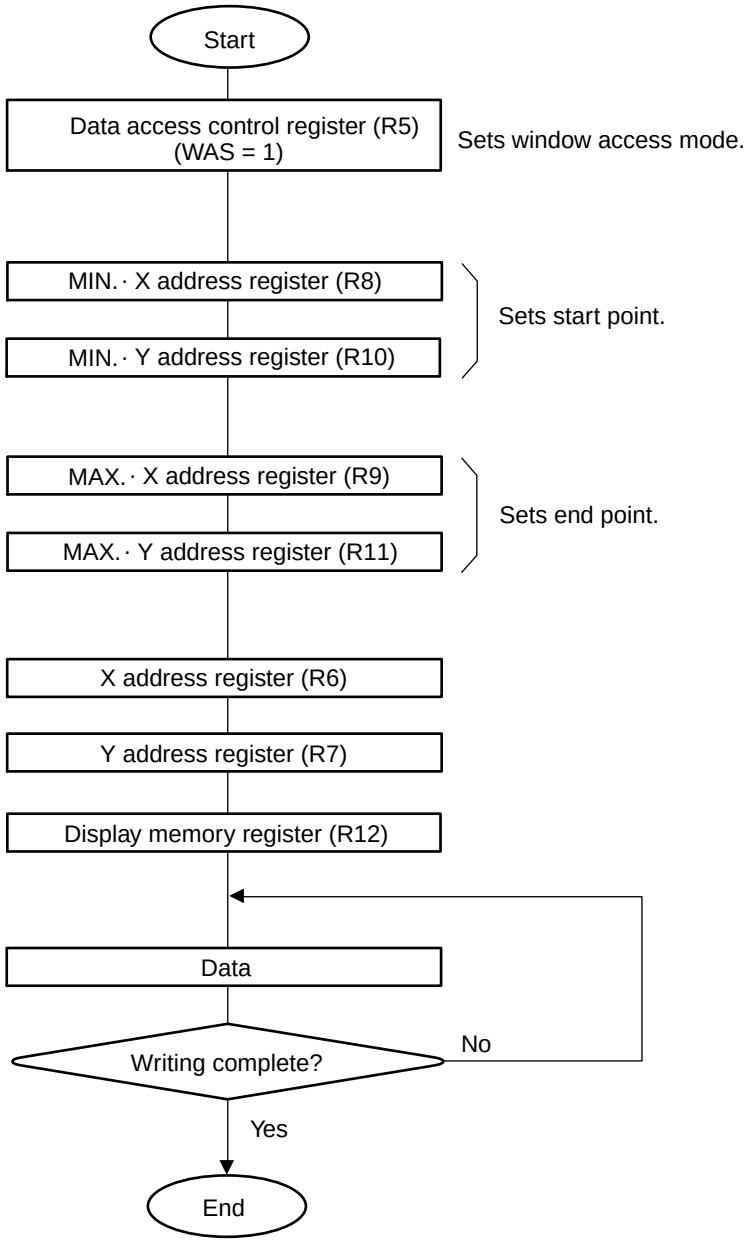
Item	Address Relation Ship
X address	00H ≤ MIN.·X address ≤ X address (R4) MAX.·X address ≤ 83H
Y address	00H ≤ MIN.·Y address ≤ Y address (R5) MAX.·Y address ≤ AFH

2. If invalid address data is set as the MIN./MAX.·address, operation is not guaranteed.

3. Do not specify any value other than the address value 4n–n (n = 1 to 33) for the X address in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

4. Access the display RAM after setting the X address register (R6) and Y address register (R7) if the window access area has been set or changed by the MIN.· X/Y address register or MAX.· X/Y address register.

Figure 5–10. Example of Sequence in Window Access Mode



5.2.5 High-speed RAM write mode

With the μPD161622, two types of access modes can be selected for accessing the display RAM.

The μPD161622 has a high-speed RAM write function, as well as an ordinary RAM write function. By using the high-speed write function, data can be written to the display RAM at an access speed four times faster than that of the ordinary RAM write function. Therefore, applications, such as motion picture display where the display data must be rewritten at high speeds, can be supported.

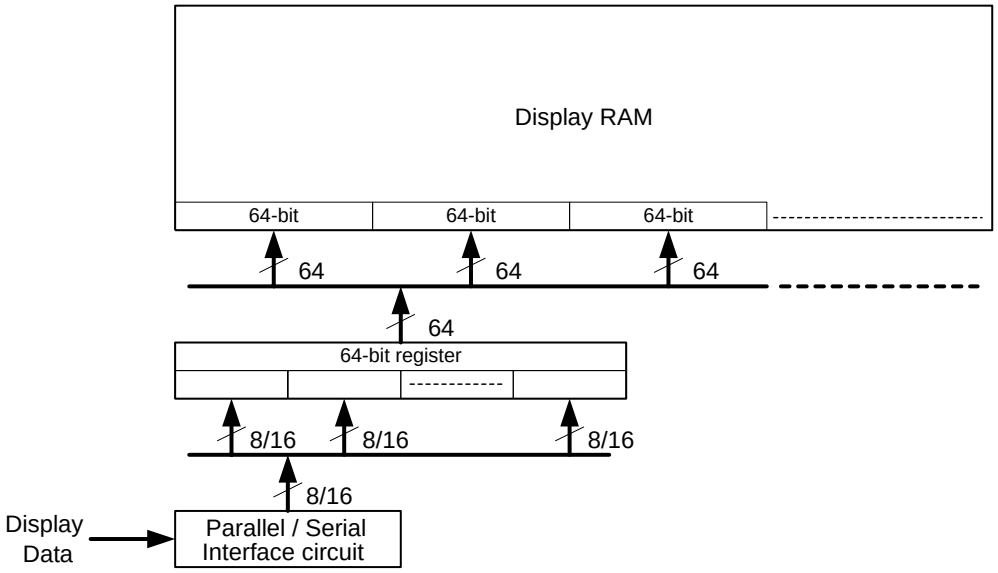
When the high-speed RAM write mode is selected by using BSTR of the data access control register (R5), data is temporarily stored in an internal register of the μPD161622.

When data of 64 bits (16 bits x 4) has been stored in the register, it is written to the display RAM. It is also possible to write the next data to the internal register while the first data is being written to the RAM.

In the high-speed RAM write mode, however, the CPU must transmit data in units of 64 bits (4 pixels) have been written to the internal register. If data of less than 64 bits is transmitted in the high-speed RAM write mode, this data is not written to the display RAM. Therefore, CPU data is not reflected on the LCD display even if it is transmitted. In this case, the data that is not reflected remains stored in the register. When the next data is transmitted, it is written to the register from where the preceding data is stored. However, if the chip select signal is disserted inactive (/CS = H) in the middle of data transfer, and then asserted active again and when the display data register (R12) is set, the register is initialized. Consequently, the data stored in the register is lost.

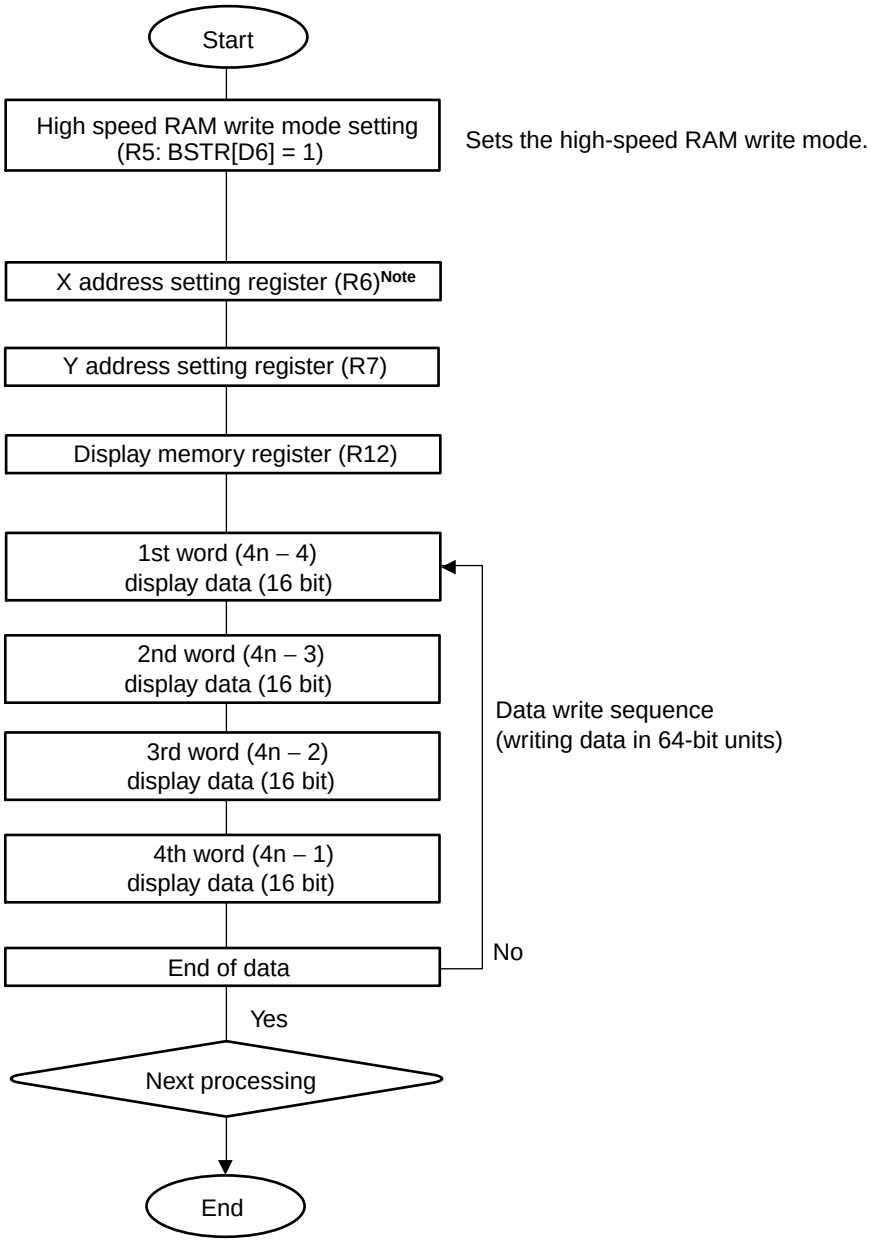
It is therefore recommended to transmit display data in 64-bit units when using the high-speed RAM write mode.

Figure 5–11. Image of Operation in High-speed Write Mode



Caution Do not specify any value other than the address value 4n–n (n = 1 to 33) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

Figure 5–12. Example of Sequence in High-Speed RAM Write Mode (with 16-Bit Parallel Interface)



n: n ≥ 1

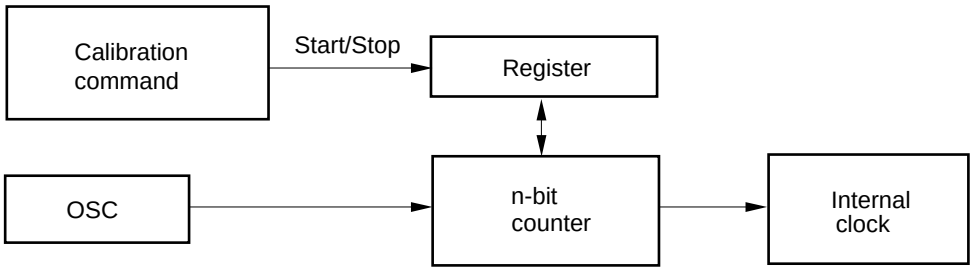
★ **Note** Do not specify any value other than the address value 4n–n (n = 1 to 33) for the X address (R6) in the high-speed RAM access mode. The operation is not guaranteed if invalid address data is set.

5.3 Oscillator

The μPD161622 has a CR oscillator (with external R), which generate the display clock. When R_{SEL} is L, an internal CR oscillator is selected. Leave both OSC_{IN} pin and OSC_{OUT} open. When R_{SEL} is H, an external oscillator is selected. Connect T.B.D. Ω resistance between OSC_{IN} and OCS_{OUT} pin.

This oscillator also has a calibration function, which is available by itself to set the number of frame frequency of display driving. Frame frequency calibration is set by calibration register (R45). The time to select one line is set by the calibration start and stop commands.

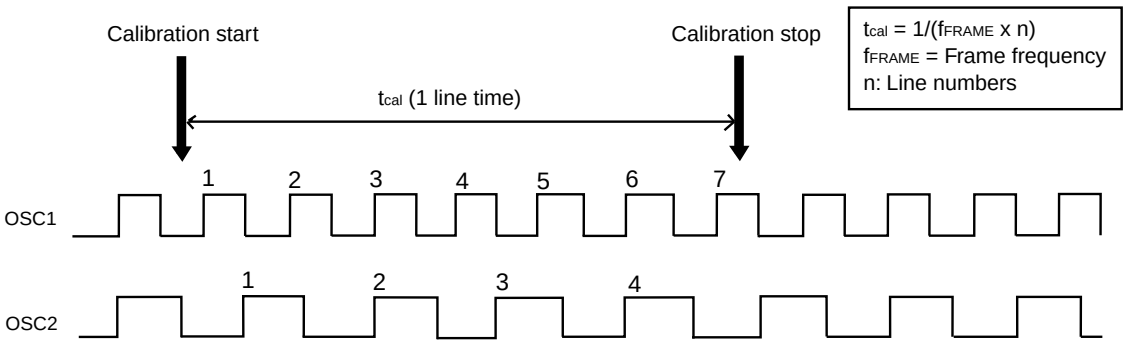
Figure 5–13. Frame Frequency Calibration



The calibration function involves counting the number of oscillation clocks generated between the start and stop signals and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

Using the time to set calibration (t_{cal}) can be selected either t_{cal} or t_{cal} x 2 through control register (R1): LTS.

Figure 5–14. Calibration Function Timing (LTS [R1] = 0)



5.4 Display Timing Generator

5.4.1 Drive timing

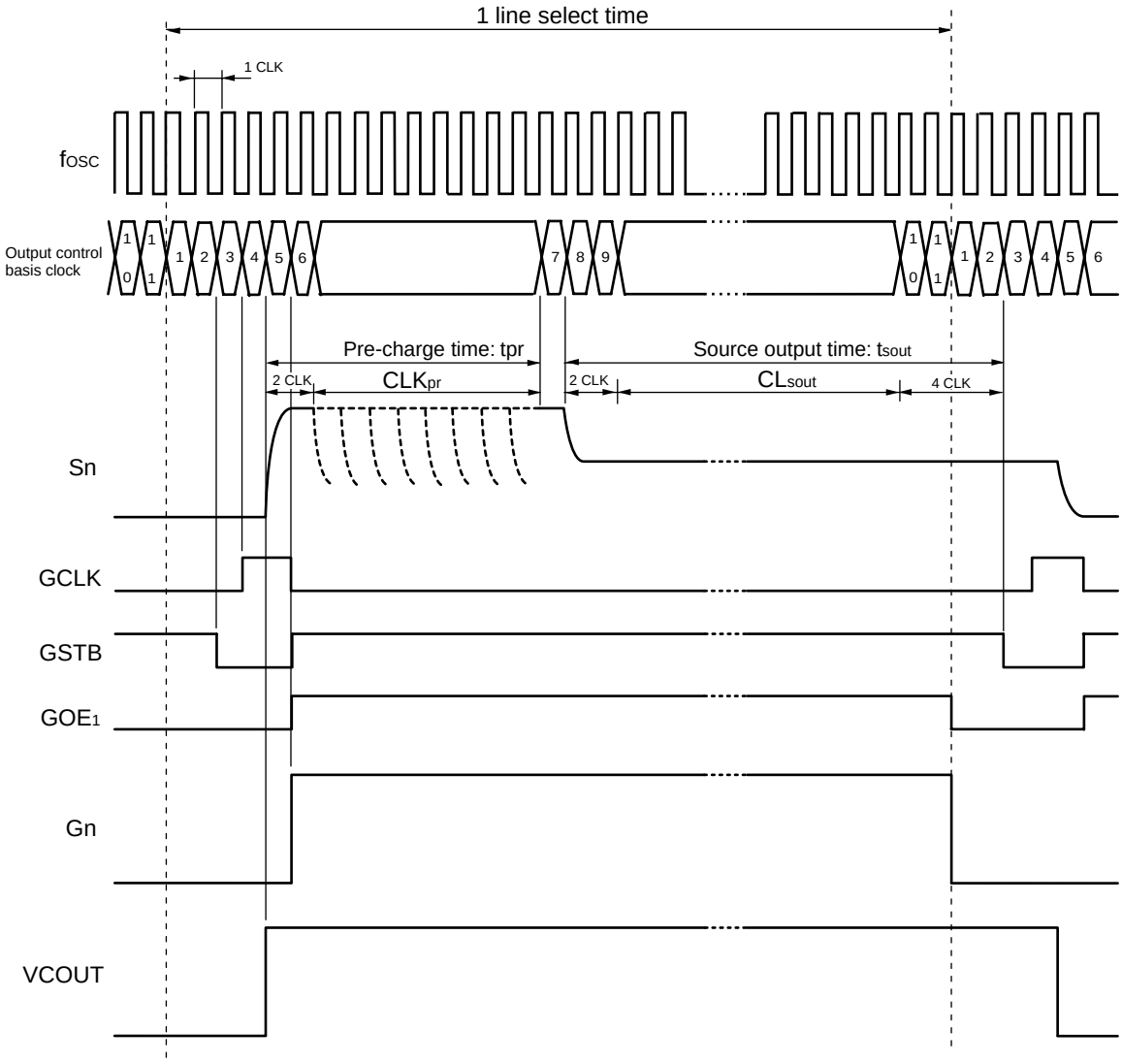
The μPD161622 generates the TFT-LCD drive timing inside the μPD161622. The TFT-LCD panel is driven at the timing of one line selection period generated based on the calibration time (t_{cal}) set by the calibration function, as shown in the figure below. One line selection period is made up of a pre-charge period, a source output period, and the μPD161622 output control clock. The pre-charge and source output periods are set by the pre-charge period setting register (R46) and calibration register (R45), respectively, based on the following expressions.

1 line selection period = t_{cal}
Pre-charge period = t_{pr}
Source output period = t_{sout}

t_{cal}: Calibration setting time [R45]
$t_{pr} = (1/f_{OSC}) \times (CLK_{pr} + 2\ CLK)$
$t_{sout} = t_{cal} - (t_{pr} + 3\ CLK)$

CLK_{cal}: Calibration setting time (t_{cal}) clock number = $t_{cal} \div (1f_{OSC})$
CLKpr: Pre-charge peiod setting register clock number [R46: PLIMn] n
1 CLK = $1/f_{OSC}$
f_{OSC}: Oscillator frequency

Figure 5–15. 1-line Select Time



The display timing generator generates the timing signals for the internal timing of the source driver and for the gate driver. The output timings for normal operation, for normal operation → stand-by mode, and for stand-by mode → normal operation, are shown below.

Figure 5–16. During Normal Operation (during line inversion)

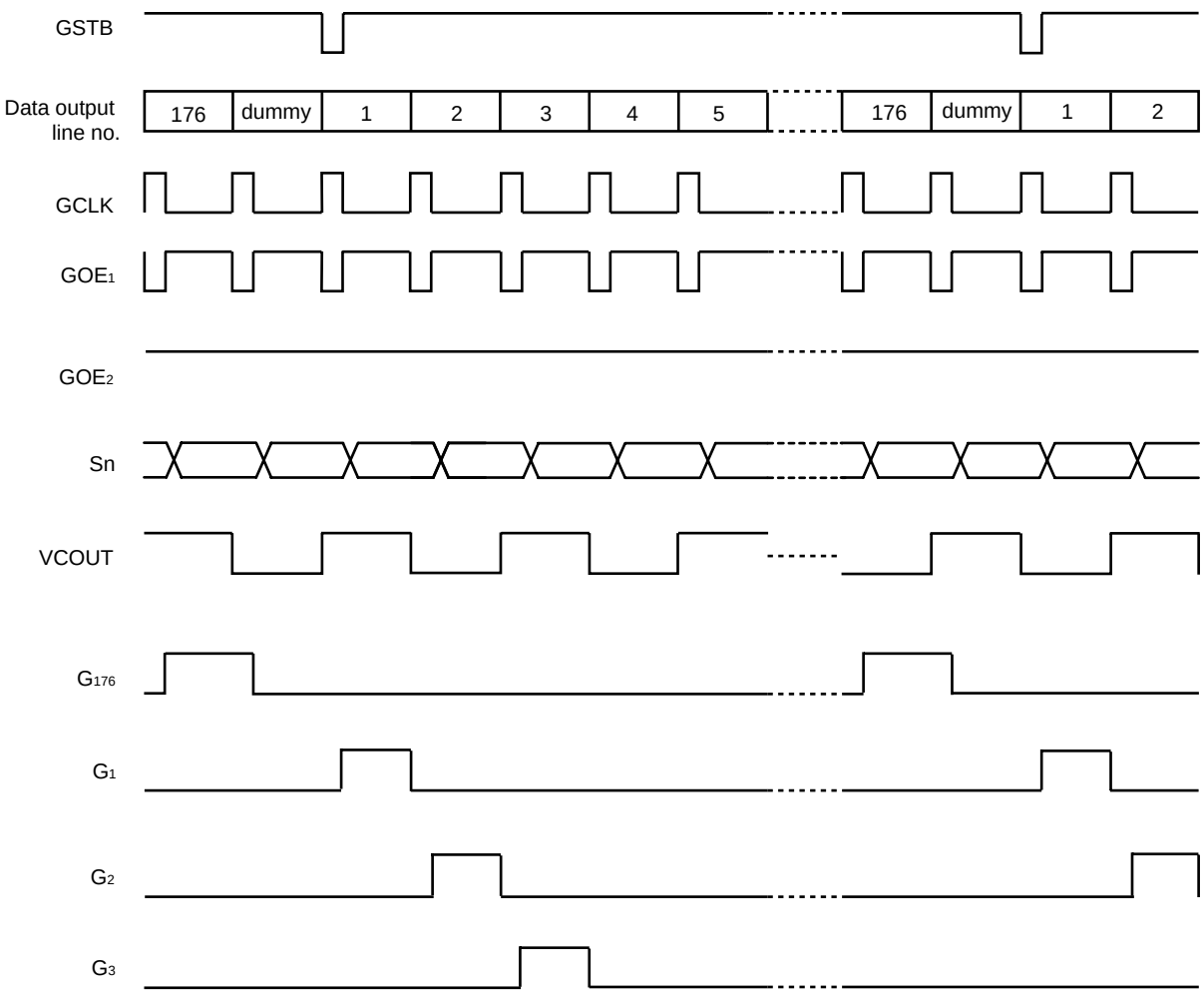


Figure 5–17. Normal Operation → Stand-by Input (during line inversion)

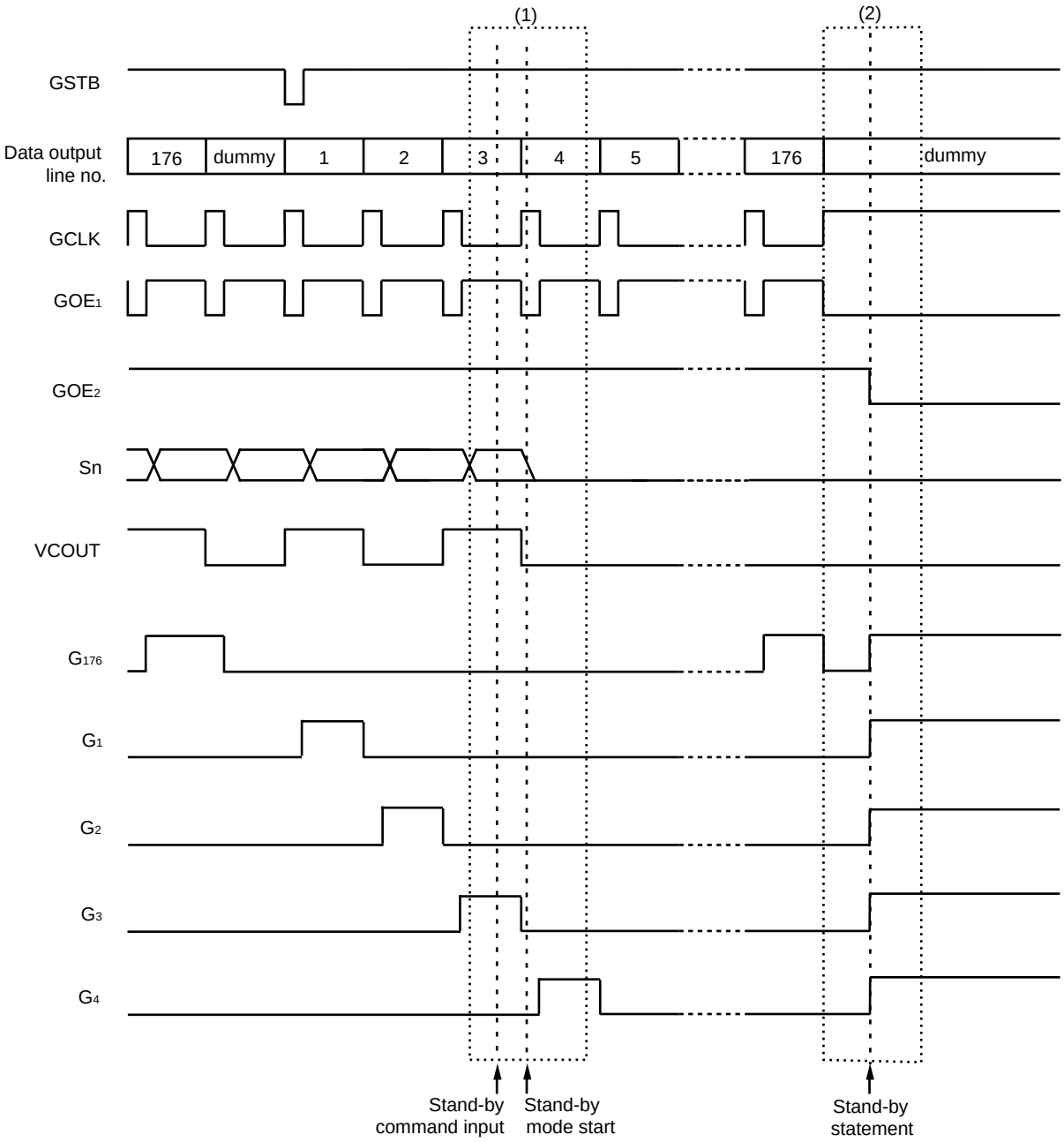


Figure 5–18. Normal Operation → Stand-by Input (during line inversion) (1) Reference

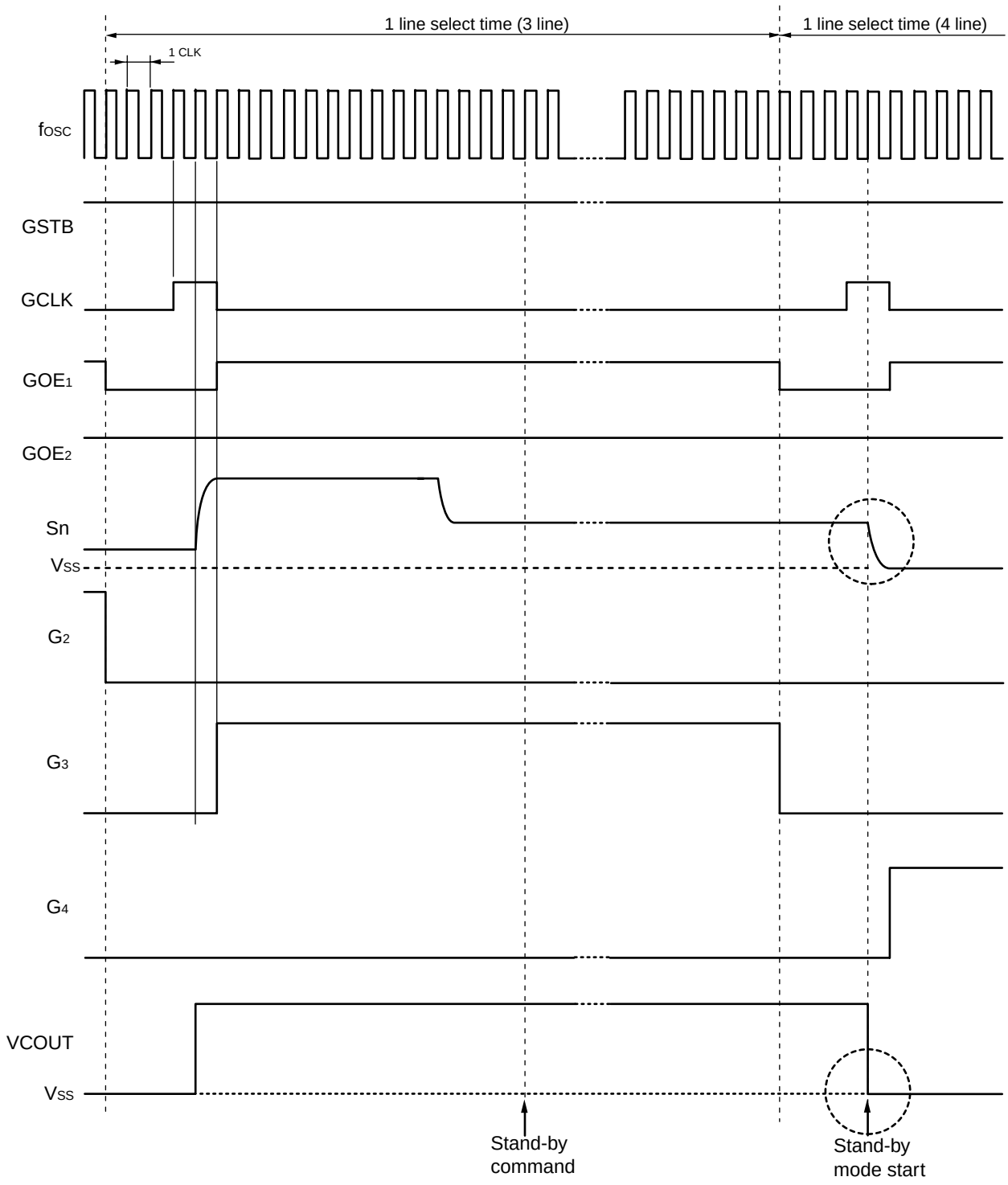


Figure 5–19. Normal Operation → Stand-by Input (during line inversion) (2) Reference

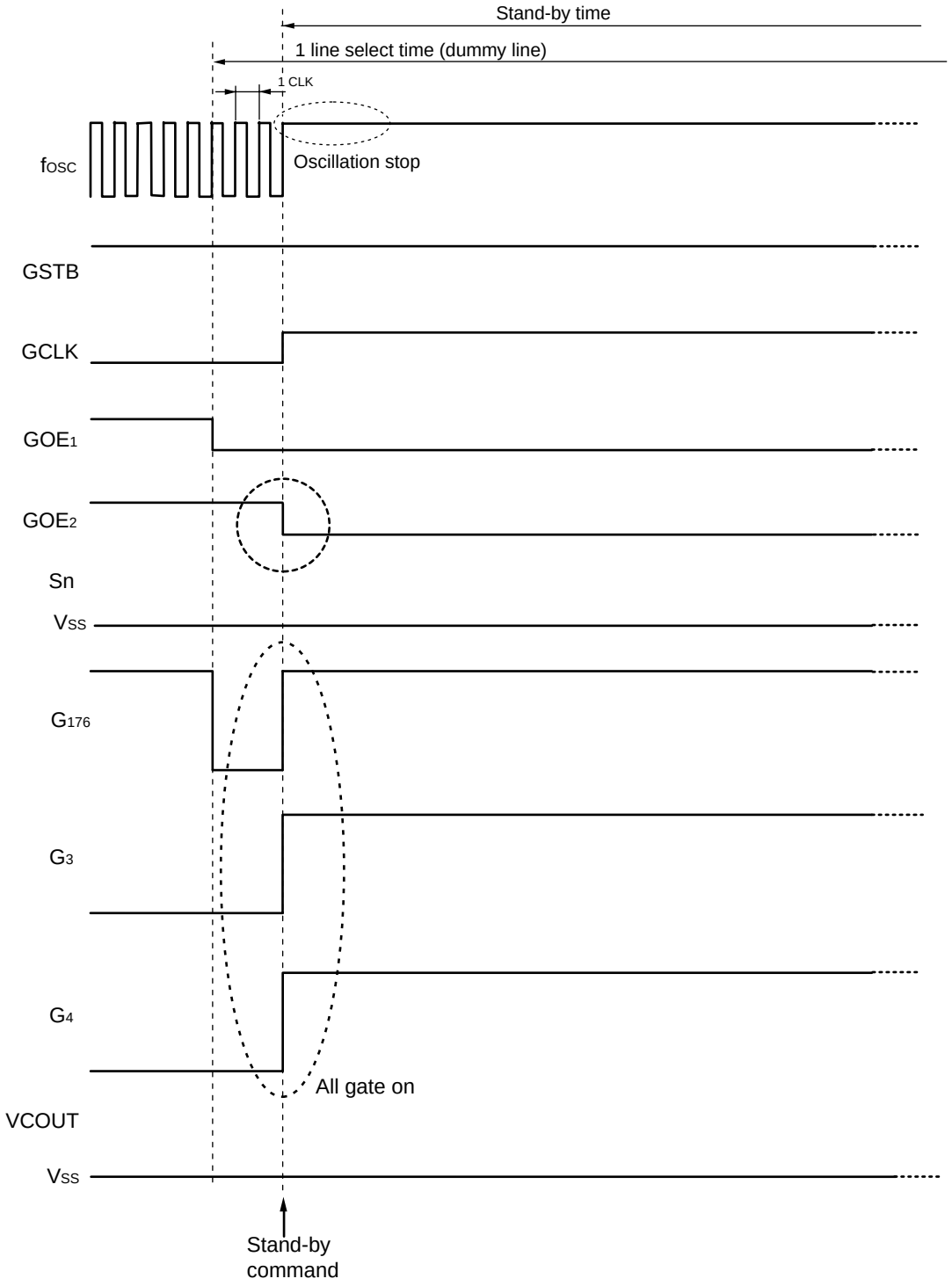
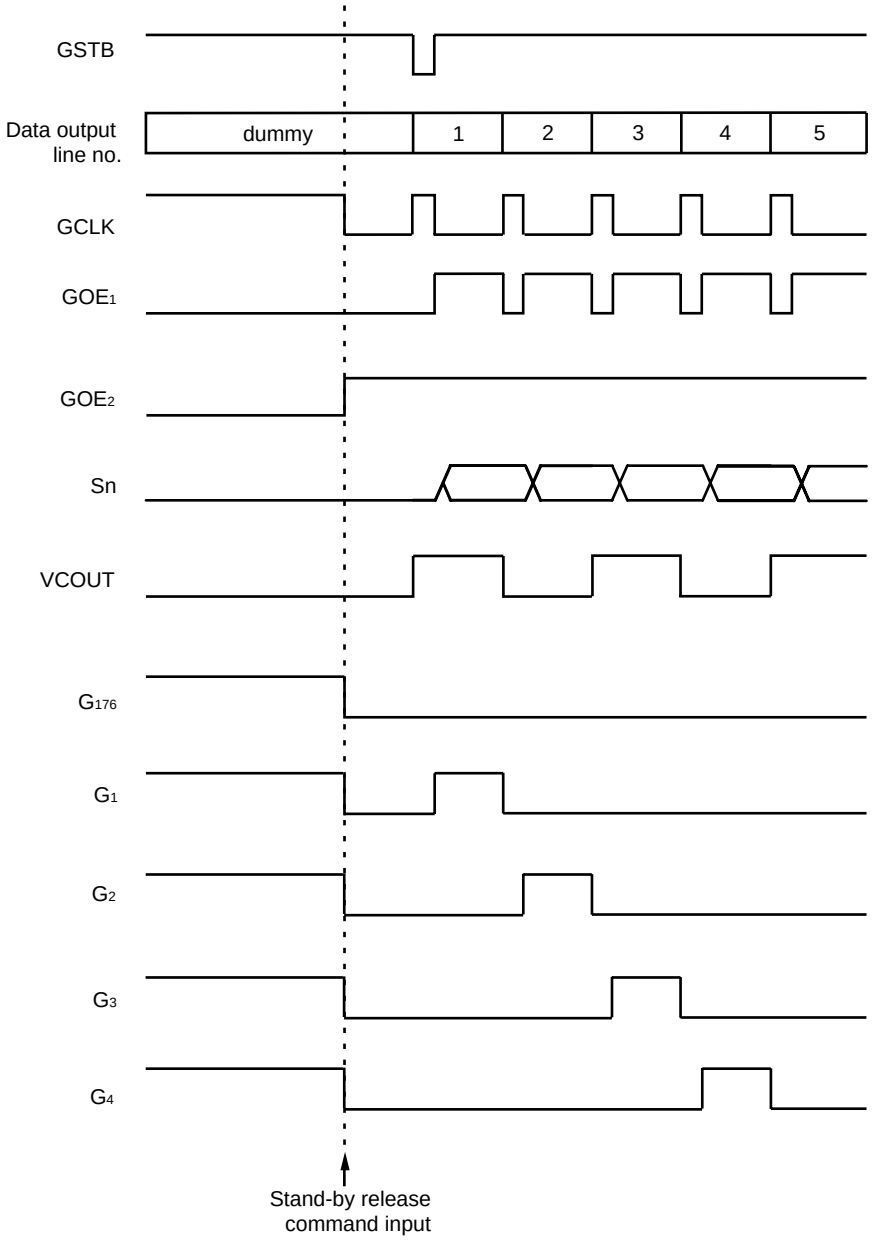


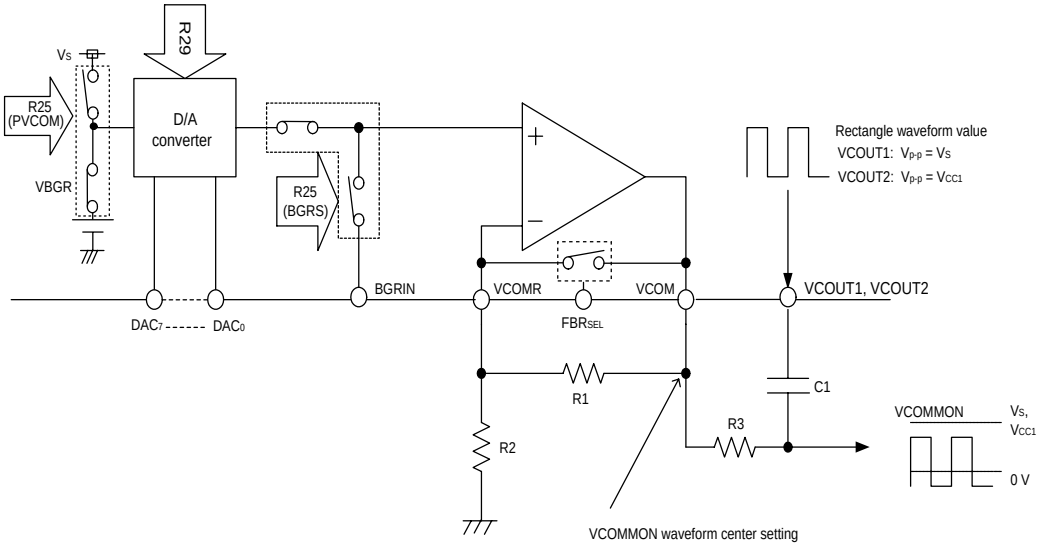
Figure 5–20. Stand-by → Return to Normal Operation (during line inversion)



5.5 Common Adjustment Circuit

To generate common output, the center voltage of the common waveform is output from the VCOM pin along with output of a 0 to V_S (V) square waveform from the VCOUT1 pin and 0 to V_{CC1} (V) from VCOUT2. The level of the VCOM output can be adjusted using as external resistor.

Figure 5–21. Common Adjustment Circuit



The VCOM voltage formulas are shown below.

<When internal power supply is used 2 (BGRS [D_6] of R25 = 0, PVCOM (D_3) = 0)>

COM voltage = (1+R1/R2) x VBGR x (α ÷ 256)

VBGR = 3.0 V TYP.

α = VCOM electronic volume register [R29]

<When internal power supply is used 2 (BGRS [D_6] of R25 = 0, PVCOM (D_3) = 1)>

COM voltage = (1+R1/R2) x V_S x (α ÷ 256)

α = VCOM electronic volume register [R29]

<When external power supply is used (BGRS [D_6] of R25 = 1)>

COM voltage = (1+R1/R2) x VBGRIN

VBGRIN = external power supply voltage (voltage input from BGRIN)

★ <Recommended values for R1 to R3, and C1>

Use the values listed below as a guideline. The user is responsible for ultimately determining the resistance values and recommended values based on careful evaluation on actual panels.

R1: 200 K

R2: 51 to 100 K

R3: 51 to 100 K

C1: 10 μF

5.6 Rectangular Signal Generator

This circuit generates a common rectangular signal. A rectangular wave of 0 to V_S (V) is output from the VCOUT1 pin, and a wave of 0 to V_{CC1} (V) is output from the VCOUT2 pin. The common output wave necessary for driving an LCD can be generated by connecting an external circuit as shown in Figure 5–21.

5.7 Reference Voltage Generator (VBGR)

The μPD161622 has a reference voltage generator for the voltage regulator. This reference voltage generator generates a constant voltage from V_{CC1}. The constant voltage generated by this circuit is connected to the input of the operational amplifier that adjusts the center level of the COMMON drive output, via a D/A converter.

By using this voltage, therefore, the center level of the COMMON drive output can be kept constant, without being affected by fluctuations in the supply voltage.

The common output waveform necessary for driving an LCD can be generated by connecting the external circuit show in Figure 5–21.

When the internal reference voltage generator is not used (R25: BGRS = 1), directly input the reference voltage to the operational amplifier that adjusts the center level of the COMMON drive output.

5.8 D/A Converter Circuit

The μPD161622 is provided with an internal D/A converter to adjust the voltage of the reference voltage generator for the voltage regulator. This D/A converter divides the constant voltage generated by the reference voltage generator (VBFR) by 256, and a level of voltage between VBGR and V_{SS} can be selected by setting the VCOM electronic volume register (R29).

In addition, this D/A converter also has a function to select a level by using an external pin. If the set value of the VCOM electronic volume register (R29) is 00H, the set statuses of the DAC_7 to DAC_0 pins are valid.

When DACn pin input is valid (R29 = 00H), these pins are pulled up internally , so only the pins that are to be set to L should be connected to V_{SS}.

Table 5–9. α Setting of VCOM Electronic Volume Register (R25: BGRS = 0)

	EV_7	EV_6	EV_5	EV_4	EV_3	EV_2	EV_1	EV_0	α	Remark
	DAC_7	DAC_6	DAC_5	DAC_4	DAC_3	DAC_2	DAC_1	DAC_0		
00H	0	0	0	0	0	0	0	0	DACn set value	R29
									0	DACn
01H	0	0	0	0	0	0	0	1	2	
02H	0	0	0	0	0	0	1	0	3	
03H	0	0	0	0	0	0	1	1	4	
↓				↓					↓	
FEH	1	1	1	1	1	1	1	0	255	
FFH	1	1	1	1	1	1	1	1	256	

5.9 γ-Curve Correction Power Supply Circuit

The μPD161622 includes a γ-curve correction power supply circuit. If the internal γ-curve correction matches the LCD characteristics, no external components are necessary. This power circuit has white level and black level reference voltage generators on the positive and negative polarity sides, and also supports unbalanced driving. The reference voltage generators consist of a D/A converter and an operational amplifier and divide V_S to V_{SS} by 256. One level of voltage can be selected by using the contrast value setting registers (R36 to R39)

★ **Figure 5–22. γ-Curve Correction Circuit**

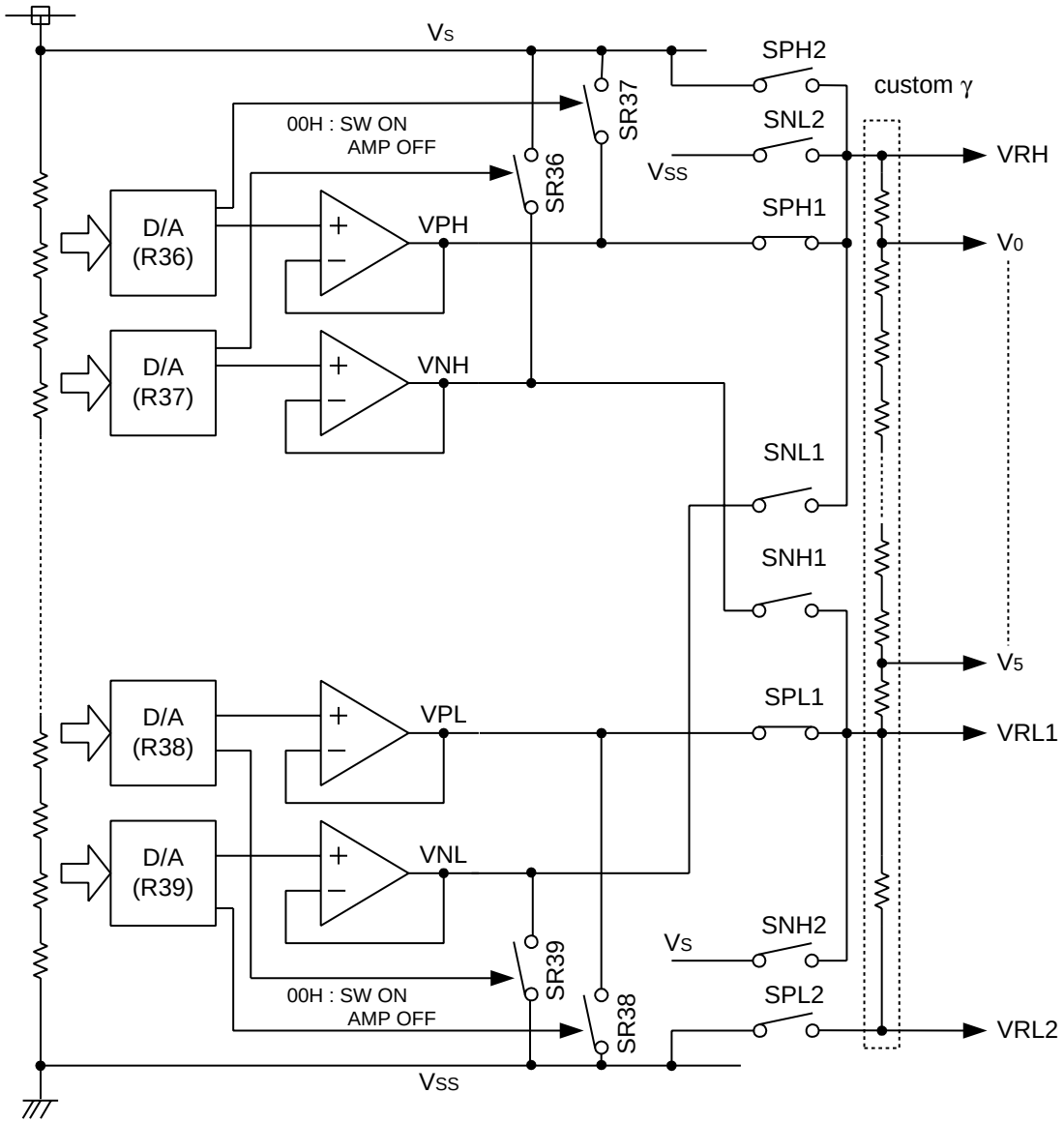
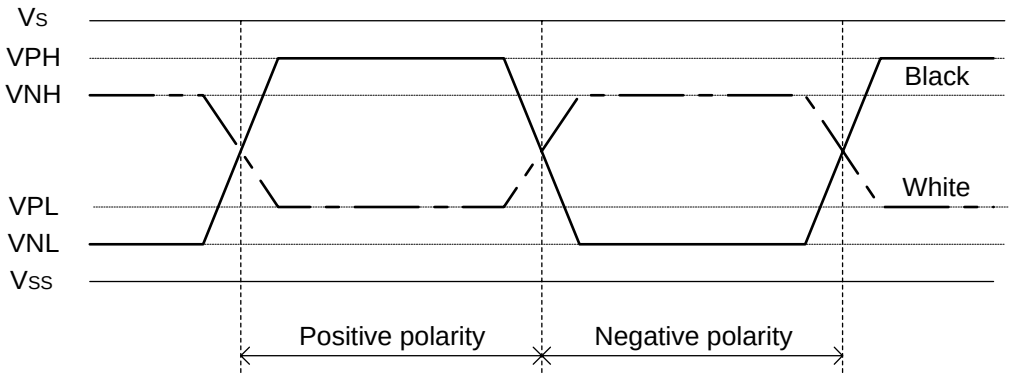


Figure 5–23. Relationship of TFT Drive Voltage (normally white)



	Drive level	Setting register	
VPH	Positive polarity, black	Contrast value setting register 1	R36
VNH	Negative polarity, white	Contrast value setting register 2	R37
VPL	Positive polarity, black	Contrast value setting register 3	R38
VNL	Negative polarity, white	Contrast value setting register 4	R39

The value of each amplifier output can be expressed as follows and the value of β can be set as shown in Table 5–10 and 5–11by using the contrast value registers (R36 to R39)

VNL, BVPL, VNH, VPH = (β ÷ 256) x Vs

Caution The usable range in which each output level of VPH, VNH, VPL, and VNL can be set depends on the γ-curve.

Table 5–10. γ-Contrast Value Setting and Electronic Volume Register β Setting 1 (VPH, VNL)

R36 R37	GPH7 GNH7	GPH6 GNH6	GPH5 GNH5	GPH4 GNH4	GPH3 GNH3	GPH2 GNH2	GPH1 GNH1	GPH0 GNH0	β value setting or status setting
00H	0	0	0	0	0	0	0	0	Fixed to Vs (amplifier OFF)
01H	0	0	0	0	0	0	0	1	255
02H	0	0	0	0	0	0	1	0	254
03H	0	0	0	0	0	0	1	1	253
↓				↓					↓
FEH	1	1	1	1	1	1	1	0	2
FFH	1	1	1	1	1	1	1	1	1

Table 5–11. γ-Contrast Value Setting and Electronic Volume Register β Setting 1 (VPL, VNL)

R36	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0	β value setting or
R37	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0	Statement setting
00H	0	0	0	0	0	0	0	0	Fixed to V_S (amplifier OFF)
01H	0	0	0	0	0	0	0	1	255
02H	0	0	0	0	0	0	1	0	254
03H	0	0	0	0	0	0	1	1	253
↓				↓					↓
FEH	1	1	1	1	1	1	1	0	2
FFH	1	1	1	1	1	1	1	1	1

★ **Relationship between Setting Value of R36 to R39 Registers and Switch Status (G_{SEL}[R1] = 1)**

Register	Setting value	Switch Status		Amplifier
R36	00H	SR36	ON	OFF
	Other than 00H		OFF	ON
R37	00H	SR37	ON	OFF
	Other than 00H		OFF	ON
R38	00H	SR38	ON	OFF
	Other than 00H		OFF	ON
R39	00H	SR39	ON	OFF
	Other than 00H		OFF	ON

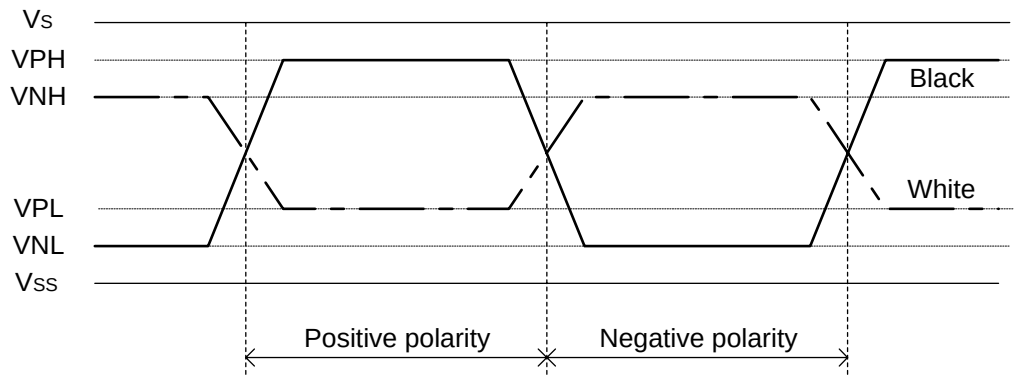
The relationship between the setting of the contrast value setting register and the driven waveform is explained next, taking the γ-curve in Figure 5–22 as an example.

★ **Table 5–12. Switch Status when γ-Curve Correction Power Supply Circuit is not used (G_{SEL}[R1] = 0)**

Polarity	Switch status							
	SPH1	SNL1	SNH1	SPL1	SPH2	SNL2	SNH2	SPL2
Positive	x	x	x	x	ON	OFF	OFF	ON
Negative	x	x	x	x	OFF	ON	ON	OFF

Remark x: Switch is normally OFF with the amplifier OFF.

Relationship of drive voltage (normally white)

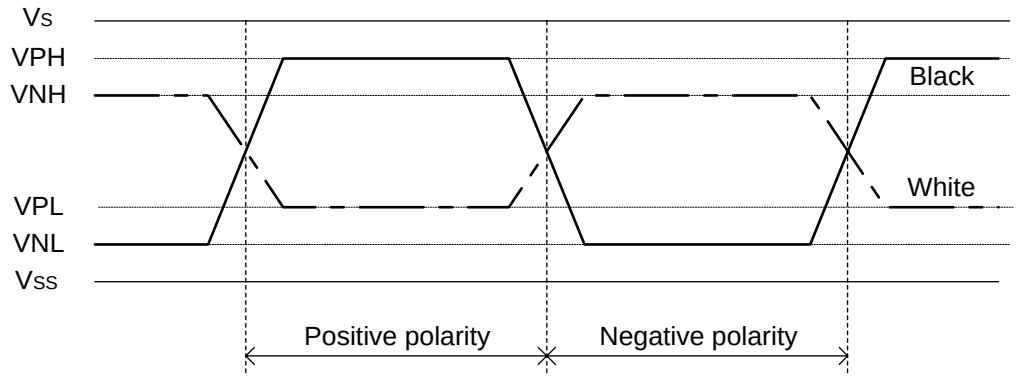


★ **Table 5–13. Switch Status when γ-Curve Correction Power Circuit is used (G_{SEL}[R1] = 1)**

Polarity	Switch status							
	SPH1	SNL1	SNH1	SPL1	SPH2	SNL2	SNH2	SPL2
Positive	ON	OFF	OFF	ON	x	x	x	x
Negative	OFF	ON	ON	OFF	x	x	x	x

Remark x: Switch is normally OFF

Relationship of drive voltage (normally white)



★ **Figure 5–24. TFT Drive Voltage Level**

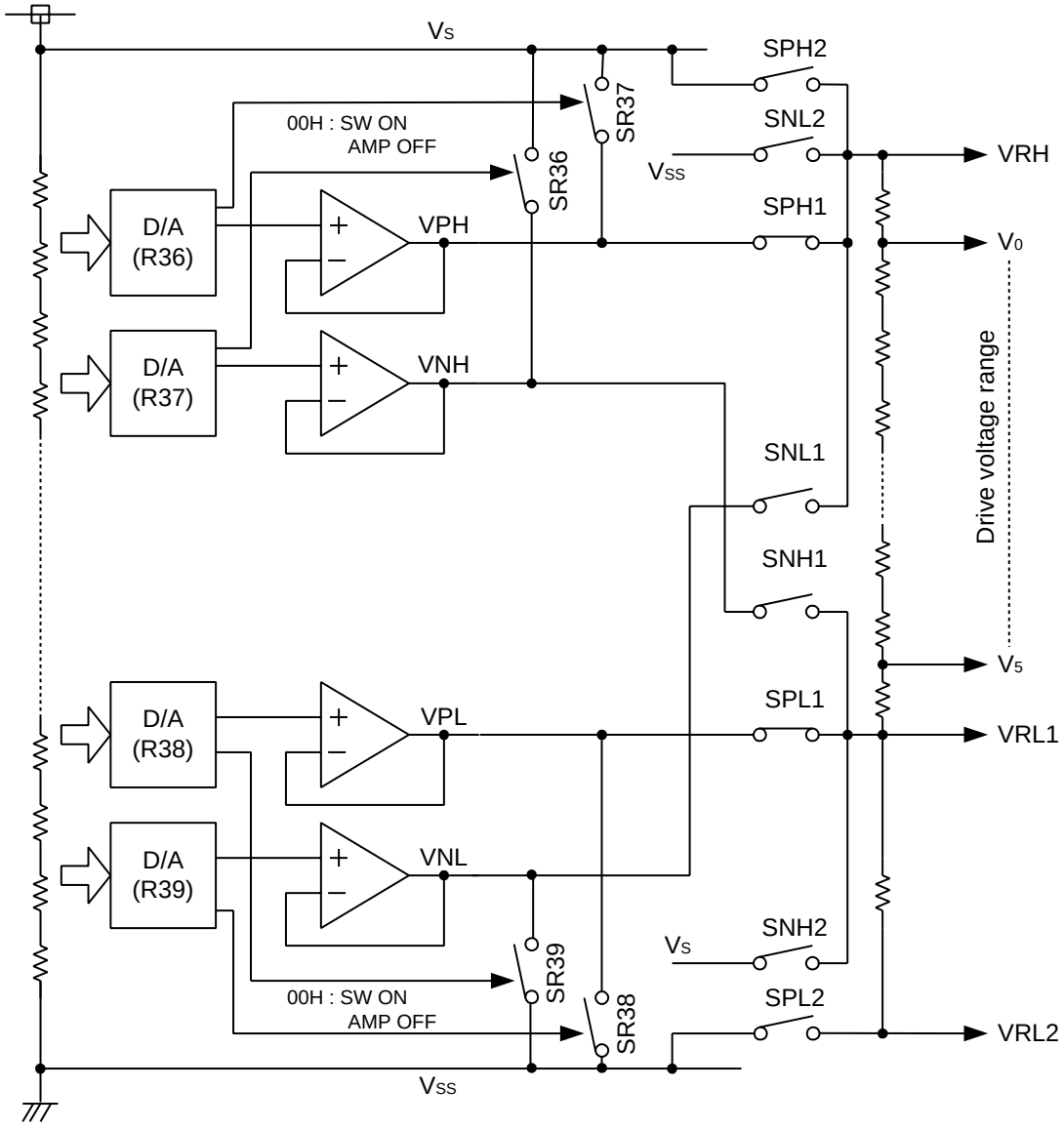


Table 5–14. γ-Curve Correction Circuit (γ-correction resistance)

Glay scale	Display Data		Resistance (kΩ)		Output Voltage (V)	
	D_{10} - D_5	D_{15} - D_{11}, D_4 - D_0	r 1	1.587	Positive Voltage	Negative Voltage
0	00H	00H	r 2	1.226	4.901	0.107
1	01H	–	r 3	2.453	4.824	0.190
2	02H	–	r 4	3.390	4.671	0.356
3	03H	01H	r 5	4.112	4.459	0.586
4	04H	–	r 6	4.905	4.202	0.864
5	05H	02H	r 7	1.731	3.895	1.196
6	06H	–	r 8	1.443	3.787	1.313
7	07H	03H	r 9	1.587	3.697	1.411
8	08H	–	r 10	1.515	3.598	1.519
9	09H	04H	r 11	1.082	3.503	1.621
10	0AH	–	r 12	1.082	3.436	1.694
11	0BH	05H	r 13	1.154	3.368	1.768
12	0CH	–	r 14	1.226	3.296	1.846
13	0DH	06H	r 15	1.298	3.219	1.929
14	0EH	–	r 16	1.082	3.138	2.017
15	0FH	07H	r 17	0.649	3.070	2.090
16	10H	–	r 18	0.721	3.030	2.134
17	11H	08H	r 19	0.794	2.985	2.183
18	12H	–	r 20	0.721	2.935	2.236
19	13H	09H	r 21	0.794	2.890	2.285
20	14H	–	r 22	0.505	2.840	2.339
21	15H	0AH	r 23	0.577	2.809	2.373
22	16H	–	r 24	0.577	2.773	2.412
23	17H	0BH	r 25	0.577	2.737	2.451
24	18H	–	r 26	0.505	2.701	2.490
25	19H	0CH	r 27	0.433	2.669	2.524
26	1AH	–	r 28	0.433	2.642	2.554
27	1BH	0DH	r 29	0.433	2.615	2.583
28	1CH	–	r 30	0.433	2.588	2.612
29	1DH	0EH	r 31	0.505	2.561	2.642
30	1EH	–	r 32	0.361	2.529	2.676
31	1FH	0FH	r 33	0.433	2.507	2.700
32	20H	–	r 34	0.433	2.480	2.729
33	21H	10H	r 35	0.433	2.453	2.759
34	22H	–	r 36	0.433	2.426	2.788
35	23H	11H	r 37	0.433	2.399	2.817
36	24H	–	r 38	0.433	2.372	2.847
37	25H	12H	r 39	0.505	2.344	2.876
38	26H	–	r 40	0.433	2.313	2.910
39	27H	13H	r 41	0.433	2.286	2.939
40	28H	–	r 42	0.433	2.259	2.969
41	29H	14H	r 43	0.505	2.232	2.998
42	2AH	–	r 44	0.361	2.200	3.032
43	2BH	15H	r 45	0.433	2.178	3.057
44	2CH	–	r 46	0.433	2.151	3.086
45	2DH	16H	r 47	0.361	2.124	3.115
46	2EH	–	r 48	0.361	2.101	3.140
47	2FH	17H	r 49	0.361	2.078	3.164
48	30H	–	r 50	0.361	2.056	3.188
49	31H	18H	r 51	0.433	2.033	3.213
50	32H	–	r 52	0.433	2.006	3.242
51	33H	19H	r 53	0.433	1.979	3.271
52	34H	–	r 54	0.505	1.952	3.301
53	35H	1AH	r 55	0.505	1.921	3.335
54	36H	–	r 56	0.505	1.889	3.369
55	37H	1BH	r 57	0.721	1.858	3.403
56	38H	–	r 58	0.721	1.812	3.452
57	39H	1CH	r 59	0.866	1.767	3.501
58	3AH	–	r 60	0.866	1.713	3.560
59	3BH	1DH	r 61	1.587	1.659	3.618
60	3CH	–	r 62	2.597	1.560	3.726
61	3DH	1EH	r 63	2.597	1.398	3.901
62	3EH	–	r 64	12.047	1.235	4.077
63	3FH	1FH	r 65	7.719	0.482	4.893
		Total		80.000		

Figure 5–25. γ-Curve Corrected Circuit (γ-corrected resistance value)

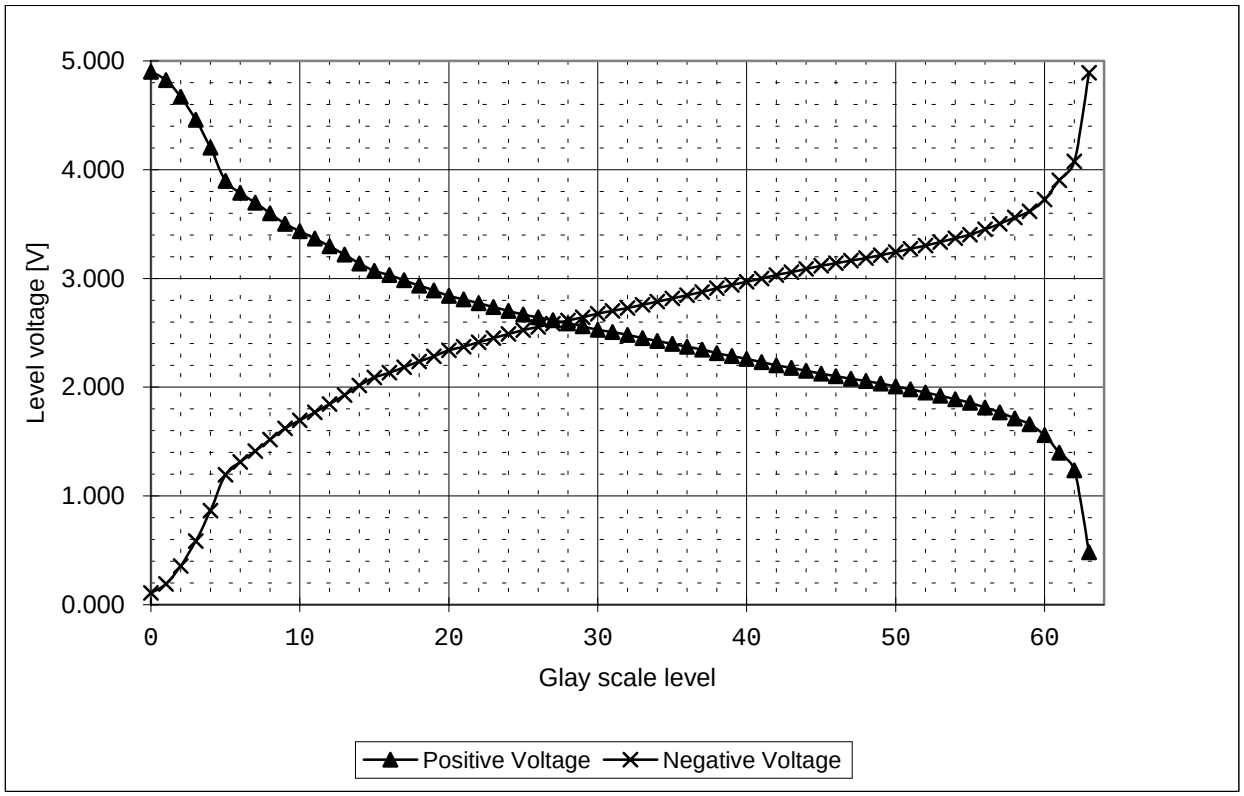
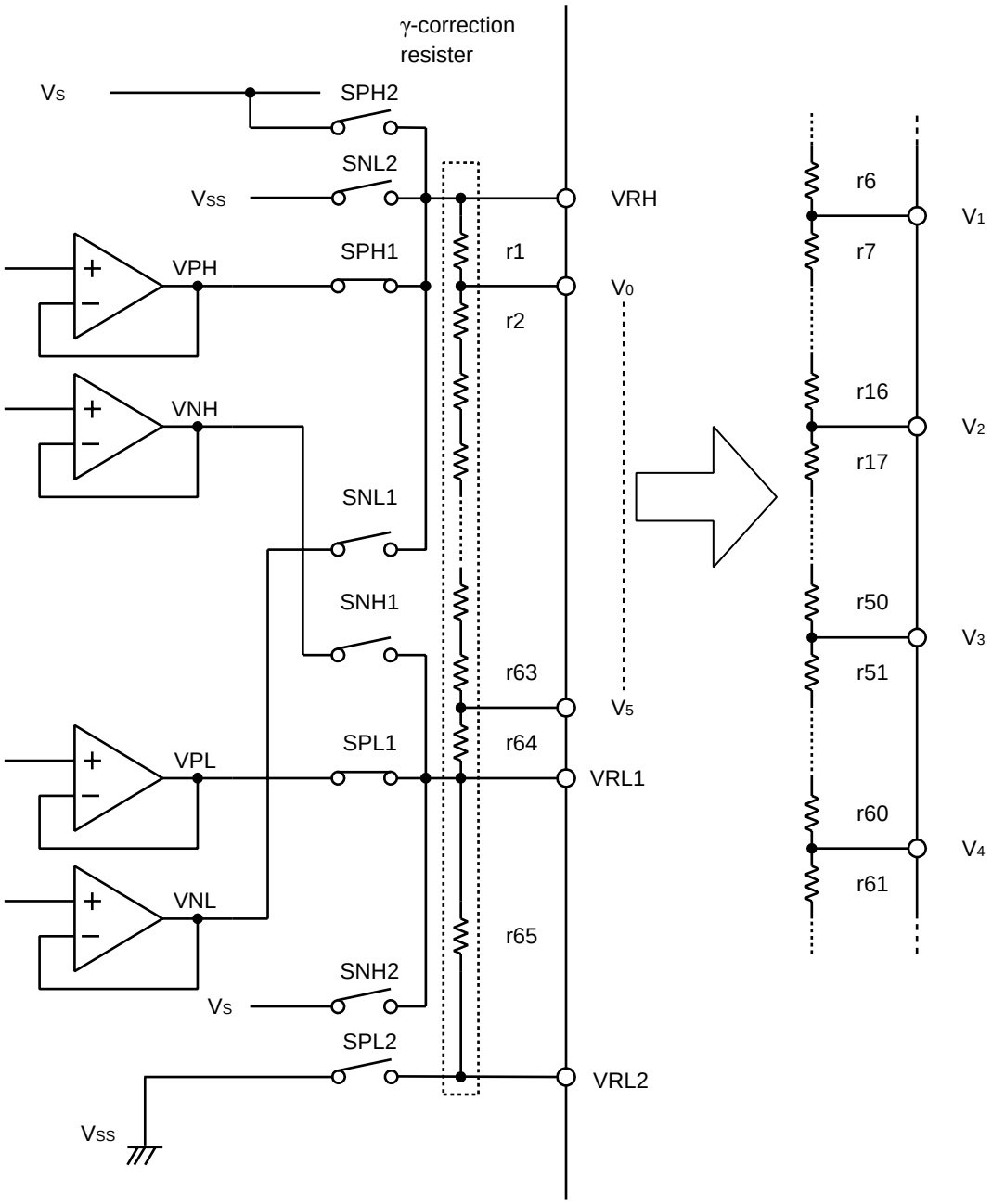


Figure 5–26. Internal Connection of V_0 to V_5, VRH, VRL1, and VRL2



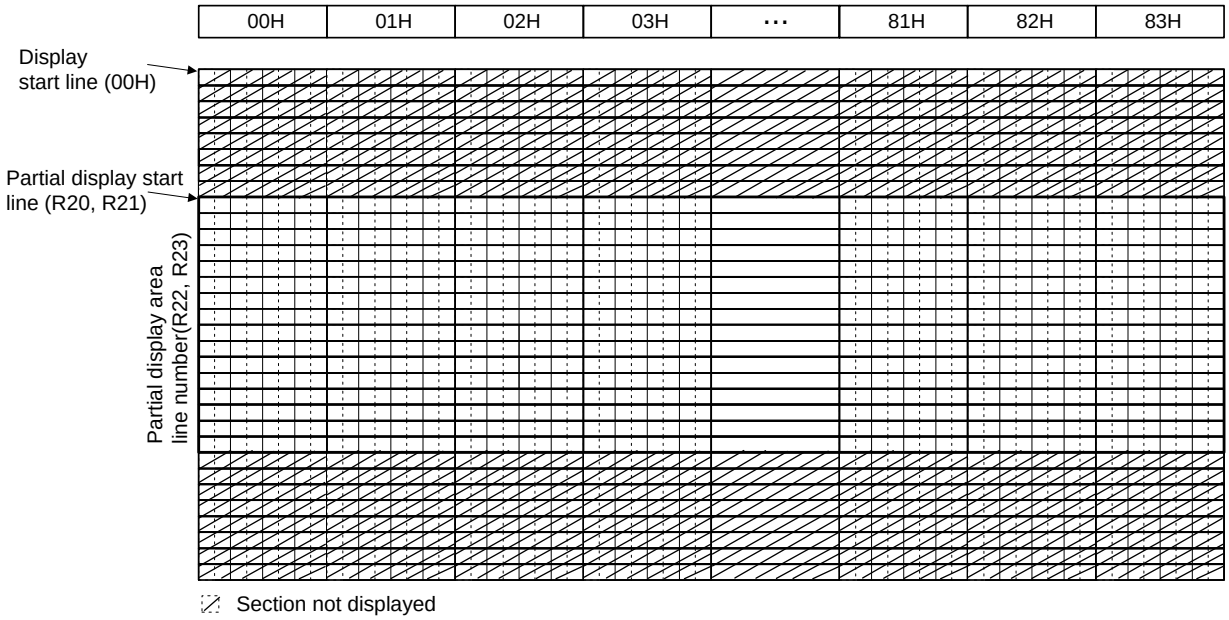
5.10 Partial Display Mode

The μPD161622 is provided with a function that allows sections within the screen to be displayed separately (partial display mode). The start line of the area to be displayed in partial display mode is set using the partial display area start line register (R20, R21), the number of lines in the area to be displayed is set using the partial display area line count register (R22, R23), and the color of the area not to be displayed is set using the partial off area color register (R19). If "1" is set in the partial display area line count registers (R22, R23), the partial display areas each become 1 line. If "0" is set, there are no partial display areas but only normal display areas.

The non-display area indicated by R20 and R22 is called Partial 1, and the non-display area indicates by R21 and R23 is called Partial 2. The Partial 2 setting is enabled only when the Partial 1 setting has been performed (when R22 ≠ 0). Therefore, to set only one area as a non-display area, perform only the setting for Partial 1.

Low power consumption cannot be achieved if only the partial mode is set. If low power consumption is required, the mode must be switched to the 8-clor mode.

Figure 5–26. Partial Display Mode



Cautions 1. The "scroll step count register (R17)" command is ignored in the partial display mode.

2. The specified partial areas must not directly overlap, and the Partial 1 area and Partial 2 area must be separated by at least one line. If the areas overlap, only the Partial 1 settings are valid, and partial display is not performed for the Partial 2 area.

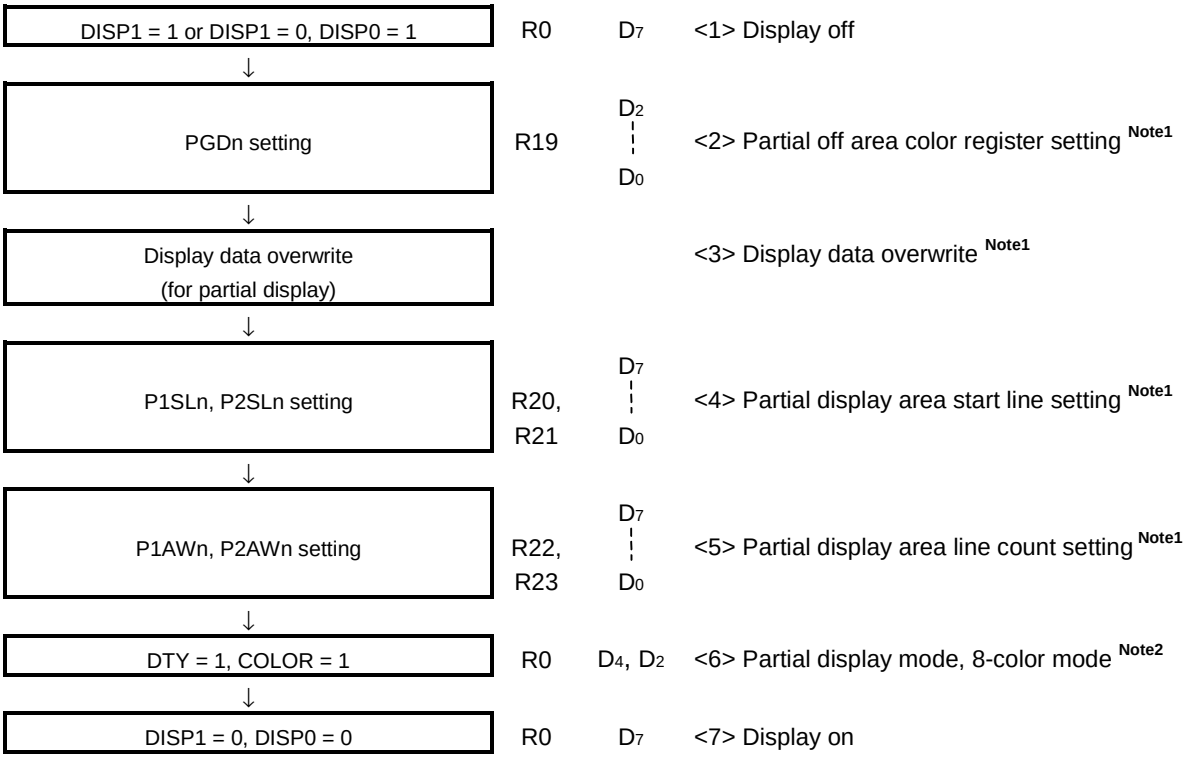
3. When setting the partial display areas, be sure to observe the following relationship.

"00H" ≤ R20 (R21)

R22 (R23) ≤ "AFH"

The following sequence is recommended to avoid display malfunction when switching from normal display mode to partial display mode and vice versa.

(1) Recommended sequence for switching from normal display mode to partial display mode



Notes 1. <2> to <5> can be executed in any order.

2. <6> must be executed after <4> and <5> have been set.

(2) Recommended sequence for switching from partial display mode to normal display mode

DISP1 = 1 or DISP1 = 0, DISP0 = 1	R0	D_7	<1> Display off
↓			
Display data overwrite (for normal display)			<2> Display data overwrite [Note]
↓			
DTY = 0, COLOR = 0	R0	D_4, D_2	<3> Partial display mode, 65,000-color mode [Note]
↓			
DISP1 = 0, DISP0 = 0	R0	D_7	<4> Display on

Note <2> to <3> can be executed in any order.

(3) Recommended sequence for switching from partial display mode to partial display mode (switching the partial display area)

DISP1 = 1 or DISP1 = 0, DISP0 = 1	R0	D_7	<1> Display off
↓			
(display data overwrite)			<2> Display data overwrite Notes [Note1, 2]
↓			
P1SLn, P2SLn setting	R20, R21	D_7 ┆ D_0	<3> Partial display area start line setting [Note1]
↓			
P1AWn, P2AWn setting	R22, R23	D_7 ┆ D_0	<4> Partial display area line count setting [Note1]
↓			
DTY = 1	R0	D_4	<5> Partial display mode [Note3]
↓			
DISP1 = 0, DISP0 = 0	R0	D_7	<6> Display on

Notes 1. <2> to <4> can be executed in any order.

2. Execute <2> only when necessary.

3. <5> must be executed after <3> and <4> have been set.

(4) Partial display setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	00H	Sets Y address 00H
Partial display area line count register (R22, R23)	58H	Sets an area of 88 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	58H	Sets Y address 58H
Partial display area line count register (R22, R23)	58H	Sets an area of 88 lines

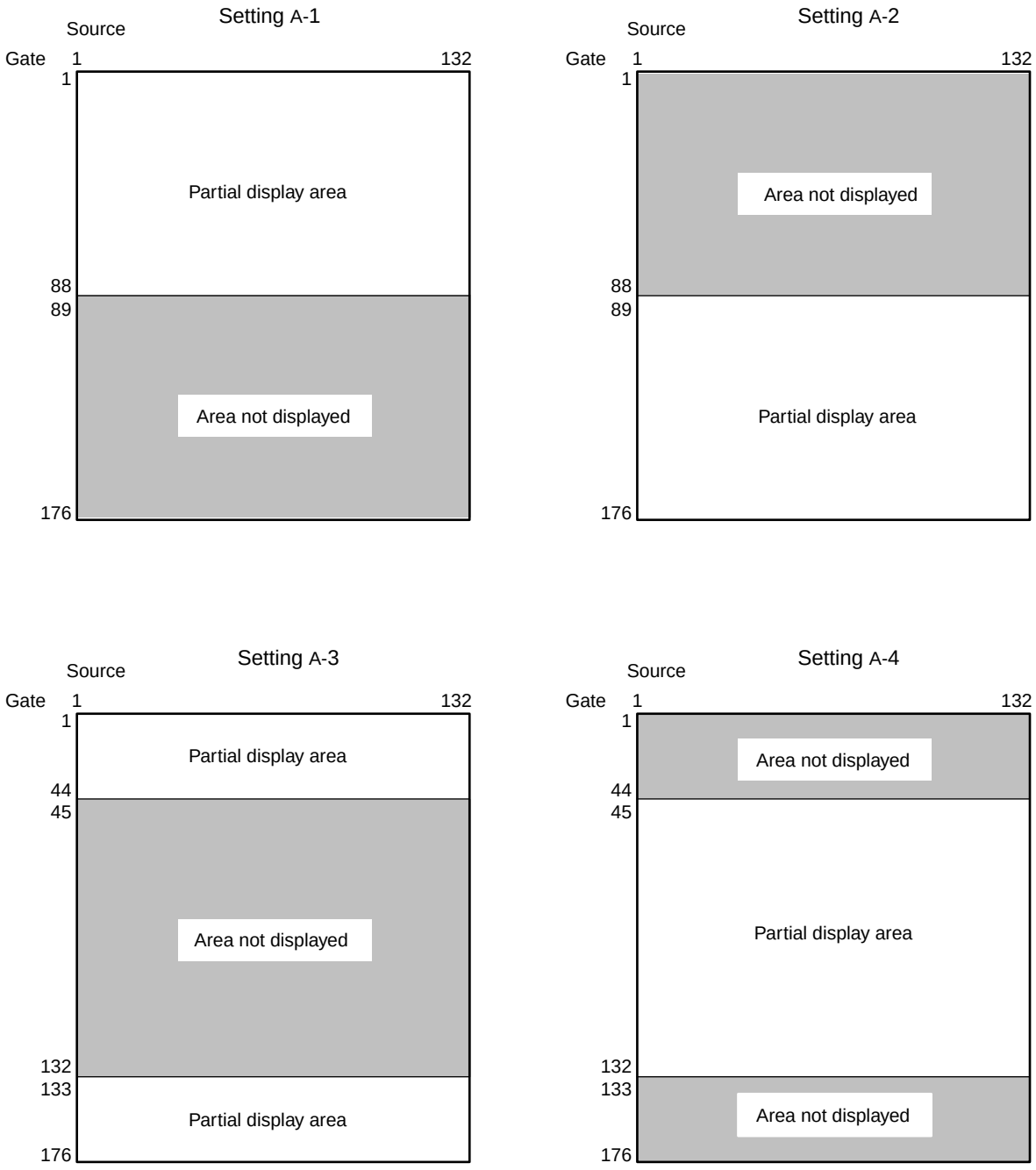
Setting A-3

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	84H	Sets Y address 84H
Partial display area line count register (R22, R23)	58H	Sets an area of 88 lines

Setting A-4

Register	Setting Value	Details of Setting Value
Partial display area start line register (R20, R21)	2CH	Sets Y address 2CH
Partial display area line count register (R22, R23)	58H	Sets an area of 88 lines

Figure 5–28. Partial Display Setting Examples



5.11 Screen Scroll

The μPD161622 has a screen scroll function. Any area of the screen can be scrolled by using the scroll area start line register (R15), scroll area line count register (R16), and scroll step count register (R17) to set the Y address of the top line of the area to be scrolled, the count of lines of the area to be scrolled, and the scroll step number, respectively.

Note that in partial mode, the screen scroll function is disabled.

Table 5–15. Scroll Area Start Line Register (R15)

SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0	Start Line Y Address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
0	0	0	0	0	0	1	1	03H
				↓				↓
1	0	1	0	1	1	0	1	ADH
1	0	1	0	1	1	1	0	AEH
1	0	1	0	1	1	1	1	AFH

Table 5–16. Scroll Area Line Count Register (R16)

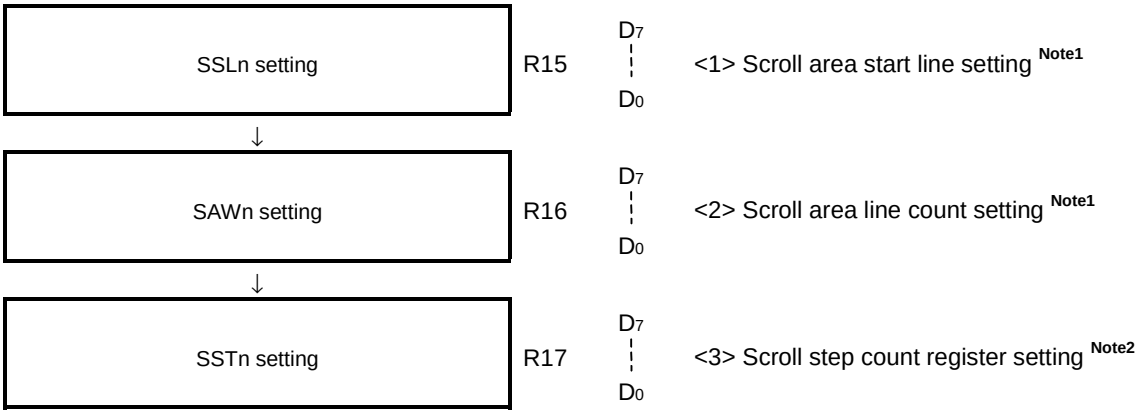
SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0	Scroll Area Line Number
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
				↓				↓
1	0	1	0	1	1	0	1	174
1	0	1	0	1	1	1	0	175
1	0	1	0	1	1	1	1	176

Table 5–17. Scroll Step Count Register (R17)

SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Step Number
0	0	0	0	0	0	0	0	0 (no scroll)
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
				↓				↓
1	0	1	0	1	1	0	1	173
1	0	1	0	1	1	1	0	174
1	0	1	0	1	1	1	1	175

Scrolling must be set using the following sequence.

(1) Recommended scroll sequence



Notes 1. <1> to <2> can be executed in any order.

2. <3> must be executed after <1> and <2> have been set.

Remark Set SSTn to 00H to disable the scroll operation. No particular sequence is required for this.

Cautions 1. If the sum of the values of SSLn and SAWn is 176 (AFH) or over, it is invalid (no scroll operation).

2. Set the step number SSTn so that it does not exceed the line number SAWn. If a value exceeding SAWn is set, it will be invalid (no scroll operation).

(2) Scroll setting examples

Setting A-1

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	00H	Sets Y address 00H
Scroll area line count register (R16)	AFH	Sets an area of 176 lines

Setting A-2

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	00H	Sets Y address 00H
Scroll area line count register (R16)	57H	Sets an area of 88 lines

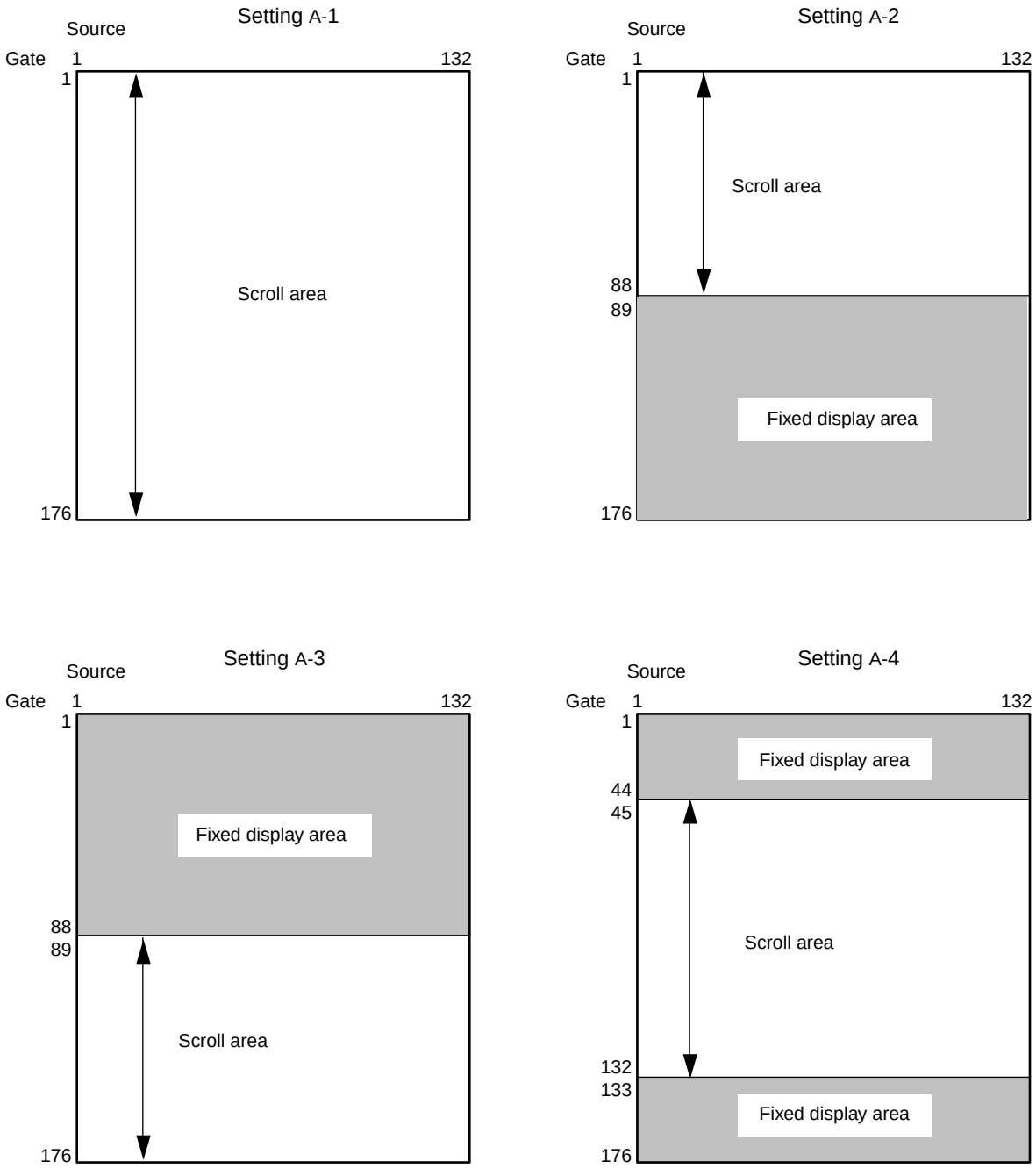
Setting A-3

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	58H	Sets Y address 58H
Scroll area line count register (R16)	57H	Sets an area of 88 lines

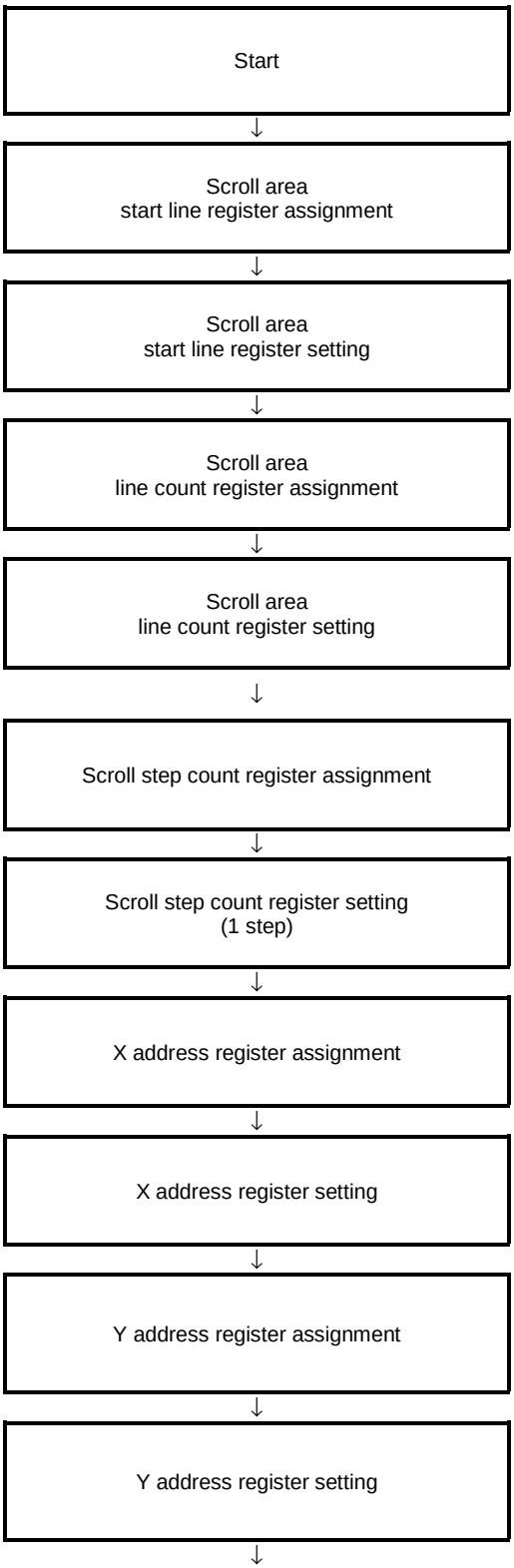
Setting A-4

Register	Setting Value	Details of Setting Value
Scroll area start line register (R15)	2CH	Sets Y address 2CH
Scroll area line count register (R16)	57H	Sets an area of 88 lines

Figure 5–29. Display Scroll Setting Examples



(3) Scroll setting flowchart example



IR D_6 to D_0 Index register

RS	MSB							LSB
L	X	0	0	0	1	1	1	1

R15 D_7 to D_0 Scroll area start line register

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 are the data for Scroll area start line.

IR D_5 to D_0 Index register

RS	MSB							LSB
L	X	0	0	1	0	0	0	0

R16 D_7 to D_0 Scroll area line count register

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 are the data for Scroll area line count register.

IR D_6 to D_0 Index register

RS	MSB							LSB
L	X	0	0	1	0	0	0	1

R17 D_7 to D_0 Scroll step count register

RS	MSB							LSB
H	0	0	0	0	0	0	0	1

IR D_6 to D_0 Index register

RS	MSB							LSB
L	X	0	0	0	0	1	1	0

R6 D_7 to D_0 X address register

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.

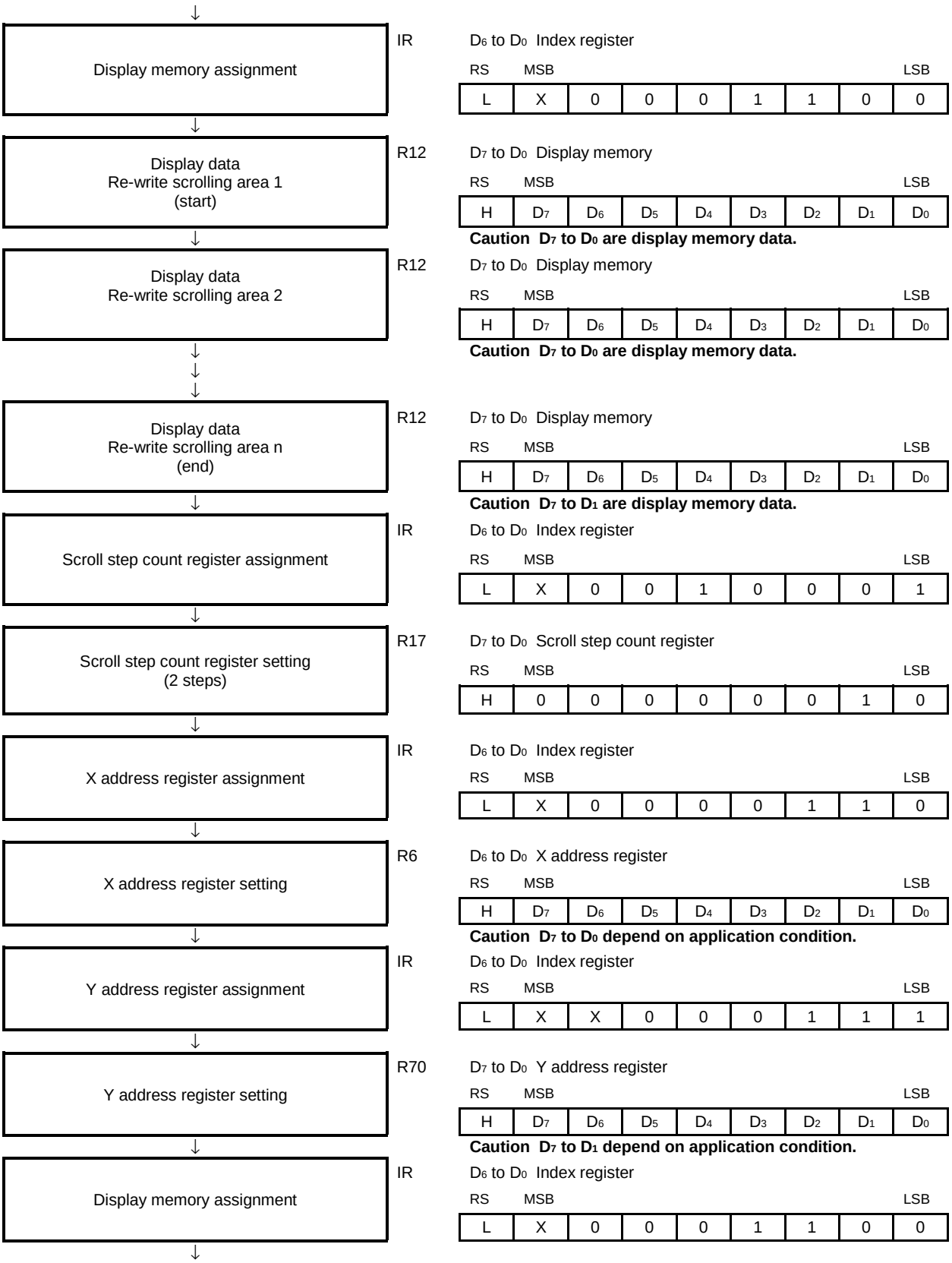
IR D_6 to D_0 Index register

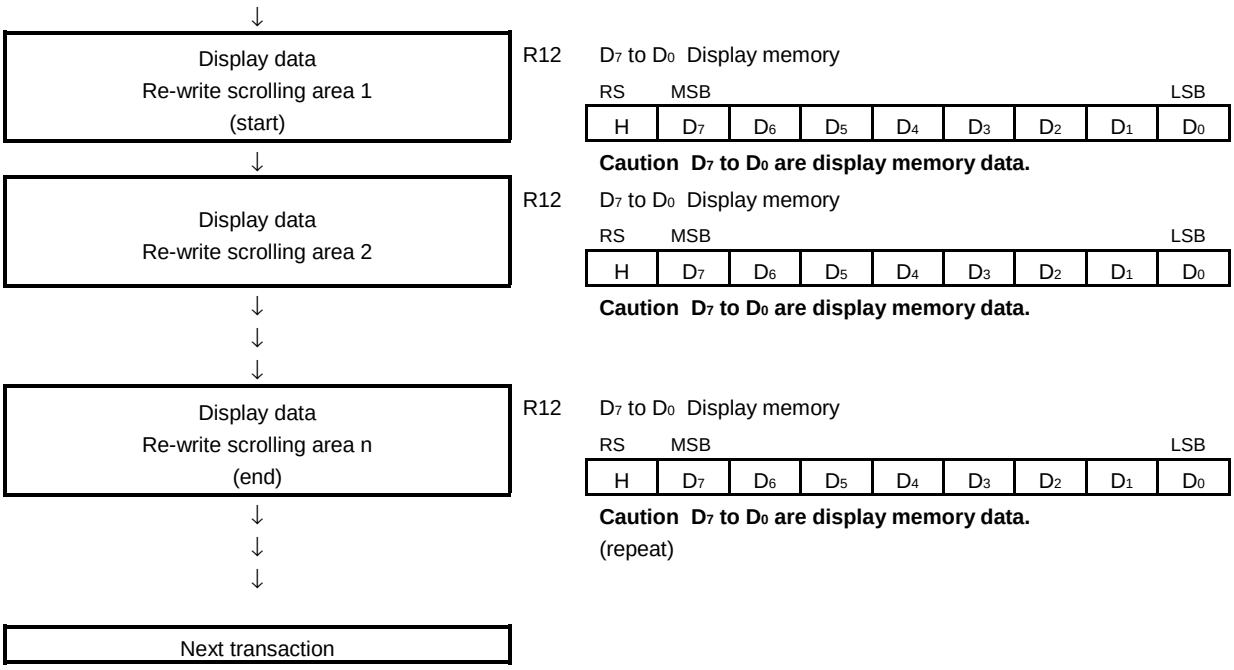
RS	MSB							LSB
L	X	0	0	0	0	1	1	1

R7 D_7 to D_0 Y address register

RS	MSB							LSB
H	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_7 to D_0 depend on application condition.


Display memory assignment
IR
D6 to D0 Index register
RS MSB LSB
L X 0 0 0 1 1 0 0
Display data Re-write scrolling area 1 (start)
R12
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Caution D7 to D0 are display memory data.
Display data Re-write scrolling area 2
R12
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Caution D7 to D0 are display memory data.
Display data Re-write scrolling area n (end)
R12
D7 to D0 Display memory
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Caution D7 to D1 are display memory data.
Scroll step count register assignment
IR
D6 to D0 Index register
RS MSB LSB
L X 0 0 1 0 0 0 1
Scroll step count register setting (2 steps)
R17
D7 to D0 Scroll step count register
RS MSB LSB
H 0 0 0 0 0 0 1 0
X address register assignment
IR
D6 to D0 Index register
RS MSB LSB
L X 0 0 0 0 1 1 0
X address register setting
R6
D6 to D0 X address register
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Caution D7 to D0 depend on application condition.
Y address register assignment
IR
D6 to D0 Index register
RS MSB LSB
L X X 0 0 0 1 1 1
Y address register setting
R70
D7 to D0 Y address register
RS MSB LSB
H D7 D6 D5 D4 D3 D2 D1 D0
Caution D7 to D1 depend on application condition.
Display memory assignment
IR
D6 to D0 Index register
RS MSB LSB
L X 0 0 0 1 1 0 0



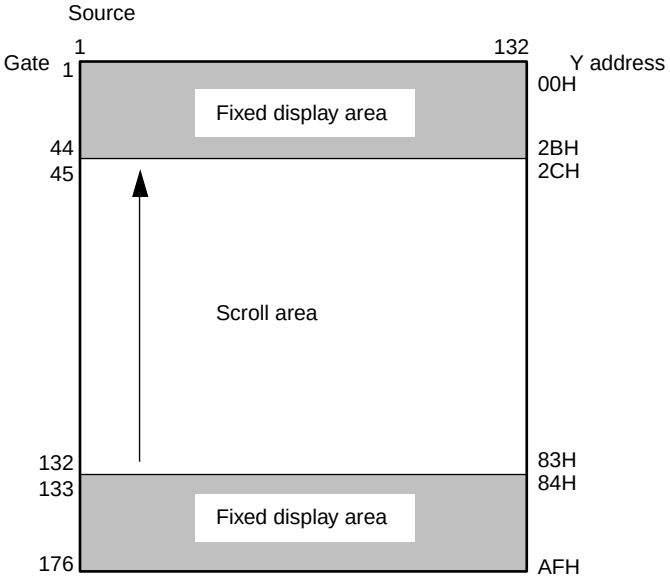
Caution This sequence is shown only for the purpose of illustrating the command sequence, and is not meant for use in mass-production design.

(4) Scroll function example

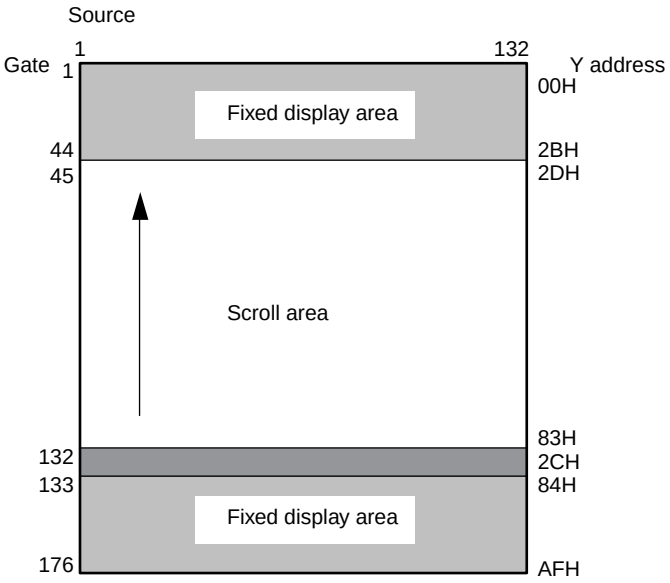
Scroll area start line register (R15): 2CH

Scroll area line count register (R16): 58H

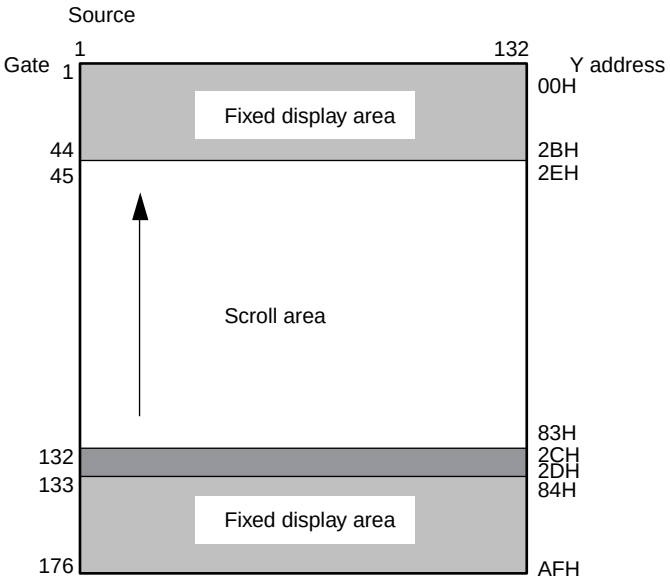
(a) Scroll step count register setting (R17): 00H



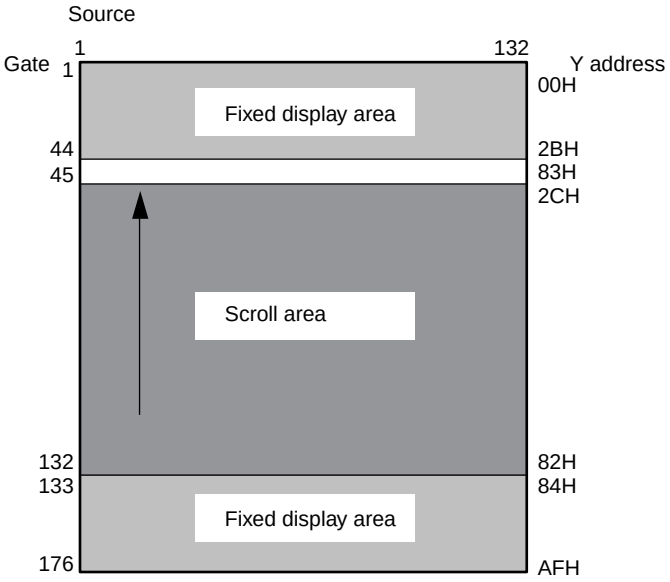
(b) Scroll step count register setting (R17): 01H



(c) Scroll step count register setting (R17): 02H



(d) Scroll step count register setting (R17): 57H



5.12 Stand-by

The μPD161622 has a stand-by function. Input of a stand-by command is acknowledged when the STBY bit of the control register 1 (R0) is set to 1.

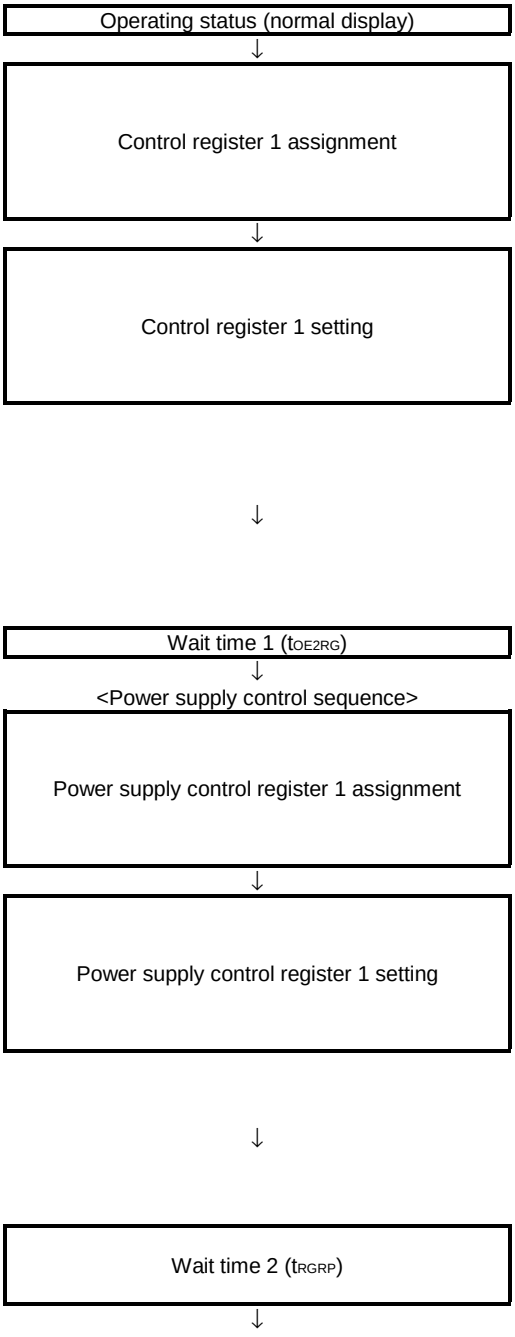
When the stand-by command has been input, the μPD161622 is forcibly placed in the V_{SS} display status, and scans the frame being display to the end. When scanning is complete, all gate outputs are turned on, the charge of the pixel on the TFT panel is decreased to 0, and the output stage amplifier and internal oscillator are stopped.

The stand-by function is valid for only the source driver IC; the gate IC (μPD161640) and power IC (μPD161660) connected to the μPD161622 are not controlled by this function.

After executing the stand-by command, therefore, execute commands that turn off the regulator for the gate IC and power IC an turn off the DC/DC converter.

When the stand-by status is released, turn on the DC/DC converter and the regulator of the gate IC and power IC, and then issue an ordinary operation command (STBY = 0), in the reverse order to which the stand-by command was input.

(1) Stand-by sequence



D_6 to D_0 Index register

RS	D_{15} to D_8							
	D_7							D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

D_7 to D_0 Control register 1

RS	D_{15} to D_8							
	D_7							D_0
H	X	X	X	X	X	X	X	X
	X	X	D_5	0	**1**	0	0	0

D_7: Don't care
D_6: Don't care
D_4: Normal display mode (not partial display mode)
D_3: Stand-by ON
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.
The source output is automatically fixed to the V_{SS} level by stand-by, so D_7 and D_6 can be set to any value.

At least one frame period

D_5 to D_0 Index register

RS	D_{15} to D_8							
	D_7							D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

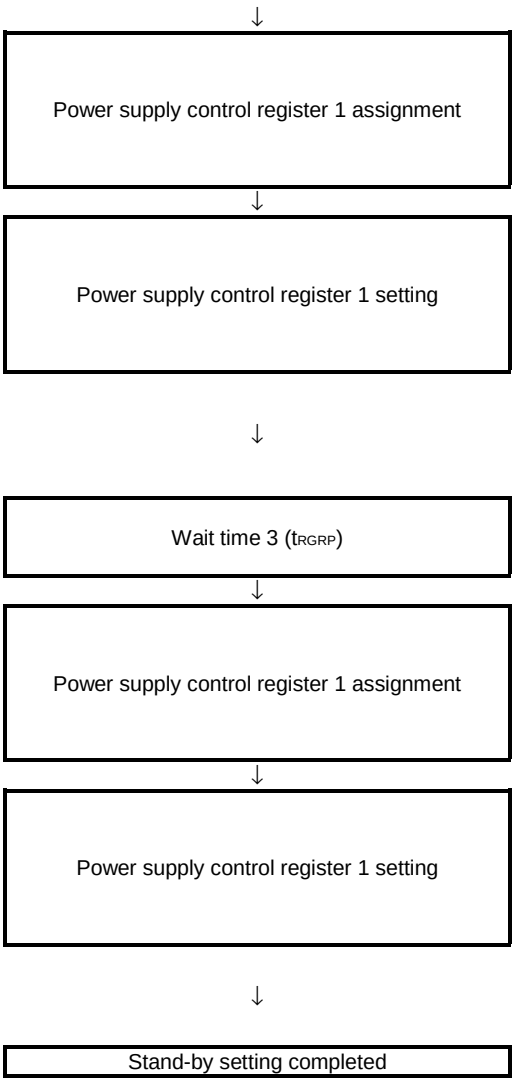
D_7 to D_0 Power supply control register 1

RS	D_{15} to D_8							
	D_7							D_0
H								
	X	D_6	D_5	D_4	D_3	**0**[Note]	1	1

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator OFF
D_1: Power supply IC regulator ON
D_0: DC/DC converter ON

Note This setting can be deleted from the sequence when using an IC with no regulator circuit for the gate driver.

Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.



D5 to D0 Index register

RS	D15 to D7							D8 to D0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

D7 to D0 Power supply control register 1

RS	D15 to D7							D8 to D0
H								
	X	D6	D5	D4	D3	0	**0**	1

D6 to D3 are set in accordance with the usage conditions.
D2: Gate driver regulator OFF
D1: Power supply IC regulator OFF
D0: DC/DC converter ON

Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.

D5 to D0 Index register

RS	D15 to D7							D8 to D0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

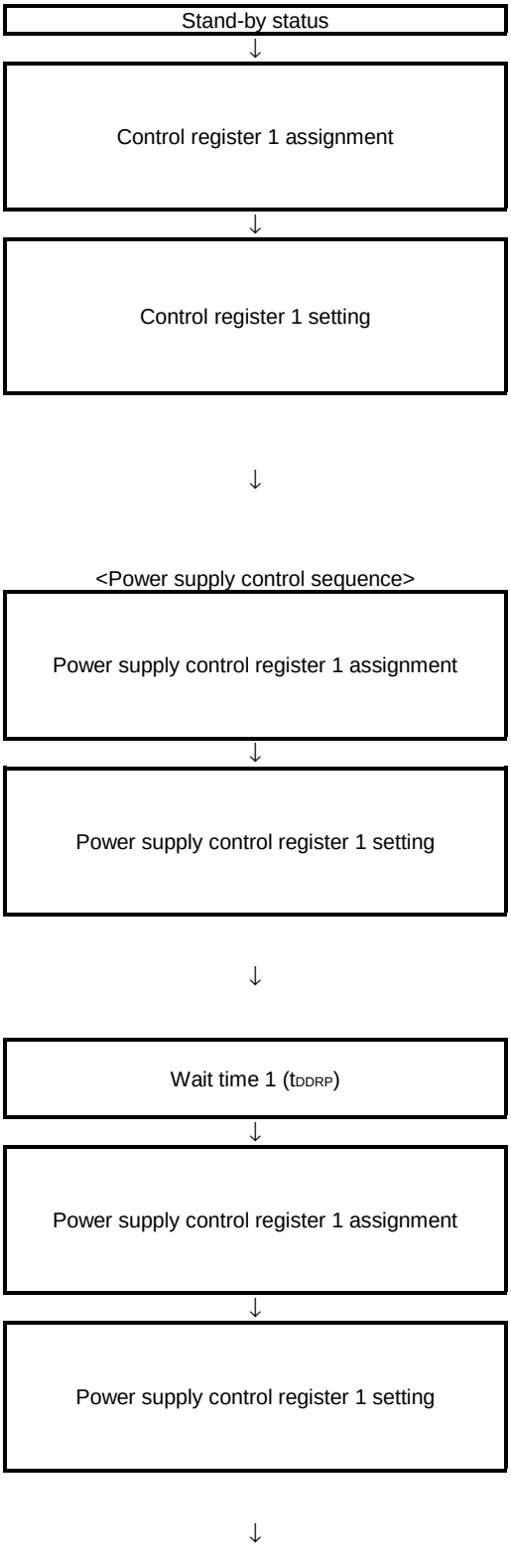
D7 to D0 Power supply control register 1

RS	D15 to D7							D8 to D0
H								
	X	D6	D5	D4	D3	0	0	**0**

D6 to D3 are set in accordance with the usage conditions.
D2: Gate driver regulator OFF
D1: Power supply IC regulator OFF
D0: DC/DC converter OFF

Caution This sequence is shown only for the purpose of illustrating the command sequence, and is not meant for use in mass-production design.

(2) Stand-by release sequence



D6 to D0 Index register

RS	D15							D8
	D7							D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

D7 to D0 Control register 1

RS	D15							D8
	D7							D0
H	X	X	X	X	X	X	X	X
	1	0	D5	0	**0**	0	0	0

D7: All data "1" output (normally white: white output)
D6: Normal display
D4: Normal display mode (not partial display mode)
D3: Normal mode (stand-by release)
D2: 65,000-color display mode
D1: Normal power mode
D5 is set in accordance with the usage conditions.

D5 to D0 Index register

RS	D15							D8
	D7							D0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

D7 to D0 Power supply control register 1

RS	D15							D8
	D7							D0
H								
	X	D6	D5	D4	D3	0	0	**1**

D6 to D3 are set in accordance with the usage conditions.
D2: Gate driver regulator OFF
D1: Power supply IC regulator OFF
D0: DC/DC converter ON

tDDRP is the output stable period of the DC/DC converter.
Although a setting of about 50 mS is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.

D5 to D0 Index register

RS	D15							D8
	D7							D0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

D7 to D0 Power supply control register 1

RS	D15							D8
	D7							D0
H								
	X	D6	D5	D4	D3	0	**1**	1

D6 to D3 are set in accordance with the usage conditions.
D2: Gate driver regulator OFF
D1: Power supply IC regulator ON
D0: DC/DC converter ON

↓

Wait time 2 (t_{RPRG})

t_{RPRG} is the output stable period of the DC/DC converter.
Although a setting of about 20 mS is the target, be sure to finalize the timing after sufficient evaluation with the LCD module.

↓

Power supply control register 1 assignment

IR

D_5 to D_0 Index register

RS	D_{15}						D_8
	D_7						D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

↓

Power supply control register 1 setting

R25

D_7 to D_0 Power supply control register 1

RS	D_{15}						D_8
	D_7						D_0
H								
	X	D_6	D_5	D_4	D_3	**1**[Note]	1	1

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator ON
D_1: Power supply IC regulator ON
D_0: DC/DC converter ON

Note This setting can be deleted from the sequence when using an IC with no regulator circuit for the gate driver.

↓

Wait time 3 (t_{RGOE1})

Input DISP ON command after all power supply is set up.
Although a setting of about 1 mS is the target in t_{RPRG}, be sure to finalize the timing after sufficient evaluation with the LCD module.

↓

<Display ON>

Control register 1 assignment

IR

D_6 to D_0 Index register

RS	D_{15}						D_8
	D_7						D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

↓

Control register 1 setting

R0

D_7 to D_0 Control register 1

RS	D_{15}						D_8
	D_7						D_0
H	X	X	X	X	X	X	X	X
	0	0	D_5	0	**0**	0	0	0

D_7: Normal display (all data "1" output → display ON)
D_6: Normal display
D_4: Normal display mode (not partial display mode)
D_3: Normal mode (stand-by release)
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

↓

Next transaction

Caution This sequence is shown only for the purpose of illustrating the command sequence, and is not meant for use in mass-production design.

5.13 8-Color Dispaly Mode

The μPD161622 contains an 8-color display function for low-power-consumption driving. The mode can be switched to 8-color display mode by setting COLOR in control register 1 (R0) to 1.

As shown in the figure below, in 8-color display mode, the μPD161622 controls ON/OFF of each dot using the MSB of each dot data in the display RAM. It is therefore necessary to overwrite the display RAM data in accordance with the screen of each mode when changing from 65,000-color display mode to 8-color mode, and vice versa.

In 8-color display mode, each source output is connected by switching the top and bottom grayscale voltages to enable direct driving of the TFT panel, which results in low power consumption.

Figure 5–30.

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Valid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid
Dot 1					Dot 2						Dot 3				
1 pixel (= 1 x address)															

(1) 8-color display mode setting sequence example

Previous statement (65.000-color display mode)

↓

Control register 1 assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

↓

Control register 1 assignment

R0

D_7 to D_0 Control register 1

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	**1**	D_5	0	0	0	0	0

D_7: Normal display
D_6: All data "0" output (normally white: black output)
D_4: Normal display mode (not partial display mode)
D_3: Stand-by OFF
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

↓

<Data overwrite sequence>

In 8-color display mode, the value of the MSB of each dot data in the internal display RAM is used as the color data, making it necessary to overwrite the display RAM data when changing from 65,000-color display mode to 8-color display mode.

X address register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	0

↓

X address register setting

R6

D_7 to D_0 X address register

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

X address: 00H

↓

Y address register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	1

↓

Y address register setting

R7

D_7 to D_0 Y address register

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

Y address: 00H

↓

↓

Display memory register assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	1	1	0	0

↓

Display data write 1 (start)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	**D_{15}^***	X	X	X	X	**D_{10}^***	X	X
	X	X	X	**D_4^***	X	X	X	X

Caution D_{15}, D_{10}, and D_4 are display memory data.
When in 8-color mode, only D_{15}, D_{10}, and D_4 data are valid.
0: OFF, 1: ON, (normally white)

↓

Display data write 2

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	**D_{15}^***	X	X	X	X	**D_{10}^***	X	X
	X	X	X	**D_4^***	X	X	X	X

Caution D_{15}, D_{10}, and D_4 are display memory data.
When in 8-color mode, only D_{15}, D_{10}, and D_4 data are valid.
0: OFF, 1: ON, (normally white)

↓

Display data write n (end)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	**D_{15}^***	X	X	X	X	**D_{10}^***	X	X
	X	X	X	**D_4^***	X	X	X	X

Caution D_{15}, D_{10}, and D_4 are display memory data.
When in 8-color mode, only D_{15}, D_{10}, and D_4 data are valid.
0: OFF, 1: ON, (normally white)

↓

Control register 1 assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

↓

Control register 1 setting

R0 — D_7 to D_0 Control register 1

RS	D_{15} / D_7							D_8 / D_0
H	X	X	X	X	X	X	X	X
	0	**0**	D_5	0	0	**1**	**D_1**	0

D_7: Normal display
D_6: Normal display (display ON [All data “0” display → normal mode])
D_4: Normal display mode (not partial display mode)
D_3: Stand-by OFF
D_2: 8-color display mode
D_1: Power mode is set in accordance with the usage conditions.
D_5 is set in accordance with the usage conditions.

↓

Next transaction

Caution This sequence is shown only for the purpose of illustrating the command sequence, and is not meant for use in mass-production design.

(2) Returning to 65,000-color display mode sequence

Previous statement (8-color display mode)

↓

Control register 1 assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

↓

Control register 1 setting

R0

D_7 to D_0 Control register 1

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	**0**	D_5	0	0	1	D_1	0

D_7: Normal display
D_6: All data "0" output (normally white: black output)
D_4: Normal display mode (not partial display mode)
D_3: Stand-by OFF
D_2: 8-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.
In 8-color display mode, the value of the MSB of each dot date in the internal display RAM is used as the color data, making it necessary to overwrite the display RAM data when returning to 65,000-color display mode from 8-color display mode.

↓

<Data overwrite sequence>

X address register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	0

↓

X address register setting

R6

D_7 to D_0 X address register

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

X address: 00H

↓

Y address register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	1

↓

Y address register setting

R7

D_7 to D_0 Y address register

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

Y address: 00H

↓

↓

Display memory register assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	1	1	0	0

↓

Display data write 1 (start)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data write 2

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data write n (end)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Control register 1 assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

↓

Control register 1 setting

R0 — D_7 to D_0 Control register 1

RS	D_{15} / D_7							D_8 / D_0
H	X	X	X	X	X	X	X	X
	0	**0**	D_5	0	0	**0**	**0**	0

D_7: Normal display
D_6: Normal display (display ON [All data "0" display → normal mode])
D_4: Normal display mode (not partial display mode)
D_3: Stand-by OFF
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

↓

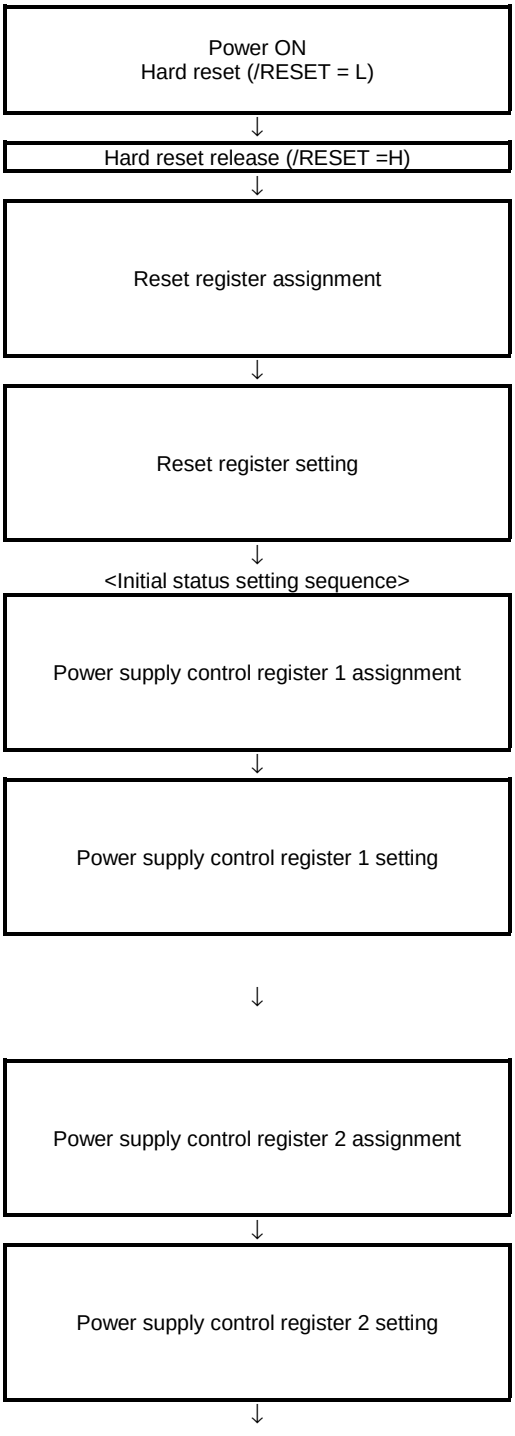
Next transaction

Caution This sequence is shown only for the purpose of illustrating the command sequence, and is not meant for use in mass-production design.

5.14 Power ON/OFF

An example of the standard power ON/OFF sequence in a chipset for driving a TFT-LCD panel that uses μPD61622 is shown below. Note that this sequence diffes depending on the chipset configuration and TFT-LCD panel used.

(1) Power ON sequence



IR D6 to D0 Index register

RS	D15 D7						D8 D0	
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	1	1

R3 D7 to D0 Reset register

RS	D15 D7						D8 D0	
H	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	1

IR D5 to D0 Index register

RS	D15 D7						D8 D0	
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

R25 D7 to D0 Power supply control register 1

RS	D15 D7						D8 D0	
H								
	X	D6	D5	D4	D3	0	0	0

D6 to D3 are set in accordance with the usage conditions.
D2: Gate driver regulator OFF
D1: Power supply IC regulator OFF
D0: DC/DC converter OFF

IR D6 to D0 Index register

RS	D15 D7						D8 D0	
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	1	0

R26 D7 to D0 Power supply control register 2

RS	D15 D7						D8 D0	
H								
	X	X	X	X	X	X	D1	D0

D1 and D0 are set in accordance with the usage conditions.

↓

Power supply control register 1 assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

↓

Power supply control register 1 setting

R25

D_7 to D_0 Power supply control register 1

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	X	D_6	D_5	D_4	D_3	1	1	1

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator ON
D_1: Power supply IC regulator ON
D_0: DC/DC converter ON

↓

VCOM output center value setting register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	1	0	1

↓

VCOM output center value setting register setting

R29

D_7 to D_0 Power supply control register 1

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	X	D_6	D_5	D_4	D_3	1	1	1

D_7 to D_3 are set in accordance with the usage conditions.
This register setting is not required when VCOMC (D_3) of the output stage capacity setting register (R30) is 0.

↓

Output stage capacity setting register assignment

IR

D_6 to D_0 Index register

RS	D_{15} to D_7							D_8 to D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	1	1	0

↓

Output stage capacity setting register setting

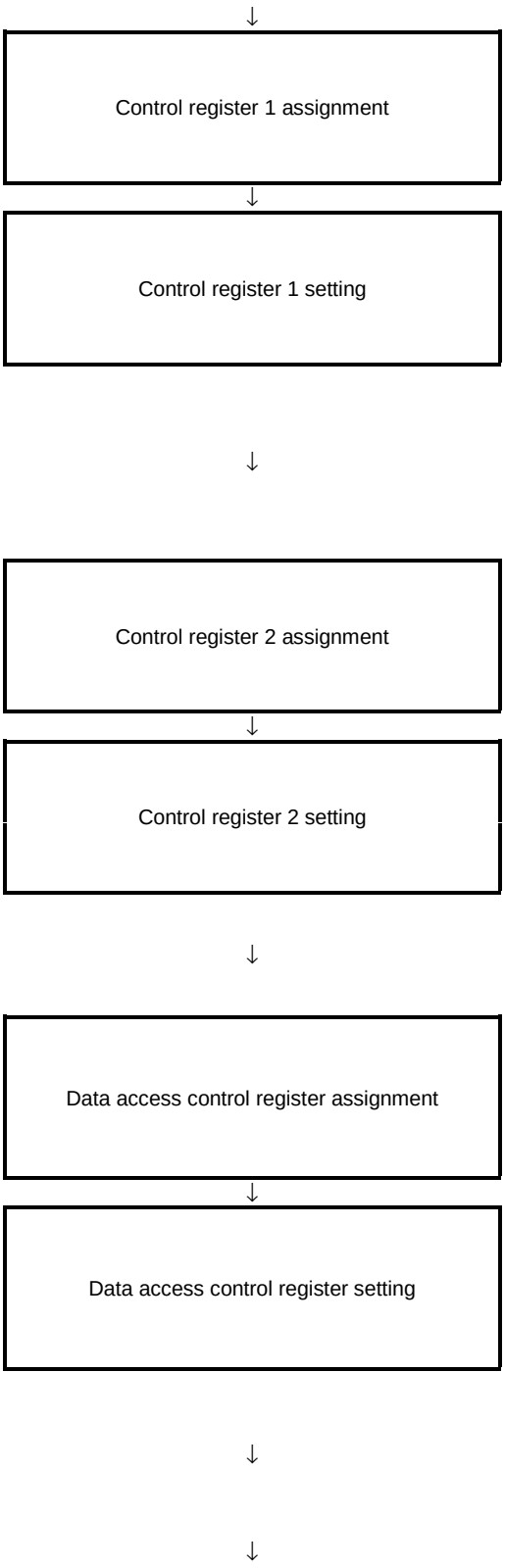
R30

D_7 to D_0 Power supply control register 1

RS	D_{15} to D_7							D_8 to D_0
H	X	X	X	X	X	X	X	X
	0	D_6	D_5	D_4	0	D_2	D_1	D_0

D_7: g-correction circuit reference voltage generation amplifier drive/normal
D_3: VCOM amplifier operation (when in used)
D_6 to D_4 are set in accordance with the usage conditions (capacity setting for COMMON center value setting amplifier (VCOM)).
D_2 to D_0 are set in accordance with the usage conditions (source output capacity setting).

↓



IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

R0 D7 to D0 Control register 1

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	1	0	D5	0	0	0	0	0

D7: All data "1" output (normally white: white output)
D6: Normal display
D4: Normal display mode (not partial display mode)
D3: Stand-by OFF
D2: 65,000-color display mode
D1: Normal power mode
D5 is set in accordance with the usage conditions.

IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	1

R1 D7 to D0 Control register 2

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	X	X	D5	D4	**0**	**0**	0	0

D1: 1 line time = t_{cal} (normal setting)
D0: Line inversion driving
D5 and D4 are set in accordance with the usage condtions.
Caution Always write 0 to D3 and D2.

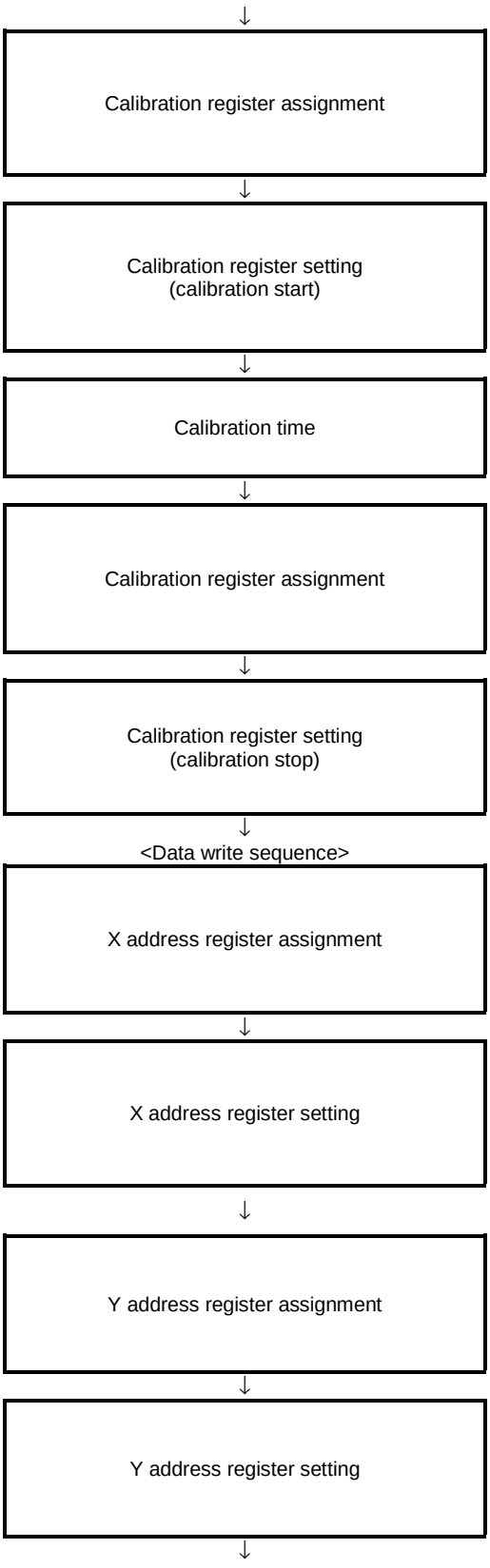
IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	0	1

R5 D7 to D0 Data access control register

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	0	0	**0**	0	**0**	0	0	0

D7: 16-bit data bus
D6: Normal write mode
D4: Normal operation (not window access mode)
D2: Access to X address direction
D1: X address increment
D0: Y address increment
Caution Always write 0 to D5 and D3.



IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	1	0	1	1	0	1

R45 D7 to D0 Calibration register

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	1

Calibration wait time (t_{cal})

t_{cal} = 1 ÷ (frame frequency ×177)

IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	1	0	1	1	0	1

R45 D7 to D0 Calibration register

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	0

IR D6 to D0 Index register

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	0

R6 D7 to D0 X address register

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

X address: 00H

IR D6 D0

RS	D15 D7							D8 D0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	1	1	1

R7 D7 to D0 Y address register

RS	D15 D7							D8 D0
H	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

Y address: 00H

↓

Display memory register assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	1	1	0	0

↓

Display data write 1 (start)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data write 2

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Display data write n (end)

R12 — D_{15} to D_0 Display memory register

RS	D_{15} / D_7							D_8 / D_0
H	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Caution D_{15} to D_0 are display memory data.

↓

Control register 1 assignment

IR — D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L								
	X	0	0	0	0	0	0	0

↓

Control register 1 setting

R0 — D_7 to D_0 Control register 1

RS	D_{15} / D_7							D_8 / D_0
H	X	X	X	X	X	X	X	X
	0	0	D_5	0	0	0	0	0

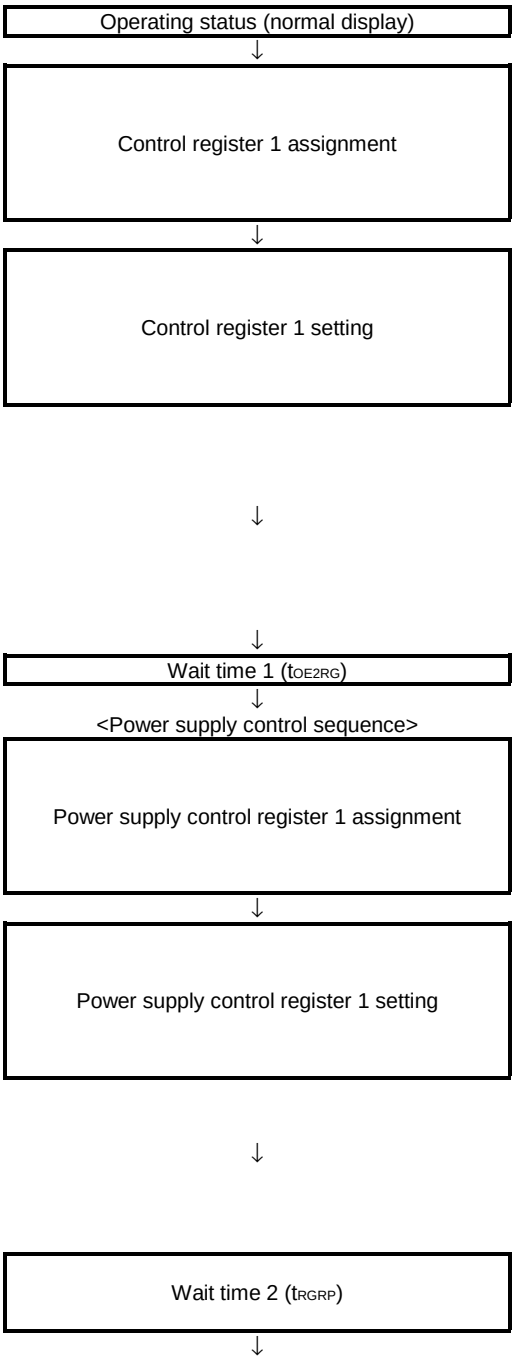
D_7: Normal display(display ON [All data "0" display → normal mode])
D_6: Normal display
D_4: Normal display mode (not partial display mode)
D_3: Stand-by OFF
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.

↓

Next transaction

Caution This sequence is shown only for the purpose of illustrating the sequence from power application to display ON, and is not meant for use in mass production design. Note also that this sequence differs depending on the configuration of the chipset and TFT-LCD module

(2) Power OFF sequence



IR

D_6 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	0	0	0	0	0

R0

D_7 to D_0 Control register 1

RS	D_{15} / D_7							D_8 / D_0
H	X	X	X	X	X	X	X	X
	X	X	D_5	0	**1**	0	0	0

D_7: Don't care
D_6: Don't care
D_4: Normal display mode (not partial display mode)
D_3: Stand-by ON
D_2: 65,000-color display mode
D_1: Normal power mode
D_5 is set in accordance with the usage conditions.
The source output is automatically fixed to the V_{SS} level by stand-by, so D_7 and D_6 can be set to any value.

At least one frame period

IR

D_5 to D_0 Index register

RS	D_{15} / D_7							D_8 / D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

R25

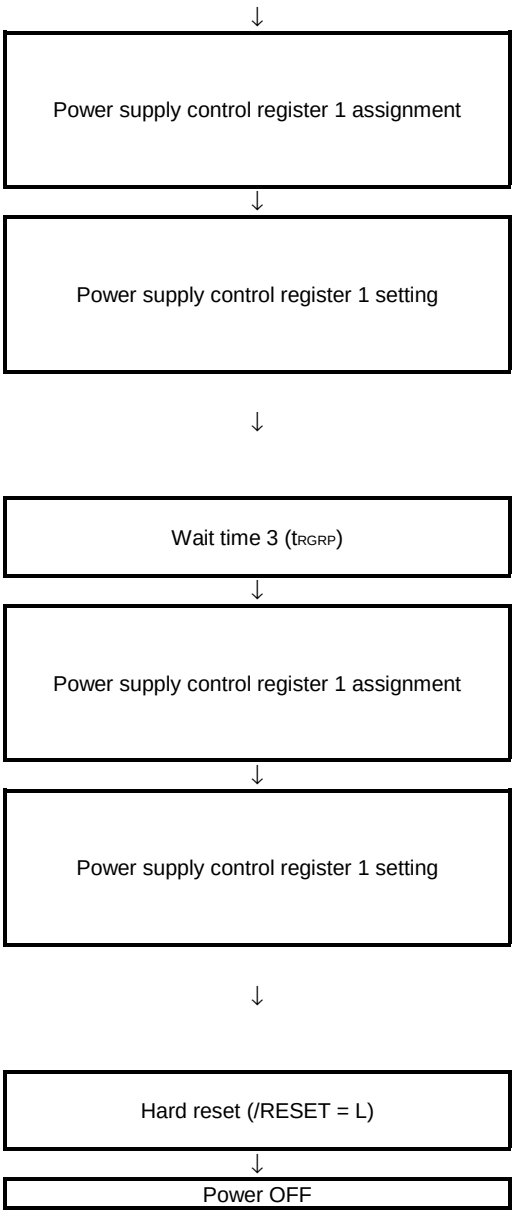
D_7 to D_0 Power supply control register 1

RS	D_{15} / D_7							D_8 / D_0
H								
	X	D_6	D_5	D_4	D_3	**0**[Note]	1	1

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator OFF
D_1: Power supply IC regulator ON
D_0: DC/DC converter ON

Note This setting can be deleted from the sequence when using an IC with no regulator circuit for the gate driver.

Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.



IR

D_5 to D_0 Index register

RS	D_{15} to D_8							
	D_7							D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

R25

D_7 to D_0 Power supply control register 1

RS	D_{15} to D_8							
	D_7							D_0
H								
	X	D_6	D_5	D_4	D_3	0	**0**	1

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator OFF
D_1: Power supply IC regulator OFF
D_0: DC/DC converter ON

Although a setting of 0 ns has no negative effect in terms of the device, be sure to finalize the timing after sufficient evaluation with the LCD module.

IR

D_5 to D_0 Index register

RS	D_{15} to D_8							
	D_7							D_0
L	X	X	X	X	X	X	X	X
	X	0	0	1	1	0	0	1

R25

D_7 to D_0 Power supply control register 1

RS	D_{15} to D_8							
	D_7							D_0
H								
	X	D_6	D_5	D_4	D_3	0	0	**0**

D_6 to D_3 are set in accordance with the usage conditions.
D_2: Gate driver regulator OFF
D_1: Power supply IC regulator OFF
D_0: DC/DC converter OFF

Do not need to input RESET in source driver, however, when power off, system reset is set up to /RESET = L by timing DCON (R25: D_0).

Caution This sequence is shown only for the purpose of illustrating the sequence up to when the power is turned off, and is not meant for use in mass-prodution design. Note also that this sequence differs depending on the configuration of the chipset and TFT-LCD module.

6. RESET

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

Register	Rn	/RESET Pin Note1	Reset Command	Default Value
Index register	IR	X	O	00H
Control register 1	R0	X	O	00H
Control register 2	R1	X	O	00H
Data access control register	R5	X	O	00H
X address register	R6	X	O	00H
Y address register	R7	X	O	00H
MIN. ·X address register	R8	X	O	00H
MAX. ·X address register	R9	X	O	00H
MIN. ·Y address register	R10	X	O	00H
MIN. ·Y address register	R11	X	O	00H
Display memory register Note2	R12	X	X	–
Scroll area start line register	R15	X	O	00H
Scroll area line count register	R16	X	O	00H
Scroll step count register	R17	X	O	00H
Partial off area color register	R19	X	O	00H
Partial 1 display area start line register	R20	X	O	00H
Partial 2 display area start line register	R21	X	O	00H
Partial 1 display area line count register	R22	X	O	00H
Partial 2 display area line count register	R23	X	O	00H
Power supply control register 1	R25	X	O	00H
Power supply control register 2	R26	X	O	00H
VCOM output center value setting register	R29	X	O	00H
Output stage capacity setting register	R30	X	O	00H
γ-reference-voltage generator capacity setting register	R31	X	O	00H
γ-contrast value setting register 1	R36	X	O	00H
γ-contrast value setting register 2	R37	X	O	00H
γ-contrast value setting register 3	R38	X	O	00H
γ-contrast value setting register 4	R39	X	O	00H
Pre-charge direction setting data register	R40	X	O	00H
γ-correction input disconnect register	R42	X	O	00H
Calibration register Note 3	R45	X	O	00H
★ Pre-charge period supplement pulse setting register	R46	X	O	06H
Output port register	R49	X	O	00H
Input port register	R50	X	O	00H
Interface operating voltage setting register	R114	X	O	00H
Internal logic operating voltage setting register	R115	X	O	00H
Test mode		X	O	00H

Remark O: Default value set, X: Default value not set

Notes 1. The internal counters are initialized only by a reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

2. The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are undifined. immediately after the power is turned on.

3. The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$tcal = 1/f_{OSC} \times 37$

7. COMMAND

The μPD161622 identifies data bus signals by a combination of the RS, /RD (E), and /WR (R,/W) signals. It interprets and executes commands only in accordance with the internal timing, without being dependent upon the external clock. Therefore, the processing speed is extremely high and, usually, no busy check is necessary.

An i80 system CPU interface inputs a low pulse to the /RD pin when it reads data to issue a command. It inputs a low pulse to the /WR pin when it writes data.

Data can be read from an M68 system CPU interface if a high-pulse signal is input to the R,/W pin, and written if a low-pulse signal is input to the R,/W pin. A command is executed if a high-pulse signal is input to the E pin in this status. Therefore, in the explanation of the commands and display commands after **7.2 Control Register 1 (R0)** and the sections that follow, the M68 system CPU interface uses H, instead of /RD (E), when reading status or display data. This is how it differs from the i80 system CPU interface.

The commands of the μPD161622 are explained below, taking an i80 system CPU interface as an example. When the serial interface is used, sequentially input data to the μPD161622, starting from D_7.

The data bus length to input commands is as follows:

- Commands other than those that manipulate the display memory register (R12) are input in one byte unit, regardless of the value of BMD (control register 2 (R1), bus length setting).
- The commands that manipulate the display memory register (R12) are input in 1-byte units when BMD = 1, or in 2-byte units when BMD = 0.

(1) Commands other than those that manipulate display memory register (R12)

BMD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	**Note**	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Note 0 or 1

(2) Display Memory Register (R12)

BMD = 1 (8-bit data bus)

Pin	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

BMD = 0 (16-bit data bus)

Pin	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DATA	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

7.1 Command List

CS	RS	Index Register							Rn	Register Name	R/W	Data Bits							
		6	5	4	3	2	1	0				7	6	5	4	3	2	1	0
1																			
0	0								IR	Index register	W	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
0	1	0	0	0	0	0	0	0	R0	Control register 1	R/W	DISP1	DISP0	ADC	DTY	STBY	COLOR	LPM	GSM
0	1	0	0	0	0	0	0	1	R1	Control register 2	R/W			VSEL	GSEL			LTS	INV
0	1	0	0	0	0	0	1	0	R2										
0	1	0	0	0	0	0	1	1	R3	Reset register	W								CRES
0	1	0	0	0	0	1	0	0	R4										
0	1	0	0	0	0	1	0	1	R5	Data access control register	R/W	BMD	BSTR		WAS		INC	XDIR	YDIR
0	1	0	0	0	0	1	1	0	R6	X address register	R/W	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
0	1	0	0	0	0	1	1	1	R7	Y address register	R/W	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	1	0	0	0	1	0	0	0	R8	MIN. ·X address register	R/W	XMIN7	XMIN6	XMIN5	XMIN4	XMIN3	XMIN2	XMIN1	XMIN0
0	1	0	0	0	1	0	0	1	R9	MAX. ·X address register	R/W	XMAX7	XMAX6	XMAX5	XMAX4	XMAX3	XMAX2	XMAX1	XMAX0
0	1	0	0	0	1	0	1	0	R10	MIN. ·Y address register	R/W	YMIN7	YMIN6	YMIN5	YMIN4	YMIN3	YMIN2	YMIN1	YMIN0
0	1	0	0	0	1	0	1	1	R11	MAX. ·Y address register	R/W	YMAX7	YMAX6	YMAX5	YMAX4	YMAX3	YMAX2	YMAX1	YMAX0
0	1	0	0	0	1	1	0	0	R12	Display memory register	W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	0	1	R13										
0	1	0	0	0	1	1	1	0	R14										
0	1	0	0	0	1	1	1	1	R15	Scroll area start line register	R/W	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
0	1	0	0	1	0	0	0	0	R16	Scroll area line count register	R/W	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0
0	1	0	0	1	0	0	0	1	R17	Scroll step count register	R/W	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
0	1	0	0	1	0	0	1	0	R18										
0	1	0	0	1	0	0	1	1	R19	Partial off area color register	R/W						PGR	PGG	PGB
0	1	0	0	1	0	1	0	0	R20	Partial 1 display area start line register	R/W	P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
0	1	0	0	1	0	1	0	1	R21	Partial 2 display area start line register	R/W	P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0
0	1	0	0	1	0	1	1	0	R22	Partial 1 display area line count register	R/W	P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
0	1	0	0	1	0	1	1	1	R23	Partial 2 display area line count register	R/W	P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
0	1	0	0	1	1	0	0	0	R24										
0	1	0	0	1	1	0	0	1	R25	Power supply control register 1	R/W		BGRS	VCE	VCD2	PVCOM	RGONG	RGONP	DCON
0	1	0	0	1	1	0	1	0	R26	Power supply control register 2	R/W							VCD12	VCD11
0	1	0	0	1	1	0	1	1	R27										
0	1	0	0	1	1	1	0	0	R28										
0	1	0	0	1	1	1	0	1	R29	VCOM output center value setting register	R/W	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0
0	1	0	0	1	1	1	1	0	R30	Output stage capacity setting register	R/W	BPL	CI2	CI1	CI0	VCOMC	SF2	SF1	SF0
0	1	0	0	1	1	1	1	1	R31	γ-reference-voltage generator setting register	R/W	WHP	WI2	WI1	WI0	BHP	BI2	BI1	BI0
0	1	0	1	0	0	0	0	0	R32										
0	1	0	1	0	0	0	0	1	R33										
0	1	0	1	0	0	0	1	0	R34										
0	1	0	1	0	0	0	1	1	R35										
0	1	0	1	0	0	1	0	0	R36	γ-contrast value setting register 1	R/W	GPH7	GPH6	GPH5	GPH4	GPH3	GPH2	GPH1	GPH0
0	1	0	1	0	0	1	0	1	R37	γ-contrast value setting register 2	R/W	GNH7	GNH6	GNH5	GNH4	GNH3	GNH2	GNH1	GNH0
0	1	0	1	0	0	1	1	0	R38	γ-contrast value setting register 3	R/W	GPL7	GPL6	GPL5	GPL4	GPL3	GPL2	GPL1	GPL0
0	1	0	1	0	0	1	1	1	R39	γ-contrast value setting register 4	R/W	GNL7	GNL6	GNL5	GNL4	GNL3	GNL2	GNL1	GNL0
0	1	0	1	0	1	0	0	0	R40	Pre-charge direction setting data register	R/W	RDTP3	RDTP2	RDTP1	RDTP0	RDTN3	RDTN2	RDTN1	RDTN0
0	1	0	1	0	1	0	0	1	R41										
0	1	0	1	0	1	0	1	0	R42	γ-correction input disconnect register	R/W								GHSW
0	1	0	1	0	1	0	1	1	R43										
0	1	0	1	0	1	1	0	0	R44										
0	1	0	1	0	1	1	0	1	R45	Calibration register	R/W								OC
0	1	0	1	0	1	1	1	0	R46	Pre-charge period supplement pulse setting register	R/W		PLIM6	PLIM5	PLIM4	PLIM3	PLIM2	PLIM1	PLIM0
0	1	0	1	0	1	1	1	1	R47										
0	1	0	1	1	0	0	0	0	R48										
0	1	0	1	1	0	0	0	1	R49	Output port register	R/W	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	1	0	1	1	0	0	1	0	R50	Input port register	R					IP3	IP2	IP1	IP0
0	1	0	1	1	0	0	1	1	R51										
0	1	0	1	1	0	1	0	0	R52										
0	1	0	1	1	0	1	0	1	R53										
0	1	0	1	1	0	1	1	0	R54										
0	1	0	1	1	0	1	1	1	R55										
0	1	0	1	1	1	0	0	0	R56										
0	1	0	1	1	1	0	0	1	R57										
0	1	0	1	1	1	0	1	0	R58										
0	1	0	1	1	1	0	1	1	R59										
0	1	0	1	1	1	1	0	0	R60										
0	1	0	1	1	1	1	0	1	R61										
0	1	0	1	1	1	1	1	0	R62										
0	1	0	1	1	1	1	1	1	R63										
0	1	0	1	0	1	1	0	1	R114	Interface operating voltage setting register	R/W							RTSC1	RTSC0
0	1	0	1	0	1	1	1	0	R115	Internal logic operating voltage setting register	R/W							RTSL1	RTSL0

Remark : These registers cannot be used.

Cautions 1. If a write-only register is read, invalid data will be output.

2. A low level is output when an unused register is read.

7.2 Command Explanation

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Resistor	Bit	Symbol	Function
R0	D_7	DISP1	This command performs the same output as when all data is 1, independently of the internal RAM data (white display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 1. DISP1 takes precedence over DISP0. When DISP1 = H, DISP0 = H is ignored.
	D_6	DISP0	This command performs the same output as when all data is 0, independently of the internal RAM data (black display in the case of normally white). This command is executed, after it has been transferred, when the next line is output. 0: Normal operation 1: Ignores data of RAM and outputs all data as 0.
	D_5	ADC	Column address direction This command can be used to select the direction of source driver output. For more detail, refer to **5.2.3 Column address circuit**
★	D_4	DTY	This pin selects the partial function. When partial display mode is selected, partial off area color is displayed by setting partial off area color register (R19). The power consumption cannot be reduced with the partial function. To reduce the power consumption, select the 8-color mode. This command is executed following transfer from the time the next line data is output. 0: Normal display mode 1: Partial display mode
	D_3	STBY	This bit selects the stand-by function. When the stand-by function is selected, a display OFF operation is executed and the amplifiers at each output stage and the operation of internal oscillation circuit are stopped. However, stand-by control cannot be performed for the gate IC (μPD161640) connected to μPD161622 and the power-supply IC (μPD161660). Therefore, after executing the stand-by function using this bit, set both the regulator for the gate IC and power-supply IC to off and set the DC/DC converter to OFF. For the sequence, refer to the preliminary product information machine of the μPD161660. Note that when releasing stand-by, perform the opposite operation, i.e., after setting the DC/DC converter to ON and setting the regulators of the gate IC and power-supply IC to ON, execute the normal operation command. 0: Normal operation 1: Stand-by function (display read off from RAM, stop both OSC and VCOM, display OFF = entire data is output as 1)
	D_2	COLOR	This pin switches the 65,000-color mode and the 8-color mode. When the 8-color mode is selected, low power supply can be selected in order to stop the amplifier at each output stage. In the 8-color mode, the value of the MSB of the internal RAM data is used as the color data. This command is executed following transfer from the time the next line data is output. 0: 65,000-color mode (16 bits/pixels) 1: 8-color mode (3 bits/pixels)

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Resistor	Bit	Symbol	Function
R0	D_1	LPM	This bit is used when setting the gate IC (μ PD161640) and power-supply IC (μ PD161660) to the low-power mode. When the low-power mode is selected, the LPMG pin and the LPMP pin signals change from low to high (output changes immediately following command execution.). The LPMG pin must be connected to the LPM pin of the gate IC, and the LPMP pin must be connected to the LPM pin of the power-supply IC. 0: Normal 1: Low power mode
	D_0	GSM	Sets output of the gate scanning signal during partial display. When 1 is selected, gate scanning of the line set in the partial non-display area is stopped. 0: Normal mode 1: Stops gate scanning in partial non-display area
R1	D_5	VSEL	Sets the potential of the pre-charge output of the LCD driver. The maximum/minimum output potential of the pre-charge output is: 0: Power supply voltage (outputs V_S and V_{SS}) 1: Maximum output level of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL) IF VSEL = 0, V_S or V_{SS} is automatically output as the pre-charge output.
	D_4	GSEL	Sets the maximum/minimum output voltage of the γ-correction resistor. If the internal γ-output adjustment circuit is selected, the maximum/minimum output potential of the γ-correction resistor is: 0: Supply voltage (outputs V_S and V_{SS}). 1: Voltage of internal γ-output adjustment circuit (uses VPH, VNH, VPL, VNL) 8-color mode (3 bits/pixels)
	D_1	LTS	Selects set time of calibration. The calibration function adjusts the frame frequency by setting time of one line. This command can select the set time of a line from the following: 0: 1 line time = t_{cal} 1: 1 line time = t_{cal} x 2 (t_{cal}: Calibration set time1 = 1 ÷ Frame frequency ÷ Number of displayed lines)
	D_0	INV	This bit selects between the line inversion function and the frame inversion function. The mode selected by this command is executed from the start of the next scan after the gate scan in progress when this command was executed has completed 176 lines. When the reset command is input, the INV register is initialized. 0: Line inversion with same line. 0: Line inversion 1: Frame inversion
R3	D_0	CRES	Command reset function. Be sure to execute this bit after power ON. Command reset automatically clears this bit following execution (CRES = 01H). Therefore, it is not necessary to set 0 (select normal operation) again by software. Moreover, since the time required for the value of this bit to change (1 → 0) following command reset execution is extremely short, it is not necessary to secure time until the next command is set following command reset setting. 0: Normal operation 1: Command reset

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Resistor	Bit	Symbol	Function
R5	D_7	BMD	Sets the bus width when the parallel interface is used. 0: 16-bit data bus 1: 8-bit data bus This command is invalid when the serial interface is used.
	D_6	BSTR	Sets the write mode for writing data to the display RAM. If the high-speed RAM write mode is selected, data is written to the display RAM in 64-bit units inside the μPD161622. When selecting the high-speed RAM write mode, be sure to write data to the display RAM in 64-bit units. 0: Normal write mode (16-bit access) 1: High-speed RAM write mode (64-bit access)
	D_4	WAS	Window access mode setting When the window access mode is set, the address is incremented/decremented only in the range set by the MIN. ·X address setting register (R8), MAX. ·X address setting register (R9), MIN. ·Y address setting register (R10), and MAX. ·Y address setting register (R11). 0: Normal operation 1: Window access mode
	D_2	INC	Selects the direction in which the display RAM address is to be incremented/decremented. Whether the X address and Y address are incremented or decremented is specified by XDIR (R5: D_1) and YDIR (R5: D_0), respectively. 0: Access in X address direction 1: Access in Y address direction
	D_1	XDIR	Specifies whether the display RAM address is incremented or decremented in the X address direction. 0: Increments X address 1: Decrements X address
	D_0	YDIR	Specifies whether the display RAM address is incremented or decremented in the Y address direction. 0: X address increment 1: X address decrement
R6	D_7 to D_0	XAn	This register sets the X address of the display RAM. Set a value between 00H and 83H.
R7	D_7 to D_0	YAn	This register sets the Y address of the display RAM. Set a value between 00H and AFH.
R8	D_7 to D_0	XMINn	Sets the minimum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MAX. ·X address register (R9), and then initialized to the address value set by this command. (R5: XDIR = 0) Set a value between 00H to 82H.
R9	D_7 to D_0	XMAXn	Sets the maximum value of the X address in the window access mode. The X address is incremented up to the maximum value set by the MIN. ·X address register (R8), and then initialized to the address value set by this command. (R5: XDIR = 0) Set a value between 01H to 83H.
★ R10	D_7 to D_0	YMINn	Sets the minimum value of the T address in the window access mode. The Y address is incremented up to the maximum value set by the MAX. ·Y address register (R11), and then initialized to the address value set by this command. (R5: YDIR = 0) Set a value between 00H to AEH.

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Resistor	Bit	Symbol	Function
R11	D_7 to D_0	YMAXn	Sets the maximum value of the Y address in the window access mode. The Y address is incremented up to the address value set by this command, and then initialized to the minimum address value set by the MIN. Y address register (R10) (R5: YDIR = 0) Set a value between 01H to AFH.
R12	D_7 to D_0	D_n	These bits are used for reading/writing data from/to display memory (internal RAM).
R15	D_7 to D_0	SSLn	Scroll area start line register (00H to AFH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by this command.
R16	D_7 to D_0	SAWn	Scroll area line count register (00H to AFH) When the screen is scrolled, the screen of the number of lines set by this command is scrolled up by the number of steps set by the scroll step count register (R17), starting from the line set by the scroll area start line register (R15)
R17	D_7 to D_0	SSTn	Scroll step count register (00H to AFH) When the screen is scrolled, the screen of the number of lines set by the scroll area line count register (R16) and the scroll step count register (R17) is scrolled up by the number of steps set by this command. Note that because this command is invalid in the partial display mode, the scroll function cannot be used.
R19	D_2	PGR	Partial off area color register Sets the color of the screen other than the partial display area during partial display (R0: DTY = 1). One of eight colors can be selected (RGB: 1 bit each) as the off color. The relationship between each color data and the bits of this register is as follows. This relationship is not dependent upon the value of ADC. PGR: R OFF= 0, ON = 1 PGG: G OFF= 0, ON = 1 PGB: B OFF= 0, ON = 1
	D_1	PGG	
	D_0	PGB	
R20	D_7 to D_0	P1SLn	Partial 1 display area start line register (00H to AFH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 1 display area line count register (R22) is the partial 1 display area.
R21	D_7 to D_0	P2SLn	Partial 2 display area start line register (00H to AFH) During partial display (R0: DTY = 1), the area starting from the line set by this command and ending as set by the partial 2 display area line count register (R23) is the partial 2 display area.
R22	D_7 to D_0	P1AWn	Partial 1 display area line count register (00H to AFH) An area starting from the line set by the partial 1 display area start register (R20) and ending as set by this command is the partial 1 display area. If this register is 0, the values of the partial 2 display area start line register (R29) and the partial 2 display area line count register (R31) are not valid.
R23	D_7 to D_0	P2AWn	Partial 2 display area line count register (00H to AFH) An area starting from the line set by the partial 2 display area start register (R21) and ending as set by this command is the partial 2 display area. If the partial 1 display area line count register is 0, the values of the partial 2 display area start line register (R21) and partial 2 display area line count register (R23) are not valid.

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Resistor	Bit	Symbol	Function
R25	D_6	BGRS	This pin selects whether to use the internal power supply or an external power supply (input from the BRGIN pin) for generation the common center voltage output from the VCOM pin. 0: The internal power-supply is selected as the VCOM power supply 1: Input from the external power-supply BGRIN is selected as the VCOM power supply
	D_5	VCE	Selects the V_O output level of the power-supply IC (μPD161660). The V_{CE} pin of the μPD161622 and the V_{CE} pin of the power-supply IC must be connected. 0: The Vo high-level booster voltage level is V_{DD1} minus 1 level 1: The Vo high-level booster voltage level is the same level as V_{DD1}
	D_4	VCD2	Selects the V_{DD2} output level of the power-supply IC (μPD161660). The V_{CD2} pin of the μPD161622 and the V_{CD2} pin of the power-supply IC must be connected. 0: $V_{DD2} = V_{DC} \times 2$ 1: $V_{DD2} = V_{CD} \times 3$
	D_3	PVCOM	Sets the pre-charge time of a 1-line output period. 0: VBGR (3.0 V TYP.) 1: V_S
	D_2	RGONG	Switches the internal regulator of the gate IC (μPD161640) ON/OFF. When OFF is selected, a low level is output from the RGONG pin, and when ON is selected, a high level is output from the RGONG pin. The RGONG pin of the μPD161622 and the RGON pin of the gate IC must be connected. 0: Regulators of gate driver (V_B) are OFF 1: Regulators of gate driver (V_B) are ON
	D_1	RGONP	Switches the internal DC/DC converter of the power-supply IC (μPD161660) ON/OFF. When OFF is selected, a low level is output from the RGONP pin, and when ON is selected, a high level is output from the RGONP pin. The RGONP pin of the μPD161622 and the RGON pin of the power-supply IC must be connected. 0: Regulators of power-supply IC (V_T, V_S) are OFF 1: Regulators of power-supply IC (V_T, V_S) are ON
	D_0	DCON	Switches the internal DC/DC converter of the power-supply IC (μPD161660) ON/OFF. When OFF is selected, a low level is output from the DCON pin, and when ON is selected, a high level is output from the DCON pin. The DCON pin of this IC and the DCON pin of the power-supply IC must be connected. 0: DC/DC converter is OFF 1: DC/DC converter is ON
R26	D_1	V_{CD12}	Performs booster control for the DC/DC converter in the power-supply IC (μPD161660) The data set with this bit is output from the V_{CD11} pin and the V_{CD12} pin. The V_{CD11} pin and V_{CD12} pin of μPD161622 must be connected to the V_{CD11} pin and the V_{CD12} pin of the power-supply IC.
	D_0	V_{CD11}	V_{CD12}, V_{CD11} = 0, 0: $V_{DD1} = V_{DC} \times 4$ = 0, 1: $V_{DD1} = V_{DC} \times 5$ = 1, 0: $V_{DD1} = V_{DC} \times 6$ = 1, 1: $V_{DD1} = V_{DC} \times 7$

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<table>
<tr><th>Resistor</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>R29</td><td>D_7 to D_0</td><td>EVn</td><td>Sets the D/A converter circuit used to adjust the voltage of the reference voltage generator circuit (VBGR) input to the voltage regulator that sets the center value of the panel common drive output. The D/A converter divides the constant voltage generated by the reference voltage generator (VBGR) by 256, and one level can be selected between VBGR and V_{SS} by setting this command.
For more detail, refer to 5.5 Common Adjustment Circuit and 5.8 D/A Converter Circuit.</td></tr>
<tr><td rowspan="4">R30</td><td>D_7</td><td>BPL</td><td>Switched the capacity of the γ-correction circuit reference voltage generation amplifiers on the side not being used (VPH, VPL, VNH, VNL) to the minimum value based on the polarity inversion timing in order to reduce the current consumption.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal
1: Reference voltage generation amplifier capacity switch drive</td></tr>
<tr><td>D_6 to D_4</td><td>CIn</td><td>Sets the bias current of the amplifier for setting the panel's COMMON drive waveform center value (VCOM), as shown in the table below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>CI2</th><th>CI1</th><th>CI0</th><th>VCOM Center Value Setting Amplifier Bias Current Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
<tr><td>D_3</td><td>VCOMC</td><td>Selects whether to use the amplifier for setting the panel's COMMON drive waveform center value (VCOM) or not.
This amplifier can be used under conditions such as when an external COMMON drive circuit is being used.
0: VCOM amplifier operating
1: VCOM amplifier stopped</td></tr>
<tr><td>D_2 to D_0</td><td>SFn</td><td>Sets the capacity of the source output (S_1 to S_{396}), as shown in the table below.
Determine the output capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>SF2</th><th>SF1</th><th>SF0</th><th>Source Output Bias Current Value</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.15 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.25 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.10 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0.30 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0.40 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
</table></td></tr>
</table>

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<table>
<tr><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="5">R31</td><td>D_7</td><td>WHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output stage capacity: twice that of normal mode)</td></tr>
<tr><td>D_6 to D_4</td><td>WIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the white level of the positive-polarity and negative-polarity sides (when VPL and VNL are normally white), as shown below.
<table>
<tr><th>WI2</th><th>WI1</th><th>WI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
<tr><td>D_3</td><td>BHP</td><td>Sets the output mode of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
0: Normal mode
1: High-power mode (output stage capacity: twice that of normal mode)</td></tr>
<tr><td>D_2 to D_0</td><td>BIn</td><td>Sets the output bias current of the reference voltage generator amplifier for setting the black level of the positive-polarity and negative-polarity sides (when VPH and VNH are normally white), as shown below.
Determine the amplifier capacity after sufficient evaluation with the actual TFT panel to be used.
<table>
<tr><th>BI2</th><th>BI1</th><th>BI0</th><th>Amplifier Bias Current</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0.20 μA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0.50 μA</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0.10 μA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0.05 μA</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.00 μA</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.50 μA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>2.00 μA</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>3.00 μA</td></tr>
</table></td></tr>
<tr><td>R36</td><td>D_7 to D_0</td><td>GPH_n</td><td>Sets the voltage value of the black level of positive polarity.
For more det020ail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R37</td><td>D_7 to D_0</td><td>GNH_n</td><td>Sets the voltage value of the white level of negative polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R38</td><td>D_7 to D_0</td><td>GPLn</td><td>Sets the voltage value of the white level of positive polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
<tr><td>R39</td><td>D_7 to D_0</td><td>GNLn</td><td>Sets the voltage value of the white level of positive polarity.
For more detail, refer to 5.9 γ-Curve Correction Power Supply Circuit.</td></tr>
</table>

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<table>
<tr><th></th><th>Register</th><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td></td><td>R40</td><td>D_7 to D_4</td><td>RDTPn</td><td>Sets the data value at which the pre-charge direction is switched during positive-polarity drive.
The value set to RDTPn corresponds to the higher 4bits of display RAM data DB_n (6 bits for each of RFB), as shown below.
<table><tr><th></th><th>RDTP3</th><th>RDTP2</th><th>RDTP1</th><th>RDTP0</th></tr><tr><td>Dot 1 (R)</td><td>D_{17}</td><td>D_{16}</td><td>D_{15}</td><td>D_{14}</td></tr><tr><td>Dot 2 (G)</td><td>D_{11}</td><td>D_{10}</td><td>D_9</td><td>D_8</td></tr><tr><td>Dot 3 (B)</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td></tr></table></td></tr>
<tr><td></td><td></td><td>D_3 to D_0</td><td>RDTNn</td><td>Sets the data value at which the pre-charge direction is switched during negative-polarity drive.
The value set to RDTNn corresponds to the higher 4 bits of display RAM data DB_n (6 bits for each of RGB), as shown below.
<table><tr><th></th><th>RDTN3</th><th>RDTN2</th><th>RDTN1</th><th>RDTN0</th></tr><tr><td>Dot 1 (R)</td><td>D_{17}</td><td>D_{16}</td><td>D_{15}</td><td>D_{14}</td></tr><tr><td>Dot 2 (G)</td><td>D_{11}</td><td>D_{10}</td><td>D_9</td><td>D_8</td></tr><tr><td>Dot 3 (B)</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td></tr></table></td></tr>
<tr><td>★</td><td>R42</td><td>D_0</td><td>GHSW</td><td>Controls the γ-correction voltage input pins (V_0 to V_5) and the switch for connecting the μPD161622 internal γ-correction resistor.
0: Switch OFF (disconnected)
1: Switch ON (connected)</td></tr>
<tr><td>★</td><td>R45</td><td>D_0</td><td>OC</td><td>This bit is used for calibration.
The time from calibration start command execution until calibration stop command execution becomes the time for 1 line.
0: Calibration stop
1: Calibration start</td></tr>
<tr><td></td><td>R46</td><td>D_7 to D_0</td><td>PLIMn</td><td>Set the pre-charge time of a 1-line output period.
The number of clocks set in this register + 2 CLK (1/f_{OSC}) becomes the pre-charge time when one line is driven.
For details, refer to 5.4.1 Drive timing</td></tr>
<tr><td></td><td>R49</td><td>D_7 to D_0</td><td>OPn</td><td>Output port (OP7 to OP0) write
When after the output port register (R49) is specified in the index register, writing to the γ-correction input disconnect register (R42) is performed, the values written to the OP7 to OP0 pins are output.</td></tr>
<tr><td></td><td>R50</td><td>D_3 to D_0</td><td>IPn</td><td>Input port (IP3 to IP0) read
To read the IP3 to IP0 inputs, use the following method.
<Read sequence>
<1> Specify the input port register (R50) from the index register.
↓
<2> Execute input port register (R50) read.</td></tr>
</table>

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	Register	Bit	Symbol	Function
★	R114	D_1, D_0	RTSCn	Selects the optimum internal circuit operation based on the operating voltage of the interface circuits. The following settings are recommended based on this register. RTSC1: 1, RTSC0: 1 **Caution Always set this register and internal logic operating voltage setting register (R115) to the same value.**
★	R115	D_1, D_0	RTSLn	Selects the optimum internal circuit operation based on the operating voltage of the internal logic circuits. The following settings are recommended based on this register. RTSC1: 1, RTSC0: 1 **Caution Always set this register and interface operating voltage setting register (R114) to the same value.**

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_S	–0.5 to +6.5	V
Power supply voltage	V_{CC1}	–0.5 to +4.0	V
Power supply voltage	V_{CC2}	–0.5 to V_{CC1} + 0.5	V
Power supply voltage for γ-curve correction	V_1 to V_5	–0.5 to V_S + 0.5	V
Input voltage	V_I	–0.5 to V_{CC1} + 0.5	V
Input current	I_I	±10	mA
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_S	4.3	5.0	5.5	V
	V_{CC1}	2.5	2.7	3.6	V
	V_{CC2}	1.7	1.8	V_{CC1}	V
Input voltage	V_{I1} **Note1**	0		V_{CC1}	V
	V_{I2} **Note2**	0		V_{CC2}	V

Notes 1. Pins of V_{CC1} power-supply system: PSX, C86, T_{OUT0} to T_{OUT15}, IP_0 to IP_3, OP_0 to OP_7, LPMG, LPMP, GOE_1, GOE_2, GSTB, GCLK, DCON, RGONP, RGONG, V_{CD11}, V_{CD12}, V_{CD2}, V_{CE}, OSC_{SEL}, $TEST_{IN}$, TSTRTST, TSTVIHL

2. Pins of V_{CC2} power-supply system: /CS, /RD(E), /WR(R,/W), D_0 to D_5, D_6(SCL), D_7(SI), RS, /RESET, OSC_{IN}

Electrical Specifications (Unless Otherwise Specified, T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 V to V_{CC1}, V_S = 4.3 to 5.5 V)

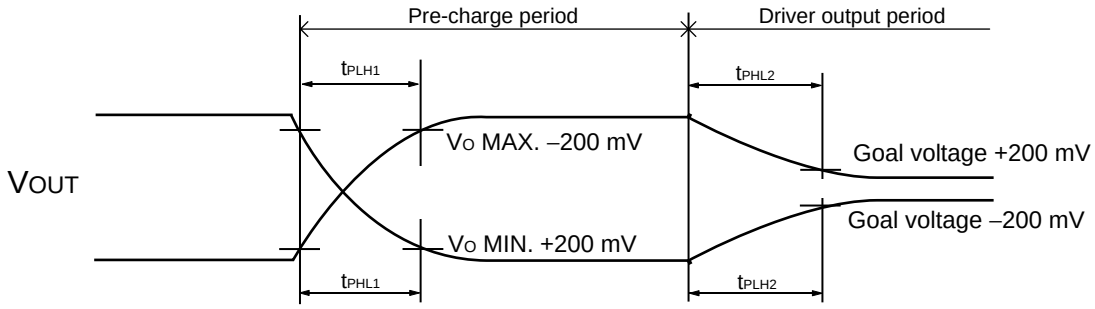
	Parameter	Symbol	Condition	Specification			Unit
				MIN.	TYP.[Note1]	MAX.	
	High level input voltage	V_{IH1}	V_{CC1}	0.8 V_{CC1}			V
		V_{IH2}	V_{CC2}	0.8 V_{CC2}			V
	Low level input voltage	V_{IL1}	V_{CC1}			0.2 V_{CC1}	V
		V_{IL2}	V_{CC2}			0.2 V_{CC2}	V
	High level output voltage	V_{OH1}	V_{CC1}, I_{OUT} = –100 μA	0.9 V_{CC1}			V
		V_{OH2}	V_{CC2}, I_{OUT} = –1 mA	0.8 V_{CC2}			V
		V_{OH3}	VCOUT1, VCOUT2, I_{OUT} = –100 μA	0.9 V_S			V
	Low level output voltage	V_{OL1}	V_{CC1}, I_{OUT} = 100 μA			0.1 V_{CC1}	V
		V_{OL2}	V_{CC2}, I_{OUT} = 1 mA			0.2 V_{CC2}	V
		V_{OL3}	VCOUT1, VCOUT2, I_{OUT} = 100 μA			0.1 V_S	V
	VCOM output voltage	V_{COMH}	I_{SOURCE} = 100 μA	VCOM – 0.3			mV
		V_{COML}	I_{SINK} = –100 μA			VCOM + 0.3	mV
	High level input current	I_{IH1}	Except D_0 to D_{15}			1	μA
	Low level input current	I_{IL1}	Except D_0 to D_{15}			–1	μA
	High level leakage current	I_{LIH}	D_0 to D_{15}			10	μA
	Low level leakage current	I_{LIL}	D_0 to D_{15}			–10	μA
★	High level driver output current	I_{VOH}	V_X = 3.5 V, V_{OUT} = 4.5 V, V_S = 5.0 V [Note2]	–85			μA
★	Low level driver output current	I_{VOL}	V_X = 1.5 V, V_{OUT} = 0.5 V, V_S = 5.0 V [Note2]			30	μA
	VCOM common output voltage fluctuation parameter	ΔV_{COM}		–10		10	%
	Current consumption	I_{CC1}	V_{CC1} (when non-access CPU)		140	240	μA
		I_{CC2}	V_{CC2} (when non-access CPU)		0.2	5	μA
		I_{STBY}	V_{CC1} (stand-by mode)		1	10	μA
		I_S	V_S (65,000-color mode)[Note3]		600	1000	μA
★			V_S (8-color mode) [Note3]		45	100	μA
★	Driver output Current (pre-charge)	I_{VOH}	V_S = 5.0 V, V_{OUT} = V_S – 0.1 V [Note2]		–0.14	–0.07	mA
		I_{VOL}	V_S = 5.0 V, V_{OUT} = V_S + 0.1 V [Note2]	0.1	0.25		mA
★	Output voltage deviation	ΔV_{O1}	V_{OUT} = 1.3 V to (V_S – 1.3 V) [Note2]	–20		20	mV
		ΔV_{O2}	V_{OUT} = 0.3 to 1.3 V[Note2], (V_S – 1.3 V) to (V_S – 0.3 V)	–30		30	mV

Notes 1. TYP. values are reference values when T_A = 25°C

2. V_X refers to the output voltage of analog output pins S_1 to S_{240}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{240}

3. Frame frequency, line inversion mode selection, dot checkerboard input pattern, no load

Switching characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 V to V_{CC1}, V_S = 5.0 V)

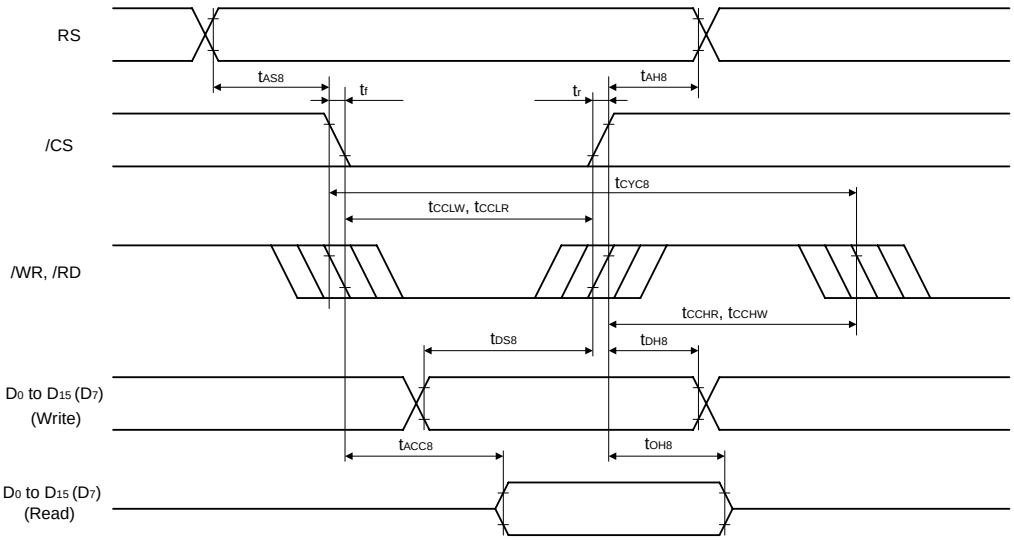


Parameter	Symbol	Condition		MIN.	TYP.[Note]	MAX.	Unit
Driver output delay time 1 (pre-charge period)	t_{PLH1}	V_S = 5.0 V, 4 kΩ +27 pF	V_O MAX. –200 mV			40	μs
	t_{PHL1}		V_O MIN. +100 mV			70	μs
Driver output delay time 2 (driver output period)	t_{PLH2}		Pre-charge completed → goal voltage –200 mV			50	μs
	t_{PHL2}					60	μs

Note TYP. values are reference values when T_A = 25°C.

AC Characteristics (Unless Otherwise Specified, T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 V to V_{CC1})

(a) i80 series CPU interface



When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$ (normal write mode, R114 and R115 = 03H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
Data setup time	t_{DS8}	D_0 to D_{15}	60			ns
Data hold time	t_{DH8}	D_0 to D_{15}	0			ns
/RD access time	t_{ACC8}	D_0 to D_{15}, C_L = 100 pF			110	ns
★ Output disable time	t_{OH8}	D_0 to D_{15}, C_L = 5 pF	10		100	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 to 2.5 V, $V_{CC1} \geq V_{CC2}$ (normal write mode, R114 and R115 = 03H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		333			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	60			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	160			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	100			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	140			ns
Data setup time	t_{DS8}	D_0 to D_{15}	60			ns
Data hold time	t_{DH8}	D_0 to D_{15}	0			ns
/RD access time	t_{ACC8}	D_0 to D_{15}, C_L = 100 pF			150	ns
★ Output disable time	t_{OH8}	D_0 to D_{15}, C_L = 5 pF	10		150	ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$ (high-speed RAM write mode, valid only for writing data R114 and R115 = 03H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		62			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	35			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	25			ns
Data setup time	t_{DS8}	D_0 to D_{15}	25			ns
Data hold time	t_{DH8}	D_0 to D_{15}	0			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 to 2.5 V, $V_{CC1} \geq V_{CC2}$, (high-speed RAM write mode, valid only for writing data, R114 and R115 = 03H)

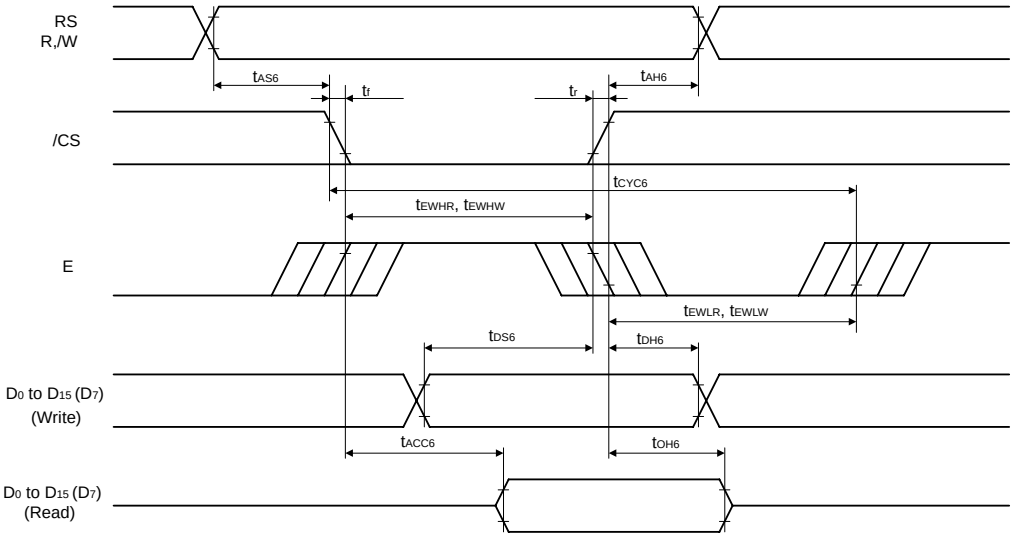
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		83			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	35			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	30			ns
Data setup time	t_{DS8}	D_0 to D_{15}	30			ns
Data hold time	t_{DH8}	D_0 to D_{15}	0			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The input signal's rise/fall times (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

(b) M68 series CPU interface



When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$ (normal mode, R114 and R115 = 03H)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		250			ns
Data setup time		t_{DS6}	D_0 to D_{15}	80			ns
Data hold time		t_{DH6}	D_0 to D_{15}	0			ns
Access time		t_{ACC6}	D_0 to D_{15}, C_L = 100 pF			110	ns
★ Output disable time		t_{OH6}	D_0 to D_{15}, C_L = 5 pF	10		100	ns
Enable high pulse width	Read	t_{EWHR}	E	140			ns
	Write	t_{EWHW}	E	120			ns
Enable low pulse width	Read	t_{EWLR}	E	80			ns
	Write	t_{EWLW}	E	60			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 to 2.5 V, $V_{CC1} \geq V_{CC2}$ (normal mode, R114 and R115 = 03H)

Parameter		Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time		t_{AH6}	RS	0			ns
Address setup time		t_{AS6}	RS	0			ns
System cycle time		t_{CYC6}		333			ns
Data setup time		t_{DS6}	D_0 to D_{15}	100			ns
Data hold time		t_{DH6}	D_0 to D_{15}	0			ns
Access time		t_{ACC6}	D_0 to D_{15}, C_L = 100 pF			150	ns
★ Output disable time		t_{OH6}	D_0 to D_{15}, C_L = 5 pF	10		150	ns
Enable high pulse width	Read	t_{EWHR}	E	160			ns
	Write	t_{EWHW}	E	120			ns
Enable low pulse width	Read	t_{EWLR}	E	140			ns
	Write	t_{EWLW}	E	100			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$ (high-speed RAM write mode, valid only for writing data, R114 and R115 = 03H)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	0			ns
Address setup time	t_{AS6}	RS	0			ns
System cycle time	t_{CYC6}		62			ns
Data setup time	t_{DS6}	D_0 to D_{15}	0			ns
Data hold time	t_{DH6}	D_0 to D_{15}	0			ns
Enable high pulse width	t_{EWHR}	E	35			ns
Enable low pulse width	t_{EWLR}	E	20			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{CC2}.

When V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 to 2.5 V, $V_{CC1} \geq V_{CC2}$ (high-speed RAM write mode, valid only for writing data)

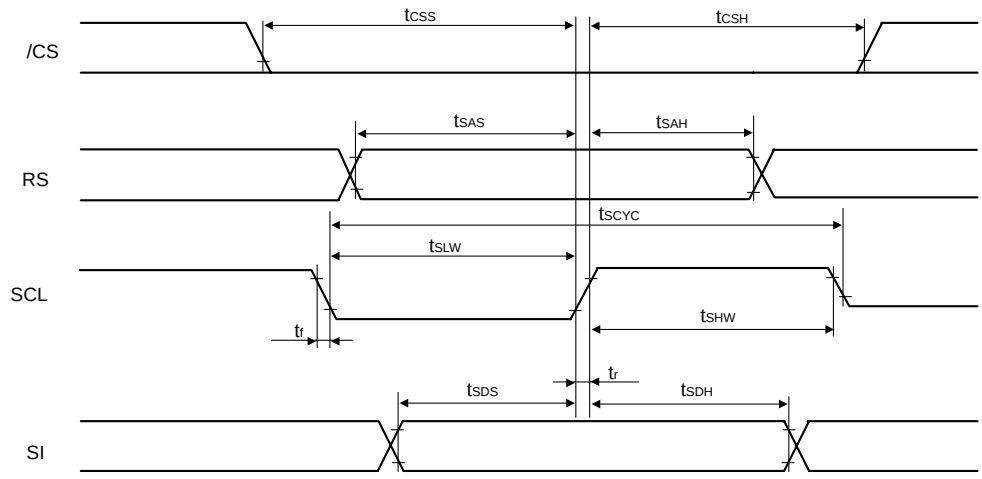
Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Address hold time	t_{AH6}	RS	0			ns
Address setup time	t_{AS6}	RS	0			ns
System cycle time	t_{CYC6}		83			ns
Data setup time	t_{DS6}	D_0 to D_{15}	0			ns
Data hold time	t_{DH6}	D_0 to D_{15}	0			ns
Enable high pulse width	t_{EWHR}	E	40			ns
Enable low pulse width	t_{EWLR}	E	30			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times (t_r and t_f) of input signals are rated at 15 ns or less. When using a fast system cycle time, the rated value range is either $(t_r + t_f) < (t_{CYC6} - t_{EWLR} - t_{EWHR})$ or $(t_r + t_f) < (t_{CYC6} - t_{EWLW} - t_{EWHW})$.

2. All timing is rated based on 20 to 80% of V_{CC2}.

(c) Serial interface



V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 1.7 to 2.5 V, $V_{CC1} \geq V_{CC2}$

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	250			ns
SCL high-level pulse width	t_{SHW}	SCL	100			ns
SCL low-level pulse width	t_{SLW}	SCL	100			ns
Address hold time	t_{SAH}	RS	150			ns
Address setup time	t_{SAS}	RS	150			ns
Data setup time	t_{SDS}	SI	100			ns
Data hold time	t_{SDH}	SI	100			ns
CS - SCL time	t_{CSS}	/CS	150			ns
	t_{CSH}	/CS	150			ns

Note TYP. values are reference values when T_A = 25°C.

V_{CC1} = 2.5 to 3.6 V, V_{CC2} = 2.5 to 3.6 V, $V_{CC1} \geq V_{CC2}$

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Serial clock cycle	t_{SCYC}	SCL	150			ns
SCL high-level pulse width	t_{SHW}	SCL	60			ns
SCL low-level pulse width	t_{SLW}	SCL	60			ns
Address hold time	t_{SAH}	RS	90			ns
Address setup time	t_{SAS}	RS	90			ns
Data setup time	t_{SDS}	SI	60			ns
Data hold time	t_{SDH}	SI	60			ns
CS - SCL time	t_{CSS}	/CS	90			ns
	t_{CSH}	/CS	90			ns

Note TYP. values are reference values when T_A = 25°C.

Remarks 1. The rise and fall times of input signal (t_r and t_f) are rated as 15 ns or less.

2. All timing is rated based on 20 to 80% of V_{CC2}.

(e) Common

	Parameter	Symbol	Condition	MIN.	TYP.[Note1]	MAX.	Unit
★	Oscillation frequency	f_{OSC1}	Internal oscillator (R_{SEL} = L)	250	450	750	kHz
		f_{OSC2}	External resistance connection oscillator (R_{SEL} = H), R = 51 kΩ [Note2]		450		kHz
★	Calibration setting time (frame frequency)	t_{cal} (f_{FRAME0})	**Note3**	14.6 (385.2)	83 (68.1)	552 (10.2)	μs (Hz)
	Frame frequency	f_{FRAME1}	Uncalibrated	38	70	115	Hz
		f_{FRAME2}	Calibrated [Note4]	72	80	88	Hz
		f_{FRAME3}	Calibrated [Note5]	77	80	83	Hz
	Reset pulse width at power on	t_{VR}	V_{CC1} or V_{CC2} to /RESET↑	100			ns
	Reset pulse width	t_{RW}		100			ns
	Reset time	t_R	/RESET↑ to interface operation	100			ns

Notes 1. TYP. values are reference values when T_A = 25°C.

★ **2.** The resistor value of "R" is depending on the characteristic of the parasitism capacity such as wiring. It is recommended to determine this value after through evaluation with actual system.

3. The relationship between the frame frequency and the calibration setting time is as follows.

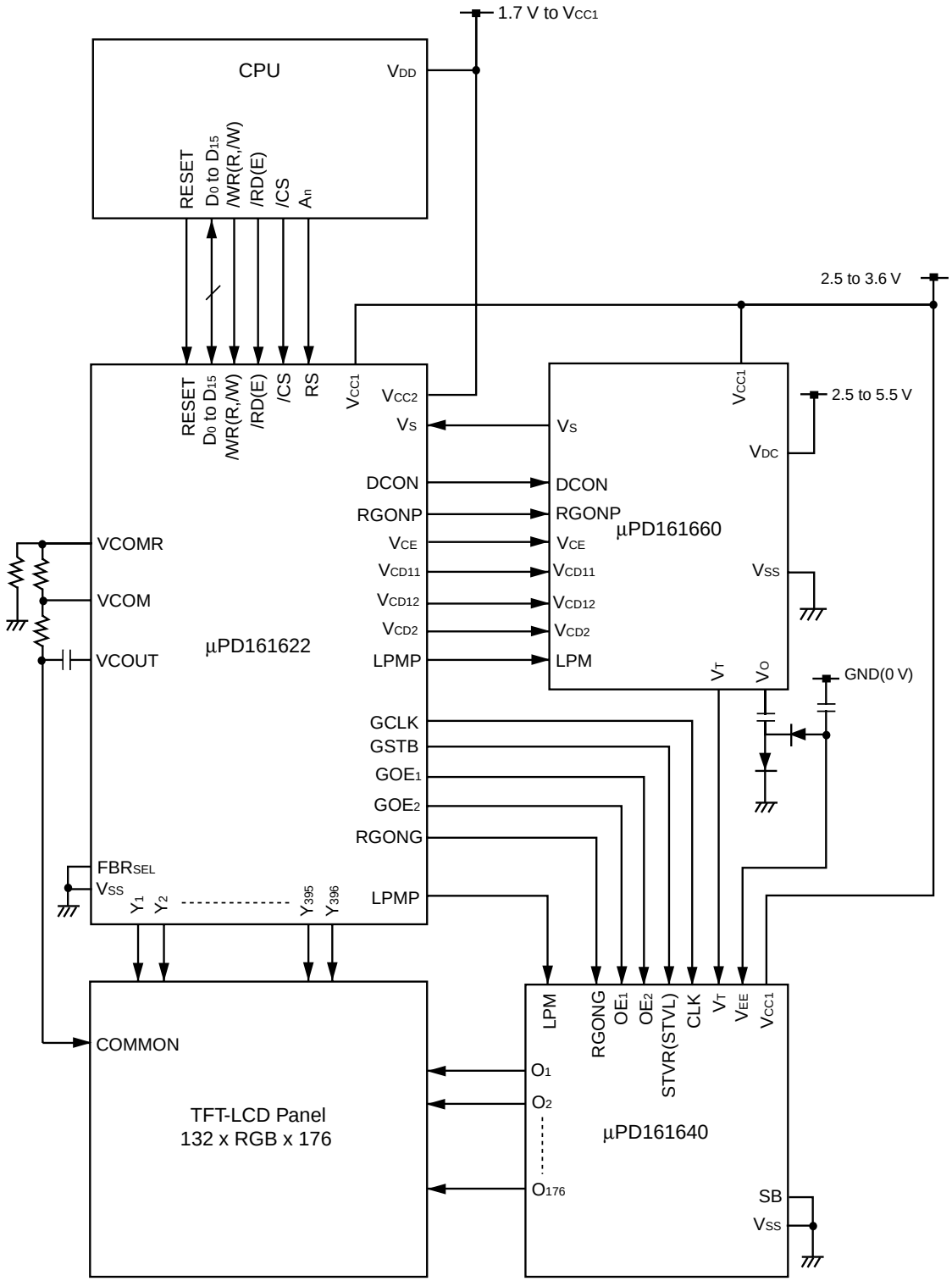
$$f_{FRAME0} = \frac{1}{t_{cal} \times 177}$$

4. Measured at T_A = –40 to +85°C, after calibration at frame frequency = 80 Hz, T_A = 25°C exactly.

5. Measured at ±5°C, after calibration at frame frequency = 80 Hz exactly.

★ 9. μPD161622, 161640, and 161660 CONNECTION DIAGRAM EXAMPLE

Connection diagram examples for the μPD161622, 161640, and 161660 are show below.

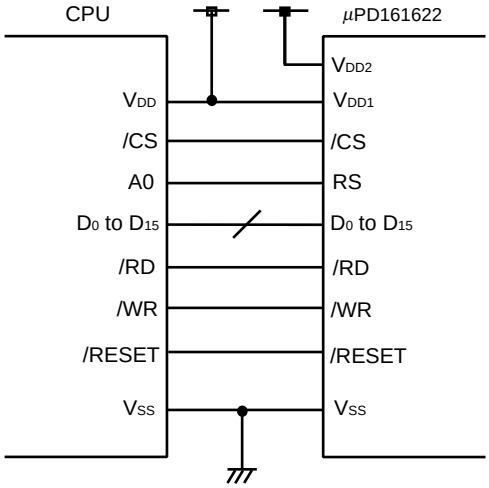


10. EXAMPLE of μPD161622 and CPU CONNECTION

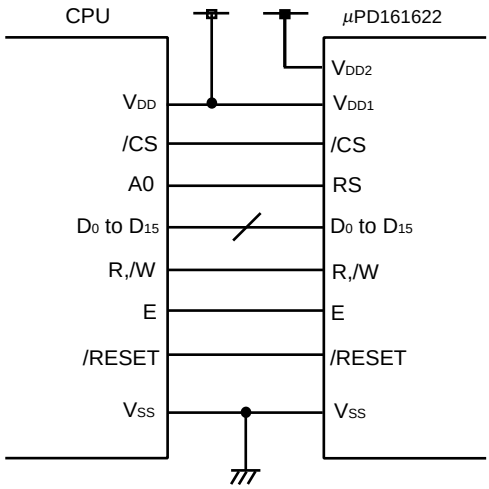
Examples of μPD161622 and CPU connection are shown below.

In the example below, RS pin control in parallel interface mode is described for the case when the least significant bit of the address bus is being used.

(1) i80 series format



(2) M68 series format



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

★ **Reference Documents**

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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