NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8105GR

400 MHz QUADRATURE MODULATOR FOR DIGITAL MOBILE COMMUNICATION

DESCRIPTION

The μPC8105GR is a sillicon monolithic integrated circuit designed as quadrature modulator for digital mobile communication systems. This modulator housed in a 16 pin plastic SSOP that is easy to install and contributes to miniaturizing the system.

The device has power save function and can operates 2.7 to 5.5 V supply voltage to realize low power consumption.

FEATURES

- Internal 90° phase shifter is accurate over an IF range from 100 MHz to 400 MHz.
- Wide supply voltage range: V_{CC} = 2.7 to 5.5 V.
- Low operation current: I_{CC} = 16 mA (typ.).
- 16 pin plastic SSOP suitable for high density surface mounting.
- Low current in sleep mode

APPLICATION

- IF modulator for Digital cellular phone (PDC, IS-54, GSM etc..)
- IF modulator for Digital cordless phone (PHS, PCS etc..)

ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC8105GR-E1	16 pin plastic SSOP (225 mil)	Carrier tape width 12 mm. Q'ty 2.5 kp/Reel Pin 1 indicated pull-out direction of tape.

To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPC8105GR)

Caution electro-static sensitive device

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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Date Published October 1999 N CP(K)
Printed in Japan

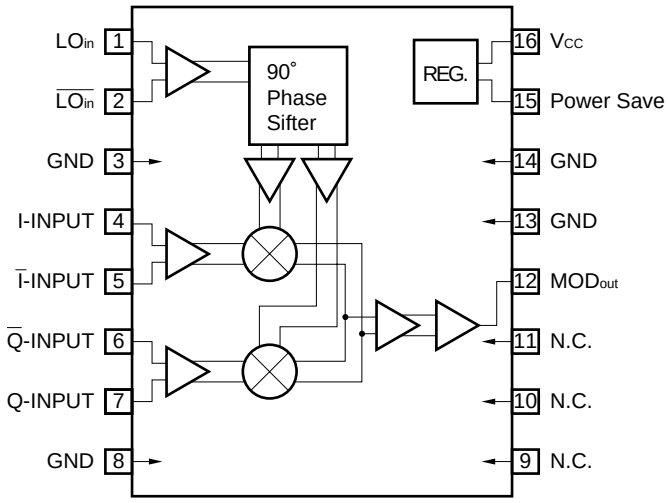
The mark ★ shows major revised points.

SERIES PRODUCTS

SERIES TYPE	PART NUMBER	f LO1 in (MHz)	f MODout (MHz)	f I/Q (MHz)	Up-Converter f RFout (MHz)	APPLICATIONS
150 MHz Quadrature MOD	μPC8101GR	100 to 300	50 to 150	DC to 0.5	External	CT2, Digital Comm.
Up-Con + Quadrature MOD	μPC8104GR	100 to 400		DC to 10	800 to 1900	Digital Comm.
400 MHz Quadrature MOD	μPC8105GR	100 to 400		DC to 10	External	Digital Comm.

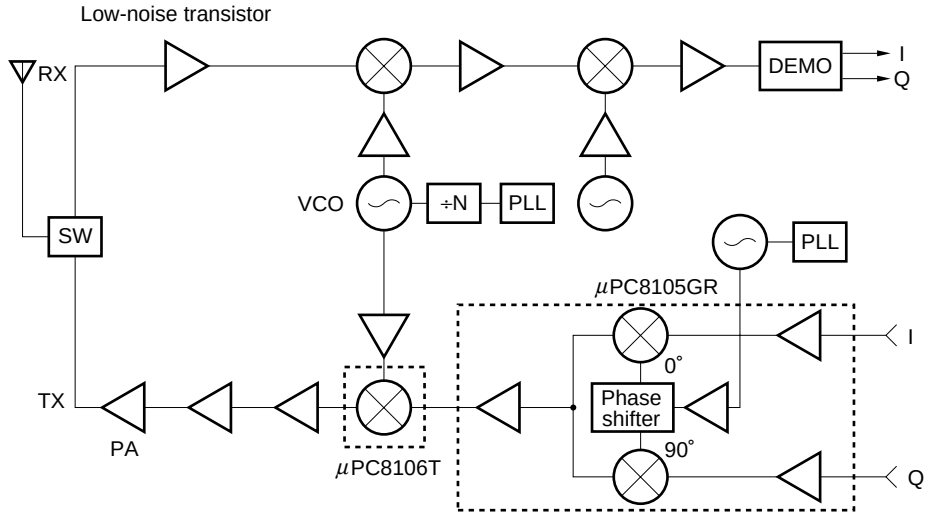
Remark: As for detail information of series products, please refer to each data sheet.

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)



APPLICATION EXAMPLE

[Digital cellular hand-held phone]



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	6.0	V	T_A = +25 °C
Power Save Voltage	V_{PS}	6.0	V	T_A = +25 °C
Power Dissipation	P_D	310	mW	T_A = +85 °C*1
Operating Temperature	T_{op}	–40 to +85	°C	
Storage Temperature	T_{stg}	–55 to +150	°C	

***1**: Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	2.7	3.0	5.5	V	
Operating Temperature	T_A	–40	+25	+85	°C	
Modulator Output Frequency	f_{MODout}	100		400	MHz	
LO1 Input Frequency	f_{LO1in}					P_{LOin} = –10 dBm
I/Q Input Frequency	$f_{I/Qin}$	DC		10	MHz	$P_{I/Qin}$ = 600 mV_{p-p} MAX (Single ended)

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified VPS ≥ 1.8 V)

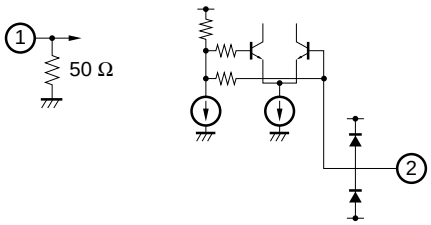
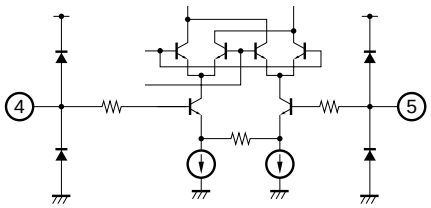
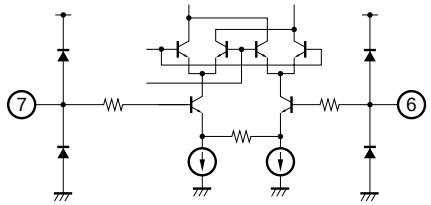
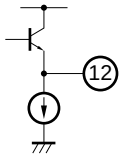
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	10	16	21	mA	No input signal
Circuit Current at Power Save Mode	I_{CC}(PS)		0.1	5	μA	V_{PS} ≤ 1.0 V
Output Power	P_{MODout}	–21.0	–16.5	–12.0	dBm	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended)
LO Carrier Leak	LOL		–40	–30	dBc	
Image Rejection (Side Band Leak)	ImR		–40	–30	dBc	

STANDARD CHARACTERISTICS FOR REFERENCE

(T_A = +25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified VPS ≥ 1.8 V)

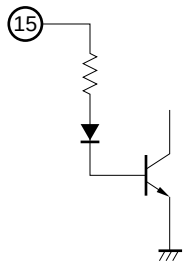
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I/Q 3rd Order Intermodulation Distortion	$IM_{3I/Q}$		–50	–30	dBc	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended)
I/Q Input Impedance	$Z_{I/Q}$		20		kΩ	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended) ($I \rightarrow \overline{I}$, $Q \rightarrow \overline{Q}$)
I/Q Bias Current	$I_{I/Q}$		5		μA	
LO1 Input VSWR	Z_{LO}		1.2:1		–	
Power Save Rise Time	$T_{PS(RISE)}$		2	5	μs	V_{PS}(OFF) → V_{PS}(ON)
Power Save Fall Time	$T_{PS(FALL)}$		2	5	μs	V_{PS}(ON) → V_{PS}(OFF)

PIN EXPLANATION

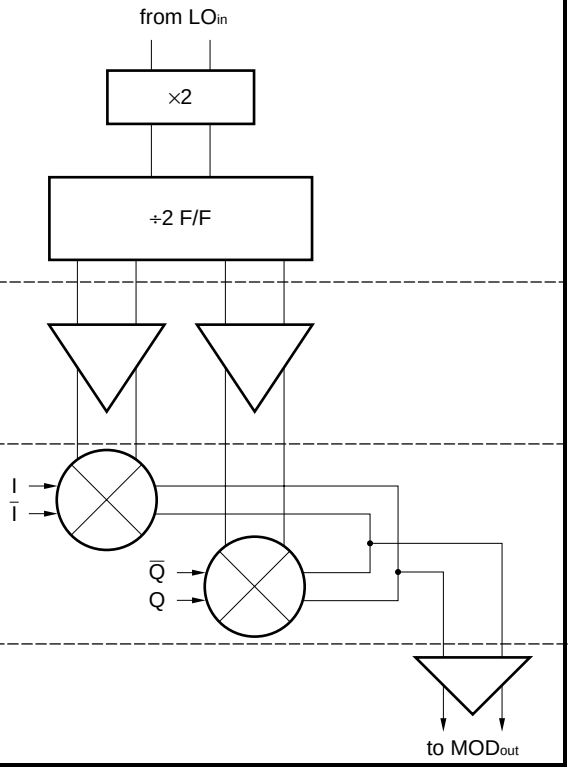
<table>
<tr><th>PIN NO.</th><th>ASSIGN-MENT</th><th>SUPPLY VOL. (V)</th><th>PIN VOL.(V)</th><th>FUNCTION AND APPLICATION</th><th>EQUIPMENT CIRCUIT</th></tr>
<tr><td>1</td><td>LOin</td><td>–</td><td>0</td><td>LO input for phase shifter.
This input impedance is 50 Ω matched internally.</td><td rowspan="2"> 
</td></tr>
<tr><td>2</td><td>$\overline{\text{LOin}}$</td><td>–</td><td>2.4</td><td>Bypass of LO input.
This pin is grounded through internal capacitor.
Open in case of single ended.</td></tr>
<tr><td>3
8</td><td>GND</td><td>0</td><td>–</td><td>Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>4</td><td>I</td><td>Vcc/2</td><td>–</td><td>Input for I signal. This in put impedance is larger than 20 kΩ.
Relations between amplitude and Vcc/2 bias of input signal are following.
<table><tr><th>Vcc/2 (v)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥ 1.35</td><td>400</td></tr><tr><td>≥ 1.5</td><td>600</td></tr><tr><td>≥ 1.75</td><td>1000</td></tr></table> *1</td><td rowspan="3"> 
</td></tr>
<tr><td>5</td><td>$\overline{\text{I}}$</td><td>Vcc/2</td><td>–</td><td>Input for I signal. This in put impedance is larger than 20 kΩ.
Vcc/2 biased DC signal should be input.</td></tr>
<tr><td>6</td><td>$\overline{\text{Q}}$</td><td>Vcc/2</td><td>–</td><td>Input for Q signal. This in put impedance is larger than 20 kΩ.
Vcc/2 biased DC signal should be input.</td></tr>
<tr><td>7</td><td>Q</td><td>Vcc/2</td><td>–</td><td>Input for Q signal. This in put impedance is larger than 20 kΩ.
Relations between amplitude and Vcc/2 bias of input signal are following.
<table><tr><th>Vcc/2 (v)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥ 1.35</td><td>400</td></tr><tr><td>≥ 1.5</td><td>600</td></tr><tr><td>≥ 1.75</td><td>1000</td></tr></table> *1</td><td> 
</td></tr>
<tr><td>12</td><td>MODout</td><td>–</td><td>1.5</td><td>Output from modulator.
This is emitter follower output.</td><td> 
</td></tr>
</table>

***1:** In case of that I/Q input signals are single ended.
Of course, I/Q signal inputs can be used either single endedly or differentially with proper terminations.

PIN EXPLANATION

PIN NO.	ASSIGN-MENT	SUPPLY VOL. (V)	PIN VOL.(V)	FUNCTION AND APPLICATION	EQUIPMENT CIRCUIT
13 14	GND	0	–	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
15	Power Save	VP/S	–	Power save control pin can be controlled ON/SLEEP state with bias as follows; VP/S (v) / STATE 1.8 to 5.5 / ON 0 to 1.0 / SLEEP	
16	V_{CC}	2.7 to 5.5	–	Supply voltage pin for modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.	

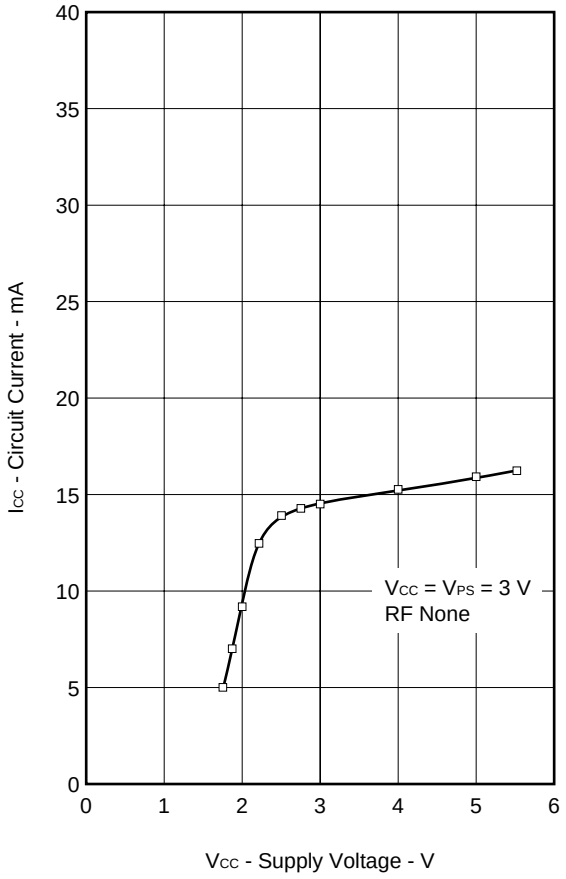
EXPLANATION OF INTERNAL FUNCTION

BLOCK	FUNCTION/OPERATION	BLOCK DIAGRAM
90° PHASE SHIFTER	Input signal from LO is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as LO input and that have quadrature phase shift, 0°, 90°, 180°, 270°. These circuits have function of self phase correction to make correctly quadrature signals.	
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	

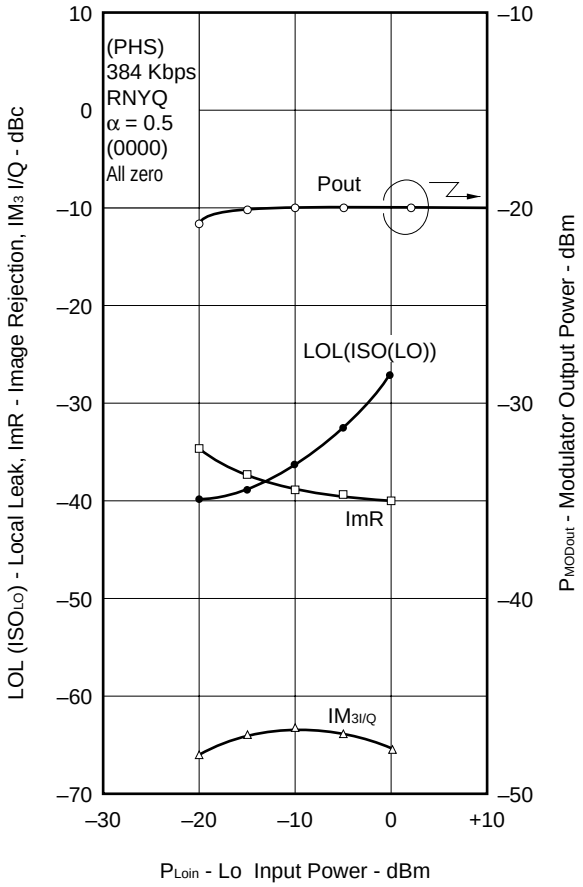
TYPICAL CHARACTERISTICS (T_A = +25 °C)

Unless otherwise specified V_{CC} = V_{PS} = 3 V, I/Q DC offset = $\overline{I}/\overline{Q}$ DC offset = 1.5 V, I/Q Input Signal = 500 mV_{p-p} (single ended), P_{LOin} = –10 dBm, (continuous wave)

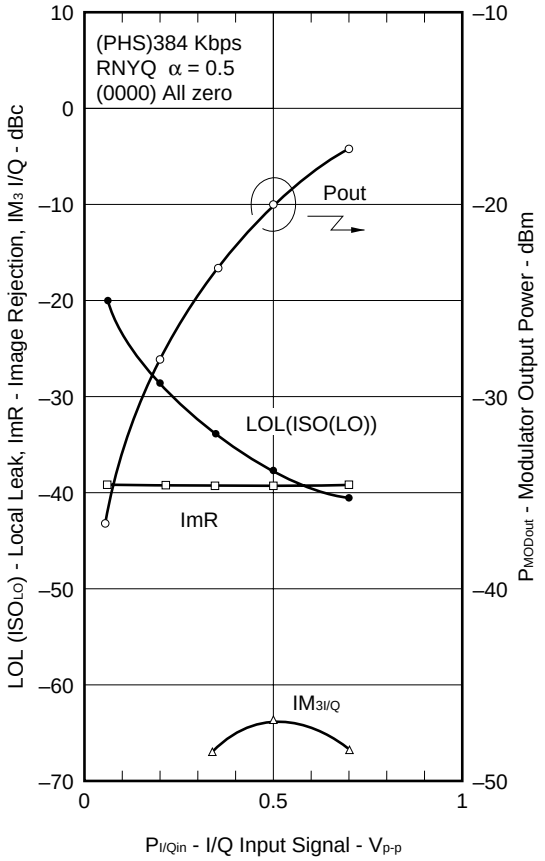
SUPPLY VOLTAGE vs CIRCUIT CURRENT



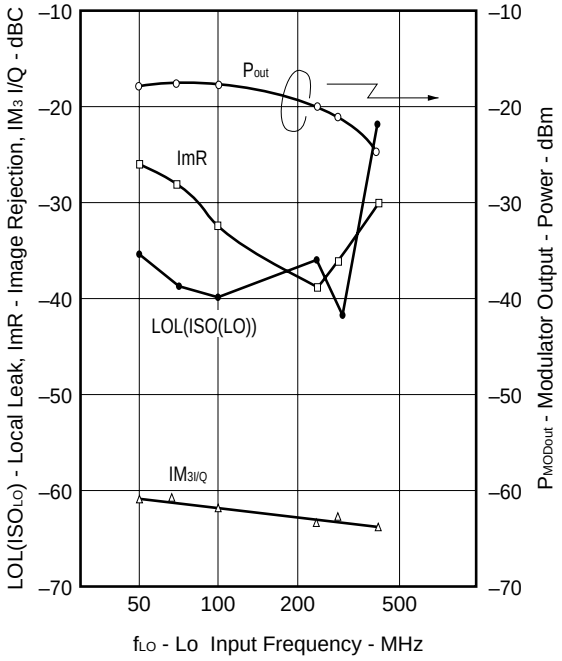
Lo INPUT POWER vs OUTPUT POWER, LOCAL LEAK, IMAGE REJECTION, I/Q 3RD ORDER INTERMODULATION DISTORTION



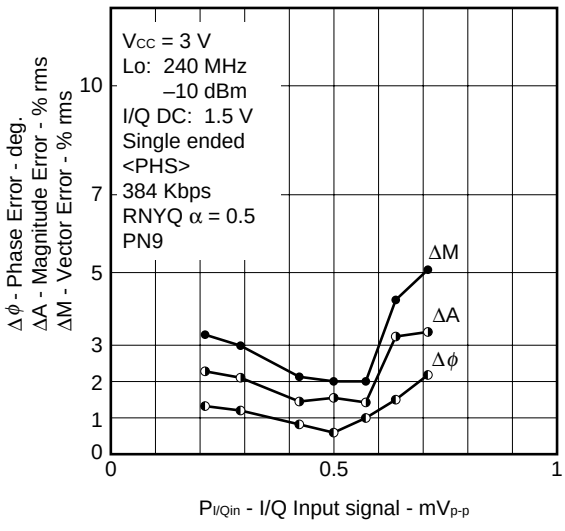
I/Q INPUT SIGNAL vs OUTPUT POWER, LOCAL LEAK, IMAGE REJECTION, I/Q 3RD ORDER INTERMODULATION DISTORTION



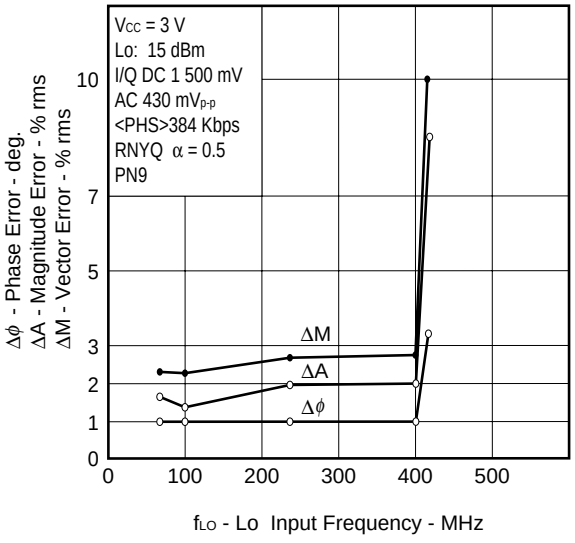
Lo INPUT FREQUENCY vs OUTPUT POWER, LOCAL LEAK, IMAGE REJECTION, I/Q 3RD, ORDER INTERMODULATION DISTORTION



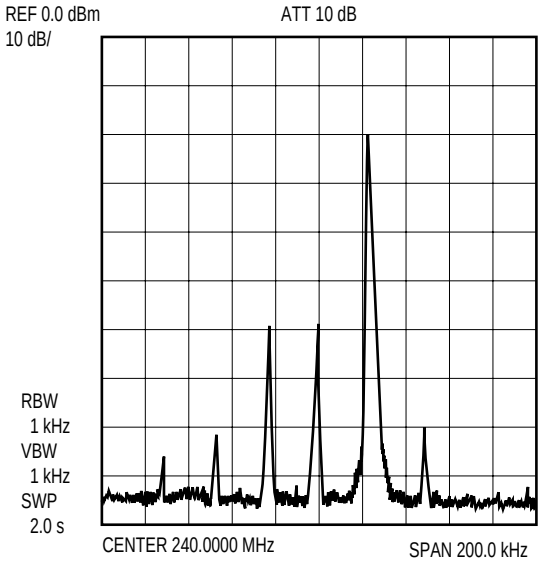
I/Q INPUT SIGNAL vs PHASE ERROR, MAGNITUDE ERROR, VECTOR ERROR



Lo INPUT FREQUENCY vs VECTOR ERROR, MAGNITUDE ERROR, PHASE ERROR

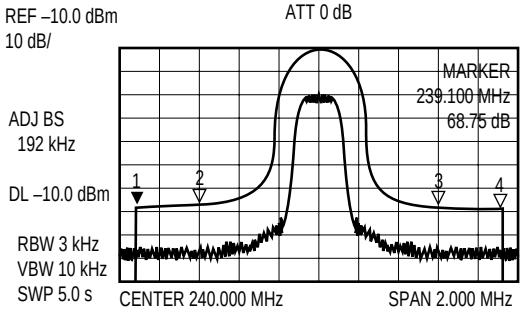


TYPICAL SINE WAVE MODULATION
OUTPUT SPECTRUM



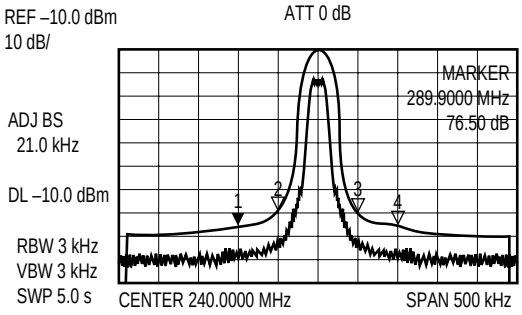
<PHS>384 kbps, RNYQ α = 0.5, MOD Pattern<000>, all zero

TYPICAL π/4 DQPSK MODULATION OUTPUT SPECTRUM
<PHS>384 kbps, RNYQ α = 0.5, MOD Pattern (PN9)



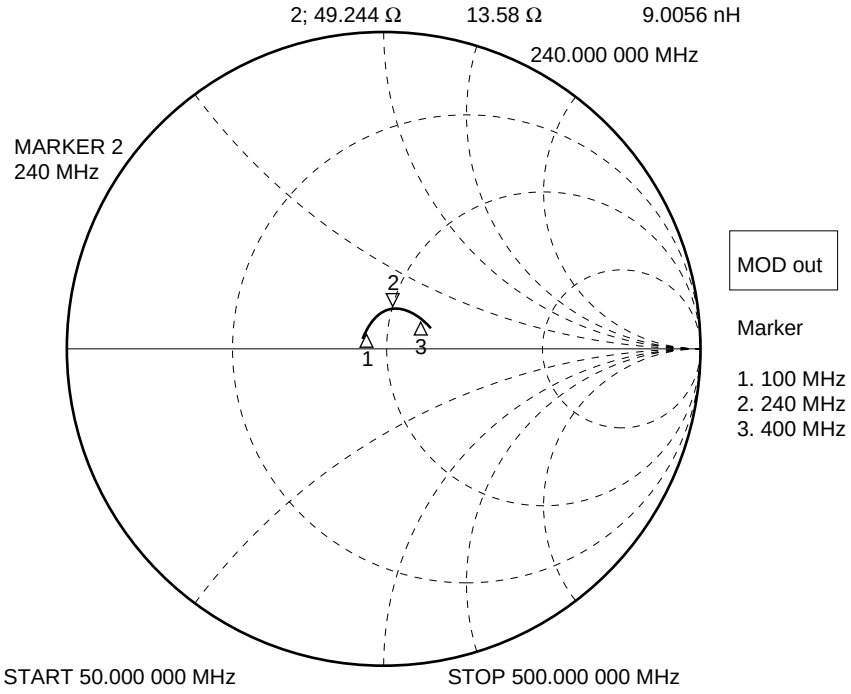
*** Multi Marker List ***
No.1: 239.100 MHz –68.75 dB
No.2: 239.400 MHz –68.25 dB
No.3: 240.600 MHz –68.25 dB
No.4: 240.900 MHz –69.00 dB

TYPICAL π/4 DQPSK MODULATION OUTPUT SPECTRUM
<PDC>42 kbps, RNYQ α = 0.5, MOD Pattern<PN9>

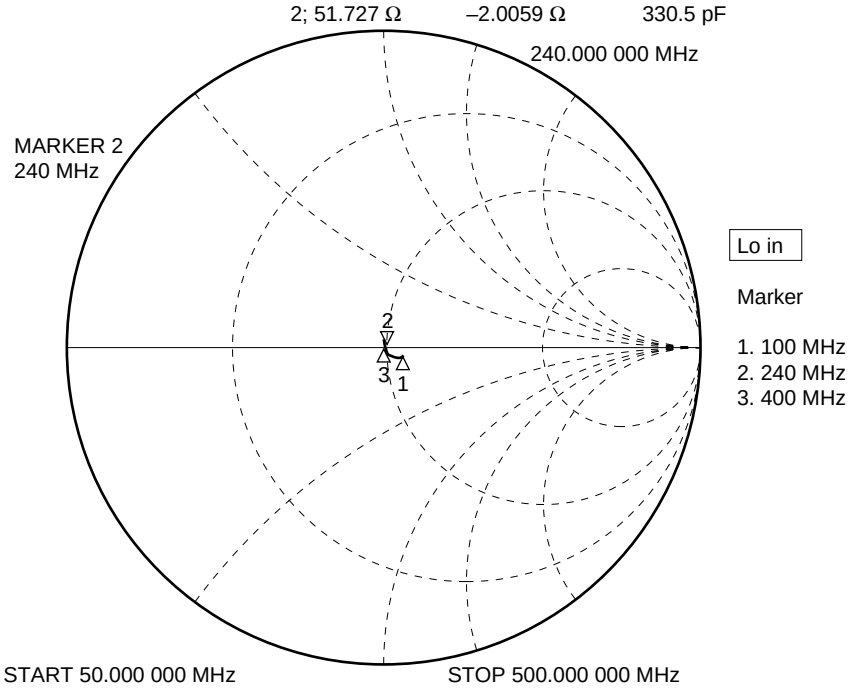


*** Multi Marker List ***
No.1: 239.9000 MHz –76.50 dB
No.2: 239.9500 MHz –70.50 dB
No.3: 240.0500 MHz –71.00 dB
No.4: 240.1000 MHz –75.75 dB

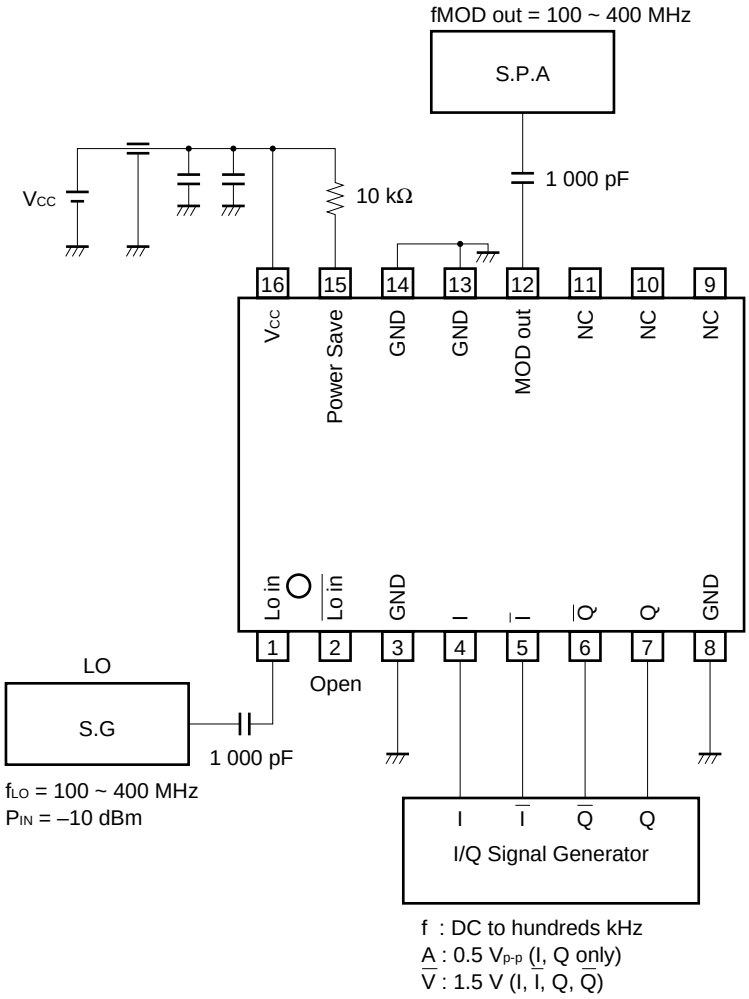
MODout OUTPUT IMPEDANCE



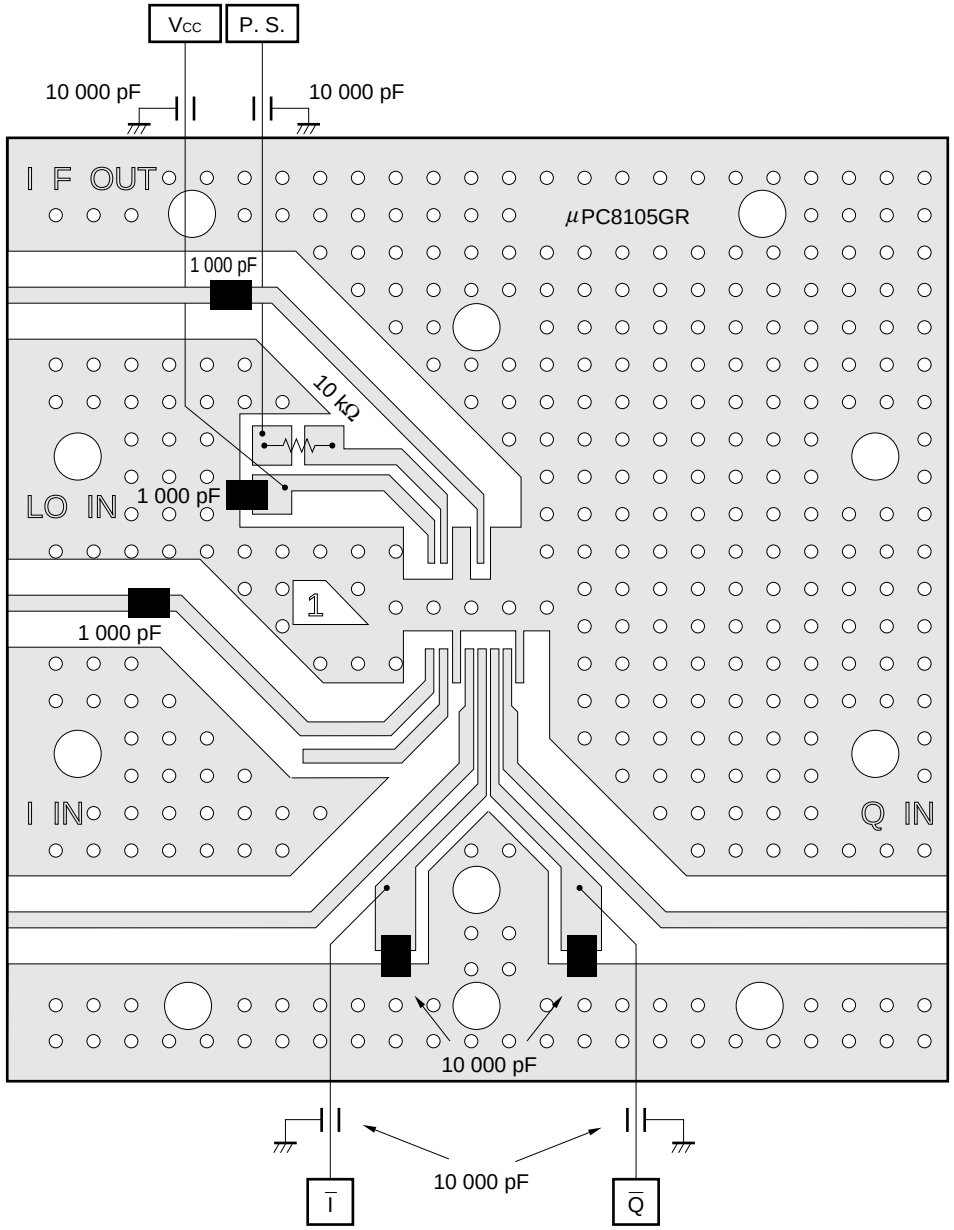
LOin INPUT IMPEDANCE



TEST CIRCUIT

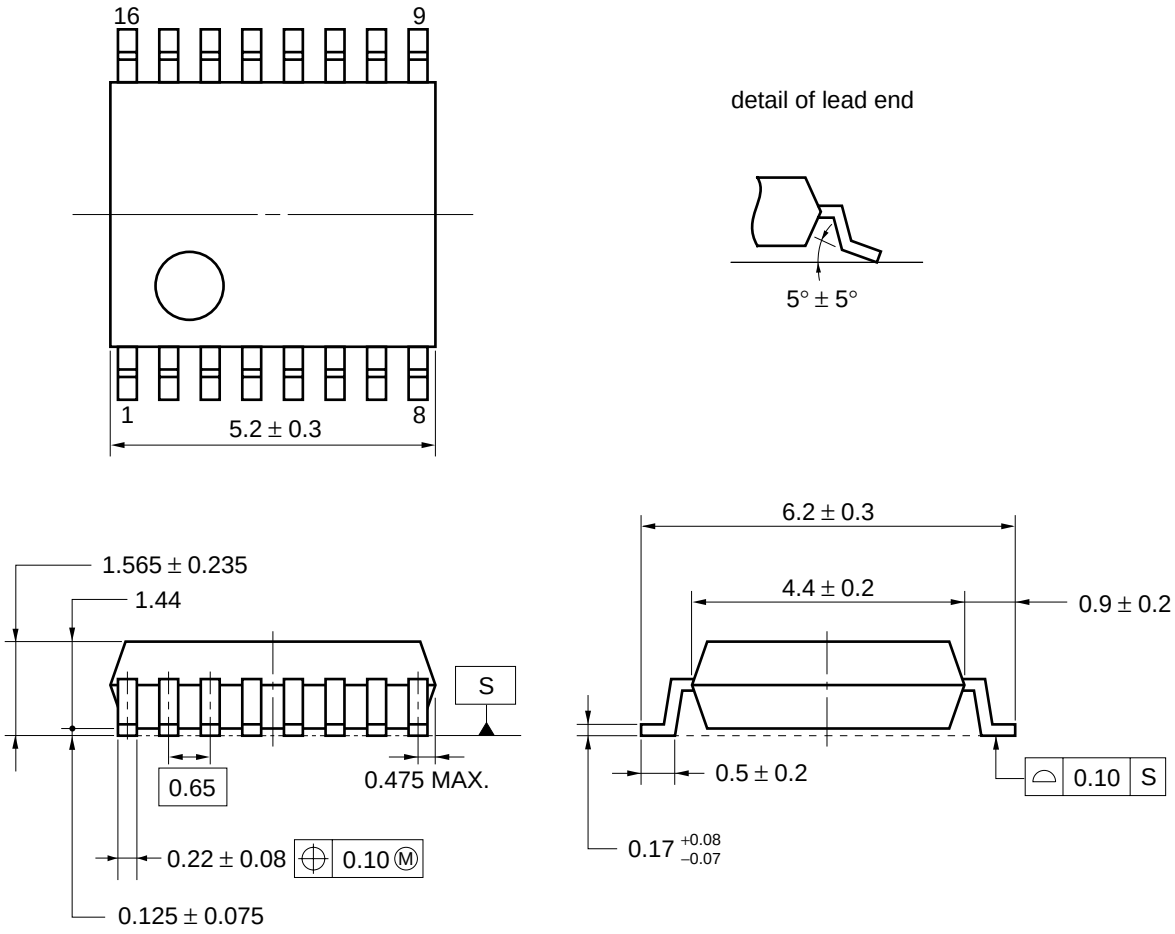


TEST BOARD


VCC
P. S.
10 000 pF
10 000 pF
I F OUT
μPC8105GR
1 000 pF
10 kΩ
LO IN
1 000 pF
1
1 000 pF
I IN
Q IN
10 000 pF
10 000 pF
Ī
Q̄

PACKAGE DIMENSIONS

★ **16 PIN PLASTIC SHRINK SOP (225 mil) (UNIT: mm)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.
(5) $\overline{I}$, $\overline{Q}$ DC offset voltage should be same as the I, Q DC offset voltage (to prevent changing the local leak level with power save control.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8105GR

Soldering process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit*: None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 30 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit*: None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below, Number of reflow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below Flow time: 3 seconds/pin or below, Exposure limit*: None	

***:** Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Apply only a single process at once, except for "Partial heating method".
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

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