NEC

MOS INTEGRATED CIRCUIT

μPD75P336

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P336 is a version of the μPD75336 in which the on-chip mask ROM is replaced by one-time PROM.

As the μPD75P336 is user-programmable, it is suitable for preproduction in system development, and for short-run and multiple device-production.

Detailed function description, etc. are described in the following User's manual. Be sure to read it when designing. μPD75336 User's Manual: IEU-725

FEATURES

- μPD75336 compatible
- Memory capacity:
  - PROM : 16256 × 8 bits
  - RAM : 768 × 4 bits
- Operable over same supply voltage range as mask ROM μPD75336
  - V_{DD} = 2.7 to 6.0 V
- On-chip 8-bits resolution A/D converter (successive approximation type)
- On-chip LCD controller/driver

ORDERING INFORMATION

Ordering Code	Package	Quality Grade	
μPD75P336GC-3B9	80-pin plastic QFP (□ 14mm)	Standard	
μPD75P336GK-BE9	80-pin plastic TQFP (fine pitch)(□12mm)	Standard	★

Note Pull-up resistor cannot be incorporated by mask option.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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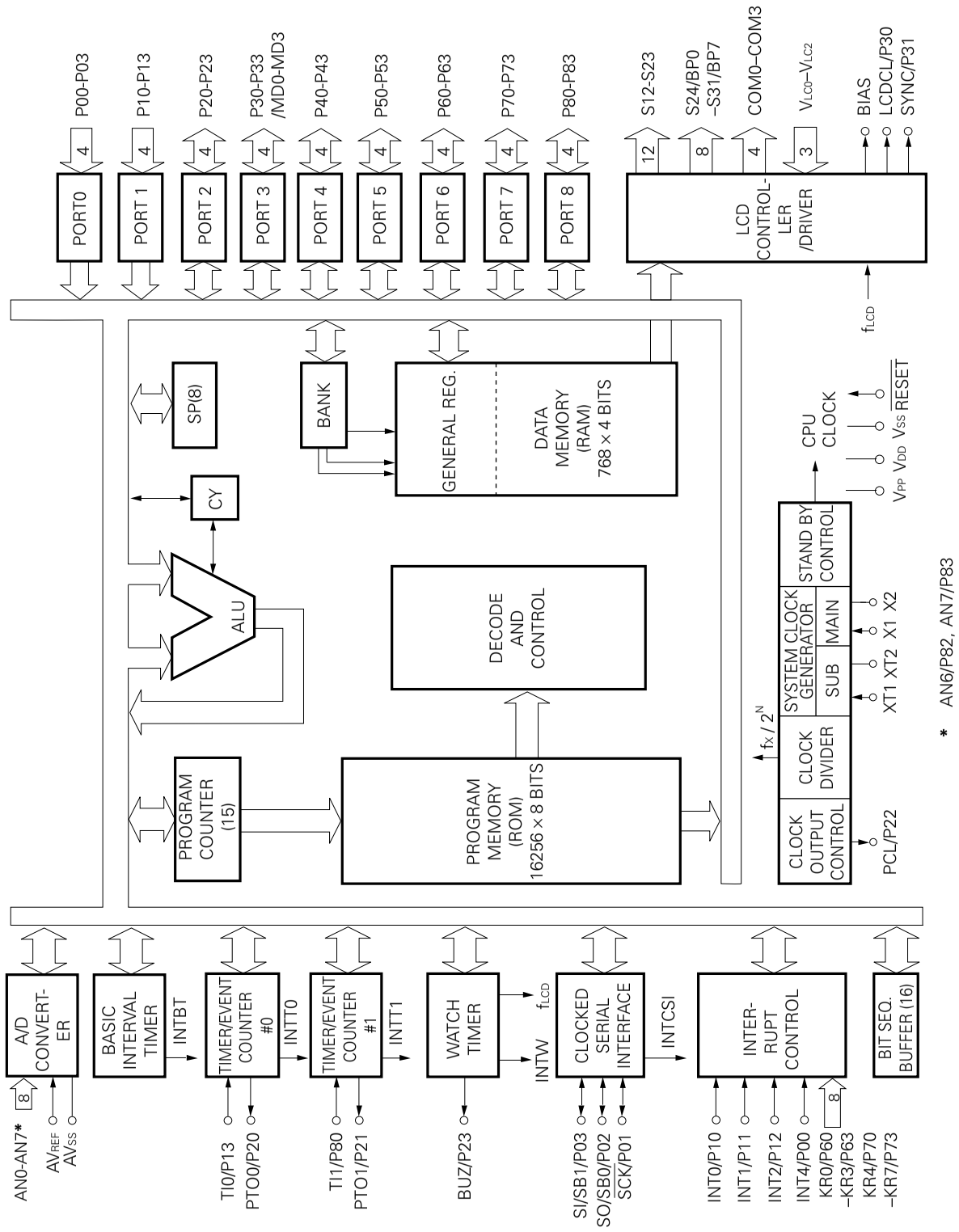
Date Published October 1993P
Printed in Japan

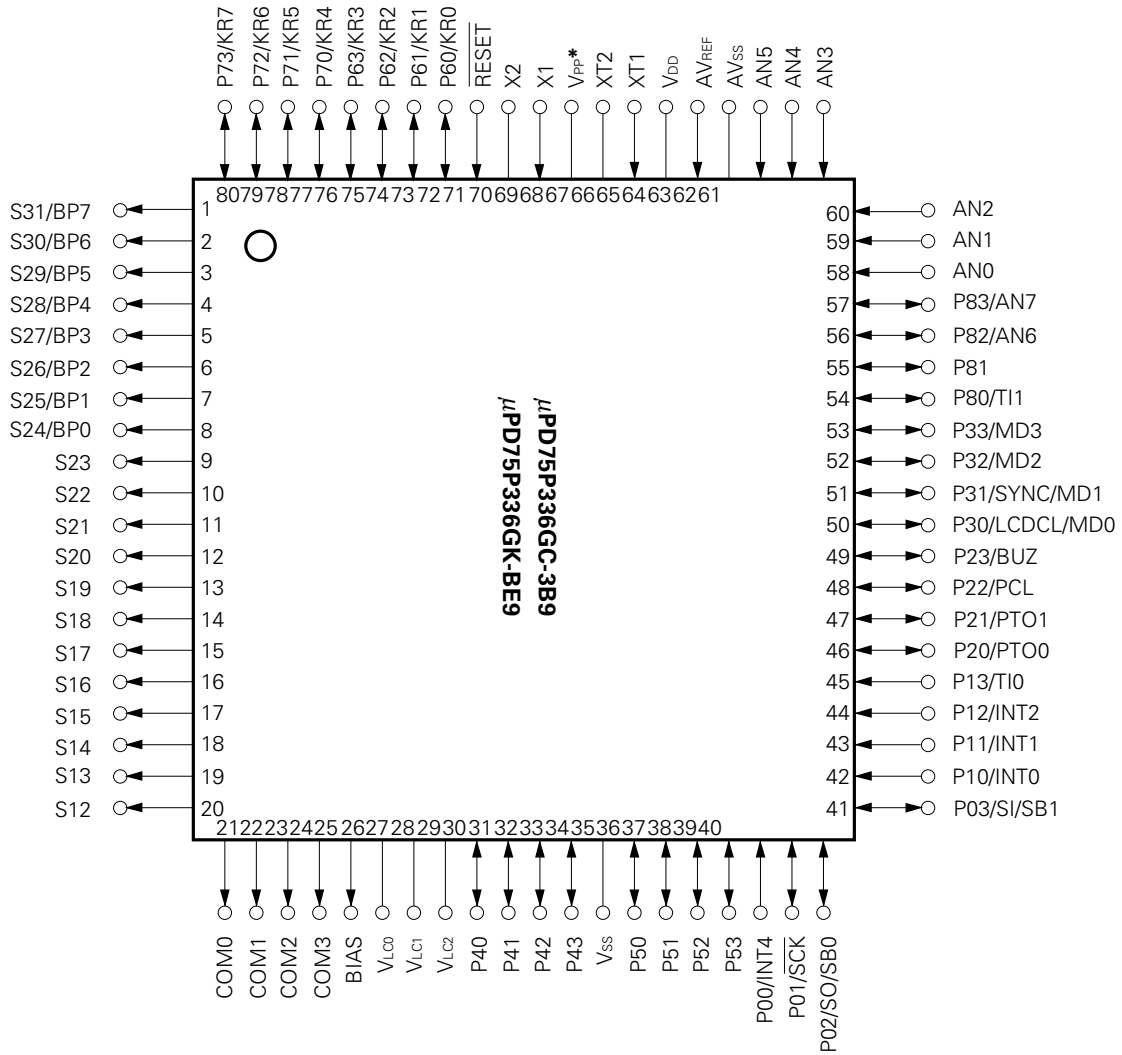
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

○ **80-pin plastic QFP (□14mm)**
○ **80-pin plastic TQFP (fine pitch) (□12mm)** ★



***** In normal operation, V_{PP} should be connected to V_{DD} directly.

PIN NAME

P00 to 03 : Port 0
P10 to 13 : Port 1
P20 to 23 : Port 2
P30 to 33 : Port 3
P40 to 43 : Port 4
P50 to 53 : Port 5
P60 to 63 : Port 6
P70 to 73 : Port 7
P80 to 83 : Port 8
BP0 to 7 : Bit Port
KR0 to 7 : Key Return
AV_{REF} : Analog Reference
AV_{SS} : Analog Ground
AN0 to 7 : Analog Input 0 to 7
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
MD0 to 3 : Mode Selection
V_{PP} : Programming/Verifying Power Supply

$\overline{SB0, 1}$: Serial Bus 0,1
$\overline{RESET}$: Reset Input
S12 to 31 : Segment Output 12 to 31
COM0 to 3 : Common Output 0 to 3
$V_{LC0\ to\ 2}$: LCD Power Supply 0 to 2
BIAS : LCD Power Supply Bias Control
LCDCL : LCD Clock
SYNC : LCD Synchronization
TI0, 1 : Timer Input 0, 1
PTO0, 1 : Programmable Timer Output 0, 1
BUZ : Buzzer Clock
PCL : Programmable Clock
INT0, 1, 4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Interrupt 2
X1, 2 : Main System Clock Oscillation 1, 2
XT1, 2 : Subsystem Clock Oscillation 1, 2
V_{DD} : Positive Power Supply
V_{SS} : Ground

CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT0) Internal pull-up resistor specification by software is possible for P01 to P03 as a 3-bit unit.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination circuit	×	Input	Ⓑ - C
P11		INT1	4-bit input port (PORT1) Internal pull-up resistor specification by software is possible as a 4-bit unit.			
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT2) Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL / MD0	Programmable 4-bit input/output port (PORT3) Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - B
P31 *2		SYNC / MD1				
P32 *2		MD2				
P33 *2		MD3				
P40 to P43 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4). Data input/output pins for program memory (PROM) write/verify (low-order 4 bits).	○	Input	M - B
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) Data input/output pins for program memory (PROM) write/verify (high-order 4 bits).		Input	M - B
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT6). Input/output settable bit-wise. Internal pull-up resistor specification by software is possible as a 4-bit unit.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT7). Internal pull-up resistor specification by software is possible as a 4-bit unit.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				

* **1.** ◯ : Indicates a Schmitt-triggered input.
2. Direct LED drive capability.

1.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type
P80	Input/output	TI1	4-bit input/output port (PORT8). Internal pull-up resistor specification by software is possible as a 4-bit unit.	×	Input	E - E
P81		—				E - B
P82		AN6				Y - B
P83		AN7				
BP0	Output	S24	1-bit output port (BIT PORT) Dual function as segment output pins.	×	*	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* V_{LCX} shown below can be selected for the display outputs.
S12 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}
However, display output levels depend on the display outputs and V_{LCX} external circuit.

1.2 OTHER PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function		After Reset	I/O Circuit Type *
TI0	Input	P13	External event pulse input pin for timer/event counter.		Input	Ⓑ - C
TI1		P80				Ⓑ - E
PTO0	output	P20	Timer/event counter output pin		Input	E - B
PTO1		P21				
PCL	output	P22	Clock output pin		Input	E - B
BUZ	output	P23	Frequency output pin (for buzzer or system clock trimming)		Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin		Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin		Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin		Input	Ⓜ - C
INT4	Input	P00	Edge-detected vectored interrupt input pin (both rising and falling edge detection valid).		Input	Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input pin (detected edge selectable)	Clocked	Input	Ⓑ - C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge-detected testable input pin (rising edge detection)	Asynchronous	Input	Ⓑ - C
KR0 to KR3	Input	P60 to P63	Parallel falling edge detected testable input pins.		Input	Ⓕ - A
KR4 to KR7	Input	P70 to P73	Parallel falling edge detected testable input pins.		Input	Ⓕ - A
X1, X2	—	—	Main system clock oscillation crystal/ceramic resonator inputs. When an external clock is used, the clock is input to X1 and the inverted clock to X2.		—	—
XT1, XT2	—	—	Subsystem clock oscillation crystal reasonator inputs When an external clock is used, the clock is input to XT1 and the inverted clock toXT2. XT1 can be used as a 1-bit input (test) pin.		—	—
$\overline{RESET}$	Input	—	System reset input pin.		—	Ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.		Input	E - B
V_{PP}	—	—	Program voltage application pin for program memory (PROM) write/verify. Applies +12.5 V in program memory write/verify. Directly connected to V_{DD} in normal operation.		—	—
V_{DD}	—	—	Positive power supply pin		—	—
V_{SS}	—	—	GND potential pin		—	—

* ◯ : indicates a Schmitt-triggered input.

1.2 OTHER PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type
S12 to S23	Output	—	Segment signal output pins	***2**	G - A
S24 to S31	Output	BP0 to 7	Segment signal output pins	***2**	G - C
COM0 to COM3	Output	—	Common signal output pins	***2**	G - B
V_{LC0} to V_{LC2}	Input	—	LCD drive power supply pins	—	—
BIAS	Output	—	External split cutting output pin	High impedance	—
LCDCL***1**	Output	P30	External extension driver drive clock output pin	Input	
SYNC ***1**	Output	P31	External extension driver synchronization drive clock output pin	Input	E - B
					E - B
AN0 to AN5	Input	—	A/D converter analog signal input pins	Input	Y
AN6		P82			Y - B
AN7		P83			
AV_{REF}	Input	—	A/D converter reference voltage input pin	—	Z
AV_{SS}	—	—	A/D converter GND potential pin	—	Z

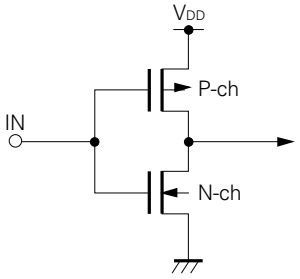
*** 1.** Pins provided for future system expansion. Currently used only as pins 30 and 31.

2. V_{LCX} shown below can be selected for the display outputs.
S12 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3:V_{LC0}
However, display output levels depend on the display outputs and V_{LCX} external circuit.

1.3 PIN INPUT/OUTPUT CIRCUITS

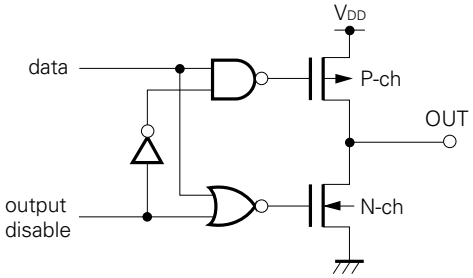
The input/output circuits for each of the pin μPD75P336 are shown below in partially simplified form.

TYPE A (For TYPE E-B)



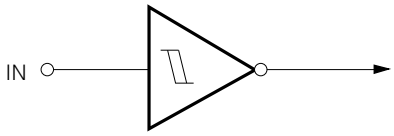
CMOS Standard Input Buffer

TYPE D (For TYPE E-B, F-A)



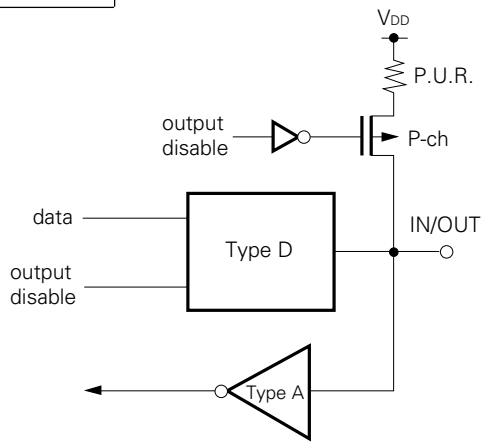
Push-Pull Output that can be Made High-Impedance Output (P-ch and N-ch OFF)

TYPE B



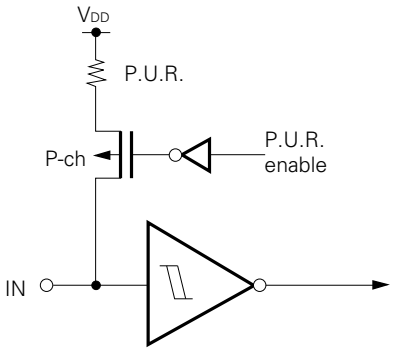
Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E-B



P.U.R.:Pull-Up Resistor

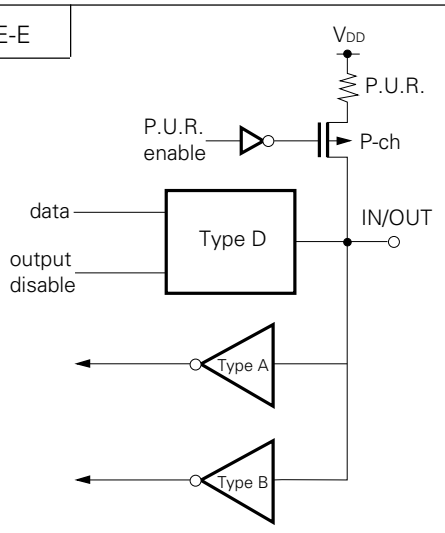
TYPE B-C



P.U.R. : Pull-Up Resistor

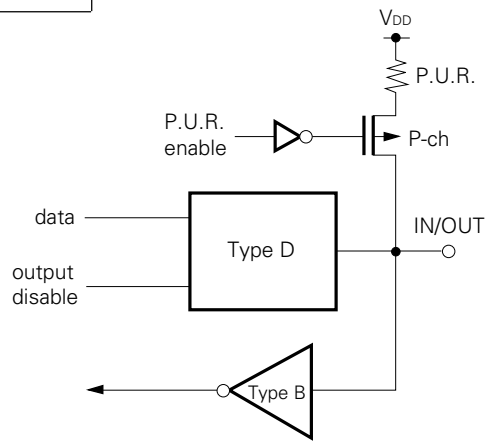
Schmitt-Trigger Input with Hysteresis Characteristic

TYPE E-E



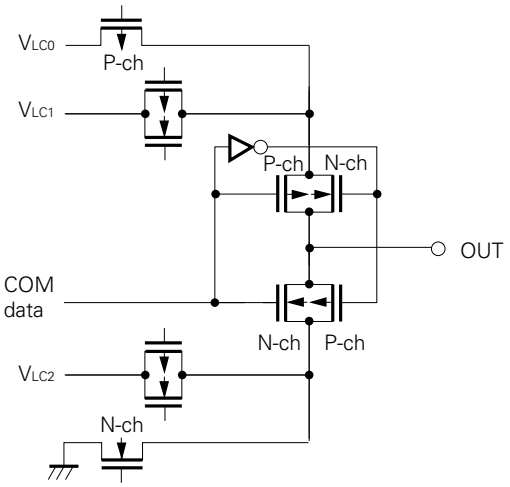
P.U.R.:Pull-Up Resistor

TYPE F-A

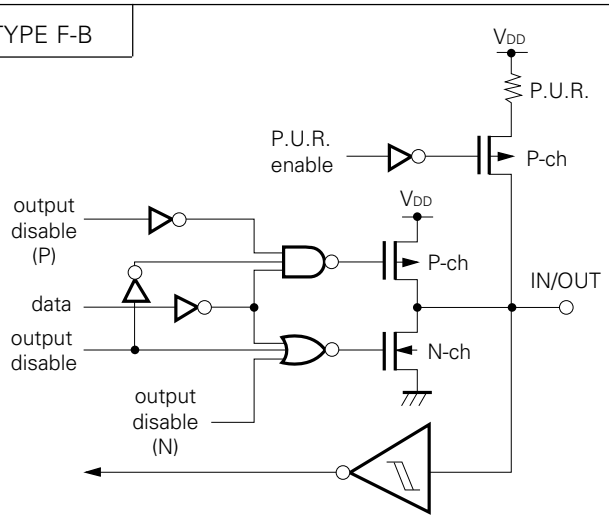


P.U.R.:Pull-Up Resistor

TYPE G-B

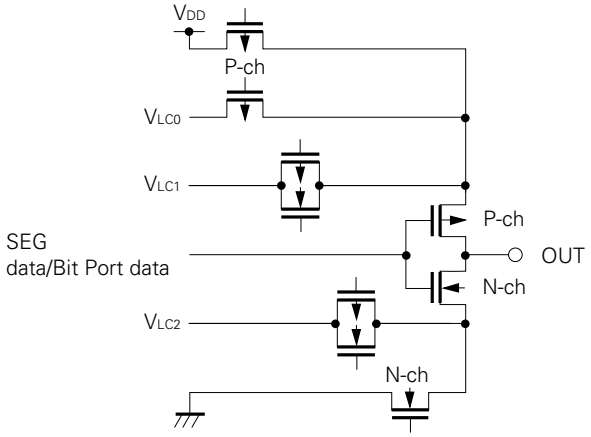


TYPE F-B

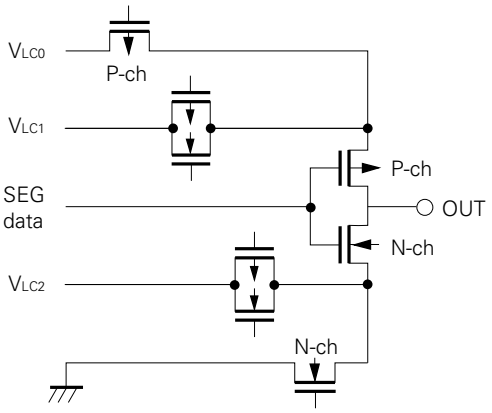


P.U.R.:Pull-Up Resistor

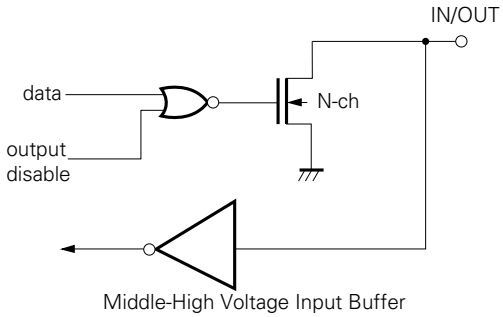
TYPE G-C



TYPE G-A

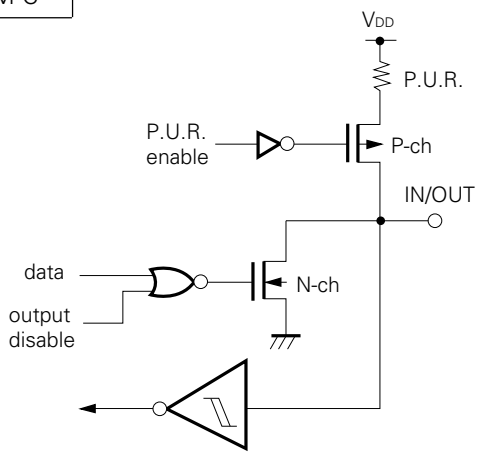


TYPE M-B



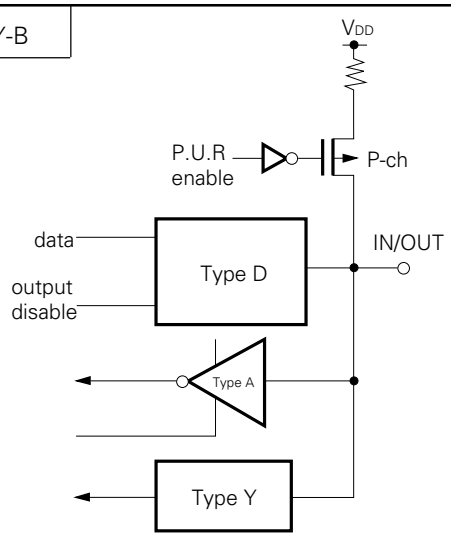
Middle-High Voltage Input Buffer

TYPE M-C



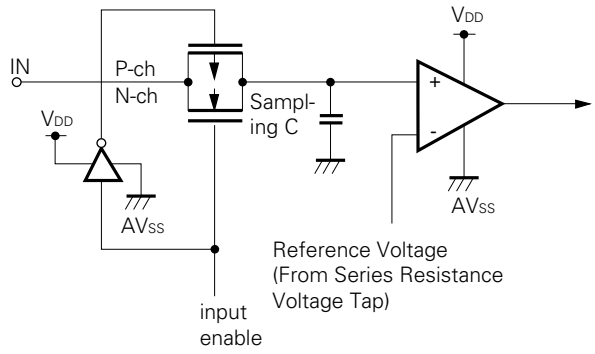
P.U.R.:Pull-Up Resistor

TYPE Y-B

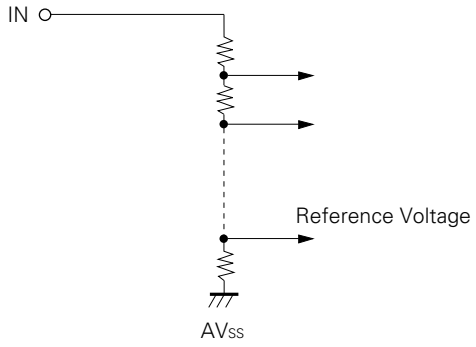


P.U.R:Pull-Up Resistor

TYPE Y



TYPE Z



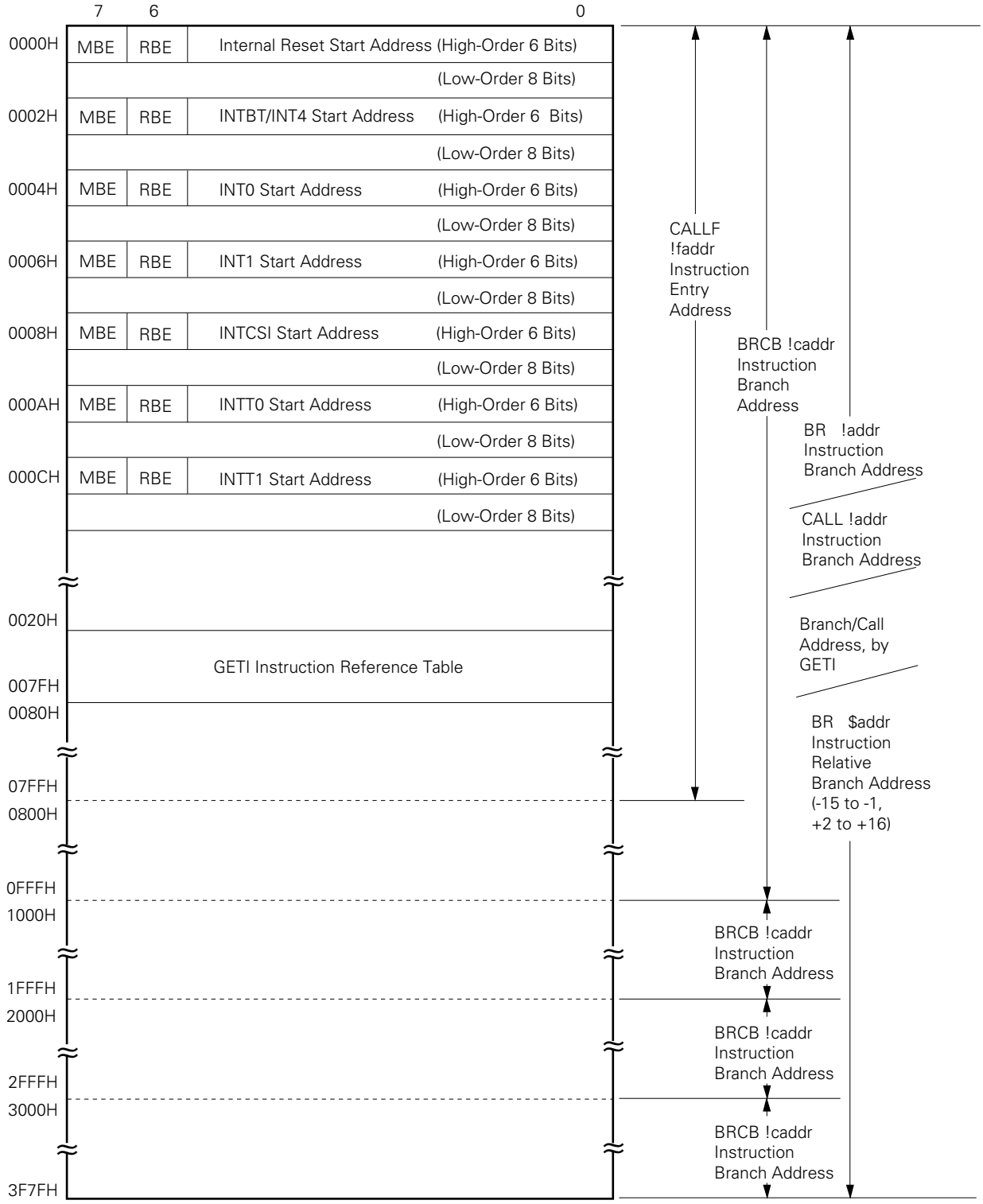
2. DIFFERENCES BETWEEN μPD75P336 AND μPD75336

Parameter	μPD75336	μPD75P336
Program memory	Mask ROM 16256 × 8 bits	One-time PROM 16256 × 8 bits
Data memory	768 × 4 bits	768 × 4 bits
Ports 4, 5 pull-up resistor	Incorporation specifiable by mask option	No
LCD drive power supply split resistor	Incorporation specifiable by mask option	No
Subsystem clock oscillation feedback resistor	Incorporation specifiable by mask option	Incorporated
Pin 69	IC	V_{PP}

2.1 PROGRAM MEMORY (PROM) ..... 16256 WORDS × 8 BITS

The program memory consists of 16256-byte PROM. The program memory map is shown in Fig. 2-1.

Fig. 2-1 Program Memory Map

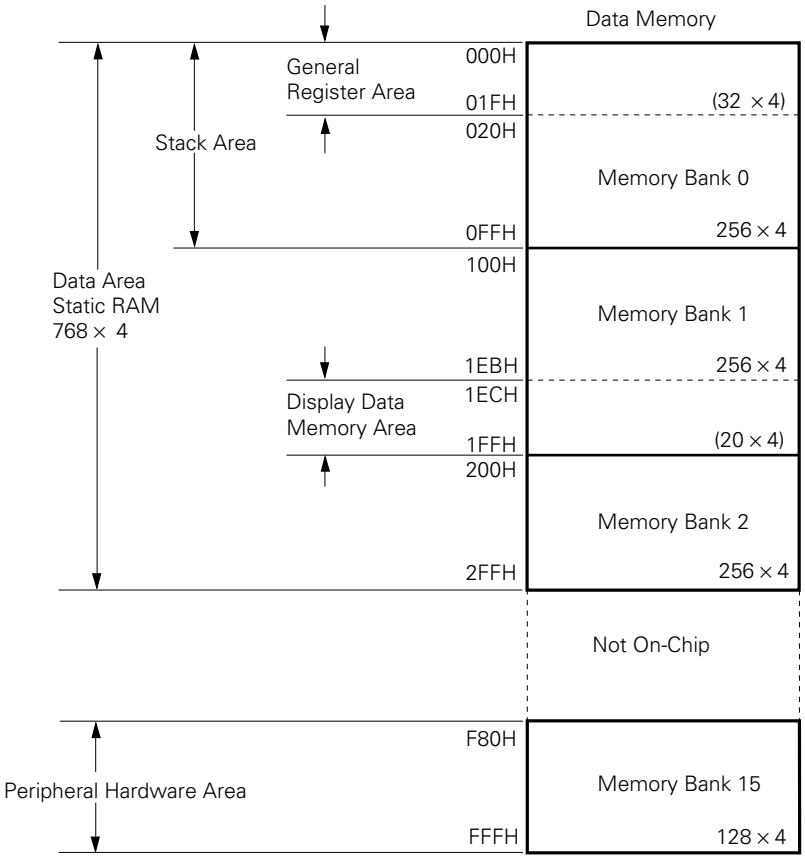


Remarks In addition to the above, branching is possible with the BR PCDE and BR PCXA instructions to addresses with the low-order 8 bits only of the PC modified.

2.2 DATA MEMORY (RAM) .....768 WORDS × 4 BITS

The configuration of the data memory is shown in Fig. 2-2. The data memory comprises a data area and peripheral hardware area, the data area comprises 768 × 4-bit static RAM.

Fig. 2-2 Data Memory Map



3. INSTRUCTION SET AND INSTRUCTION OPERATIONS

(1) Operand identifier and description

Operand identifiers and description method operands are written in the operand column for each instruction in accordance with the description method for the operand identifier for that instruction (refer to **"RA75X Assembler Package User's Manual Language Volume (EEU-730)"** for details). Where multiple items are included in the description method, one of those elements should be selected. Uppercase letters and the symbols + and – are keywords and should be written as they are.

In the case of immediate data, an appropriate number or label is written.

Descriptor	Description Method
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE' HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate date or label
n8	8-bit immediate date or label
mem	8-bit immediate date or label*
bit	2-bit immediate date or label
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label
pmem	FC0H to FFFH immediate data or label
addr	0000H to 3F7FH immediate data or label
caddr	12-bit immediate date or label
faddr	11-bit immediate date or label
taddr	20H to 7FH immediate date (bit 0 = 0) or label
PORTn	PORT0 to PORT8
IE×××	IEBT, IECSI, IET0, IET1, IE0 to IE2, IE4, IEW
RBn	RB0 to RB3
MBn	MB0, MB1, MB2, MB15

***** In 8-bit data processing, only an even address can be specified.

(2) Operation description legend

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
XA'	:	Extended register pair (XA')
BC'	:	Extended register pair (BC')
DE'	:	Extended register pair (DE')
HL'	:	Extended register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Portn (n = 0 to 8)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority selection register
IE×××	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Address, bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of addressing area field symbols

*1	MB = MBE • MBS MBS = 0, 1, 2, 15	Data Memory Addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 2, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3F7FH	Program Memory Addressing
*7	addr = (Current PC) –15 to (Current PC) –1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H to 0FFFH ($PC_{13,12}$ = 00B) or 1000H to 1FFFH ($PC_{13,12}$ = 01B) or 2000H to 2FFFH ($PC_{13,12}$ = 10B) or 3000H to 3FFFH ($PC_{13,12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	

Remarks 1. MB indicates the accessible memory bank.
2. MB=0 irrespective of MBE and MBS in *2.
3. MB=15 irrespective of MBE and MBS in *4 and *5.
4. *6 to *10 indicate accessible area.

(4) Explanation of machine cycle column

"S" indicates the number of machine cycles required when an instruction with a skip function performs a skip operation. The value of "s" is as follows:

- When a skip is not performed ..... S = 0
- When the skipped instruction is a 1-byte or 2-byte instruction ..... S = 1
- When the skipped instruction is a 3-byte instruction (BR !addr or CALL !addr) ..... S = 2

Note A GETI instruction is skipped in one machine cycle.

One machine cycle is equivalent to one cycle (=t_{CY})of the CPU clock cycle Φ : any of four times can be selected according to the PCC setting.

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		Stack A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		Stack A
		HL, #n8	2	2	HL ← n8		Stack B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ↔ (HL), then L← L –1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A,reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Note 2	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		

Note 1. Instruction Group

2. Table reference

Note	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← (H + mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0})) ← CY	*5	
		@H + mem.bit, CY	2	2	(H + mem_{3-0}.bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA – rp'		borrow
		rp'1, XA	2	2 + S	rp'1← rp'1 – XA		borrow
	SBUC	A, @HL	1	1	A , CY← A – (HL) – CY	*1	
		XA, rp'	2	2	XA, CY← XA – rp' – CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 – XA – CY		
	AND	A, #n4	2	2	A←A ∧ n4		
		A, @HL	1	1	A←A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1← rp'1 ∧ XA		
	OR	A, #n4	2	2	A←A ∨ n4		
		A, @HL	1	1	A←A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A←A ∀ n4		
		A, @HL	1	1	A←A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∇ rp'		
		rp'1, XA	2	2	rp'1← rp'1 ∀ XA		

Note Instruction Group

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Note 3	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp'	2	2 + S	rp' ← rp' – 1		rp' = FFH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Note 4	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Note 1. Instruction Group
2. Accumulator operation
3. Increment and decrement
4. Carry flag manipulation

Note	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 1	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) ← 0	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))= 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∨̄ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨̄ (pmem$_{7-2}$ + L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨̄ (H + mem$_{3-0}$.bit)	*1	
Branch	BR	addr	—	—	PC$_{13-0}$ ← addr (The assembler selects the optimum instruction from among the BRCB !caddr, and BR $addr instructions.)	*6	
	BR	!addr	3	3	PC$_{13-0}$ ← addr	*6	
	BRCB	!caddr	2	2	PC$_{13-0}$ ← PC $_{13.12}$ + caddr$_{11-0}$	*8	
	BR	$addr	1	2	PC$_{13-0}$ ← addr	*7	
	BR	PCDE	2	3	PC$_{13-0}$ ← PC $_{13-8}$ + DE		
		PCXA	2	3	PC$_{13-0}$ ← PC $_{13-8}$ + XA		

Note Instruction Group

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALL	!addr	3	3	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13-12} PC_{13-0} ← addr, SP ← SP – 4	*6	
	CALLF	!faddr	2	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, PC_{13-12} PC_{13-0} ← 000 + faddr, SP ← SP – 4	*9	
	RET		1	3	MBE, RBE, PC_{13-12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4		
	RETS		1	3 + S	MBE, RBE, PC_{13-12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4 the skip unconditionally		Unconditional
	RETI		1	3	×, ×, PC_{13-12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Note 2	EI		2	2	IME (IPS.3) ← 1		
		IE×××	2	2	IE ××× ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IE×××	2	2	IE ××× ← 0		
Input/Output	IN*1	A, PORTn	2	2	A ← $PORT_n$ (n = 0–8)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$, $PORT_n$ (n = 4, 6)		
	OUT*1	PORTn, A	2	2	$PORT_n$ ← A (n = 2–8)	*10	
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA (n =4, 6)		
Note 3	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0–3)		
		MBn	2	2	MBS ← n (n = 0,1,2,15)		
	GETI*2	taddr	1	3	• TBR Instruction PC_{13-0} ← (taddr) $_{5-0}$ + (taddr + 1)		
					• TCALL Instruction (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, $PC_{13, 12}$ PC_{13-0} ← (taddr) $_{5-0}$ ← (taddr + 1) SP ← SP – 4		
					• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.

* **1.** At IN/OUT instruction execution, MBE = 0 or MBE = 1, MBS = 15 must be set in advance.
2. TBR and TCALL instructions are assembler pseudo-instructions for table definition.

Note **1.** Instruction Group
2. Interruput control
3. CPU control

4. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY OPERATIONS

The program memory incorporated in the μPD75P336 is 32640 × 8-bit electrically writable one-time PROM. Write/verify operations on this one-time PROM are executed using the pins shown in the table below.

Address updating is performed by means of clock input from the X1 pin rather than by address input.

Pin Name	Function
V_{PP}	Voltage applecation pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock inputs for program memory write/verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pin for program memory write/verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for progrm memory write/verify.
V_{DD}	Supply voltage application pin. Applies 2.7 to 6.0 V in normal operation, and 6 V for program memory write/verify.

Note 1. Pins not used in a program memory write/verify operation are handled as follows:

- **Pins other than XT2 ..... Connect to V_{SS} with a pull-down resistor**
- **XT2 pins ..... Leave open**

2. Since the μPD75P336 is not provided with an erase window, program memory contents cannot be erased with ultra-violet light.

4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P336 enters the program memory write/verify mode. This mode comprises one of the operating modes shown below according to the setting of pins MD0 to MD3.

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

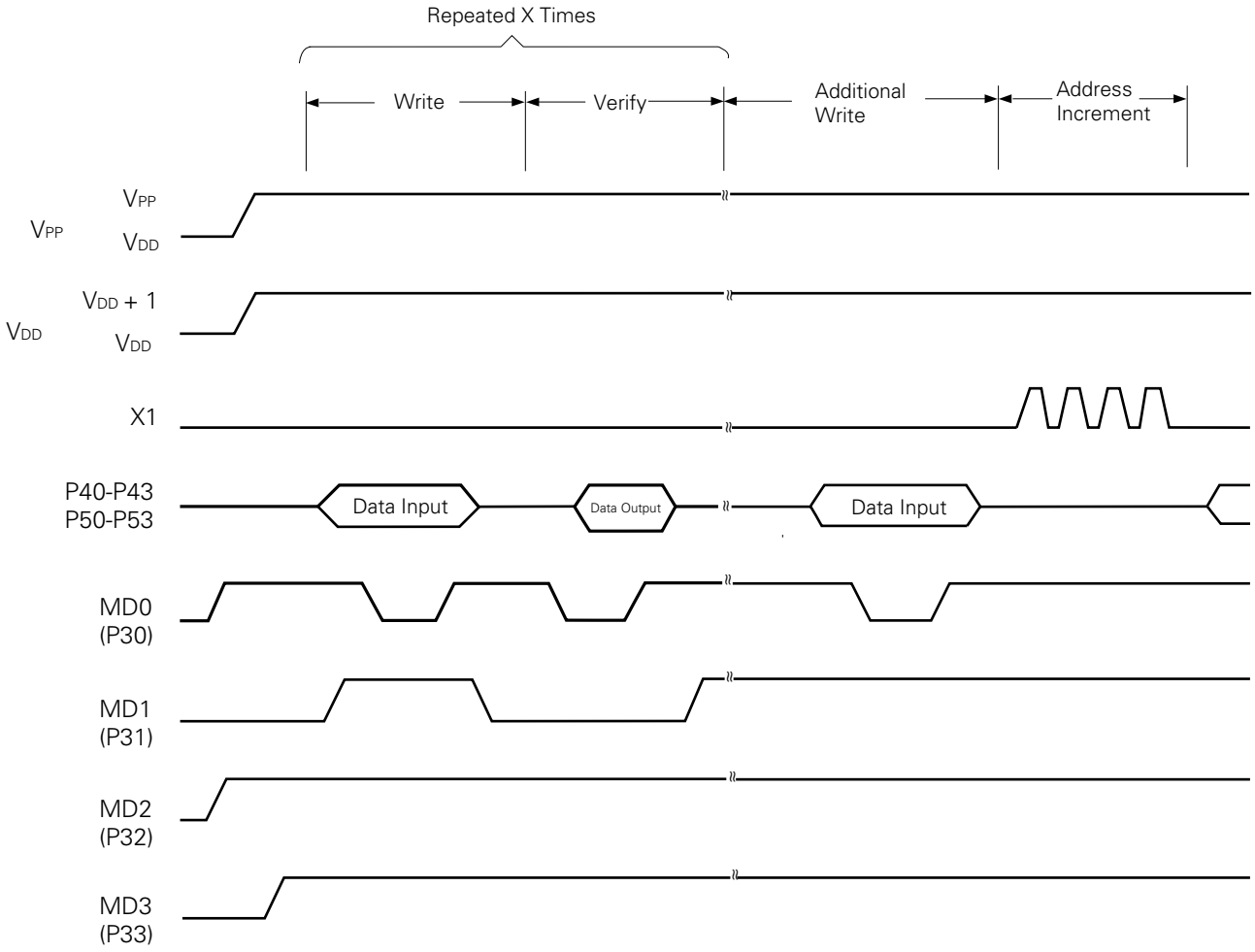
X: L or H

4.2 PROGRAM MEMORY WRITE PROCEDURE

The procedure for writing to program memory is as shown below, allowing high-speed writing.

(1) Unused pins are connected to V_{SS} with a pull-down resistor. The X1 pin is driven low.
(2) 5 V is supplied to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) Program memory address zero-clear mode.
(5) 6 V is supplied to V_{DD}, 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Data is written in 1 ms write mode.
(8) Program inhibit mode.
(9) Verify mode. If write is successful go to (10), otherwise repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) × 1 ms additional writes.
(11) Program inhibit mode.
(12) Program memory address is updated (+1) by inputting 4 pulses to the X1 pin.
(13) Steps (7) to (12) are repeated until the last address.
(14) Program memory address zero-clear mode.
(15) V_{DD}/ V_{PP} pin voltage is changed to 5 V.
(16) Power-off.

Steps (2) to (12) of this procedure are shown in the figure below.

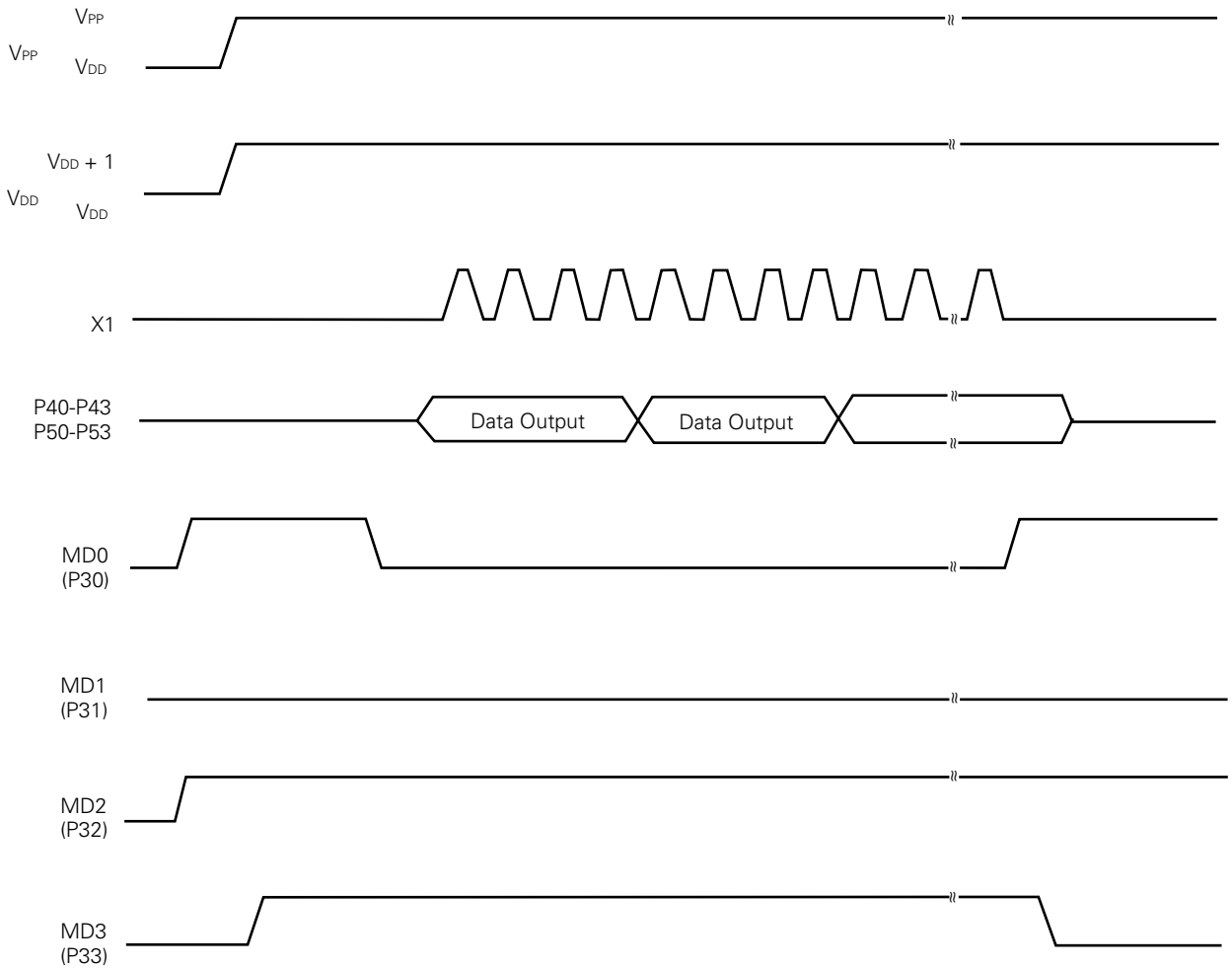


4.3 PROGRAM MEMORY READ PROCEDURE

μPD75P336 program memory contents can be read using the following procedure.

(1) Unused pins are connected to V_{SS} with a pull-down resistor. The X1 pin is driven low.
(2) 5 V is supplied to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) Program memory address zero-clear mode.
(5) 6 V supplied to V_{DD}, and 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Verify mode. When clock pulses are input to the X1 pin, data is output sequentially, one address per 4-pulse-input cycle.
(8) Program inhibit mode.
(9) Program memory address zero-clear mode.
(10) V_{DD} / V_{PP} pin voltage is changed to 5 V.
(11) Power-off.

Steps (2) to (9) of this procedure are shown in the figure below.



5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

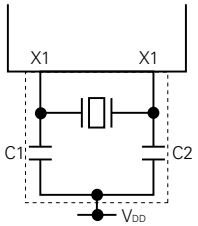
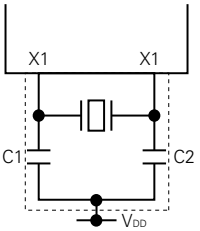
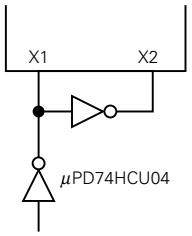
PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
★ Power supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
Input voltage	V_{I1}	Except ports 4, 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5	Open-drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	1 pin		–15	mA
		All pins		–30	mA
Output current low	I_{OL}*	1 pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 3, 5, 18	Peak value	100	mA
			Effective value	60	mA
		Total of ports 4, 6, 7	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* Rms value is calculated from [effective value] = [peak value] × $\sqrt{\text{duty}}$

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

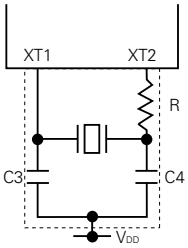
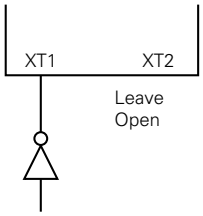
ESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_x)***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time***2**	After V_{DD} reached the MIN. of the oscillator voltage range.			4	ms
Crystal resonator		Oscillator frequency (f_x)***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_x)***1**		1.0		5.0***3**	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		100		500	ns

* **1.** Shows the oscillator characteristics only. For the instruction execution time, see the AC characteristics.

2. Time necessary for oscillation to stabilize after V_{DD} applied or STOP mode released.

3. When the oscillator frequency is "4.19 MHz < fx ≤ 5.0 MHz", it is impossible to select of "PCC = 0011" with 1 machine cycle of less than 0.95 μs as instruction execution time.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CONSTANT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high-/low-level width (t_{XTH},t_{XTL})		5		15	μs

Note When the main system clock and subsystem clock oscillation circuit are used, area inside doted lines in the figure should be wired as follows to prevent influence from the wiring capacitance, etc..

- **Wiring should be as short as possible.**
- **Do not cross other signal lines, and do not place the oscillator close to line in which varying high current flows.**
- **Potential at the oscillator capacitor connecting point should always be the same as V_{DD}. Do not connect to the power supply pattern in which high current flows.**
- **Do not fetch signals from the oscillator.**

In the subsystem clock oscillator, which is designed to be a circuit with low amplification ratio to suppress consumption current, misoperation due to noise occurs more often than in the main system clock oscillator. Therefore, when using the subsystem clock, special care should be taken in the wiring method.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/3)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Ports 2, 3, 8		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	Open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 4, 5, 8		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage high	V_{OH1}	Ports 0, 2, 3, 6, 7, 8 BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1 mA	V_{DD} –1.0			V
			I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (I_{OH} 2 outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –50 μA	V_{DD} –1.0			V

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (2/3)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output voltage low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6 7, 8	Ports 3, 4, 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.4	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1 resistor ≥ 1 kΩ	Open-drain pull-up			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (I_{OL} 2 outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4, 5 (when open-drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (when open-drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Built-in Pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 7, 8 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%	15	40	80	kΩ
			V_{DD} = 3.0 V ±10%	30		300	kΩ
LCD drive voltage	V_{LCD}			2.5		V_{DD}	V

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (3/3)

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
LCD output voltage deviation*1 (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$, $V_{LCD1} = V_{LCD} \times 2/3$, $V_{LCD2} = V_{LCD} \times 1/3$, 2.7 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2V	V
LCD output voltage deviation*1 (segment)	V_{ODS}	I_O = ±1 μA			0		±0.2V	V
Power supply current *2	I_{DD1}	4.19 MHz crystal oscillation C1= C2 = 22 pF*3	V_{DD} = 5 V ±10 %*4			5	15	mA
			V_{DD} = 3 V ±10 %*5			1	3	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		500	1500	μA
				V_{DD} = 3 V ±10 %		300	900	μA
	I_{DD3}	32 kHz crystal oscillation*6	Operating mode	V_{DD} = 3 V ±10 %		100	300	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10 %		20	60	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10 %			0.5	20	μA
			V_{DD} = 3 V ±10 %			0.1	10	μA
				T_a = 25 °C		0.1	5	μA

* **1.** The voltage deviation means a difference between the ideal value of segment or common output (V_{LCDn}; n = 0, 1, 2) and the output voltage.

2. Current flowing in the built-in pull-up resistor and the LCD split resistor is not include.

3. Including the case where the subsystem clock is operating.

4. When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.

5. When PCC is set to 0000 and operated in the low-speed mode.

6. The case where the system clock control register (SCC) is set to 1001, the main system clock oscillatio stopped and the device is operated on the subsystem clock.

A/D CONVERTER CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
Resolution					8	8	8	bit
Absolute accuracy***1**		2.5 V ≤ AV_{REF} ≤ V_{DD} AV_{REF} ≥ 0.6 V_{DD}	–10 ≤ Ta ≤ + 85 °C				±1.5	LSB
			–40 ≤ Ta < –10 °C				±2.0	
		2.5 V ≤ AV_{REF} ≤ V_{DD} AV_{REF} < 0.6 V_{DD}	t_{CY} ≥ 1.91 μs	–10 ≤ Ta ≤ + 85 °C			±1.5	
				–40 ≤ Ta ≤ – 10 °C			±2.0	
			t_{CY} < 1.91 μs	–40 ≤ Ta ≤ + 85 °C			±3.0	
Conversion time	t_{CONV}	***2**					168/fx	s
Sampling time	t_{SAMP}	***3**					44x	s
Analog input voltage	V_{IAN}				AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}					1000		MΩ
AV_{REF} current	I_{REF}					1.0	2.0	mA

* **1.** Absolute accuracy excluding quantization (±1/2LSB) error.

2. Time up to end of conversion (EOC = 1) after execution of the conversion start instruction.
(40.1 μs: fx = 4.19 MHz operation)

3. Time up to end of sampling after execution of the conversion start instruction.
(10.5 μs: fx = 4.19 MHz operation)

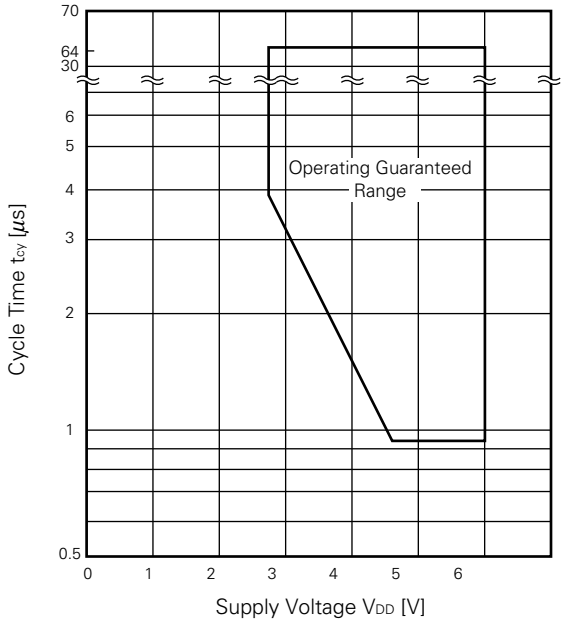
AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)***1**	t_{CY}	Operated by main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operated by subsystem clock		114	122	125	μs
TI0, 1 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0, 1 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

*** 1.** The CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator and the system clock control register (SCC) and the processor clock control register (PCC). The figure below shows the main system clock operation power supply voltage V_{DD} vs cycle time t_{CY} characteristics.

2. Becomes $2t_{CY}$ or 128/f_X depending on the interrupt mode register (IM0) setting.

t_{CY} vs V_{DD}
(Operating on Main System Clock)



SERIAL TRANSFER OPERATION

2-wired and 3-wired serial I/O modes ($\overline{SCK}$ ... Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL1}, t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1} /2-50			ns
				t_{KCY1} /2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

2-wired and 3-wired serial I/O modes ($\overline{SCK}$ ... External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL2}, t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are the SO output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$ ... Internal clock output (master))

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3} /2-50			ns
	t_{KH3}			t_{KCY3} /2-150			ns
SB0,1 setup time (to $\overline{SCK}$↑)	t_{SIK3}			150			ns
SB0,1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0,1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ , C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0,1 ↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, 1 ↓	t_{SBK}			t_{KCY3}			ns
SB0,1 low level width	t_{SBL}			t_{KCY3}			ns
SB0,1 high level width	t_{SBH}			t_{KCY3}			ns

* R_L and C_L are the SB0 and SB1 output line load resistance and load capacitance, respectively.

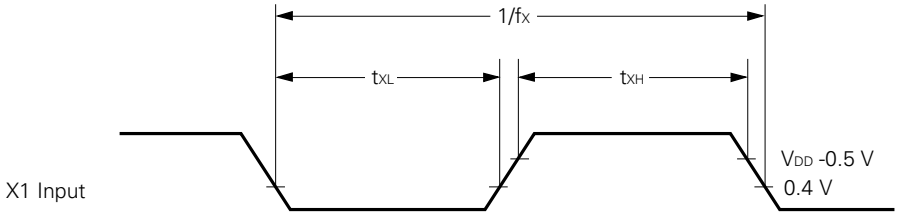
SBI mode ($\overline{SCK}$ ... External clock input (slave))

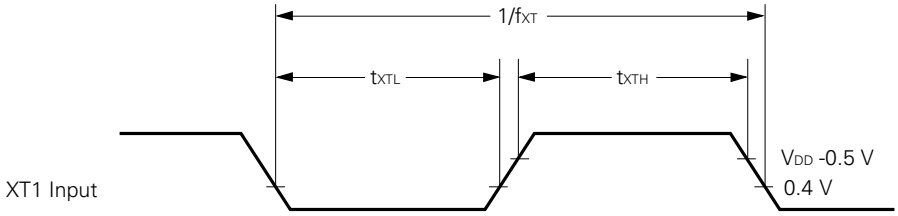
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0,1 setup time (to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0,1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0,1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0,1 ↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, 1 ↓	t_{SBK}			t_{KCY4}			ns
SB0,1 low level width	t_{SBL}			t_{KCY4}			ns
SB0,1 high level width	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are the SB0 and SB1 output line load resistance and load capacitance, respectively.

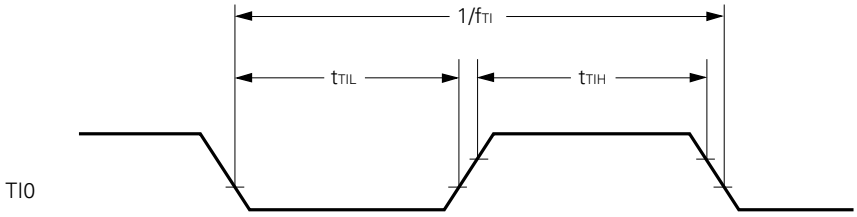
AC Timing Test Point(Exculuding X1 and XT1 Inputs)

Clock Timings



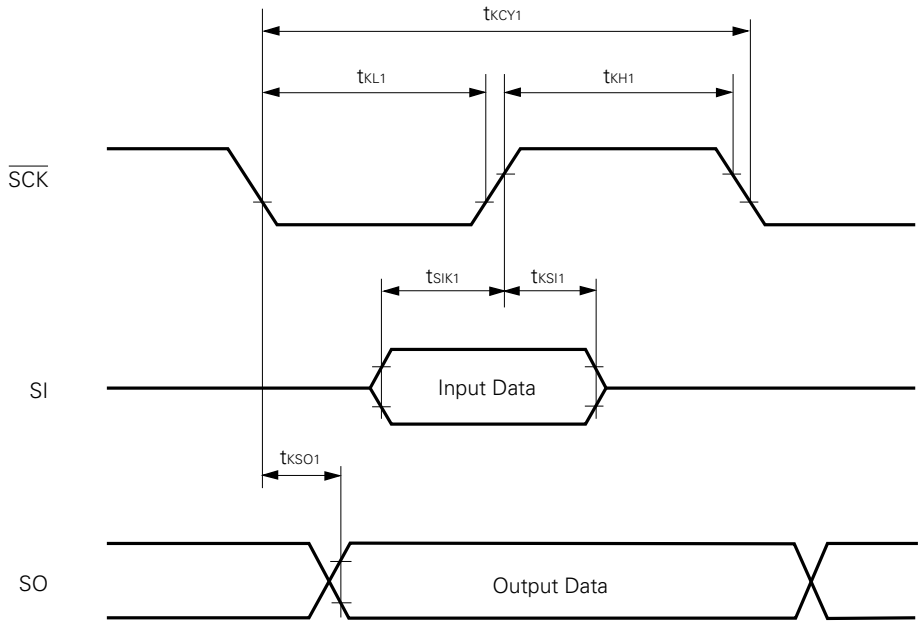


TI0 Timing

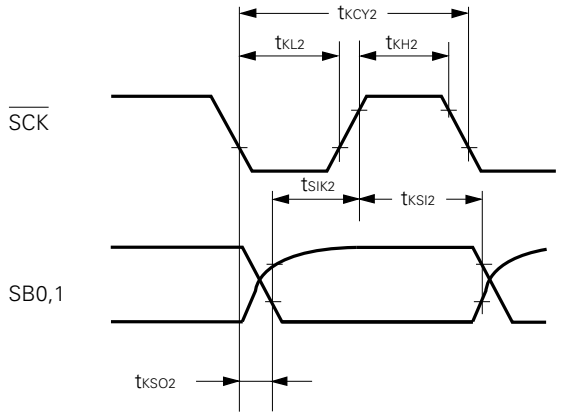


Serial Transfer Timing

3-wired serial I/O mode:

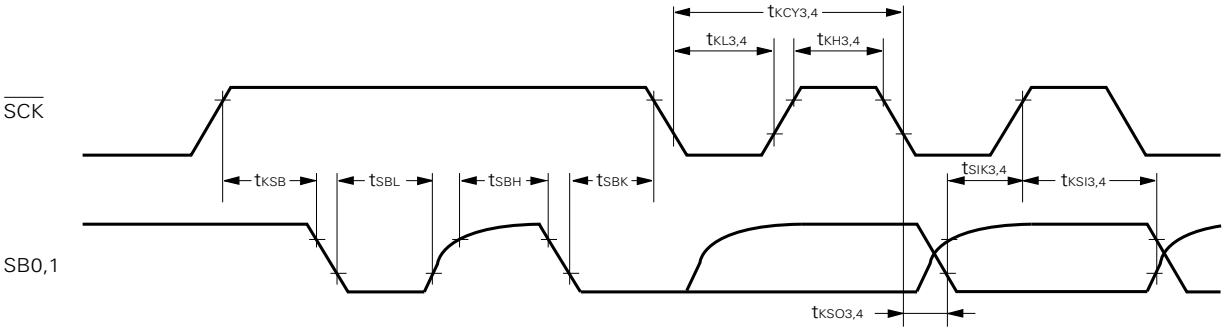


2-wired serial I/O mode:

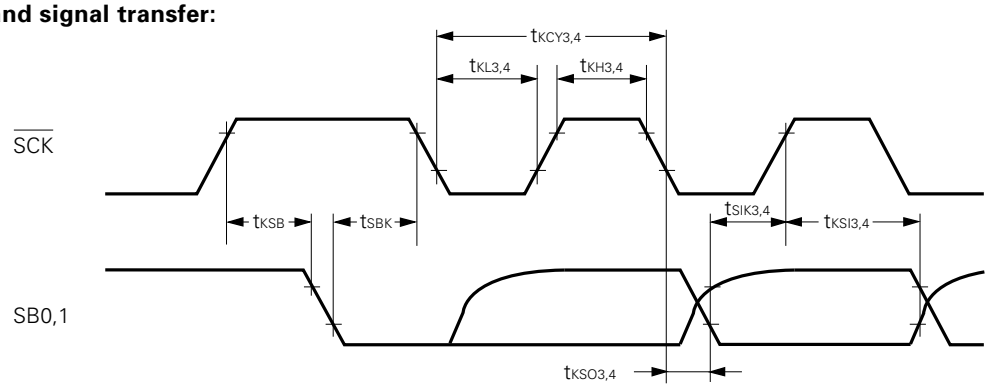


Serial Transfer Timing

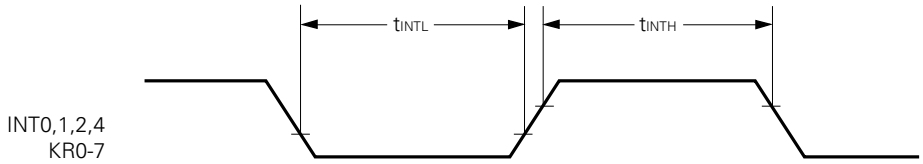
Bus release signal transfer:



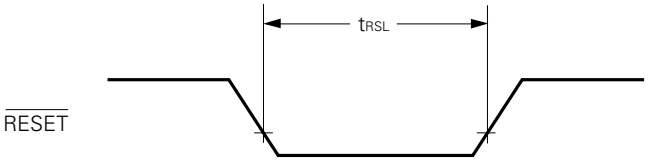
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DAT RETENTION CHARACTERISTICS (Ta = –40 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time***2**	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt request		***3**		ms

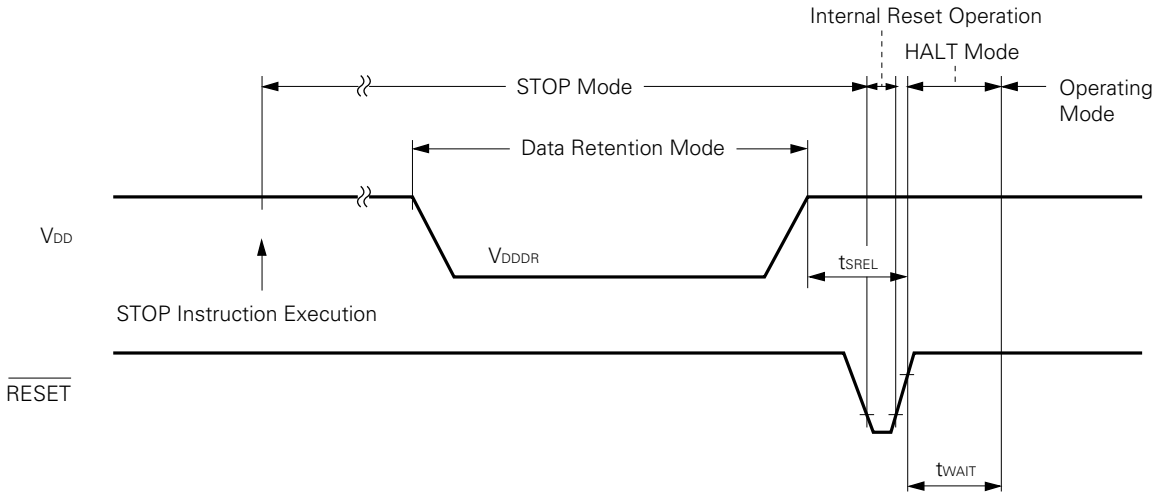
* **1.** Current flng in the built-in pull-up resistor is not included.

2. The oscillation stabilization wait time is the time CPU operation is stopped to prevent unstable operation at start of oscillation.

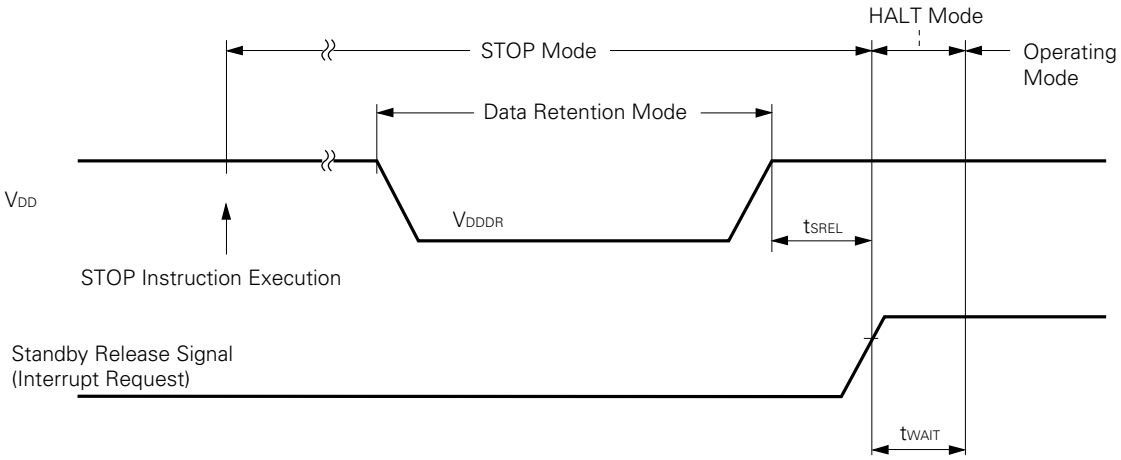
3. Depends on the basic interval timer mode register (BTM) setting (table below).

BTM3	BTM2	BTM1	BTM0	Waite Time (Figures in parentheses are for operation at fxx = 4.19 MHz)
—	0	0	0	2^{20}/fxx (approx. 250 ms)
—	0	1	1	2^{17}/fxx (approx. 31.3 ms)
—	1	0	1	2^{15}/fxx (approx. 7.82 ms)
—	1	1	1	2^{13}/fxx (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



D/C PROGRAMING CHARACTERISTICS (Ta = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1, X2	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} -0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1, X2	0		0.3V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	V_{L1}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD} -1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL} , MD1 = V_{IH}			30	mA

* **1.** V_{PP} must not exceed +13.5 V including overshoot.
2. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

A/D PROGRAMING CHARACTERISTICS (Ta = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V) (1/2)

PARAMETER	SYMBOL	*1	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Address setup time *2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{MIS}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time *2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0↑	t_{DF}	t_{DF}		0		130	μs
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms

* **1.** Symbol of the corresponding μPD27C256.
2. The internal address signal is incremented (+1) at the rising edge of the forth X1 input. The signal is not connected to pins.

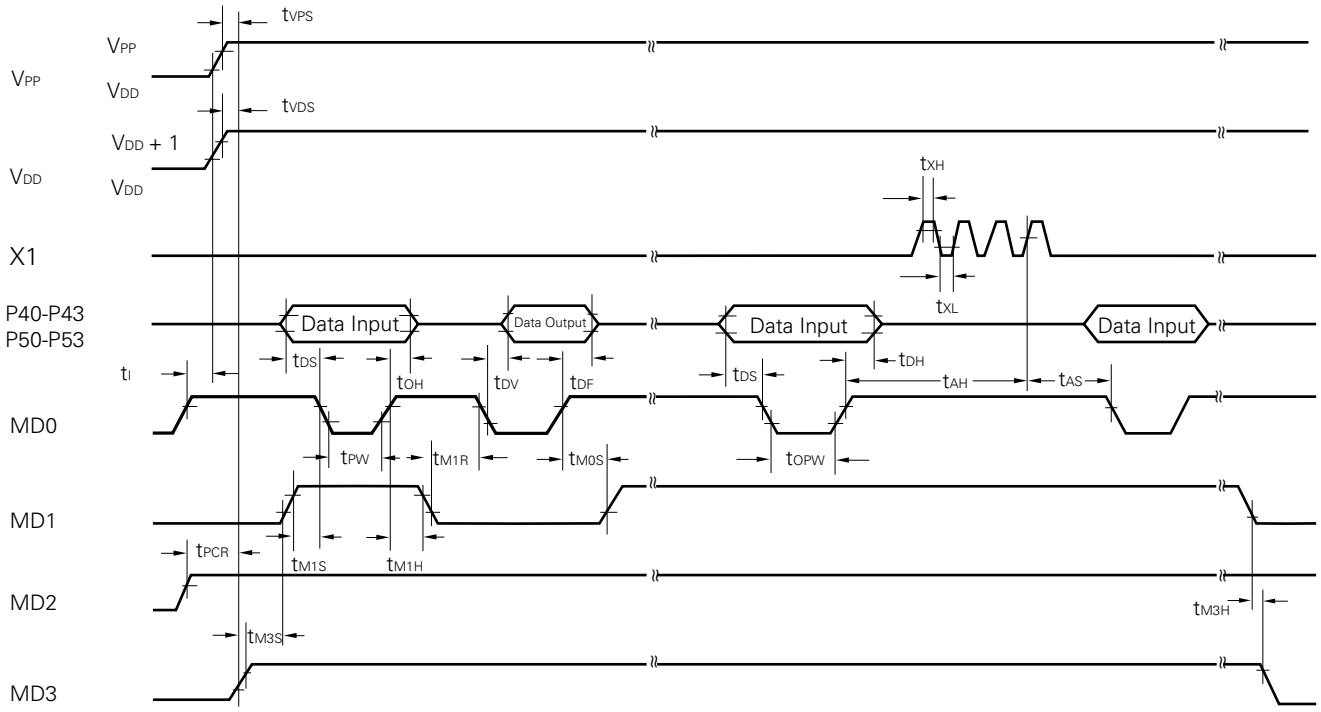
A/D PROGRAMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V) (2/2)

PARAMETER	SYMBOL	*1	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recover time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program conuter reset time	t_{PCR}	—		10			μs
X1 input high/low width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	fx	—				4.19	MHz
Initial mode set time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (to MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0 ↓)	t_{M3SR}	—	Program memory read	2			μs
Data output delay time from address ***2**	t_{DAD}	t_{ACC}	Program memory read			2	μs
Data output hold time from address ***2**	t_{HAD}	t_{OH}	Program memory read	0		130	μs
MD3 hold time (from MD0↑)	t_{M3HR}	—	Program memory read	2			μs
Data output float delay time from MD3 ↓	t_{DFR}	—	Program memory read			2	μs

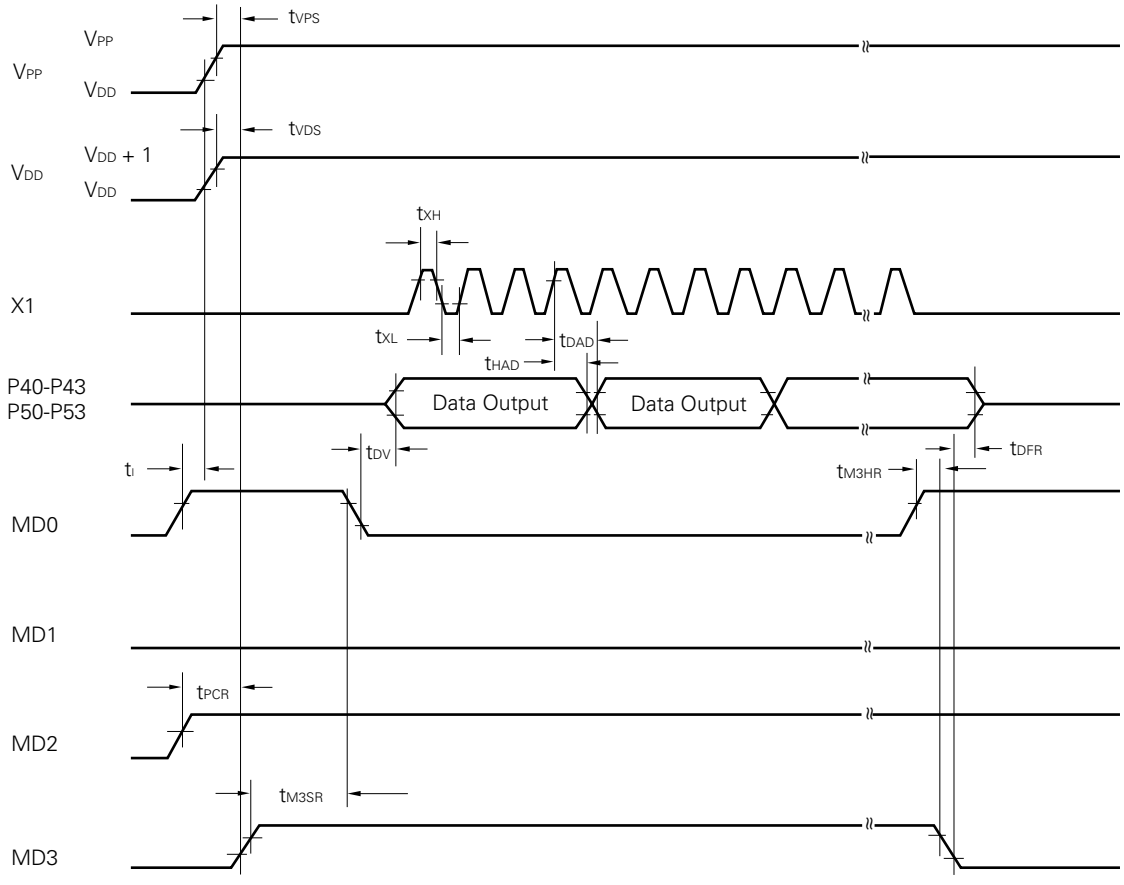
* **1.** Symbol of the corresponding μPD27C256.

2. The internal address signal is incremented (+1) at the rising edge of the fourth X1 input. The signal is not connected to pins.

Program Memory Write Timing mode:

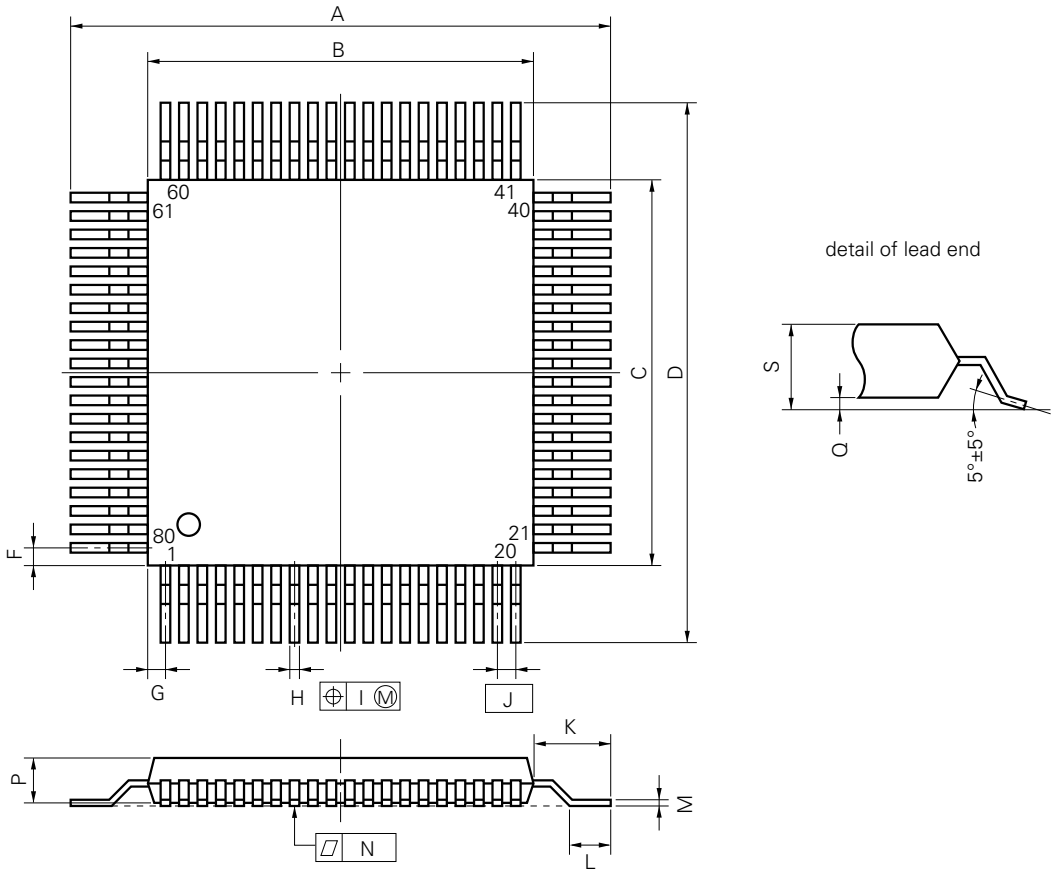


Program Memory Read Timing mode:



6. PACKAGE INFORMATION ★

80 PIN PLASTIC QFP (□14)



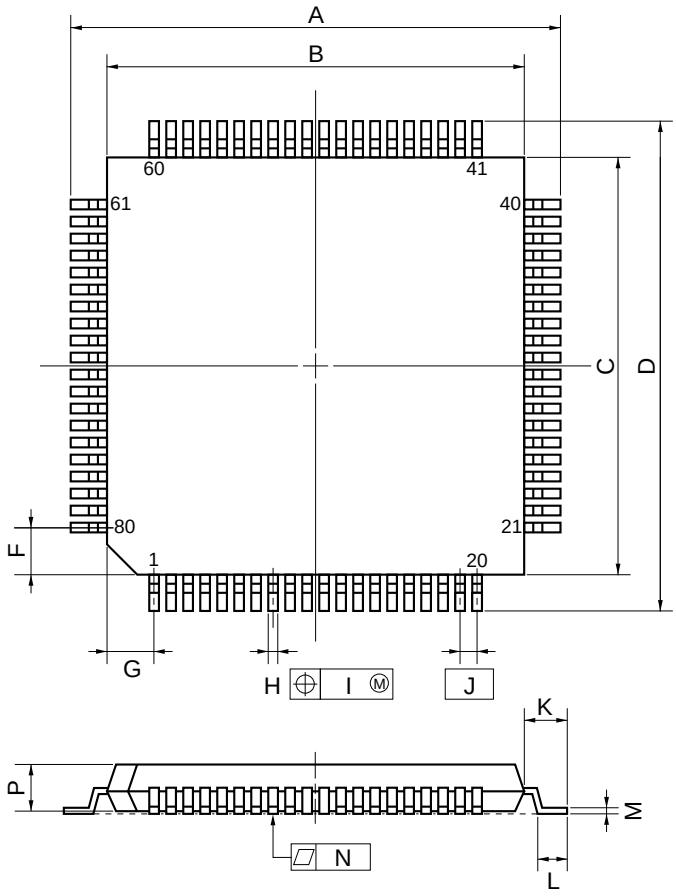
S80GC-65-3B9-3

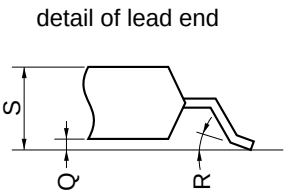
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

7. RECOMMENDED SOLDERING CONDITIONS ★

This product should be soldered and mounted under the conditions in the table below.

For detail of recommended soldering conditions, refer to the information document **"Surface Mount Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 7-1 Soldering Conditions

(1) μPD75P336GC-3B9 : 80-pin plastic QFP (□14mm)

Solderring Method	Solderring Conditions	Recommended Condition Symbol
Wave soldering	Solder bath temperature: 260 °C. max., Duration: 10 sec. max., Number of times: Once, Time limit: 2 days* (thereafter 20 hours prebaking required at 125 °C) Preheat temperature: 120 °C max. (package surface temperature)	WS60-202-1
Infrared reflow	Package Peak temperature: 230 °C, Duration: 30 sec. max., (at 210 °C or above), Number of times: Once, Time limit: 2 days* (thereafter 20 hours prebaking required at 125 °C)	IR30-202-1
VPS reflow	Package Peak temperature: 215 °C, Duration: 40 sec. max., (at 200 °C or above), Number of times: Once, Time limit: 2 days* (thereafter 20 hours prebaking required at 125 °C)	VP15-202-1
Pin part heating	Pin part temperature: 300 °C or below, Duration: 3 sec. max. (per device side)	——

(2) μPD75P336GK-BE9 : 80-pin plastic TQFP (fine pitch) (□12mm)

Solderring Method	Solderring Conditions	Recommended Condition Symbol
Infrared reflow	Package Peak temperature: 235 °C, Duration: 30 sec. max., (at 210 °C or above), Number of times: Once, Time limit: 1 day* (thereafter 10 hours prebaking required at 125 °C)	IR35-101-1
VPS reflow	Package Peak temperature: 215 °C, Duration: 40 sec. max., (at 200 °C or above), Number of times: Once, Time limit: 1 day* (thereafter 10 hours prebaking required at 125 °C)	VP15-101-1
Pin part heating	Pin part temperature: 300 °C or below, Duration: 3 sec. max. (per device side)	——

* For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

APPENDIX A. LIST OF FUNCTIONS

Item \ Name		μPD75336		μPD75P336	μPD75328
CPU core		75X-High End			75X-Standard
ROM (bytes)		16256 (mask ROM)		16256 (PROM)	8064 (mask ROM)
RAM (× 4 bits)		768			512
General registers		4 bits × 8 × 4 banks			4 bits × 8 × 1 bank
Instruction cycle	Main system clock	0.95 μs, 1.91 μs, 3.81 μs, 15.3 μs (at 4.19 MHz operation)			0.95 μs, 1.91 μs, 15.3 μs (at 4.19 MHz operation)
	Subsystem clock	122 μs (at 32.768 KHz operation)			
Input/ output ports	CMOS input	44	8	Internal pull-up resistor specifiable by software	
	CMOS input/output		20		
	CMOS output		8	Dual function as segment pins	
	N-ch open-drain input/output		8 (10 V withstand voltage, mask option pull-up capability)	Same as at left (but no pull-up resistor)	8 (10 V, withstand voltage mask option pull-up capability)
LCD controller/driver		Max.20 × 4 segment drive, variable duty: static, 1/2, 1/3, 1/4			
A/D converter		• 8-bit resolution × 8-ch (successive approximation type) • Low-voltage operation capability: V_{DD} = 2.7 to 6.0 V			• 8-bit resolution × 6-ch (successive approximation type) • Low-voltage operation capability: V_{DD} = 3.5 to 6.0 V
Timer/counter		• Basic interval timer × 1 • Timer/event counter × 2 • Watch timer × 1			• Basic interval timer × 1 • Timer/event counter × 1 • Watch timer × 1
Serial Interface		• NEC standard serial interface (SBI) • Clocked serial interface			
Vectored interrupt		External: 3 Internal: 4			External: 3 Internal: 3
Test input		External: 1 Internal: 1			External: 1 Internal: 1
Clock output (PCL)		Φ, 524kHz, 262kHz, 65.5kHz (at 4.19MHz operation)			
Buzzer output (BUZ)		2kHz, 4kHz, 32kHz			2kHz
8-bit data processing		Transfer, addition/subtraction, increment/decrement, comparison			Transfer
Operating voltage		V_{DD} = 2.7 - 6.0 V			
★ Package		80-pin plastic QFP (□14 mm) 80-pin plastic TQFP (fine pitch) (□12mm)			
On-chip PROM product		μPD75P336		—	μPD75P328

APPENDIX B. DEVELOPMENT TOOLS

The following support tools are available for system development using the μPD75P336.

Language Processor

	Host Machine	OS	Supply Medium	Ordering Code (Product Name)
RA75X relocatable assembler	PC-9800 series	MS-DOS™ Ver. 3.30 to Ver. 5.00A*	3.5-inch 2HD	μS5A13RA75X
			5-inch 2HD	μS5A10RA75X
	IBM PC/AT™	PC DOS™ (Ver. 3.1)	5-inch 2HC	μS7B10RA75X

Remarks Assembler operation is only guaranteed for the host machines and operating systems quoted above.

PROM Write Tools

Hardware	PG-1500	PROM programmer which enables a single-chip microcomputer with on-chip PROM to be programmed in stand-alone mode or by operations from a host machine by connection of the supplied board and a separately available programmer adapter. Typical PROMs from 256K bits to 4M bits can also be programmed.			
	PA-75P328GC	PROM programmer adapter for the μPD75P336GC, used connected to the PG-1500.			
	PA-75P336GK	PROM program adapter for the μPD75P336GK, used connect to the PG-1500.			
Software	PG-1500 controller	Controls the PG-1500 on the host machine, with the PG-1500 and host machine connected via a serial or parallel interface.			
		Host Machine	OS	Supply Medium	Ordering Code (Product Name)
		PC-9800 series	MS-DOS Ver. 3.30 to Ver. 5.00A*	3.5-inch 2HD	μS5A13PG1500 ★
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10PG1500

* The task-swap function is provided with Ver.5.00/5.00A, but the function cannot be used with this software. ★

Remarks PG-1500 controller operation is only guaranteed for the host machines and operating systems quoted above.

Debugging Tools

Hardware	IE-75000-R***1**	The IE-75000-R is an in-circuit emulator which corresponds to the 75X series. For μPD75P336 development the IE-75000-R is used in conjunction with an emulation probe. Efficient debugging is possible by connection to a host machine and PROM programmer.		
	IE-75000-R-EM	Emulation board for the IE-75000-R and IE-75001-R. Incorporated in the IE-75000-R. Used in conjunction with the IE-75000-R or IE-75001-R to perform μPD75P336 evaluation.		
	IE-75001-R	The IE-75001-R is an in-circuit emulator which corresponds to 75X series. For μPD75P336 development the IE-75001-R is used in conjunction with an emulation board IE-75000-R-EM***2** and emulation probe. Efficient debugging is possible by connection to a host machine and PROM programer.		
	EP-75338GC-R	Emulation probe for μPD75P336GC. Used connect with the IE-75000-R or IE-75001-R, IE-75000-R-EM.		
	EV-9200G-80	An 80-pin LCC socket (EV-9200GC-80) is also available to simplify connection to the user system.		
	EP-75336GK-R	Emulation probe for μPD75336GK. Used connected with the IE-75000-R or IE-75001-R, IE-75000-R-EM. An 80-pin conversion adapter (EV-9500GK-80 is also available to simplify connection to the user system.		
	EV-9500GK-80			
Software	IE control program	Connects the IE-75000-R or IE-75001-R to the host machine via by RS-232-C and contronix I/F and controls the IE-75000-R or IE-75001-R on the host machine.		
		Host Machine	OS	Supply Medium / Ordering Code (Product Name)
		PC-9800 series	MS-DOS Ver. 3.30 to Ver. 5.00A***3**	3.5-inch 2HD: μS5A13IE75X
				5-inch 2HD: μS5A10IE75X
		IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC: μS7B10IE75X

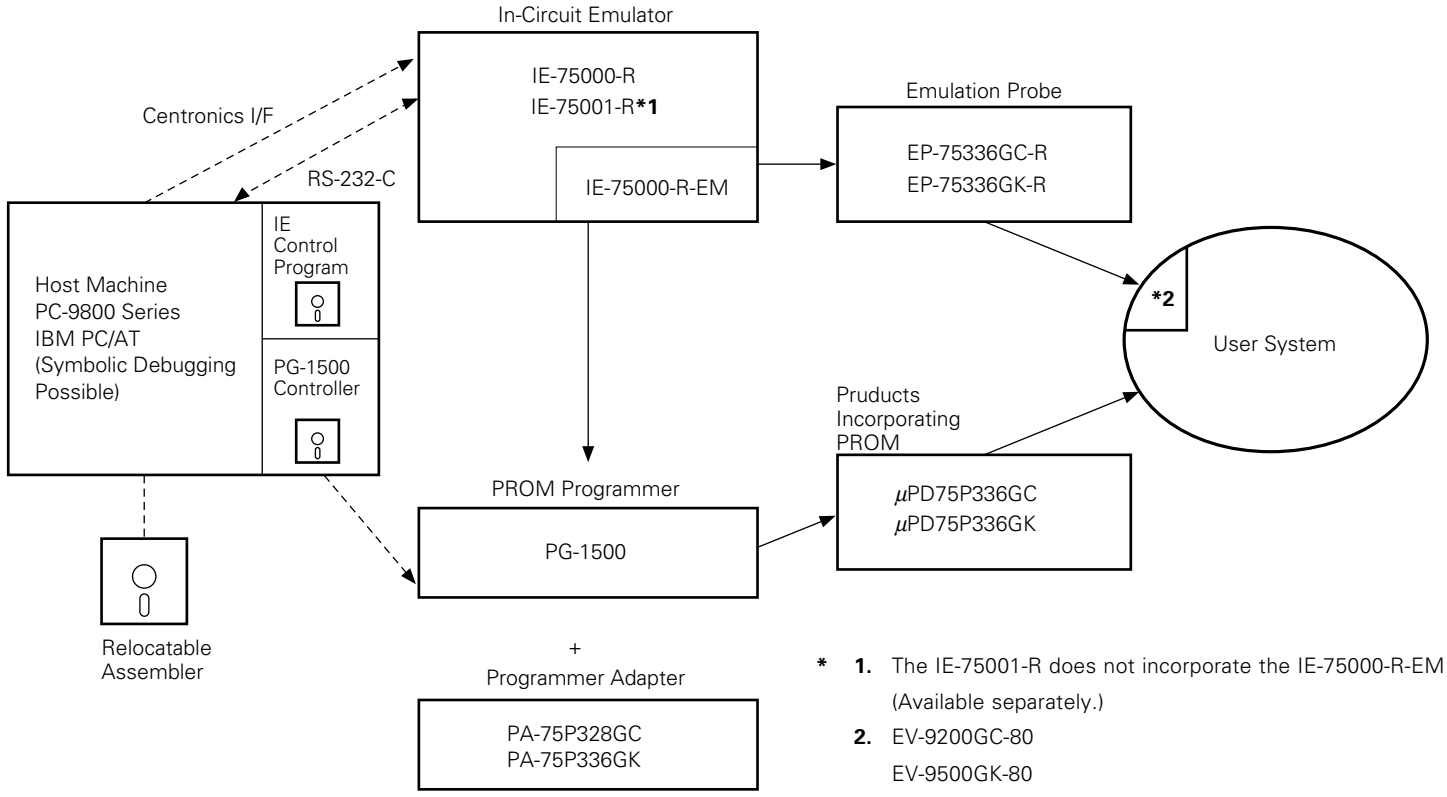
* **1.** Maintenance product

2. IE-75000-R-EM sold sparately

★ **3.** The task-swap function is provided with Ver.5.00/5.00A, but the function cannot be used with this software.

Remarks Operations of the IE control program is only guaranteed for the host machines and operating systems quoted above.

Development Tools Configuration ★



* **1.** The IE-75001-R does not incorporate the IE-75000-R-EM (Available separately.)

2. EV-9200GC-80
EV-9500GK-80

[MEMO]

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