

# BIPOLAR ANALOG INTEGRATED CIRCUIT

# $\mu$ PC1854A

## I<sup>2</sup>C BUS-COMPATIBLE US MTS PROCESSING LSI

The  $\mu$ PC1854A is an integrated circuit for US MTS (Multichannel Television Sound) system with the addition of the I<sup>2</sup>C bus interface. All functions required for US MTS system are incorporated on a single chip.

The  $\mu$ PC1854A allows users to switch modes and adjust filter and separation circuits through the I<sup>2</sup>C bus.

### FEATURES

- Stereo demodulation, SAP (Sub Audio Program) demodulation, dbx noise reduction decoding, and I<sup>2</sup>C bus interface incorporated on a single chip
- Mode switching and filter/separation adjustments through the I<sup>2</sup>C bus
- Power supply: 8 V to 10 V
- On-chip input attenuator for simple interface with intermediate frequency processing IC (I<sup>2</sup>C bus control)
- Output level: 1.4 V<sub>p-p</sub> (with L+R signals, 100% modulation)

### APPLICATIONS

- TV sets and VCRs for north America

### ORDERING INFORMATION

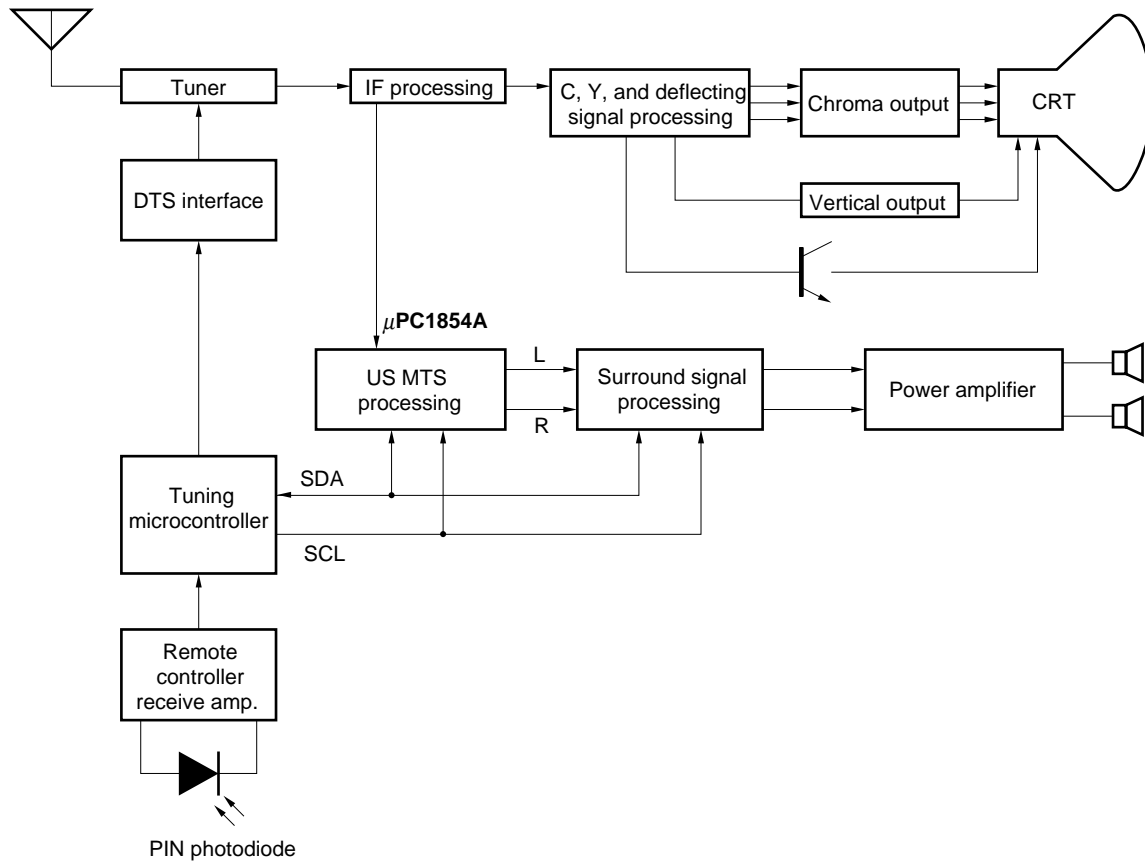
Part Number	Package
$\mu$ PC1854ACT	28-pin plastic SDIP (10.16 mm (400))
$\mu$ PC1854AGT	28-pin plastic SOP (9.53 mm (375))

**The  $\mu$ PC1854A is available only to licensees of THAT Corporation.**

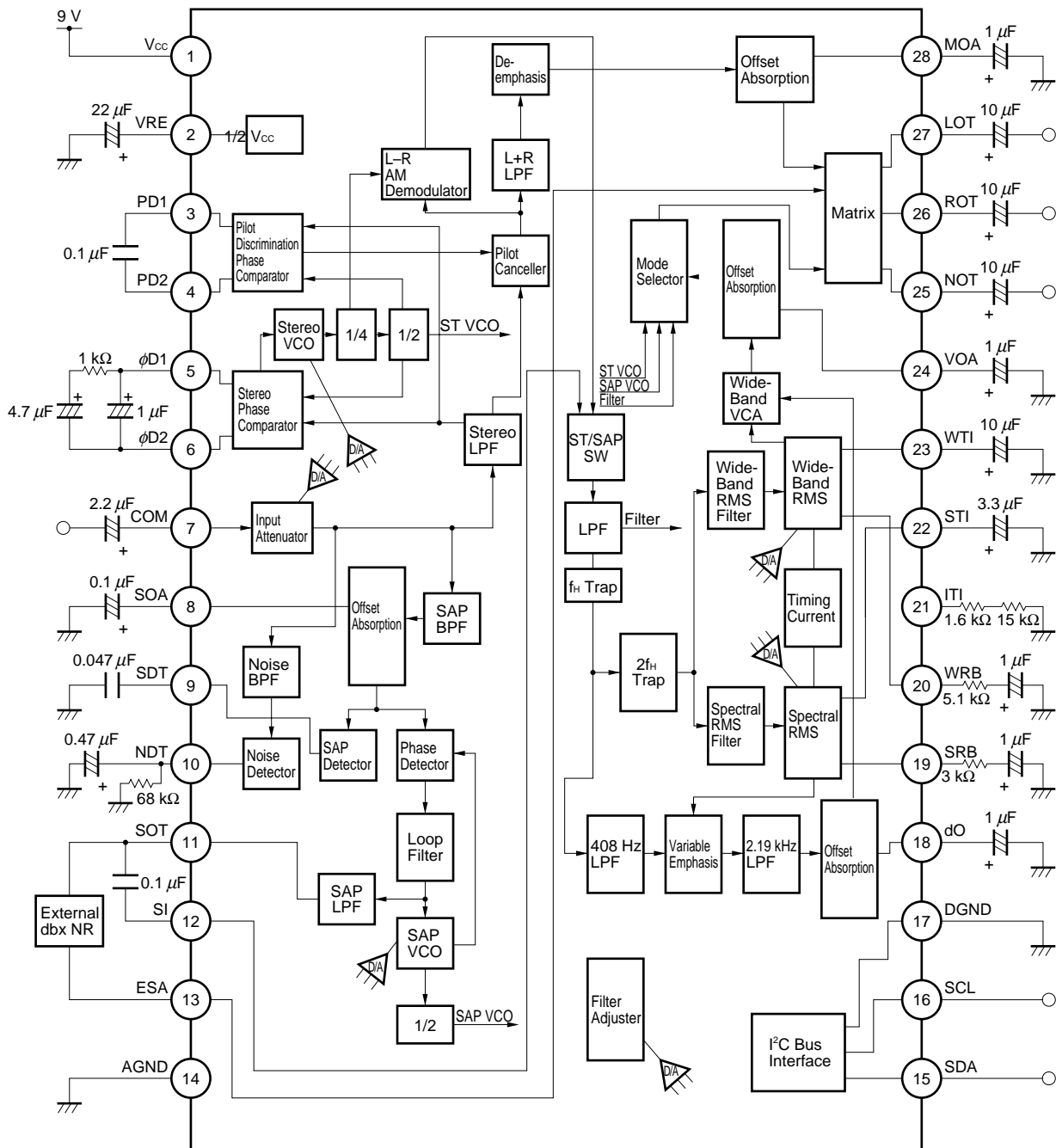
**For information, please call: (508) 229-2500 (U.S.A.), or (03) 5790-5391 (Tokyo).**

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



**Remark** Use the following for external parts.

Resistor : Metal film resistor ( $\pm 1\%$ ) for an ITI pin (pin 21). Unless otherwise specified;  $\pm 5\%$

Capacitor : Tantalum capacitor ( $\pm 10\%$ ) for STI and WTI pins (pins 22 and 23). Unless otherwise specified;  $\pm 20\%$

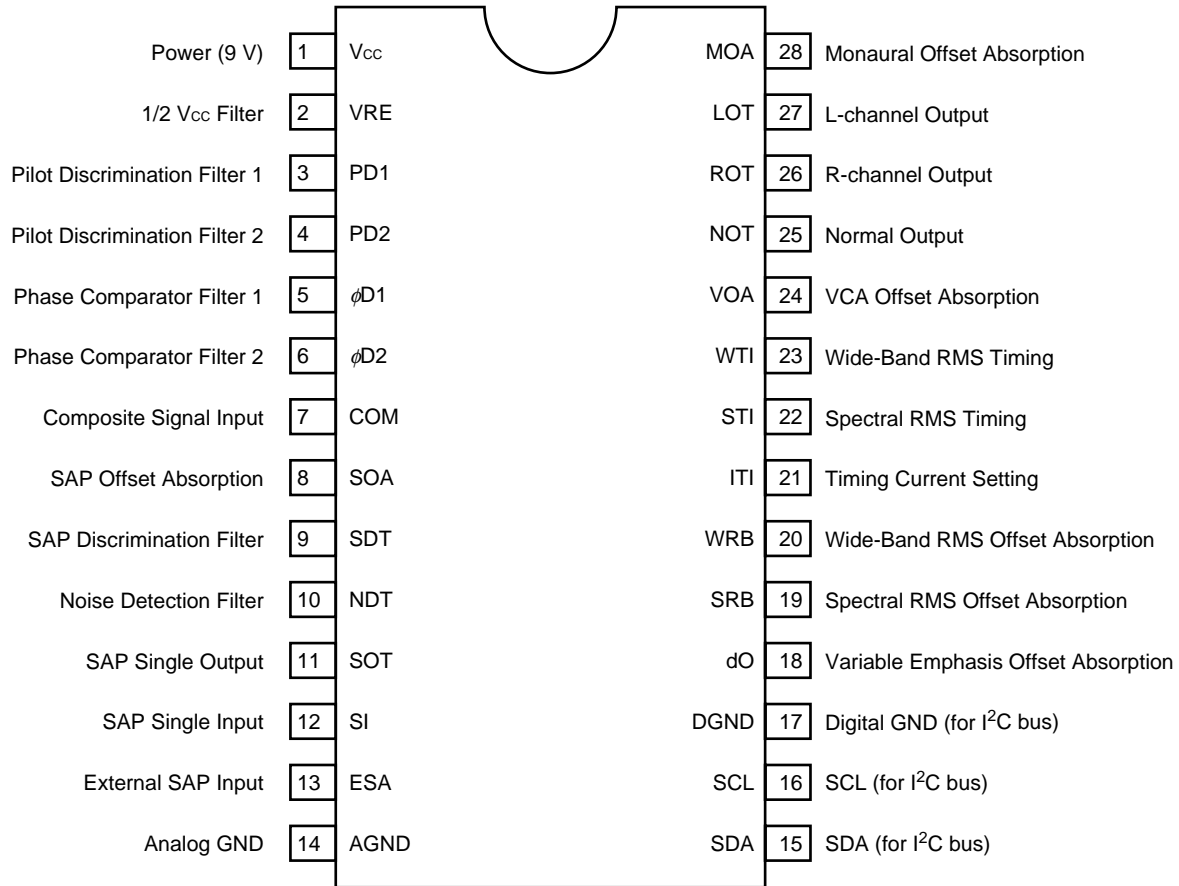
**PIN CONFIGURATION (Top View)**

**28-pin plastic SDIP (10.16 mm (400))**

- μPC1854ACT

**28-pin plastic SOP (9.53 mm (375))**

- μPC1854AGT



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1. PIN EQUIVALENT CIRCUITS

(1/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
1	Power (9 V)	Vcc	
2	1/2 Vcc Filter	VRE	
3	Pilot Discrimination Filter 1	PD1	
4	Pilot Discrimination Filter 2	PD2	

(2/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
5	Phase Comparator Filter 1	$\phi D1$	
6	Phase Comparator Filter 2	$\phi D2$	
7	Composite Signal Input	COM	
8	SAP Offset Absorption	SOA	

(3/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
9	SAP Discrimination Filter	SDT	
10	Noise Detection Filter	NDT	



Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
11	SAP Single Output	SOT	
12	SAP Single Input	SI	
13	External SAP Input	ESA	

(5/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
14	Analog GND	AGND	
15	SDA (for I <sup>2</sup> C bus)	SDA	<p><b>Note</b></p>
16	SCL (for I <sup>2</sup> C bus)	SCL	<p><b>Note</b></p>
17	Digital GND (for I <sup>2</sup> C bus)	DGND	
18	Variable Emphasis Offset Absorption	dO	Same as Pin 8
19	Spectral RMS Offset Absorption	SRB	

**Note** No protection diode is provided on the Vcc side so that the I<sup>2</sup>C bus line is not pulled to 0 V when the power is OFF (Vcc = 0 V).

(6/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
20	Wide-Band RMS Offset Absorption	WRB	Same as pin 19
21	Timing Current Setting	ITI	
22	Spectral RMS Timing	STI	
23	Wide-Band RMS Timing	WTI	Same as pin 22
24	VCA Offset Absorption	VOA	Same as pin 8

(7/7)

Pin No.	Pin Name	Symbol	Internal Equivalent Circuit
25	Normal Output	NOT	
26	R-channel Output	ROT	Same as pin 25
27	L-channel Output	LOT	
28	Monaural Offset Absorption	MOA	Same as pin 8

2. BLOCK FUNCTIONS

In the US, TV audio signals are broadcast in FM modulation. The stereo (L–R), Sub Audio Program (SAP) and telemetry signals are multiplexed in a higher frequency band than the monaural (L+R) signal (50 Hz to 15 kHz).

The US MTS system base-band spectrum is described before:

Figure 2-1. US MTS System Base-Band Spectrum

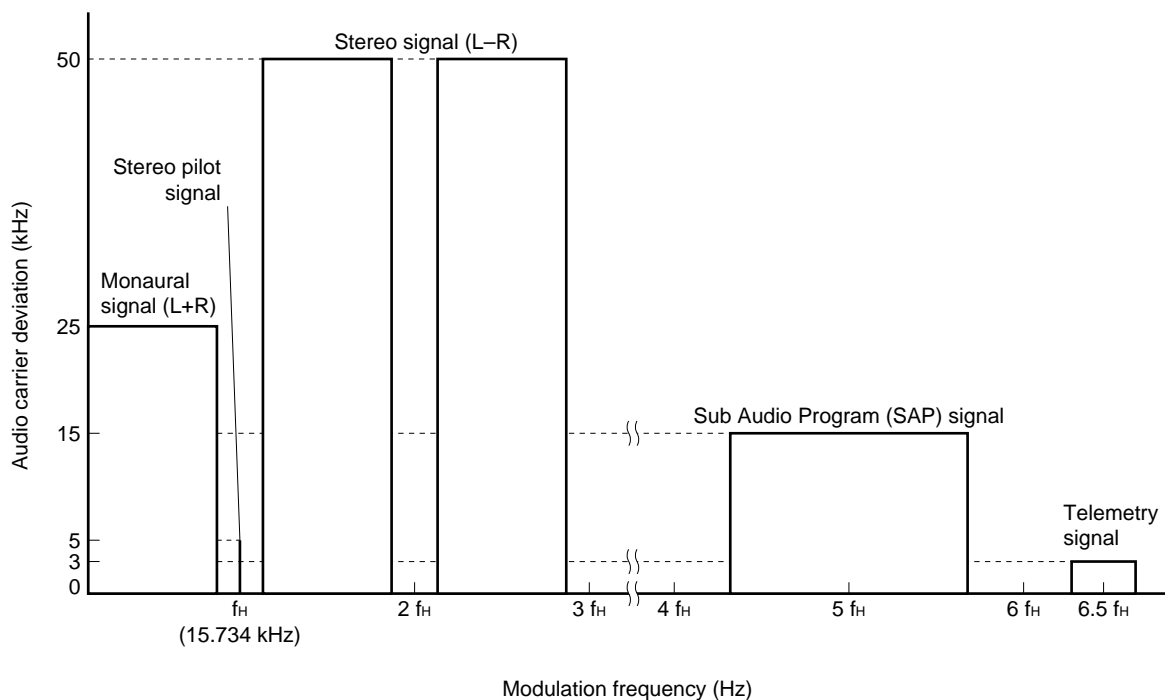


Table 2-1. US MTS System Base-Band Spectrum

	Signal frequency band	Signal processing system	Maximum audio carrier deviation (kHz)
Monaural signal (L+R)	50 Hz to 15 kHz		25
Stereo pilot signal	15.734 kHz	Only stereo broadcasting	5
Stereo signal (L–R)	50 Hz to 15 kHz	AM modulation (carrier frequency $2 f_H$ ), dbx noise reduction processing	50
Sub Audio Program (SAP) signal	50 Hz to 10 kHz	FM modulation (carrier frequency $5 f_H$ ), maximum frequency deviation 10 kHz) dbx noise reduction processing	15
Telemetry signal	Audio	FM modulation (carrier frequency $6.5 f_H$ maximum frequency deviation 3 kHz)	3
	Data		

## 2.1 Stereo Demodulation Block

### (1) Stereo LPF

This filter eliminates signals in the vicinity of  $5 f_H$  to  $6 f_H$ , such as SAP (Sub Audio Program) ( $5 f_H$ ) and telemetry signals ( $6.5 f_H$ ). The  $\mu$ PC1854A's internal L–R demodulator, which uses a double-balanced circuit, demodulates L–R signals by multiplication of the L–R signal with the signal at the L–R carrier frequency ( $2 f_H$ ). The L–R signal tends to receive interference from the  $6 f_H$  signal because a square waveform is used as the switching carrier in this method. To eliminate this interference, the  $\mu$ PC1854A incorporates traps at  $5 f_H$  and  $6 f_H$ . The filter response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

### (2) Stereo phase comparator

The  $8 f_H$  signal generated at the stereo VCO is divided by 8 ( $4 \times 2$ ) and then multiplied by the pilot signal passed through the stereo LPF. The two signals differ from each other by 90 degrees in terms of phase.

The resistor and capacitor connected to Pins  $\phi D1$  and  $\phi D2$  form a filter that smooths the phase error signal output from the stereo phase comparator, converting the error signal to the DC voltage. When the voltage difference between pins  $\phi D1$  and  $\phi D2$  becomes 0 V (strictly speaking, not 0 V by the internal offset voltage), the VCO runs at  $8 f_H$ .

The lag/lead filter externally connected to the pins  $\phi D1$  and  $\phi D2$  determines the capture range.

### (3) Stereo VCO

The VCO runs at  $8 f_H$  with the internal capacitor. The frequency is adjusted by setting the Stereo VCO setting bits (write register, subaddress 01H, bits D0 to D5).

### (4) Divider (Flip-flop)

Produces two separate  $f_H$  signals: the inphase  $f_H$  signal, and the  $f_H$  signal differing by 90 degrees from the input pilot signal by dividing the  $8 f_H$  frequency from the stereo VCO by 8 ( $4 \times 2$ ).

### (5) Pilot discrimination phase comparator (Level detector)

Multiplies the pilot signal from the COM pin with the inphase  $f_H$  signal from the divider. The resulting signal is smoothed by passing it through the external filter connected to the PD1 and PD2 pins and converted into DC voltage value that is used to determine whether or not a stereo pilot signal (read register, bit D6) is present.

### (6) Pilot canceler

The  $f_H$  signal from the divider is added to the stereo signal in resistor matrix depending on the level of the input pilot signal to cancel the pilot signal.

### (7) L+R LPF

This LPF which has traps at  $f_H$  and 24 kHz, allows only the monaural signal to pass through. The filter response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

### (8) De-emphasis

The filter is a 75- $\mu$ s de-emphasis filter for the monaural signal. The response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

### (9) L–R AM demodulator

Demodulates the L–R AM-DSB modulated signal by multiplying with the  $2f_H$  signal which is synchronized to the pilot signal. The  $2f_H$  square wave is used as the switching carrier.

## 2.2 SAP Demodulation Block

### (1) SAP BPF

Picks up the SAP signal by the 50-kHz and 102-kHz traps and a response peak at  $5 f_H$ . The filter response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

### (2) Noise BPF

The  $\mu$ PC1854A monitors signals picked up by the noise band-pass filter ( $f_o \cong 180$  kHz), and distinguishes noise from signals. By this method, the  $\mu$ PC1854A prevents faulty SAP detection in a weak electric field. The filter response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

### (3) Noise detector

Performs full-wave rectification of noise from noise band-pass filter, changes it to the DC voltage, and inputs it to the comparator. When the noise level exceeds the reference level, the detector recognizes noise, and the noise detection bit (read register, bit D4) is set "1".

The sensitivity and time constant of the circuit are adjusted by setting the values of the resistor and capacitor connected to the NDT.

### (4) SAP detector

Detects the signal from the SAP band-pass filter and smooths it through the SDT pin and inputs it to the comparator. When the SAP signal is detected, the SAP signal bit (read register, bit D5) is set "1".

### (5) SAP demodulation circuit

The SAP demodulator consists of a phase detector, a loop filter and an SAP VCO (PLL detection circuit).

The SAP VCO oscillates at  $10 f_H$ , and performs phase comparison between the signal divided by 2 of the VCO frequency and the SAP signal to make the PLL. The SAP VCO oscillating frequency is adjusted by setting the SAP VCO setting bits (write register, subaddress 05H, bits D0 to D5).

### (6) SAP LPF

Eliminates the SAP carrier and high-frequency buzz. The filter consists of a 2nd-order low-pass filter and  $f_H$  trap filter. The filter response is adjusted by setting the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

**2.3 dbx Noise Reduction Block**

All the filters required for TV-dbx noise reduction are incorporated. The response to these filters is adjusted by setting all the Filter setting bits (write register, subaddress 02H, bits D0 to D5).

**(1) LPF**

This LPF has traps at  $f_H$  and 24 kHz each. The  $f_H$  trap filter minimizes interference by the  $f_H$  signal which is not synchronized with the pilot signal (for example, leakage of the synchronous idle and buzz from the video signal).

**(2) 408-Hz LPF**

This filter is a de-emphasis filter. Its transfer function is as follows:

$$T(f) = \frac{1 + j \frac{f}{5.23k}}{1 + j \frac{f}{408}}$$

**(3) Variable emphasis**

Also called the spectral VCA. It is controlled by the spectral RMS. The transfer function is as follows:

$$S^{-1}(f, b) = \frac{1 + j \frac{f}{20.1k} \times \frac{1 + 51b}{b + 1}}{1 + j \frac{f}{20.1k} \times \frac{1 + 51}{b + 1}}$$

where “b” is the variable transferred from the spectral RMS for controlling.

**(4) Wide-band VCA**

A VCA whose operating frequency range is mainly low to mid frequencies and controlled by the wide-band RMS. The transfer function is as follows:

$$W^{-1}(a) = a$$

where “a” is the variable transferred from the wide-band RMS for controlling.

**(5) 2.19-kHz LPF**

This filter is a de-emphasis filter. Its transfer function is as follows:

$$T(f) = \frac{1 + j \frac{f}{62.5k}}{1 + j \frac{f}{2.19k}}$$



**(6) Spectral RMS filter**

A filter that limits the band width of the signal input to the RMS which controls the variable emphasis. The transfer function is as follows:

$$T(f) = \frac{(j \frac{f}{7.66k})^2}{1 + j \frac{f}{7.31k} + (j \frac{f}{7.66k})^2} \times \frac{j \frac{f}{3.92k}}{1 + j \frac{f}{3.92k}}$$

**(7) Wide-band RMS filter**

A filter that limits the band width of the signal input to the wide-band RMS which controls the wide-band VCA. The transfer function is as follows:

$$T(f) = \frac{1}{1 + j \frac{f}{2.09k}}$$

**(8) Spectral RMS**

Detects the RMS value of the signal passed through the spectral RMS filter, and converts the signal to the DC voltage. The release time is set by adjusting the current I<sub>r</sub> of the μPC1854A and the capacitance of the external capacitor connected to the STI pin. The current I<sub>r</sub> is set by the current value output from the ITI pin.

**(9) Wide-band RMS**

Detects the RMS value of the signal passed through the wide-band RMS filter, and converts the signal to the DC voltage. The release time is set by adjusting the current I<sub>r</sub> of the μPC1854A and the capacitance of the external capacitor connected to the WTI pin. The current I<sub>r</sub> is set by the current value output from the ITI pin.

**2.4 Matrix Block**

**(1) Matrix**

Adds L+R signal and L-R signal to output L signal, and subtracts L+R signal from L-R signal to output R signal.

**(2) Mode selector**

Selects the user-selected mode among the monaural, stereo, SAP, external SAP input signals, and mute, then outputs it from the NOT, ROT and LOT pins.

### 3. I<sup>2</sup>C BUS INTERFACE

The μPC1854A uses the I<sup>2</sup>C bus interface that is developed by Philips. The serial clock line (SCL) and serial data line (SDA) employ the 2-wire configuration as shown in **Figure 3-1**.

The μPC1854A contains seven (1 byte 8 bits) write registers and one read register through the I<sup>2</sup>C bus interface circuit.

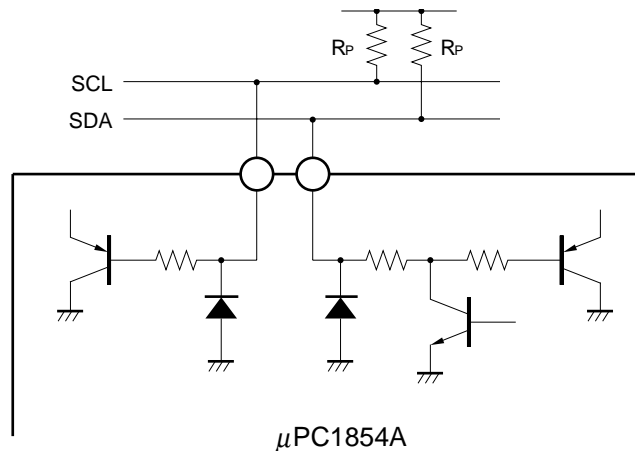
#### Serial Clock Line (SCL)

The master CPU outputs a serial clock to achieve data synchronization. The μPC1854A receives serial data based on this clock. The input level is CMOS-compatible. The clock frequency is from 0 to 100 kHz.

#### Serial Data Line (SDA)

The master CPU outputs data synchronously with the serial clock. The μPC1854A receives this data based on the serial clock. The input level is CMOS-compatible.

**Figure 3-1. Internal Equivalent Circuit of Interface Pins**



No protection diode is provided on the V<sub>cc</sub> side for the SCL and SDA pins so that the I<sup>2</sup>C bus line is not pulled to 0 V when the power is OFF (V<sub>cc</sub> = 0 V).

3.1 Data Transfer

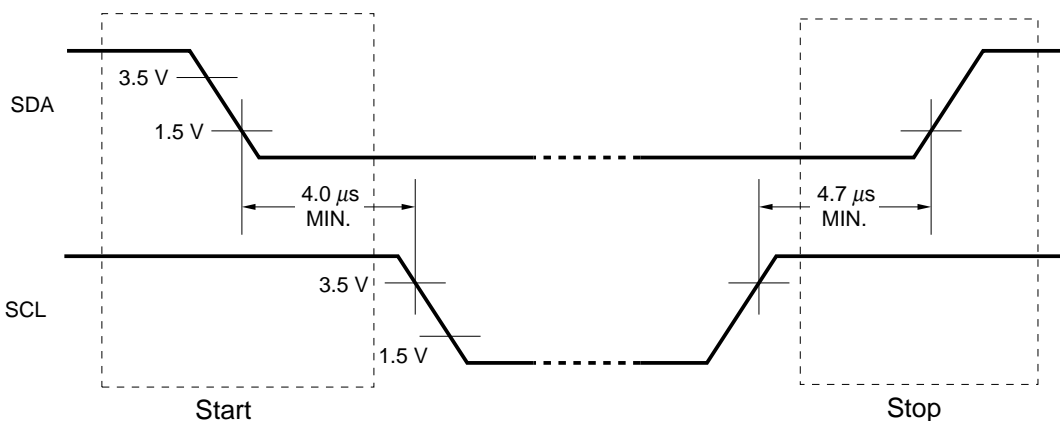
(1) Start condition

The start condition is created when SDA changes from high to low while SCL is high, as shown in **Figure 3-2**. When the μPC1854A receives this information, it captures data sent in synchronization with the clock.

(2) Stop condition

The stop condition is created when SDA changes from low to high while SCL is high, as shown in **Figure 3-2**. When the μPC1854A receives this information, it stops receiving or outputting data.

Figure 3-2. Data Transfer Start/Stop Condition

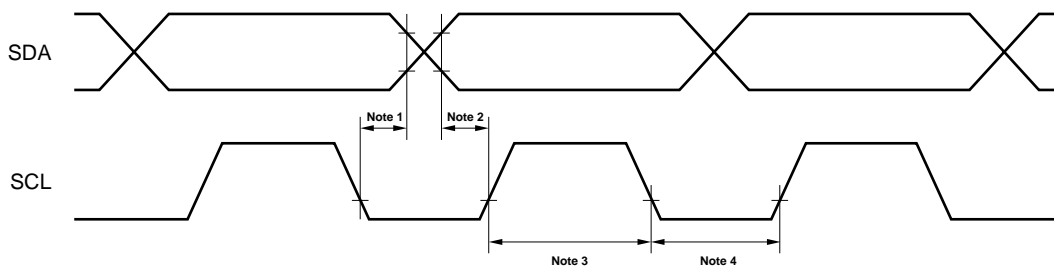


(3) Data transfer

When transferring data, be sure to switch data only when SCL is low, as shown in **Figure 3-3**. When SCL is high, the data must not be changed.

★

Figure 3-3. Data Transfer

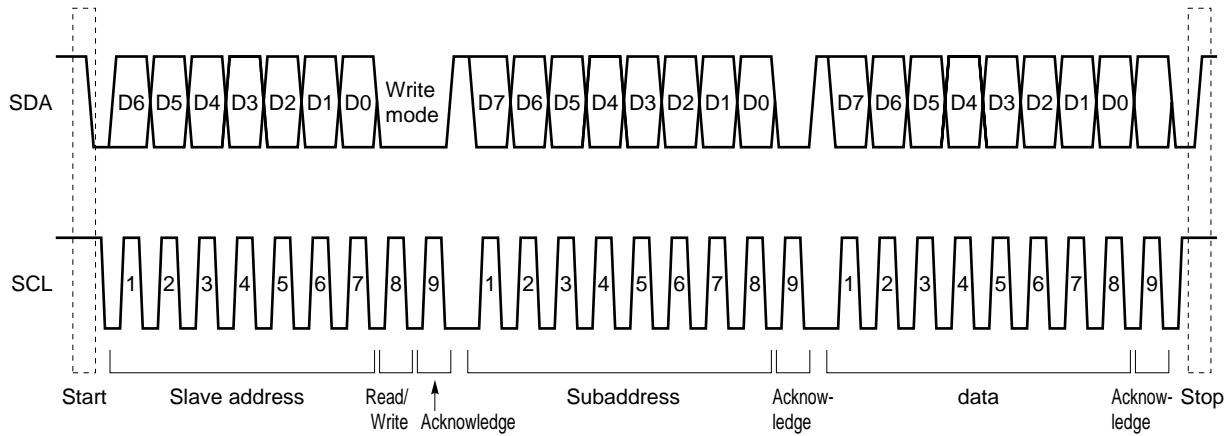


- Notes 1. Data hold time: 300 ns MIN.
- 2. Data setup time: 250 ns MIN.
- 3. Interval when data cannot be changed
- 4. Interval when data can be changed

3.2 Data Transfer Format

An example of data transfer in the write mode is shown in Figure 3-4.

Figure 3-4. Data Transfer Example in Write Mode



Data consists of 8-bit units. This 8-bit data must always be followed by an acknowledge bit. Data transfer must be done on an MSB-first basis.

The first byte after a start condition specifies the slave address. The slave address consists of 7 bits.

Table 3-1 shows the slave addresses of the μPC1854A. These slave addresses are registered by Philips.

Table 3-1. Slave Addresses of μPC1854A

Slave address	D6	D5	D4	D3	D2	D1	D0	Read/Write
Write	1	0	0	0	1	1	1	0
Read	1	0	0	0	1	1	1	1

The bit following the slave address is the read/write bit specifying the direction of the data to be transferred.

During the read operation, data is transferred from the μPC1854A to the master CPU. During the write operation, data is transferred from the master CPU to the μPC1854A. “0” and “1” are written to the Read/Write bit during the Write and Read modes, respectively.

The byte following the slave address is the subaddress of the μPC1854A in the write mode.

The μPC1854A has seven subaddresses, SA<sub>0</sub> to SA<sub>6</sub>, which are made up of 8 bits. Following the subaddress byte is the data to be set to the subaddress.

**(1) 1-byte data transfer**

The format for 1-byte data transfer is the following:

Start	Slave address	Write mode	Acknow-ledge	Subaddress	Acknow-ledge	Data	Acknow-ledge	Stop
-------	---------------	------------	--------------	------------	--------------	------	--------------	------

**(2) Continuous data transfer**

The format when transferring multiple (7) bytes of data at one time is the following:

Start	Slave address	Write mode	Acknow-ledge	Subaddress	Acknow-ledge	Data1	Acknow-ledge	Data2	Acknow-ledge	-----	Data7	Acknow-ledge	Stop
-------	---------------	------------	--------------	------------	--------------	-------	--------------	-------	--------------	-------	-------	--------------	------

The master CPU transfers “00H” as subaddress SA0 following the start condition and slave address. After the subaddress SA<sub>0</sub>, the master CPU transfers the SA<sub>0</sub> data, and continues with SA<sub>1</sub>, SA<sub>2</sub>, ..., SA<sub>6</sub> data without transferring stop conditions in between.

The subaddress is automatically incremented. Finally, the stop condition is transferred and the transfer is completed.

**(3) Data read**

The μPC1854A has one read register. The contents of this register can be read by the master CPU.

The format when data is read is the following:

Start	Slave address	Read	Acknow-ledge	Data	Non-acknow-ledge	Stop
-------	---------------	------	--------------	------	------------------	------

**(4) Acknowledge**

In the case of the I<sup>2</sup>C bus, an acknowledge bit is added to the data as the 9th bit to determine whether data transfer was successful. The master determines the success or failure of data transfer based on whether this acknowledge bit is a logical low or high.

If the acknowledge interval is a logical low, this indicates that data transfer was successful. If it is a logical high, this indicates that data transfer was unsuccessful or that the slave side forcibly released the bus as a non-acknowledge state.

## 4. I<sup>2</sup>C BUS COMMANDS

### 4.1 Subaddress List

#### (1) Write register (command list)

Subaddress	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	0	During noise detection Stereo/SAP output stop 0: SAP OFF 1: Stereo, SAP OFF	Input level setting					
01H	0	f <sub>H</sub> monitor ON/OFF 0: OFF 1: ON	Stereo VCO setting					
02H	0	Pilot canceler ON/OFF 0: ON 1: OFF	Filter setting					
03H	0	0	Low-band separation setting					
04H	0	0	High-band separation setting					
05H	0	5 f <sub>H</sub> monitor ON/OFF 0: OFF 1: ON	SAP VCO setting					
06H	0	0	Normal track output select 1 0: SAP 1: External SAP	Normal track output select 2 0: SAP 1: Monaural	SAP1/SAP2 switch <sup>Note</sup> 0: SAP1 1: SAP2	Stereo/SAP switch 0: Stereo 1: SAP	Forced monaural ON/OFF 0: OFF 1: ON	Mute ON/OFF 0: ON 1: OFF

**Note** Output when SAP1 or SAP2 is selected is as follows:

	LOT pin (L-channel output)	ROT pin (R-channel output)
SAP1	SAP	
SAP2	Monaural (L+R)	SAP

**Remark** The initial value of write register after power-on reset

- Mute register (subaddress 06H, bit D0) = 0 (Mute: ON)
- Other registers = undefined (setting properly after power-on reset)

#### (2) Read register

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Power-on reset 1: Detection	Broadcast status		Noise detection	Reception status		1	1
	Stereo pilot 0: Not available 1: Available	SAP signal 0: Not available 1: Available	0: Not available 1: Available	Stereo broadcast reception 0: Not available 1: Available	SAP broadcast reception 0: Not available 1: Available		

## 4.2 Setting Procedure

Precise adjustment of the dbx decoder is absolutely critical for optimum performance. Where possible, the adjustment should be performed after the  $\mu$ PC1854A is mounted on the chassis and with the video system active.

Set the data of write register as follows before the adjustment, because the registers other than the Mute register are defined.

**Table 4-1. Default Setting of Write Register**

Subaddress	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	1	0	0	0	0	0
01H	0	0	1	0	0	0	0	0
02H	0	0	1	1	1	1	1	1
03H	0	0	1	0	0	0	0	0
04H	0	0	1	0	0	0	0	0
05H	0	0	1	0	0	0	0	0
06H	0	0	0	0	0	0	0	1

### (1) Input level setting (write register, subaddress 00H, bits D5 to D0)

- <1> Write "1" to bit D0 (Mute: OFF) of subaddress 06H.
- <2> Input sine wave of 300 Hz, 150 mV<sub>rms</sub> to COM pin.
- <3> Set bits D5 to D0 (Input level setting bits) of subaddress 00H so that the output level of ROT pin is 500 mV<sub>rms</sub> ( $\pm 10$  mV<sub>rms</sub>).

### (2) Stereo VCO setting (write register, subaddress 01H, bits D6 to D0)

Perform this adjustment with no signal applied.

- <1> Write "1" to bit D0 (Mute: OFF) of subaddress 06H.
- <2> Write "1" to bit D6 (f<sub>H</sub> monitor: ON) of subaddress 01H.
- <3> Connect frequency counter to ROT pin, and set bits D5 to D0 (Stereo VCO setting bits) of subaddress 01H so that frequency counter displays 15.73 kHz ( $\pm 0.1$  kHz).
- <4> When setting is completed, write "0" to bit D6 (f<sub>H</sub> monitor: OFF) of subaddress 01H.

### (3) Filter setting (write register, subaddress 02H, bits D6 to D0)

- <1> Write "1" to bit D6 (Pilot canceler: OFF) of subaddress 02H.
- <2> Input pilot signal (15.734 kHz, 30 mV<sub>rms</sub> or higher<sup>Note</sup>) to COM pin and set data of bits D5 to D0 (Filter setting bits) of subaddress 02H so that the output level of the ROT pin becomes as small as possible (Decrease the set data from 63 (decimal)).
- <3> When setting is completed, write "0" to bit D6 (Pilot canceler: ON) of subaddress 02H.

**Note** 100 mV<sub>rms</sub> is recommended.

**(4) Separation setting (write register, subaddresses 03H and 04H, bits D5 to D0)**

- <1> Write "1" to bit D0 (Mute: OFF) of subaddress 06H.
- <2> Write "20H" to bits D5 to D0 (High-band separation setting bits) of subaddress 04H.
- <3> Input composite signal to COM pin (300 Hz, 30% modulation, L-only, with noise reduction), and set bits D5 to D0 (Low-band separation setting bits) of subaddress 03H so that the output level of the ROT pin is as small as possible.
- <4> Change the modulation frequency of the composite signal to 3 kHz, and set bits D5 to D0 of subaddress 04H so that the output level of the ROT pin is as small as possible.
- <5> While bits D5 to D0 of subaddress 04H are set as in step <4> above, repeat the setting procedure of step <3> for bits D5 to D0 of subaddress 03H.

**(5) SAP VCO setting (write register, subaddress 05H, bits D6 to D0)**

Perform this adjustment with no signal applied.

- <1> Add a 1 M $\Omega$  resistor between the SOA pin and GND.
- <2> Write "1" to bit D0 (Mute: OFF) of subaddress 06H.
- <3> Write "1" to bit D6 (5 f<sub>H</sub> monitor: ON) of subaddress 05H.
- <4> Connect a frequency counter to the ROT pin, and set bits D5 to D0 of subaddress 05H (SAP VCO setting bits) so that 78.67 kHz ( $\pm 0.5$  kHz) is displayed on the frequency counter.
- <5> When setting is completed, write "0" to bit D6 (5 f<sub>H</sub> monitor: OFF) of subaddress 05H.
- <6> Delete the 1 M $\Omega$  resistor between the SOA pin and GND.



4.3 Explanation of Write Register

(1) Stereo/SAP output stop function during noise detection

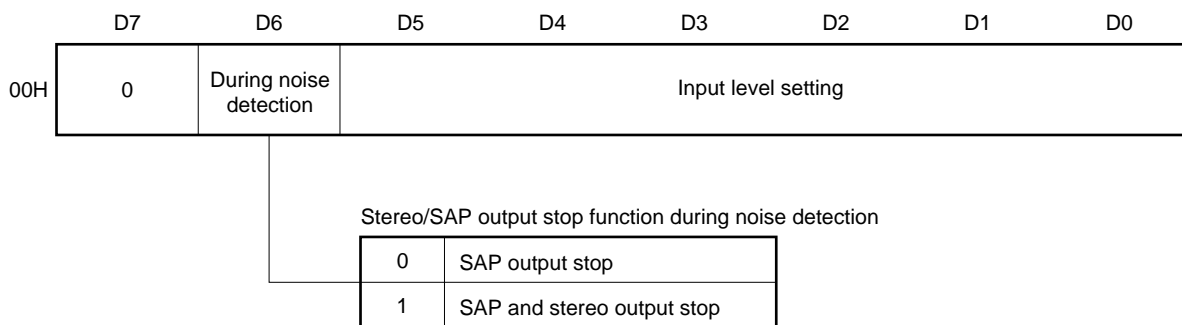
Stereo/SAP output stop can be selected with the data of bit D6 of subaddress 00H during weak electrical field conditions (noise level during recommended circuit use is 30 mVrms (TYP.) or more).

SAP output stop : Only SAP output is stopped.

SAP and stereo output stop : SAP and stereo outputs are stopped, switch to monaural output.

Noise level detection is performed, when detected a noise about 11.5 fH (180 kHz), a frequency that is sufficiently apart from that of the high frequency signals such as the stereo, SAP, and telemetry signal. If noise is detected, "1" is set to bit D4 of the read register (Refer to section 4.4 (4) Noise detection).

Figure 4-1. Stereo/SAP Output Stop Function during Noise Detection

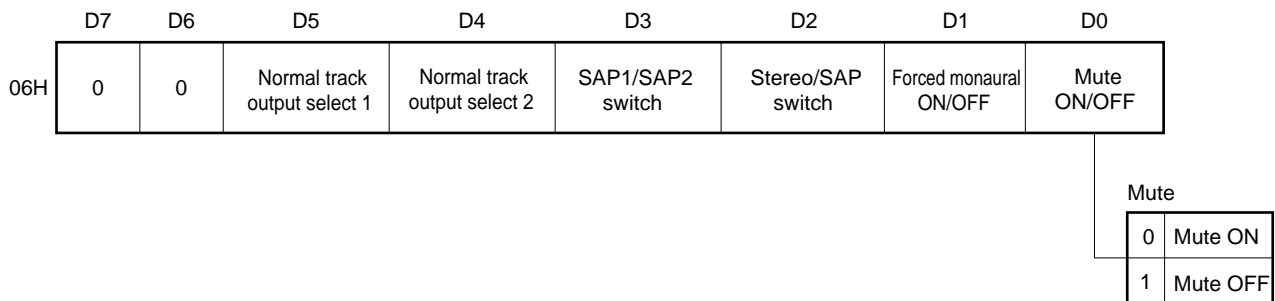


(2) Mute

The mute function can be set ON/OFF with the data of bit D0 of subaddress 06H.

The mute on state is entered when bit D0 is set to 0 after power-on reset.

Figure 4-2. Mute



**Caution** When switching the power ON/OFF, use the mute function (200 ms) outside the μPC1854A in order to minimize shock noise.

**(3) Mode switch (L-, R-channel output (LOT, ROT pins))**

The signal to be output can be selected from the L- and R-channel outputs (LOT, ROT pins) with bits D3 to D1 of subaddress 06H. For the combinations of bit and output signal, refer to section 5.1 L-, R-Channel Output (LOT, ROT pins) Matrix.

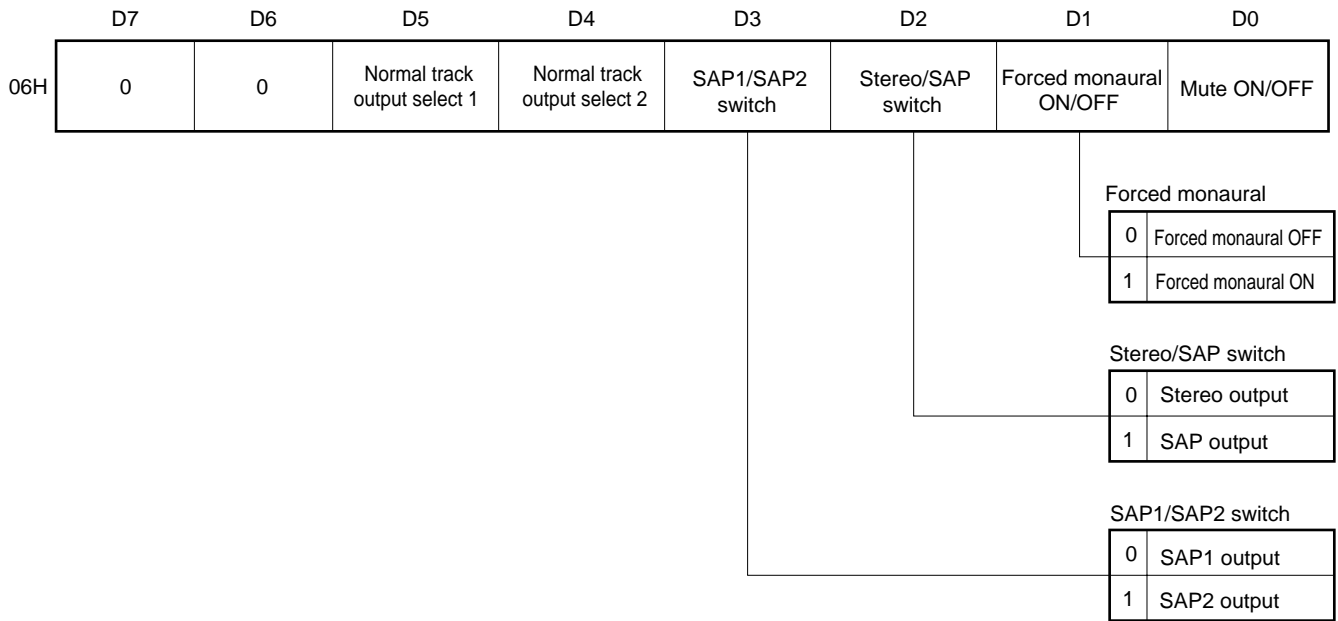
Forced monaural ON/OFF : When set to ON, a monaural signal is forcibly output regardless of the selection of other bits.

Stereo/SAP switch : When forced monaural is set to OFF, performs selection of stereo or SAP.

SAP1/SAP2 switch : When SAP output is selected with the stereo/SAP switch, performs selection of SAP1 or SAP2.

	L-Channel Output (LOT pin)	R-Channel Output (ROT pin)
SAP1	SAP output	
SAP2	Monaural (L+R) output	SAP output

**Figure 4-3. Mode Switch (L-, R-Channel Output (LOT, ROT pins))**



**(4) Mode switch (normal signal output (NOT pin))**

The signal output from the normal signal output (NOT pin) can be selected with bits D5 to D1 of subaddress 06H. For the combinations of bit and output signal, refer to section **5.2 Normal Output (NOT pin) Matrix**.

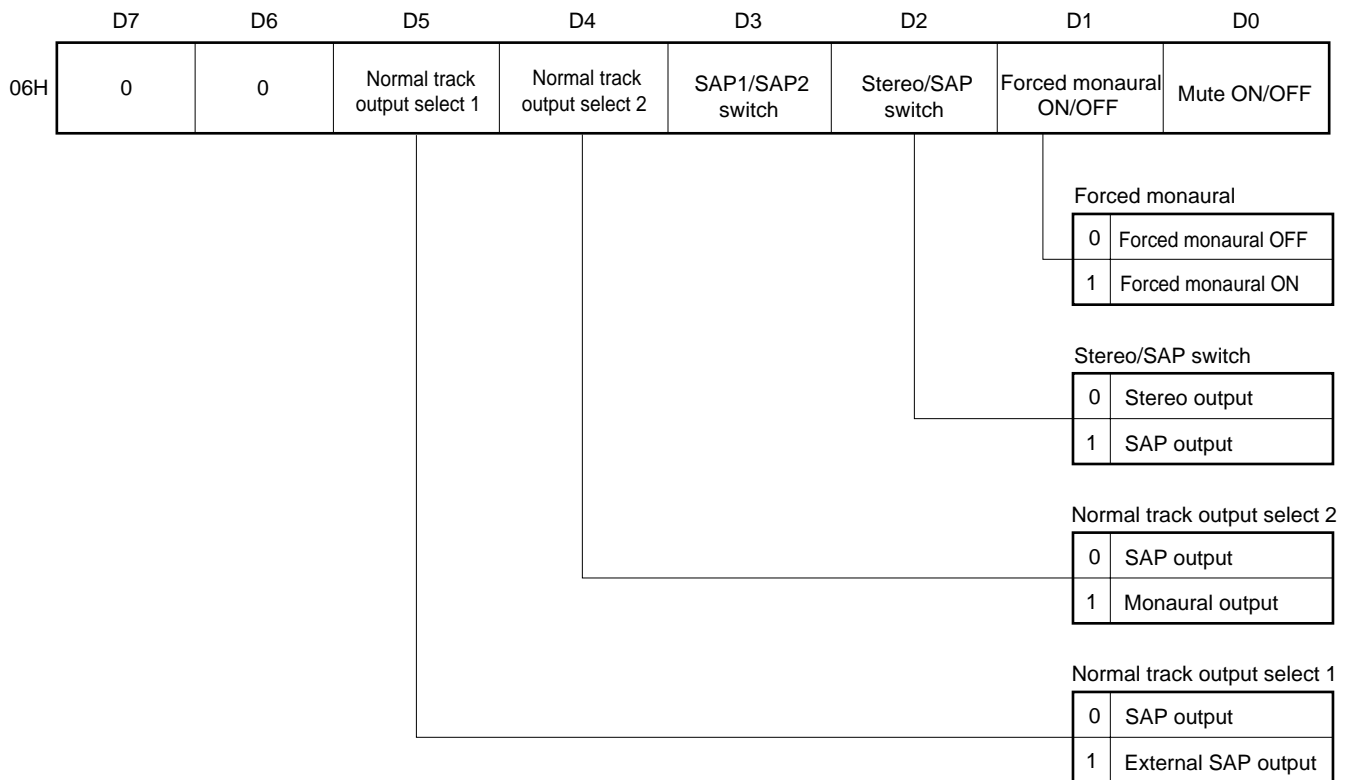
Normal track output select 2 : Selects SAP or monaural signal.

Normal track output select 1 : Selects SAP signal or external SAP signal.

Forced monaural ON/OFF : When ON is selected, monaural signal is forcibly output regardless of stereo/SAP switch selection.

Stereo/SAP switch : Selects SAP or stereo signal when other switches are selected as follows;  
 Normal track output select 1: SAP  
 Normal track output select 2: SAP  
 Forced monaural: OFF

**Figure 4-4. Mode Switch (Normal Signal Output (NOT Pin))**

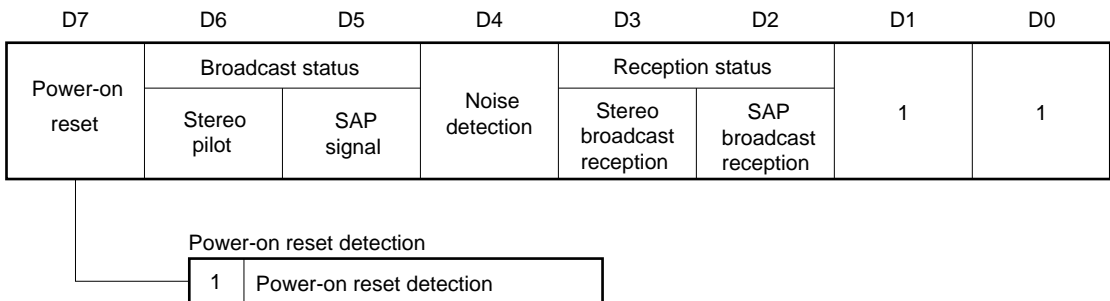


4.4 Explanation of Read Register

(1) Power-on reset detection

Whether a power-on reset was detected is detected with bit D7 of the read register.

Figure 4-5. Power-On Reset Detection

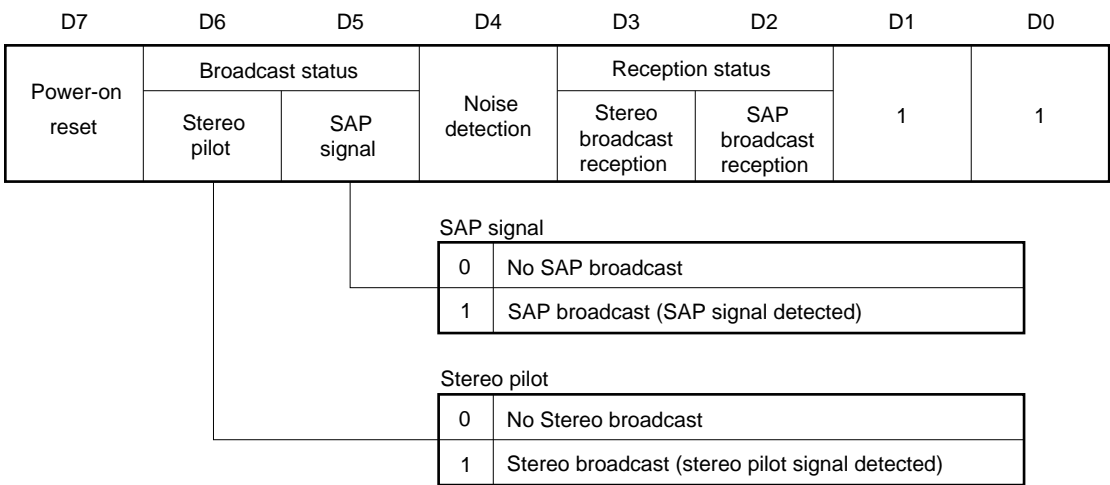


(2) Stereo, SAP broadcast (broadcast status) detection

Whether SAP or stereo broadcast from a broadcasting station is being broadcast is detected with bits D5 and D6 of the read register.

When a SAP signal (5 fH) or stereo pilot signal is detected, the register data becomes “1”.

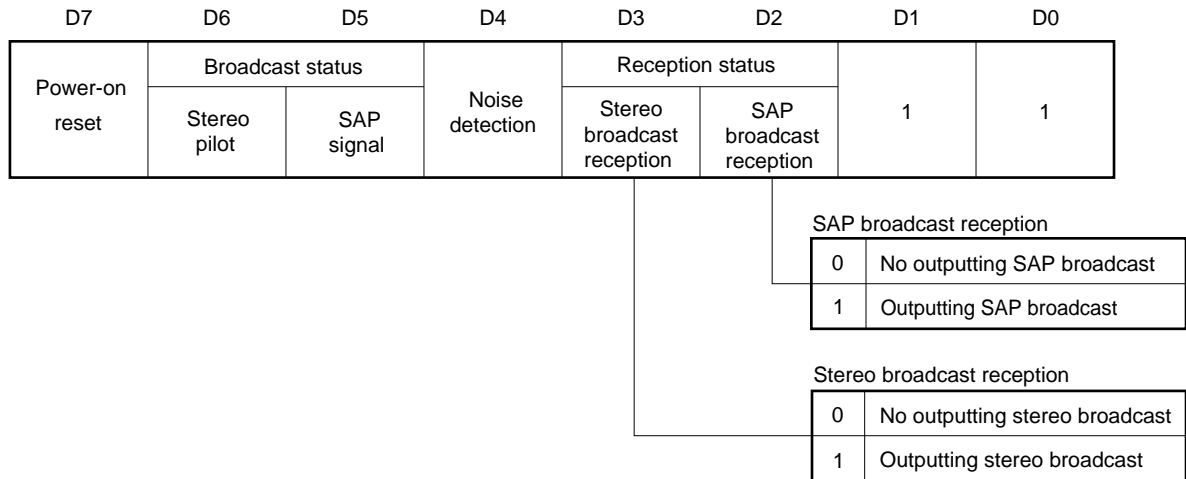
Figure 4-6. Stereo, SAP Broadcast (Broadcast Status) Detection



**(3) Stereo, SAP broadcast reception (reception status) detection**

Whether SAP or stereo broadcast is being received and the μPC1854A outputs the audio signal can be detected with bits D2 and D3 of the read register. The register data become “1” only if the SAP signal (5 f<sub>H</sub>) is detected when the SAP broadcast reception is selected, or if the stereo pilot signal is detected when the stereo broadcast reception is selected.

**Figure 4-7. Stereo, SAP Broadcast Reception (Reception Status) Detection**

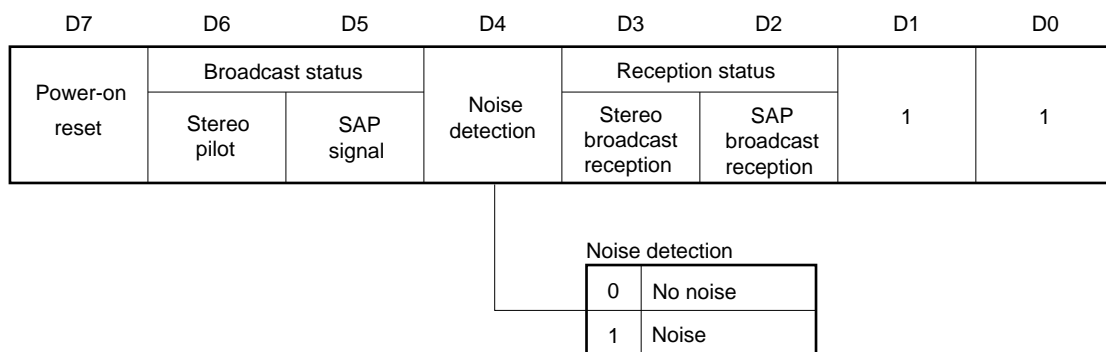


**(4) Noise detection**

Noise can be detected with bit D4 of the read register. It is monitored in the vicinity of the 11.5 f<sub>H</sub> (180 kHz) signal level and noise is detected.

During noise detection, the operation of the SAP demodulator block and the stereo demodulation block is interrupted (Refer to section 4.3 (1) **Stereo/SAP output stop function during noise detection**).

**Figure 4-8. Noise Detection**



5. MODE MATRIX

5.1 L-, R-Channel Output (LOT, ROT pins) Matrix

Mute OFF (Write register, subaddress 06H, bit D0 : “1”)

(1) Read register, bit D4: 0

Broadcast mode	Write Register				Output		Read Register			
	Forced monaural ON/OFF	Stereo/SAP switch	SAP1/SAP2 switch	Stereo/SAP output stop	L-ch output (LOT)	R-ch output (ROT)	Broadcast status		Reception status	
	Subaddress 06H			Subaddress 00H			Stereo pilot	SAP signal	Stereo broadcast reception	SAP broadcast reception
	Bit D1	Bit D2	Bit D3	Bit D6	Bit D6	Bit D5	Bit D3	Bit D2		
Monaural	—	—	—	—	L+R		0	0	0	0
Stereo	0	—	—	—	L	R	1	0	1	0
	1				L+R				0	
Monaural + SAP	0	0	—	—	L+R		0	1	0	0
		1	0		SAP					
	1	—	—	L+R	SAP	L+R			0	
Stereo + SAP	0	0	—	—	L	R	1	1	1	0
		1	0		SAP				1	
	1	—	—	L+R	SAP	L+R			0	

(2) Read register, bit D4: 1

Broadcast mode	Write Register				Output		Read Register			
	Forced monaural ON/OFF	Stereo/SAP switch	SAP1/SAP2 switch	Stereo/SAP output stop	L-ch output (LOT)	R-ch output (ROT)	Broadcast status		Reception status	
	Subaddress 06H			Subaddress 00H			Stereo pilot	SAP signal	Stereo broadcast reception	SAP broadcast reception
	Bit D1	Bit D2	Bit D3	Bit D6	Bit D6	Bit D5	Bit D3	Bit D2		
Monaural	—	—	—	—	L+R		0	0	0	0
Stereo	0	—	—	0	L	R	1	0	1	0
				1	L+R				0	
Monaural + SAP	0	1	0	0	L+R		0	0	0	0
			1	0						
			1	0						
			1	0						
Stereo + SAP	0	0	—	0	L	R	1	0	1	0
			1	0	L+R				0	
	1	1	0	0	0	L+R		0	0	0
				1	0					
				1	0					

- Remarks 1. When the μPC1854A recognizes a weak electric field, bit D4 of the read register becomes “1”.
- 2. — : Don't care.

5.2 Normal Output (NOT pin) Matrix

Mute OFF (Write register, subaddress 06H, bit D0 : “1”)

Broadcast mode	Write Register					Output Normal output (NOT pin)
	Normal track output select 2	Normal track output select 1	Forced monaural ON/OFF	Stereo /SAP switch	SAP1/SAP2 switch	
	Subaddress : 06H					
	Bit: D4	Bit: D5	Bit: D1	Bit: D2	Bit: D3	
Monaural	—	—	—	—	—	L+R
Stereo	—	—	—	—	—	L+R
Monaural + SAP	0	0	0	0	—	L+R
				1		SAP
	1	—	—	—		L+R
				—		External SAP <sup>Note</sup>
Stereo + SAP	0	0	0	0	—	L+R
				1		SAP
	1	—	—	—		L+R
				—		External SAP <sup>Note</sup>

**Note** SAP signal input from ESA pin.

**Remark** — : Don't care.

**Caution** All normal outputs with weak electric field are L+R.

## 6. USAGE CAUTIONS

### 6.1 Caution on Shock Noise Reduction

When switching the power ON/OFF, use the mute function (approx. 200 ms) outside the μPC1854A in order to minimize shock noise.

### 6.2 Supply Voltage

Pass data through the I<sup>2</sup>C bus only after stabilizing the supply voltage of the entire application system.

### 6.3 Impedance of Input and Output Pins

**Table 6-1. Impedance of Input and Output Pins**

Input pin			Output pin		
Symbol	Description	Impedance	Symbol	Description	Impedance
COM	Composite signal input	80 kΩ	SOT	SAP single output	360 Ω
SI	SAP single input		NOT	Normal output	15 Ω
ESA	External SAP input		ROT	R-channel output	
		LOT	L-channel output		

### 6.4 Drive Capability of Output Pins

**Table 6-2. Drive Capability of Output Pins**

Pin symbol	Pin description	Output pin-GND Connection Resistance	Drive capability
SOT	SAP single output	10 kΩ	3-kΩ load or less
NOT	Normal output		700-Ω load or less
ROT	R-channel output		
LOT	L-channel output		

**Remark** If the load capacitance of the output pins (SOT, NOT, ROT, LOT pins) exceeds 100 pF, parasitic oscillation may occur. In this case, connect a resistor between the output pins and the load capacitance. Bear in mind that the load capacitance is changed by wiring pattern on the printed circuit board.



**6.5 Caution on External Components**

According to the license contract with THAT Corporation, use the following for external components.

- ★ With regard to the use of other external components, please contact to THAT Corporation.

**Table 6-3. External Components**

Pin symbol	Pin description	External component
ITI	Timing current setting	Metal film resistor (±1 %)
STI	Spectral RMS timing	Tantalum capacitor (±10 %)
WTI	Wide-band RMS timing	

**6.6 Change of Electrical Characteristics by External Components**

- (1) SAP sensitivity can be lowered by inserting a resistor between the SDT pin and GND.
- (2) Noise sensitivity can be changed by changing the value of the resistor between the NDT pin and GND.
- (3) The capture range can be changed by changing the recommended 1 μF value of the capacitor between the φD1 and φD2 pins (Refer to **BLOCK DIAGRAM**).  
 Reducing the capacitor value increases the capture range, and increasing it reduces the capture range. However, too small a capacitor value may cause the distortion rate to become worse during stereo output, or may cause malfunction. In this case, please contact NEC.

7. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (Unless otherwise specified, T<sub>A</sub> = +25°C)**

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V <sub>CC</sub>			11	V
I <sup>2</sup> C bus input pin voltage	V <sub>cont</sub>	To SDA, SCL pins		V <sub>CC</sub>	V
Composite signal input voltage	V <sub>in</sub>	COM pin		V <sub>CC</sub>	V
Power dissipation	P <sub>D</sub>	T <sub>A</sub> = 75 °C	μPC1854ACT (SDIP)	600	mW
			μPC1854AGT (SOP)	340	mW
Operating ambient temperature	T <sub>A</sub>	V <sub>CC</sub> = 9 V		-20 to +75	°C
Storage temperature	T <sub>stg</sub>			-40 to +125	°C

**Caution** If any of the parameters exceeds the absolute maximum ratings, even momentarily, the device reliability may be impaired. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.

**Recommended Operating Range (Unless otherwise specified, T<sub>A</sub> = +25°C)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply voltage	V <sub>CC</sub>			8.0	9.0	10.0	V
Output load impedance 1	R <sub>L1</sub>	AC load impedance that can be driven by outputs of NOT, ROT and LOT pins (at 100% modulation)		2			kΩ
Output load impedance 2	R <sub>L2</sub>	AC load impedance that can be driven by output of SOT pin (at 100% modulation)		10			kΩ
Signal input voltage	V <sub>in</sub>	Signal voltage to COM pin	L+R signal (100% modulation)		0.424		V <sub>p-p</sub>
			L-R signal (100% modulation)		0.848		V <sub>p-p</sub>
			Pilot signal		0.0848		V <sub>p-p</sub>
			SAP signal		0.254		V <sub>p-p</sub>
I <sup>2</sup> C bus input pin voltage (High)	V <sub>contH</sub>	SDA, SCL pins		3.5	5.0	5.0	V
I <sup>2</sup> C bus input pin voltage (Low)	V <sub>contL</sub>			0.0	0.0	1.5	V
Clock frequency	f <sub>SCL</sub>	SCL pin				100	kHz

Electrical Characteristics (unless otherwise specified, T<sub>A</sub> = 25°C, RH ≤ 70 %, V<sub>CC</sub> = 9.0 V)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	I <sub>CC</sub>	No signal	33	45	60	mA
Stereo detection input sensitivity	ST <sub>SENCE</sub>	15.734 kHz, sine wave	11	16	21	mV <sub>rms</sub>
Stereo detection hysteresis	ST <sub>HY</sub>	Only stereo pilot signal input	3.0	6.0	9.0	dB
Stereo detection capture range	ST <sub>CCL</sub>	V <sub>in</sub> = 30 mV <sub>rms</sub>	-5.5	-4.0	-2.5	%
	ST <sub>CCH</sub>	Only stereo pilot signal input	2.5	4.0	5.5	%
SAP detection input sensitivity	SAP <sub>SENCE</sub>	78.67 kHz, 0% modulation	17	23	30	mV <sub>rms</sub>
SAP detection hysteresis	SAP <sub>HY</sub>	Only SAP carrier input	3.3	4.8	6.3	dB
Noise detection input sensitivity	NO <sub>SENCE</sub>	Sine wave input f: Noise BPF peak	20	30	40	mV <sub>rms</sub>
Noise detection hysteresis	NO <sub>HY</sub>	Sine wave input f: Noise BPF peak	1.0	2.0	3.0	dB
Monaural total output voltage	V <sub>OMO</sub>	300 Hz, 100% modulation	450	500	550	mV <sub>rms</sub>
Stereo total output voltage	V <sub>OST</sub>		450	500	550	mV <sub>rms</sub>
SAP total output voltage	V <sub>OSAP1</sub>		400	500	600	mV <sub>rms</sub>
SAP single output voltage	V <sub>OSAP2</sub>	300 Hz, 100% modulation Noise reduction: OFF	420	470	520	mV <sub>rms</sub>
Normal output voltage	V <sub>ONO</sub>	300 Hz, 100% modulation Monaural signal	450	500	550	mV <sub>rms</sub>
Difference between monaural L and R output voltage	V <sub>OLR</sub>	300 Hz, 100% modulation	-0.5	0	+0.5	dB
Monaural total frequency characteristics 1	V <sub>OMO1</sub>	1 kHz, 30% modulation (300 Hz: 0 dB)	-0.5	0	+0.5	dB
Monaural total frequency characteristics 2	V <sub>OMO2</sub>	3 kHz, 30% modulation (300 Hz: 0 dB)	-1.0	-0.3	+0.5	dB
Monaural total frequency characteristics 3	V <sub>OMO3</sub>	8 kHz, 30% modulation (300 Hz: 0 dB)	-1.5	-0.5	+1.0	dB
Monaural total frequency characteristics 4	V <sub>OMO4</sub>	12 kHz, 30% modulation (300 Hz: 0 dB)	-6.5	-4.0	-1.5	dB
Stereo total frequency characteristics 1	V <sub>OST1</sub>	1 kHz, 30% modulation (300 Hz: 0 dB)	-0.5	0	+0.5	dB
Stereo total frequency characteristics 2	V <sub>OST2</sub>	3 kHz, 30% modulation (300 Hz: 0 dB)	-1.0	0	+0.5	dB
Stereo total frequency characteristics 3	V <sub>OST3</sub>	8 kHz, 30% modulation (300 Hz: 0 dB)	-1.0	0	+1.0	dB
Stereo total frequency characteristics 4	V <sub>OST4</sub>	12 kHz, 30% modulation (300 Hz: 0 dB)	-11.0	-7.0	-3.0	dB
SAP total frequency characteristics 1	V <sub>OSAP11</sub>	1 kHz, 30% modulation (300 Hz: 0 dB)	-1.2	-0.1	+1.2	dB
SAP total frequency characteristics 2	V <sub>OSAP12</sub>	3 kHz, 30% modulation (300 Hz: 0 dB)	-1.0	+0.4	+2.0	dB
SAP total frequency characteristics 3	V <sub>OSAP13</sub>	8 kHz, 30% modulation (300 Hz: 0 dB)	-0.5	+1.7	+4.0	dB

(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SAP single frequency characteristics 1	V <sub>OSAP21</sub>	1 kHz, 30% modulation (300 Hz: 0 dB) Noise reduction: OFF	-0.5	0	+0.5	dB
SAP single frequency characteristics 2	V <sub>OSAP22</sub>	3 kHz, 30% modulation (300 Hz: 0 dB) Noise reduction: OFF	-0.5	0	+0.5	dB
SAP single frequency characteristics 3	V <sub>OSAP23</sub>	8 kHz, 30% modulation (300 Hz: 0 dB) Noise reduction: OFF	-1.0	0	+1.0	dB
Stereo channel separation 1	Sep <sub>1</sub>	300 Hz, 30% modulation	27	32	—	dB
Stereo channel separation 2	Sep <sub>2</sub>	1 kHz, 30% modulation	25	30	—	dB
Stereo channel separation 3	Sep <sub>3</sub>	3 kHz, 30% modulation	27	35	—	dB
Monaural total harmonic distortion	THD <sub>MO</sub>	1 kHz, 100% modulation	—	0.1	0.5	%
Stereo total harmonic distortion 1	THD <sub>ST1</sub>	1 kHz, 100% modulation	—	0.3	1.5	%
Stereo total harmonic distortion 2	THD <sub>ST2</sub>	8 kHz, 30% modulation with DIN/AUDIO filter used	—	0.8	1.8	%
SAP total harmonic distortion	THD <sub>SAP1</sub>	1 kHz, 100% modulation	—	0.5	2.0	%
SAP single harmonic distortion	THD <sub>SAP2</sub>	1 kHz, 100% modulation Noise reduction: OFF	—	0.7	2.0	%
Normal output harmonic distortion	THD <sub>NO</sub>	1 kHz, 100% modulation Monaural signal	—	0.1	0.5	%
Crosstalk 1 (SAP → Stereo)	CT <sub>1</sub>	SAP: f = 3 kHz, 30% modulation Stereo: L-only, f = 800 Hz, 30% modulation	—	-60	-50	dB
Crosstalk 2 (Stereo → SAP)	CT <sub>2</sub>	SAP: f = 800 Hz, 30% modulation Stereo: L-only, f = 3 kHz, 30% modulation	—	-60	-50	dB
Monaural total S/N	S/N <sub>MO</sub>	300 Hz, 100% modulation Pre-emphasis: ON	65	68	—	dB
Stereo total S/N	S/N <sub>ST</sub>	300 Hz, 100% modulation	65	68	—	dB
SAP total S/N	S/N <sub>SAP</sub>	Noise reduction: ON	70	80	—	dB
Normal output S/N	S/N <sub>NO</sub>	Signal: 300 Hz, 100% modulation Monaural signal	65	68	—	dB
Total muting level	Mute	1 kHz, 100% modulation	60	70	—	dB
dbx timing current	I <sub>T</sub>	STI- and WTI-pin current flow	7.1	7.5	7.9	μA
Inter-mode DC offset 1	V <sub>DOF1</sub>	Mute → Monaural, no signal	-50	0	+50	mV
Inter-mode DC offset 2	V <sub>DOF2</sub>	Mute → Stereo, only pilot signal input	-50	0	+50	mV
Inter-mode DC offset 3	V <sub>DOF3</sub>	Mute → SAP1, only 5 fH signal input	-50	0	+50	mV
Inter-mode DC offset 4	V <sub>DOF4</sub>	Mute → Monaural (Normal output)	-50	0	+50	mV
Inter-mode DC offset 5	V <sub>DOF5</sub>	Mute → External SAP (Normal output)	-50	0	+50	mV

**Test Condition Parameters for Electrical Characteristics**  
 (Unless otherwise specified, T<sub>A</sub> = 25°C, RH ≤ 70 %, V<sub>CC</sub> = 9 V)

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Supply current	I <sub>CC</sub>	I <sub>CC</sub> : Current sent to V <sub>CC</sub> pin when there is no signal	Monaural
Stereo detection input sensitivity	ST <sub>SENSE</sub>	ST <sub>SENSE</sub> : Input signal level of COM pin (input signal: 15.734 kHz) Read register D6 : when changed from 0 to 1	Stereo
Stereo detection hysteresis	ST <sub>HY</sub>	ST <sub>HY</sub> = 20 log (ST <sub>SENSE</sub> ÷ V) ST <sub>SENSE</sub> : Stereo detection input sensitivity V : Input signal level of COM pin (Input signal: 15.734 kHz) Read register D6 : First set to 1, then changed to 0 by gradually lowering input signal level.	
Stereo detection capture range	ST <sub>CCL</sub>	ST <sub>CCL</sub> = Δf ÷ 15.734 kHz Δf : Difference between f and 15.734 kHz f : With signal (14.5 kHz, 30 mV <sub>rms</sub> ) input to COM pin; The frequency, which is gradually raised and measured when read register D6 becomes 1	
	ST <sub>CCH</sub>	ST <sub>CCH</sub> = Δf ÷ 15.734 kHz Δf : Difference between f and 15.734 kHz f : With signal (17.0 kHz, 30 mV <sub>rms</sub> ) input to COM pin; The frequency, which is gradually lowered and measured when read register D6 becomes 1	
SAP detection input sensitivity	SAP <sub>SENSE</sub>	SAP <sub>SENSE</sub> : Input signal level of COM pin (input signal: 78.67 kHz) Read register D5 : when changed from 0 to 1	SAP
SAP detection hysteresis	SAP <sub>HY</sub>	SAP <sub>HY</sub> = 20 log (SAP <sub>SENSE</sub> ÷ V) SAP <sub>SENSE</sub> : SAP detection input sensitivity V : Input signal level of COM pin (Input signal: 78.67 kHz) Read register D5 : First set to 1, then changed to 0 by gradually lowering input signal level.	
Noise detection input sensitivity	NO <sub>SENSE</sub>	NO <sub>SENSE</sub> : Input signal level of COM pin Read register D4 : Changed to 0 by applying 6-V DC voltage to SDT pin. Read register D4 : With signal (160 kHz, 10 mV <sub>rms</sub> ) input to COM pin; Changed to 1 by raising the frequency until the DC voltage of the NDT pin reaches the maximum level and, with maintaining this frequency, gradually raising the input signal level.	
Noise detection hysteresis	NO <sub>HY</sub>	NO <sub>HY</sub> = 20 log (NO <sub>SENSE</sub> ÷ V) NO <sub>SENSE</sub> : Noise detection input sensitivity V : Input signal level of NDT pin COM pin : Signal (160 kHz, 90 mV <sub>rms</sub> ) input Read register D4 : First set to 1, then changed to 0 by raising the frequency until the DC voltage of the NDT pin reaches the maximum level and, with maintaining this frequency, gradually raising the input signal level.	
Monaural total output voltage	V <sub>OMO</sub>	V <sub>OMO</sub> : Output voltage of ROT and LOT pins COM pin: Monaural signal (300 Hz, 100% modulation) input	Monaural

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Stereo total output voltage	V <sub>OST</sub>	L-channel V <sub>OST</sub> : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 100% modulation) input R-channel V <sub>OST</sub> : Output voltage of ROT pin COM pin : Stereo signal (R-only, 300 Hz, 100% modulation) input	Stereo
SAP total output voltage	V <sub>OSAP1</sub>	V <sub>OSAP1</sub> : Output voltage of ROT and LOT pins COM pin : SAP signal (300 Hz, 100% modulation) input	SAP1
SAP single output voltage	V <sub>OSAP2</sub>	V <sub>OSAP2</sub> : Output voltage of SOT pin COM pin : SAP signal (300 Hz, 100% modulation, Noise reduction: OFF) input	SAP
Normal output voltage	V <sub>ONO</sub>	V <sub>ONO</sub> : Output voltage of NOT pin COM pin : Monaural signal (300 Hz, 100% modulation) input	Monaural
Difference between monaural L and R output voltage	V <sub>OLR</sub>	$V_{OLR} = 20 \log (V_L \div V_R)$ V <sub>L</sub> : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 100% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : Monaural signal (300 Hz, 100% modulation) input	
Monaural total frequency characteristics 1	V <sub>OMO1</sub>	$V_{OMO1} = 20 \log \{V(1k) \div V(300)\}$ V(1k) : Output voltage of LOT pin COM pin : Monaural signal (1 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 30% modulation) input	
Monaural total frequency characteristics 2	V <sub>OMO2</sub>	$V_{OMO2} = 20 \log \{V(3k) \div V(300)\}$ V(3k) : Output voltage of LOT pin COM pin : Monaural signal (3 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 30% modulation) input	
Monaural total frequency characteristics 3	V <sub>OMO3</sub>	$V_{OMO3} = 20 \log \{V(8k) \div V(300)\}$ V(8k) : Output voltage of LOT pin COM pin : Monaural signal (8 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 30% modulation) input	
Monaural total frequency characteristics 4	V <sub>OMO4</sub>	$V_{OMO4} = 20 \log \{V(12k) \div V(300)\}$ V(12k) : Output voltage of LOT pin COM pin : Monaural signal (12 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 30% modulation) input	
Stereo total frequency characteristics 1	V <sub>OST1</sub>	$V_{OST1} = 20 \log \{V(1k) \div V(300)\}$ V(1k) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 1 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input	Stereo
Stereo total frequency characteristics 2	V <sub>OST2</sub>	$V_{OST2} = 20 \log \{V(3k) \div V(300)\}$ V(3k) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 3 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input	

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Stereo total frequency characteristics 3	V <sub>OST3</sub>	$V_{OST3} = 20 \log \{V(8k) \div V(300)\}$ V(8k) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 8 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input	Stereo
Stereo total frequency characteristics 4	V <sub>OST4</sub>	$V_{OST4} = 20 \log \{V(12k) \div V(300)\}$ V(12k) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 12 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input	
SAP total frequency characteristics 1	V <sub>OSAP11</sub>	$V_{OSAP11} = 20 \log \{V(1k) \div V(300)\}$ V(1k) : Output voltage of LOT pin COM pin : SAP signal (1 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : SAP signal (300 Hz, 30% modulation) input	SAP1
SAP total frequency characteristics 2	V <sub>OSAP12</sub>	$V_{OSAP12} = 20 \log \{V(3k) \div V(300)\}$ V(3k) : Output voltage of LOT pin COM pin : SAP signal (3 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : SAP signal (300 Hz, 30% modulation) input	
SAP total frequency characteristics 3	V <sub>OSAP13</sub>	$V_{OSAP13} = 20 \log \{V(8k) \div V(300)\}$ V(8k) : Output voltage of LOT pin COM pin : SAP signal (8 kHz, 30% modulation) input V(300) : Output voltage of LOT pin COM pin : SAP signal (300 Hz, 30% modulation) input	
SAP single frequency characteristics 1	V <sub>OSAP21</sub>	$V_{OSAP21} = 20 \log \{V(1k) \div V(300)\}$ V(1k) : Output voltage of SOT pin COM pin : SAP signal (1 kHz, 30% modulation, Noise reduction: OFF) input V(300) : Output voltage of SOT pin COM pin : SAP signal (300 Hz, 30% modulation, Noise reduction: OFF) input	SAP
SAP single frequency characteristics 2	V <sub>OSAP22</sub>	$V_{OSAP22} = 20 \log \{V(3k) \div V(300)\}$ V(3k) : Output voltage of SOT pin COM pin : SAP signal (3 kHz, 30% modulation, Noise reduction: OFF) input V(300) : Output voltage of SOT pin COM pin : SAP signal (300 Hz, 30% modulation, Noise reduction: OFF) input	
SAP single frequency characteristics 3	V <sub>OSAP23</sub>	$V_{OSAP23} = 20 \log \{V(8k) \div V(300)\}$ V(8k) : Output voltage of SOT pin COM pin : SAP signal (8 kHz, 30% modulation, Noise reduction: OFF) input V(300) : Output voltage of SOT pin COM pin : SAP signal (300 Hz, 30% modulation, Noise reduction: OFF) input	

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Stereo channel separation 1	Sep <sub>1</sub>	L-channel $Sep_1 = 20 \log (V_L + V_R)$ V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (L-only, 300 Hz, 30% modulation) input R-channel $Sep_1 = 20 \log (V_R + V_L)$ V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (R-only, 300 Hz, 30% modulation) input V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (R-only, 300 Hz, 30% modulation) input (465Z manufactured by EIDEN Co., Ltd.)	Stereo
Stereo channel separation 2	Sep <sub>2</sub>	L-channel $Sep_2 = 20 \log (V_L + V_R)$ V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (L-only, 1 kHz, 30% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (L-only, 1 kHz, 30% modulation) input R-channel $Sep_2 = 20 \log (V_R + V_L)$ V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (R-only, 1 kHz, 30% modulation) input V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (R-only, 1 kHz, 30% modulation) input (465Z manufactured by EIDEN Co., Ltd.)	
Stereo channel separation 3	Sep <sub>3</sub>	L-channel $Sep_3 = 20 \log (V_L + V_R)$ V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (L-only, 3 kHz, 30% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (L-only, 3 kHz, 30% modulation) input R-channel $Sep_3 = 20 \log (V_R + V_L)$ V <sub>R</sub> : Output voltage of ROT pin COM pin : Stereo signal (R-only, 3 kHz, 30% modulation) input V <sub>L</sub> : Output voltage of LOT pin COM pin : Stereo signal (R-only, 3 kHz, 30% modulation) input (465Z manufactured by EIDEN Co., Ltd.)	
Monaural total harmonic distortion	THD <sub>MO</sub>	THD <sub>MO</sub> : Distortion rate of LOT and ROT pins COM pin : Monaural signal (1 kHz, 100% modulation) input	Monaural
Stereo total harmonic distortion 1	THD <sub>ST1</sub>	L-channel THD <sub>ST1</sub> : Distortion rate of LOT pin COM pin : Stereo signal (L-only, 1 kHz, 100% modulation) input R-channel THD <sub>ST1</sub> : Distortion rate of ROT pin COM pin : Stereo signal (R-only, 1 kHz, 100% modulation) input	Stereo

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**



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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Stereo total harmonic distortion 2	THD <sub>ST2</sub>	L-channel THD <sub>ST2</sub> : Distortion rate of LOT pin COM pin : Stereo signal (L-only, 8 kHz, 30% modulation) input R-channel THD <sub>ST2</sub> : Distortion rate of ROT pin COM pin : Stereo signal (R-only, 8 kHz, 30% modulation) input	Stereo
SAP total harmonic distortion	THD <sub>SAP1</sub>	THD <sub>SAP1</sub> : Distortion rate of LOT and ROT pins COM pin : SAP signal (1 kHz, 100% modulation) input	SAP1
SAP single harmonic distortion	THD <sub>SAP2</sub>	THD <sub>SAP2</sub> : Distortion rate of SOT pin COM pin : SAP signal (1 kHz, 100% modulation, Noise reduction off) input	SAP
Normal output harmonic distortion	THD <sub>NO</sub>	THD <sub>NO</sub> : Distortion rate of NOT pin COM pin : Monaural signal (1 kHz, 100% modulation) input	Monaural
Crosstalk 1 (SAP → stereo)	CT <sub>1</sub>	$CT_1 = 20 \log (V_{CT1} \div V_L)$ V <sub>CT1</sub> : V <sub>L</sub> after BPF (3 kHz) V <sub>L</sub> : Output voltage of LOT pin COM pin : Composite signal {Stereo signal (L-only, 800 Hz, 30% modulation) and SAP signal (3 kHz, 30 % modulation) } input BPF : Attenuation of 0 dB at 3 kHz and 80 dB at 800 Hz, or more	Stereo
Crosstalk 2 (stereo → SAP)	CT <sub>2</sub>	$CT_2 = 20 \log (V_{CT2} \div V_L)$ V <sub>CT2</sub> : V <sub>L</sub> after BPF (3 kHz) V <sub>L</sub> : Output voltage of LOT pin COM pin : Composite signal {SAPsignal (800 Hz, 30% modulation) and Stereo signal (L-only, 3 kHz, 30 % modulation) } input BPF : Attenuation of 0 dB at 3 kHz and 80 dB at 800 Hz, or more	SAP1
Monaural total S/N	S/N <sub>MO</sub>	L-channel $S/N_{MO} = 20 \log (V_{OMOL} \div V_L)$ V <sub>OMOL</sub> : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 100% modulation) input V <sub>L</sub> : Output voltage of LOT pin (no signal) R-channel $S/N_{MO} = 20 \log (V_{OMOR} \div V_R)$ V <sub>OMOR</sub> : Output voltage of ROT pin COM pin : Monaural signal (300 Hz, 100% modulation) input V <sub>R</sub> : Output voltage of ROT pin (no signal)	Monaural
Stereo total S/N	S/N <sub>ST</sub>	L-channel $S/N_{ST} = 20 \log (V_{OSTL} \div V_L)$ V <sub>OSTL</sub> : Output voltage of LOT pin COM pin : Stereo signal (L-only, 300 Hz, 100% modulation) input V <sub>L</sub> : Output voltage of LOT pin COM pin : Pilot signal input R-channel $S/N_{ST} = 20 \log (V_{OSTR} \div V_R)$ V <sub>OSTR</sub> : Output voltage of ROT pin COM pin : Stereo signal (R-only, 300 Hz, 100% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : Pilot signal input	Stereo

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
SAP total S/N	S/N <sub>SAP</sub>	L-channel $S/N_{SAP} = 20 \log (V_{OSAP1L} \div V_L)$ V <sub>OSAP1L</sub> : Output voltage of LOT pin COM pin : SAP signal (300 Hz, 100% modulation) input V <sub>L</sub> : Output voltage of LOT pin COM pin : SAP carrier (0 % modulation) input R-channel $S/N_{SAP} = 20 \log (V_{OSAP1R} \div V_R)$ V <sub>OSAP1R</sub> : Output voltage of ROT pin COM pin : SAP signal (300 Hz, 100% modulation) input V <sub>R</sub> : Output voltage of ROT pin COM pin : SAP carrier (0 % modulation) input	SAP1
Normal output S/N	S/N <sub>NO</sub>	$S/N_{NO} = 20 \log (V_{ONO} \div V_M)$ V <sub>ONO</sub> : Output voltage of NOT pin COM pin : Monaural signal (300 Hz, 100% modulation) input V <sub>M</sub> : Output voltage of NOT pin (no signal)	Monaural
Total muting level	Mute	Mute = 20 log (V <sub>OMOL</sub> ÷ V <sub>M</sub> ) V <sub>OMOL</sub> : Output voltage of LOT pin COM pin : Monaural signal (300 Hz, 100% modulation) input V <sub>M</sub> : Output voltage of LOT pin Write register 06H, D0 : 0 COM pin : Monaural signal (300 Hz, 100% modulation) input	Monaural mute
dbx timing current	I <sub>T</sub>	I <sub>T</sub> : Current that flows from V <sub>CC</sub> to STI and WTI pins STI and WTI pins : 6-V DC is applied.	
Inter-mode DC offset 1	V <sub>DOF1</sub>	V <sub>DOF1</sub> = V <sub>MONO</sub> – V <sub>Mute</sub> V <sub>MONO</sub> : DC voltage at LOT and ROT pins User mode : Monaural NDT pin : 6-V DC is applied. V <sub>Mute</sub> : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1 : 0) NDT pin : 6-V DC is applied.	Mute to Monaural
Inter-mode DC offset 2	V <sub>DOF2</sub>	V <sub>DOF2</sub> = V <sub>ST</sub> – V <sub>Mute</sub> V <sub>ST</sub> : DC voltage at LOT and ROT pins User mode : Stereo NDT pin : 6-V DC is applied. V <sub>Mute</sub> : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1 : 0) NDT pin : 6-V DC is applied.	Mute to Stereo
Inter-mode DC offset 3	V <sub>DOF3</sub>	V <sub>DOF3</sub> = V <sub>SAP</sub> – V <sub>Mute</sub> V <sub>SAP</sub> : DC voltage at LOT and ROT pins User mode : SAP1 NDT pin : 6-V DC is applied. V <sub>Mute</sub> : DC voltage at LOT and ROT pins User mode : Mute (write register 06H, D1 : 0) NDT pin : 6-V DC is applied.	Mute to SAP1

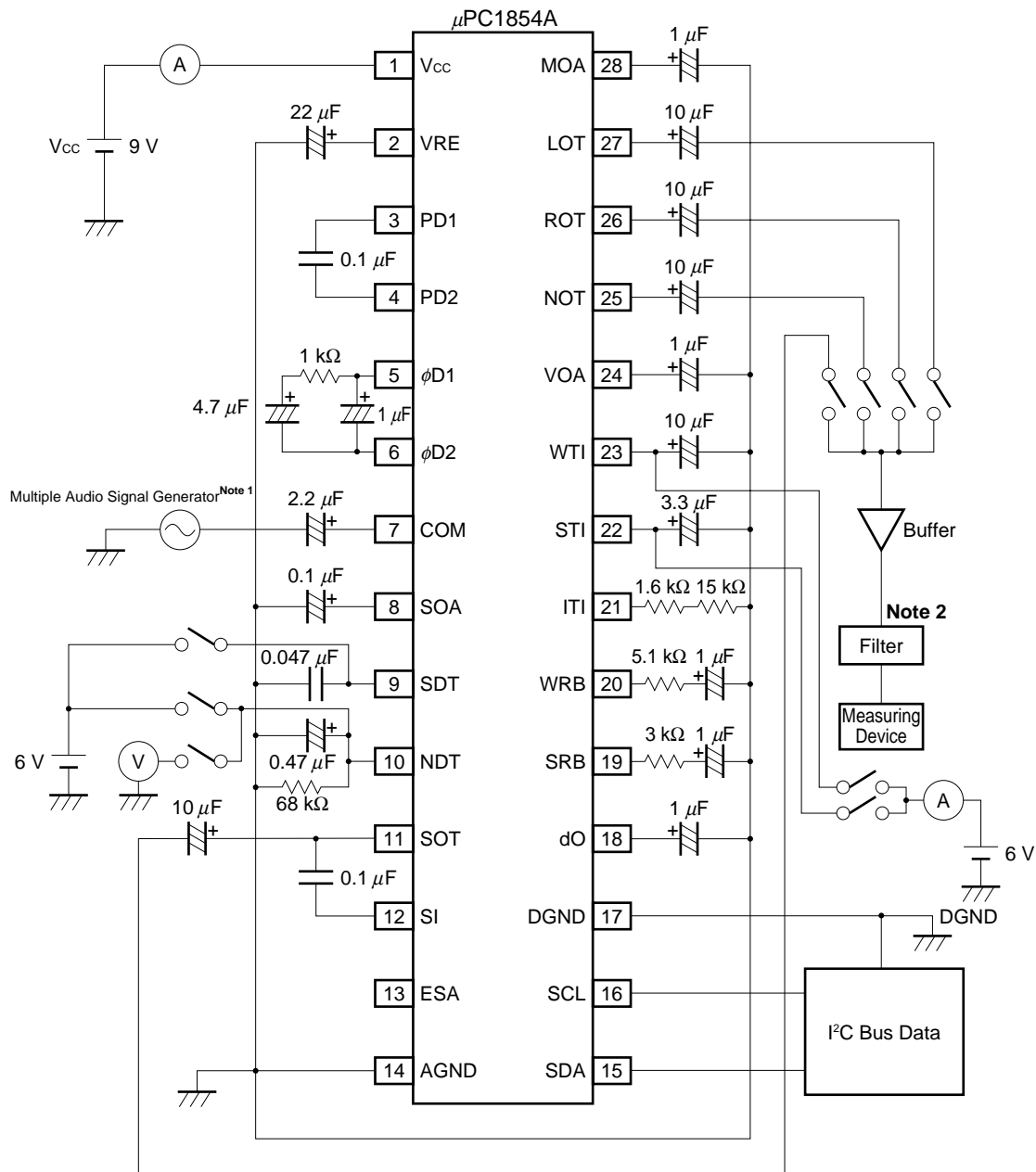
**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

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Parameter	Symbol	Test Conditions	User Mode <sup>Note</sup>
Inter-mode DC offset 4	$V_{DOF4}$	$V_{DOF4} = V_{MONO} - V_{Mute}$ $V_{MONO}$ : DC voltage at NOT pin User mode : Monaural NDT pin : 6-V DC is applied. $V_{Mute}$ : DC voltage at NOT pin User mode : Mute (write register 06H, D1: 0) NDT pin : 6-V DC is applied.	Mute to Monaural
Inter-mode DC offset 5	$V_{DOF5}$	$V_{DOF5} = V_{EXT} - V_{Mute}$ $V_{EXT}$ : DC voltage at NOT pin User mode : External SAP NDT pin: 6-V DC is applied. $V_{Mute}$ : DC voltage at NOT pin User mode : Mute (write register 06H, D1 : 0) NDT pin: 6-V DC is applied.	Mute to External SAP

**Note** For details about the User Mode, refer to chapter 5. **MODE MATRIX.**

8. MEASURING CIRCUIT



**Notes 1.** 465Z manufactured by EIDEN Co., Ltd.

**2.** 30 kHz LPF, DIN/AUDIO filter, or 3kHz BPF

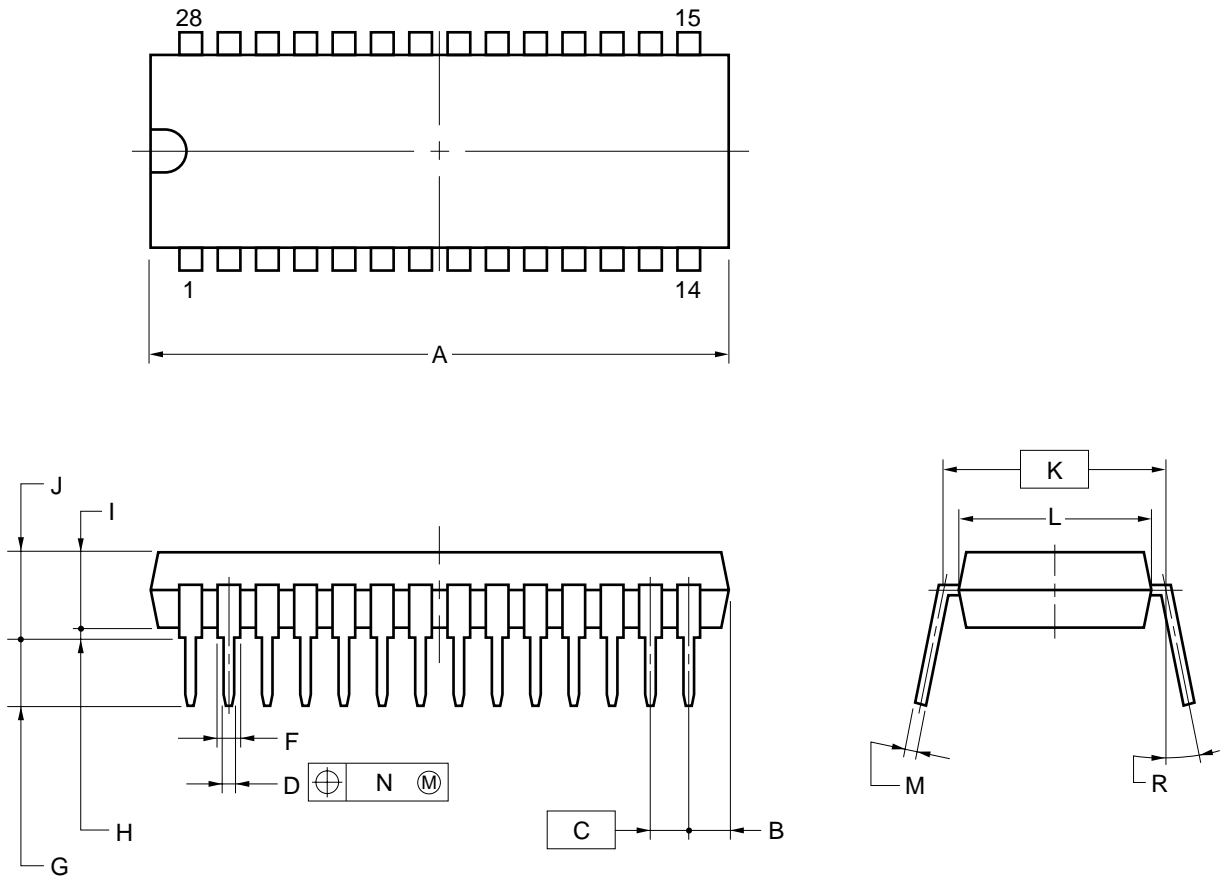
**Remark** Use the following for external parts.

Resistor : Metal film resistor ( $\pm 1\%$ ) for an ITI pin. Unless otherwise specified;  $\pm 5\%$

Capacitor : Tantalum capacitor ( $\pm 10\%$ ) for STI and WTI pins. Unless otherwise specified;  $\pm 20\%$

9. PACKAGE DRAWINGS

28-PIN PLASTIC SDIP (10.16mm400)



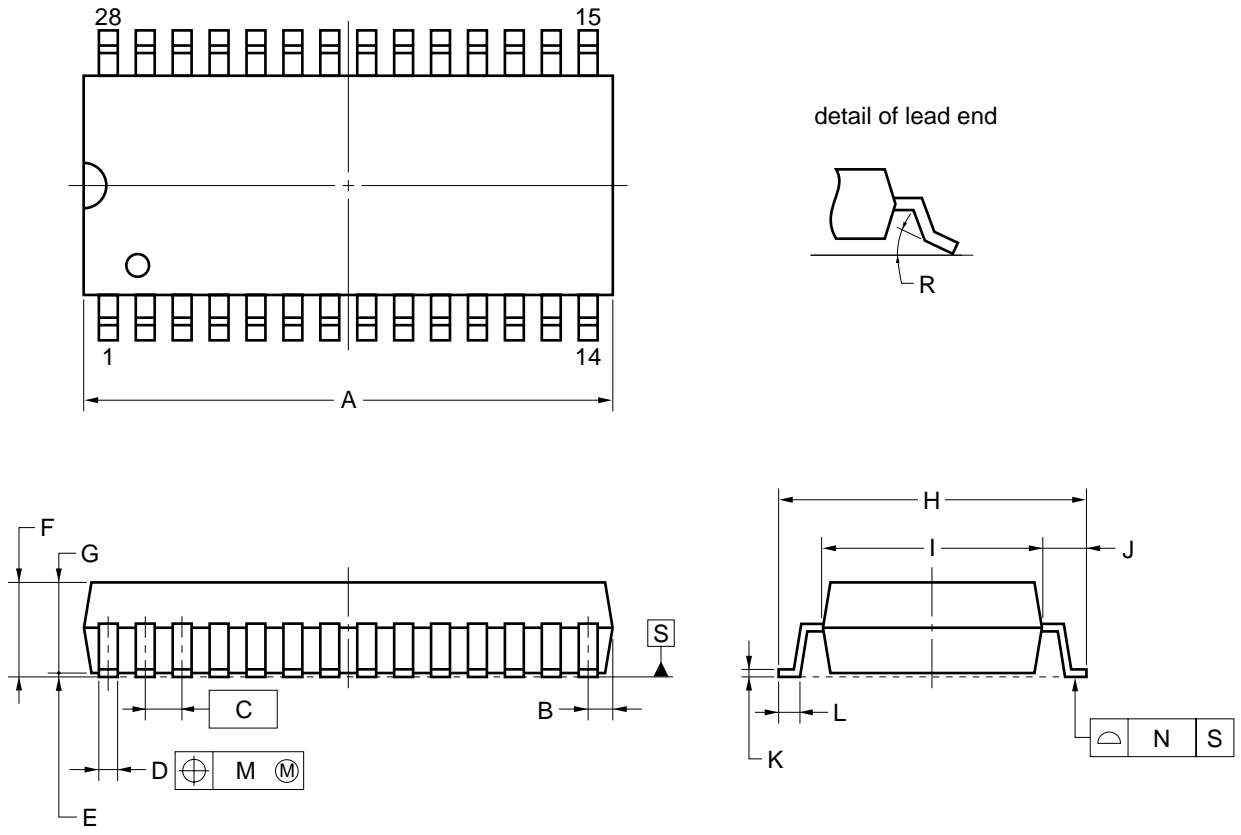
NOTES

1. Each lead centerline is located within 0.17 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	28.46 MAX.
B	2.67 MAX.
C	1.778 (T.P.)
D	0.50±0.10
F	0.85 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	10.16 (T.P.)
L	8.6
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>
N	0.17
R	0-15°

S28C-70-400B-2

28-PIN PLASTIC SOP (9.53 mm (375))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.9±0.2
B	0.845 MAX.
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.125±0.075
F	2.9 MAX.
G	2.50±0.2
H	10.3±0.2
I	7.2±0.2
J	1.6±0.2
K	0.17 <sup>+0.08</sup> <sub>-0.07</sub>
L	0.8
M	0.12
N	0.10
R	3° <sup>+7°</sup> <sub>-3°</sub>

P28GT-50-375B-3

**10. RECOMMENDED SOLDERING CONDITIONS**

The μPC1854A should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 10-1. Surface Mounting Type Soldering Conditions**

**μPC1854AGT : 28-pin plastic SOP (9.53 mm (400))**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max., Number of times: Once, Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin row)	—

**Caution Do not use different soldering methods together (except in the case of partial heating).**

**Table 10-2. Inserting Type Soldering Conditions**

**μPC1854ACT : 28-pin plastic SDIP (10.16 mm (400))**

Soldering Method	Soldering Conditions
Wave soldering (only pins)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin row)

**Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.**

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