NEC

MOS FIELD EFFECT TRANSISTOR

μPA1915

P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

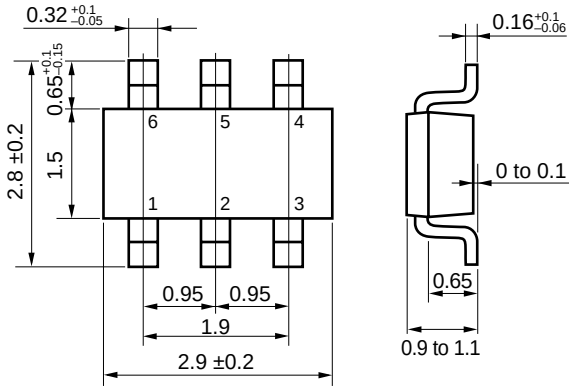
The μPA1915 is a switching device which can be driven directly by a 2.5-V power source.

The μPA1915 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- Can be driven by a 2.5-V power source
- Low on-state resistance
  - $R_{DS(on)1}$ = 55 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.5 A)
  - $R_{DS(on)2}$ = 58 mΩ MAX. (V_{GS} = –4.0 V, I_D = –2.5 A)
  - $R_{DS(on)3}$ = 82 mΩ MAX. (V_{GS} = –2.7 V, I_D = –2.5 A)
  - $R_{DS(on)4}$ = 90 mΩ MAX. (V_{GS} = –2.5 V, I_D = –2.5 A)

PACKAGE DRAWING (Unit : mm)

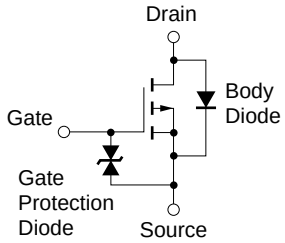


1, 2, 5, 6 : Drain
3 : Gate
4 : Source

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1915TE	SC-95 (Mini Mold Thin Type)

EQUIVALENT CIRCUIT



Marking: TH

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	–20	V
Gate to Source Voltage	V_{GSS}	±12	V
Drain Current (DC)	$I_{D(DC)}$	±4.5	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±18	A
Total Power Dissipation	P_{T1}	0.2	W
Total Power Dissipation Note2	P_{T2}	2	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on FR-4 Board, t ≤ 5 sec.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

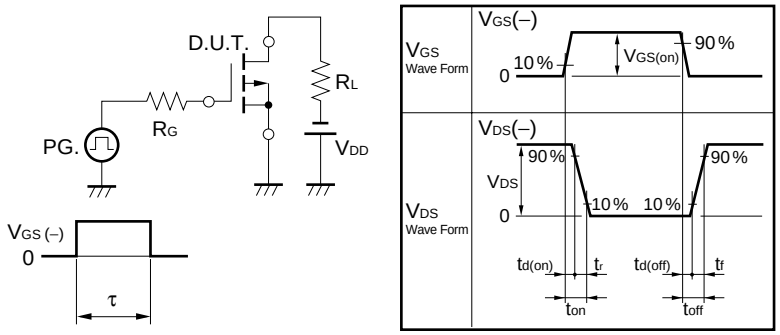
Document No. G14761EJ2V0DS00 (2nd edition)
Date Published May 2001 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

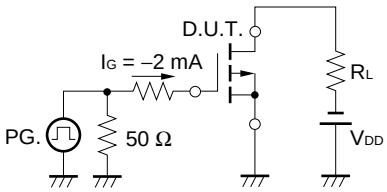
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–0.5	–1.1	–1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.5 A	3	8.8		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –2.5 A		45	55	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –2.5 A		47	58	mΩ
	$R_{DS(on)3}$	V_{GS} = –2.7 V, I_D = –2.5 A		61	82	mΩ
	$R_{DS(on)4}$	V_{GS} = –2.5 V, I_D = –2.5 A		67	90	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		820		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		210		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		100		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –10 V		16		ns
Rise Time	t_r	I_D = –2.5 A		14		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = –4.0 V		58		ns
Fall Time	t_f	R_G = 10 Ω		46		ns
Total Gate Charge	Q_G	V_{DD} = –16 V		5.0		nC
Gate to Source Charge	Q_{GS}	I_D = –4.5 A		2.0		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –4.0 V		2.5		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 4.5 A, V_{GS} = 0 V		0.86		V

TEST CIRCUIT 1 SWITCHING TIME



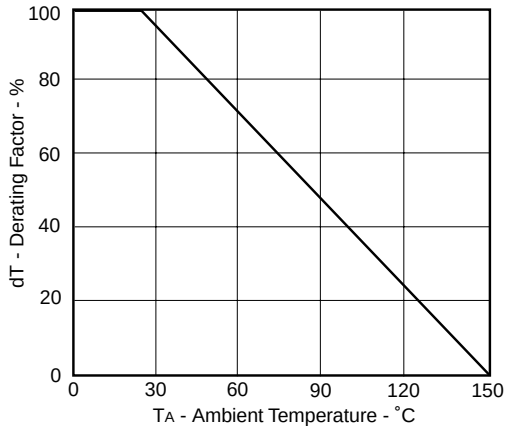
τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

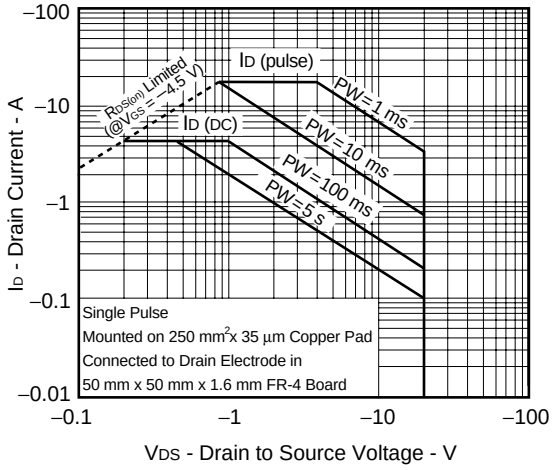


TYPICAL CHARACTERISTICS (T_A = 25°C)

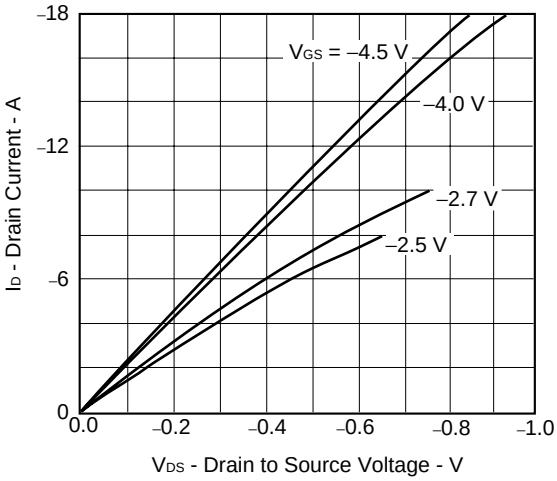
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



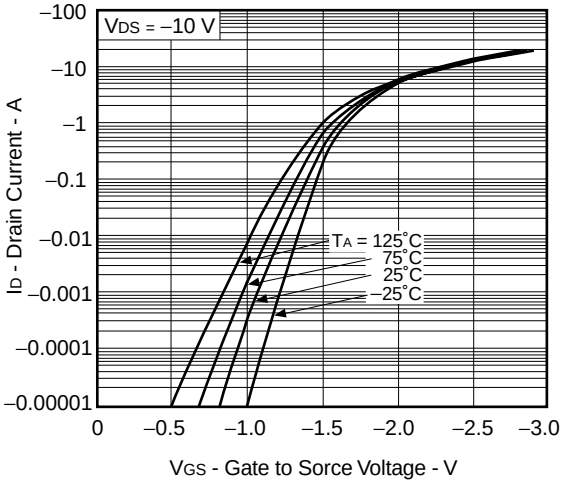
★ FORWARD BIAS SAFE OPERATING AREA



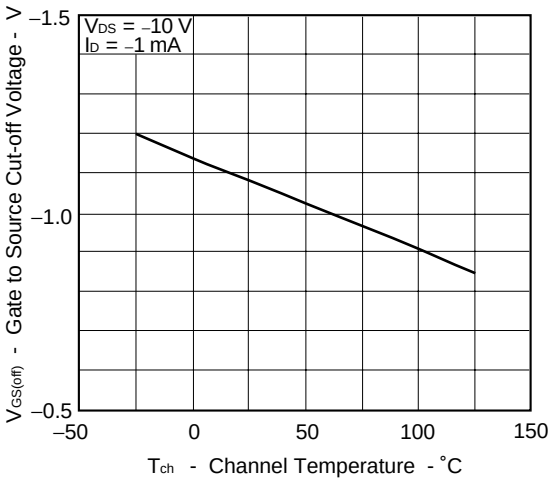
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



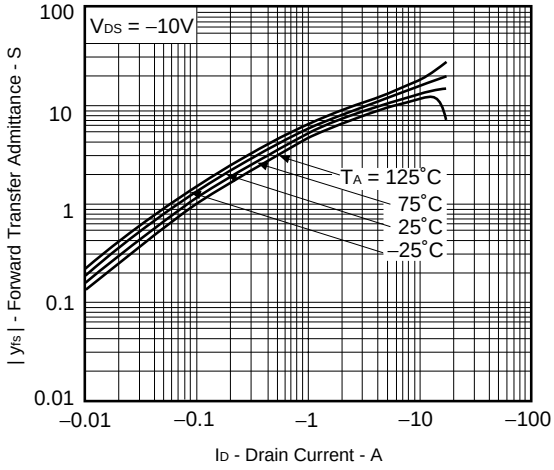
TRANSFER CHARACTERISTICS



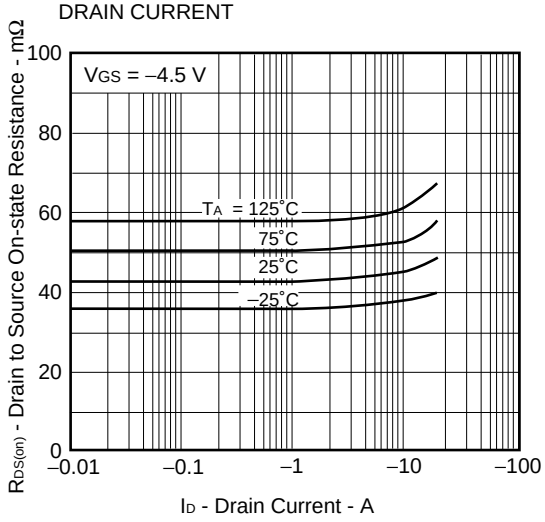
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



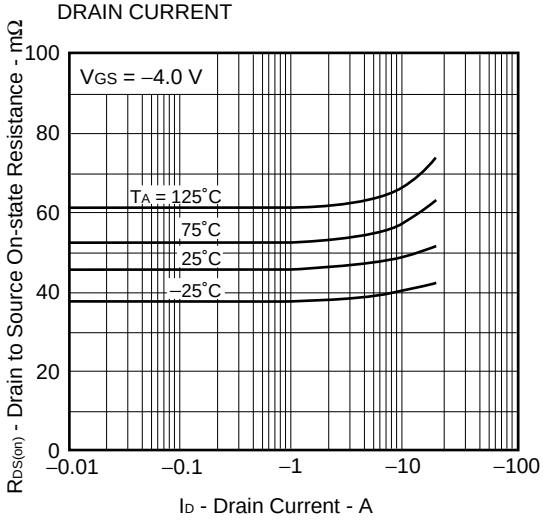
FORWARD TRANSFER ADMITTANCE Vs. DRAIN CURRENT



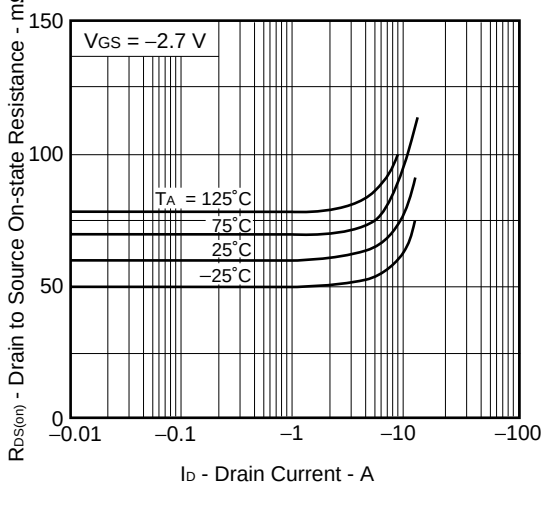
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



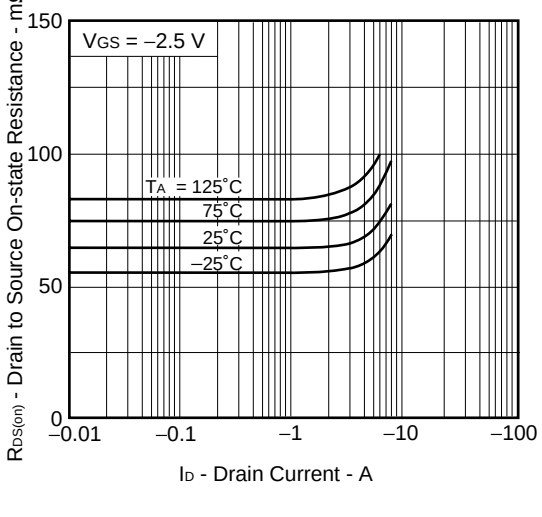
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



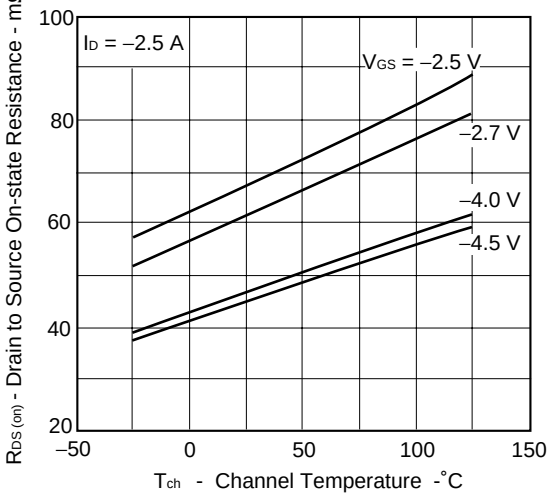
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



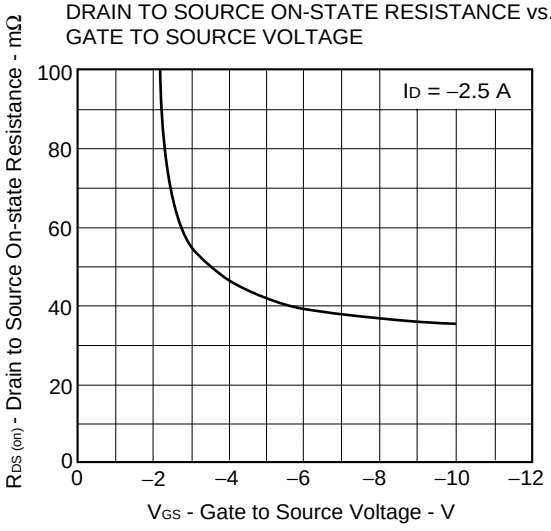
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



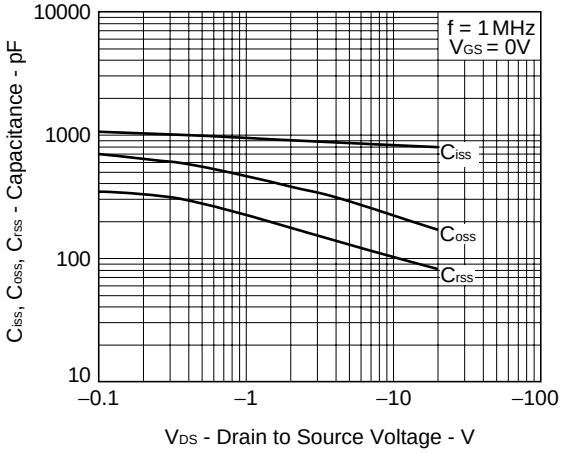
DRAIN TO SOURCE ON STATE RESISTANCE vs. CHANNEL TEMPERATURE



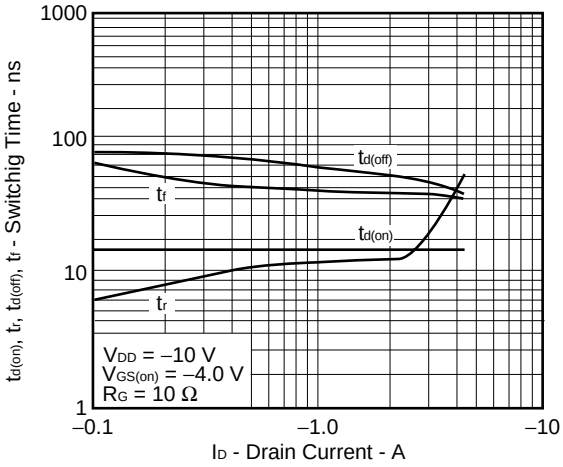
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



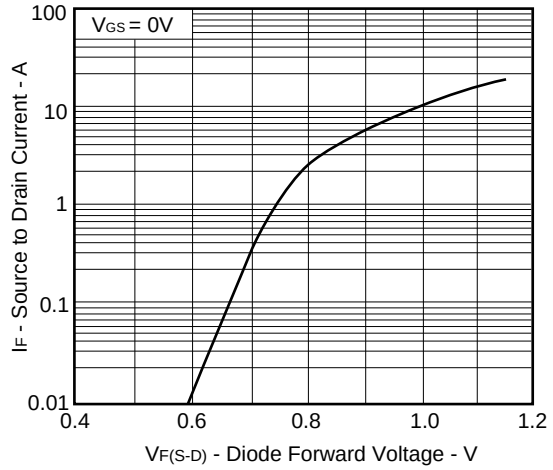
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



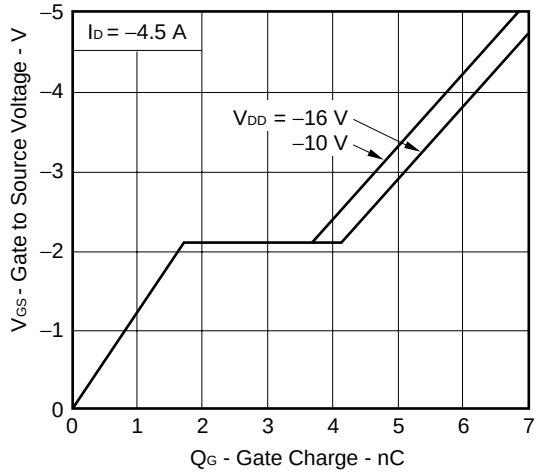
SWITCHING CHARACTERISTICS



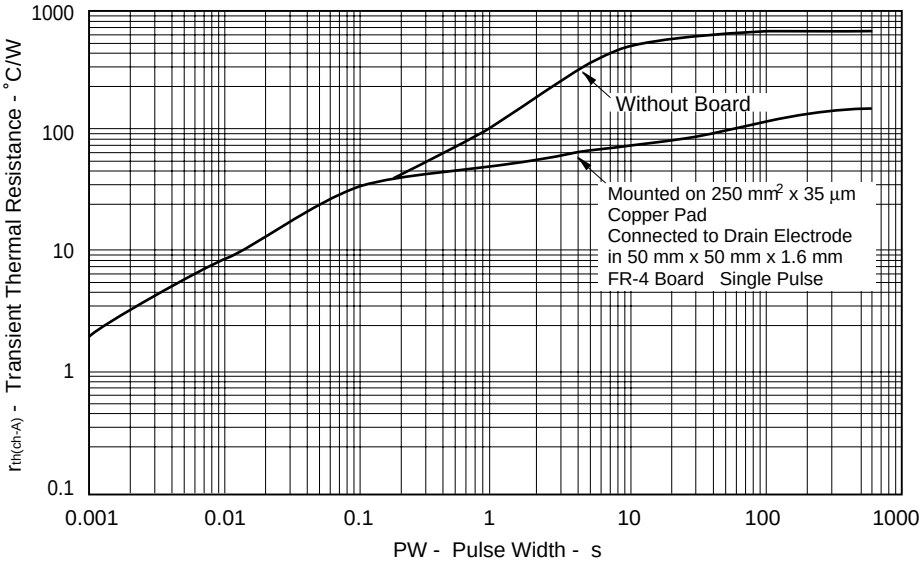
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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