NEC

MOS FIELD EFFECT TRANSISTOR

μPA1890

N- AND P-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μPA1890 is a switching device which can be driven directly by a 4.0-V power source.

The μPA1890 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

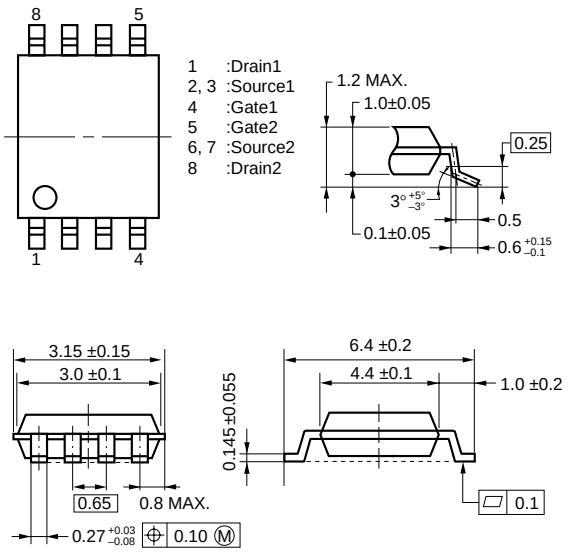
FEATURES

- Can be driven by a 4.0-V power source
- Low on-state resistance
  - N-Channel $R_{DS(on)1}$ = 27 mΩ MAX. (V_{GS} = 10 V, I_D = 3.0 A)
  - $R_{DS(on)2}$ = 37 mΩ MAX. (V_{GS} = 4.5 V, I_D = 3.0 A)
  - $R_{DS(on)3}$ = 47 mΩ MAX. (V_{GS} = 4.0 V, I_D = 3.0 A)
  - P-Channel $R_{DS(on)1}$ = 37 mΩ MAX. (V_{GS} = –10 V, I_D = –2.5 A)
  - $R_{DS(on)2}$ = 56 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.5 A)
  - $R_{DS(on)3}$ = 64 mΩ MAX. (V_{GS} = –4.0 V, I_D = –2.5 A)
- Built-in G-S protection diode against ESD

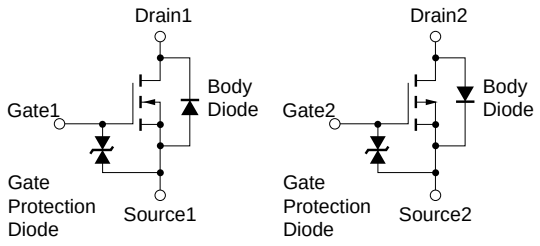
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1890GR-9JG	Power TSSOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



N-Channel P-Channel

To keep good radiate condition, it is recommended that all pins are soldering to print board.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

		N-Channel / P-Channel	
Drain to Source Voltage	V_{DSS}	30/–30	V
Gate to Source Voltage	V_{GSS}	±20/∓20	V
Drain Current (DC)	$I_{D(DC)}$	±6.0/∓5.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±24/∓20	A
Total Power Dissipation Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 5000 mm^2 x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Document No. G14762EJ2V0DS00 (2nd edition)
Date Published May 2001 NS CP(K)
Printed in Japan

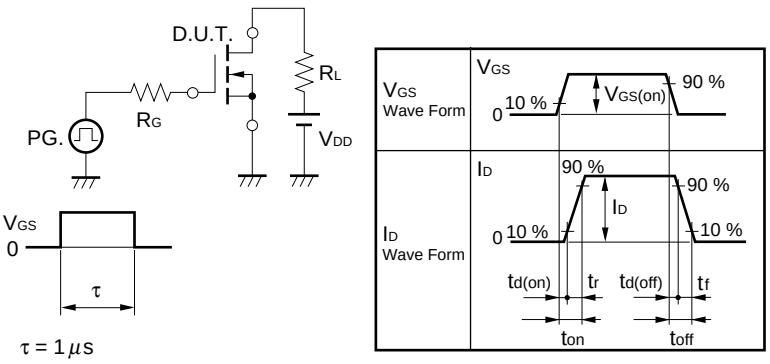
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

A) N-Channel

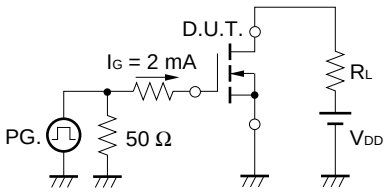
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	1.8	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.0 A	3	7.6		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.0 A		18	27	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 3.0 A		24	37	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 3.0 A		27	47	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		748		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		227		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		107		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V		20		ns
Rise Time	t_r	I_D = 3.0 A		80		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = 10 V		48		ns
Fall Time	t_f	R_G = 10 Ω		30		ns
Total Gate Charge	Q_G	V_{DD} = 24 V		14		nC
Gate to Source Charge	Q_{GS}	I_D = 6.0 A		1.9		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		3.8		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 6.0 A, V_{GS} = 0 V		0.82		V
Reverse Recovery Time	t_{rr}	I_F = 6.0 A, V_{GS} = 0 V		31		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		32		nC

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1 %

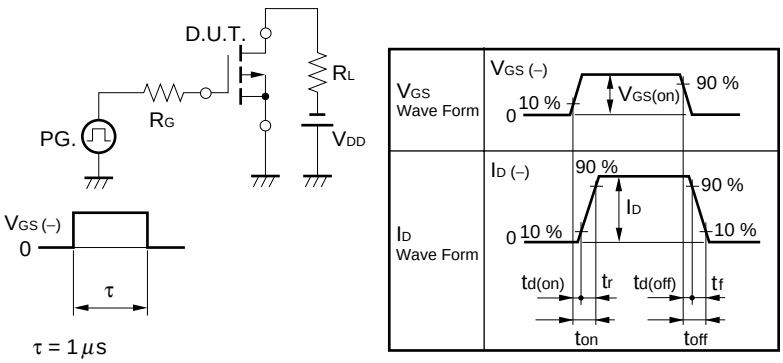
TEST CIRCUIT 2 GATE CHARGE



B) P-Channel

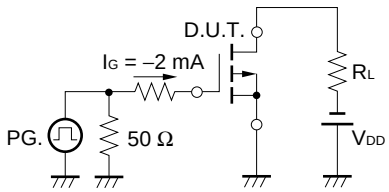
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.3	–1.8	–2.3	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.5 A	3	7.8		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –2.5 A		28	37	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –2.5 A		42	56	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –2.5 A		47	64	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		851		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		279		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		128		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V		17		ns
Rise Time	t_r	I_D = –2.5 A		52		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = –10 V		84		ns
Fall Time	t_f	R_G = 10 Ω		73		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		15		nC
Gate to Source Charge	Q_{GS}	I_D = –5.0 A		1.9		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		4.2		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 5.0 A, V_{GS} = 0 V		0.83		V
Reverse Recovery Time	t_{rr}	I_F = 5.0 A, V_{GS} = 0 V		38		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		35		nC

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1 %

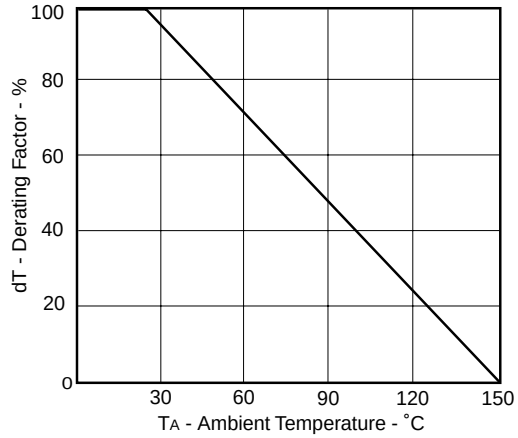
TEST CIRCUIT 2 GATE CHARGE



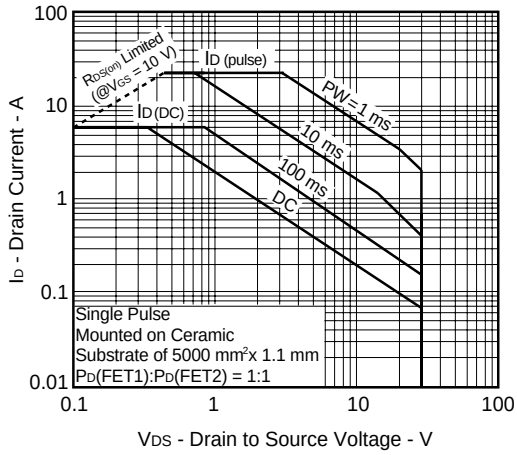
TYPICAL CHARACTERISTICS (T_A = 25°C)

A) N-Channel

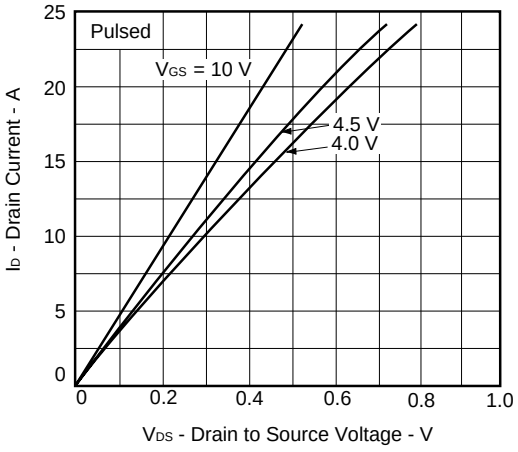
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



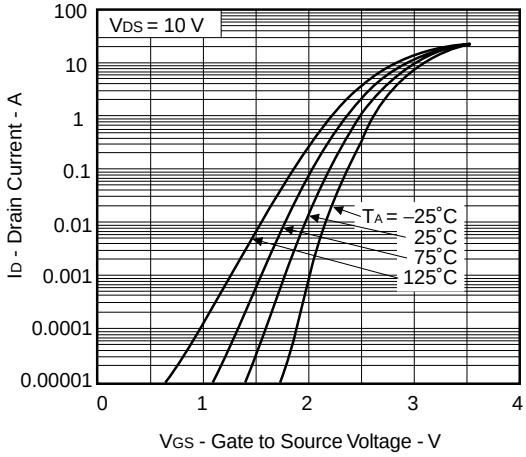
★ FORWARD BIAS SAFE OPERATING AREA



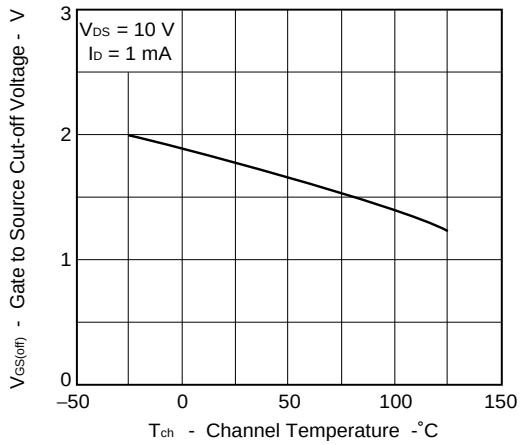
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



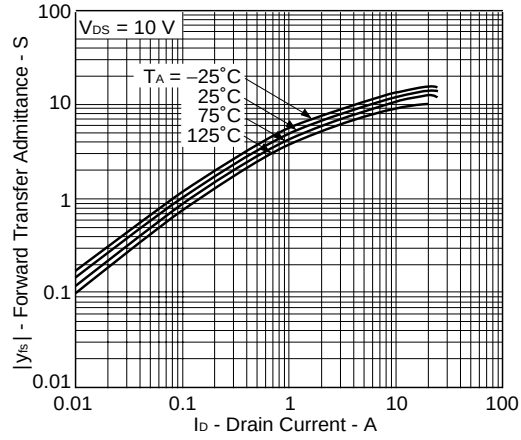
TRANSFER CHARACTERISTICS



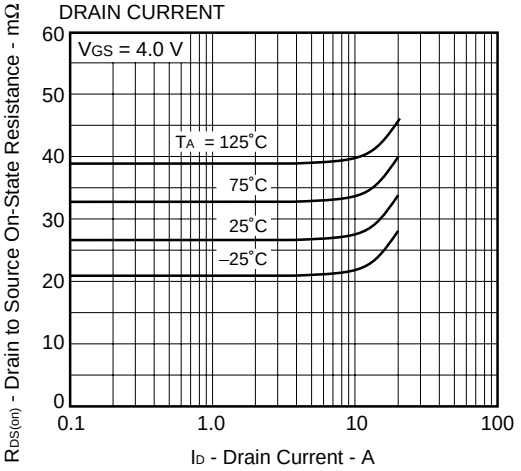
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



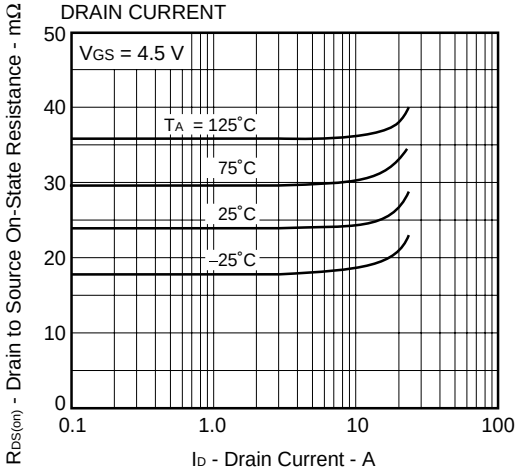
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



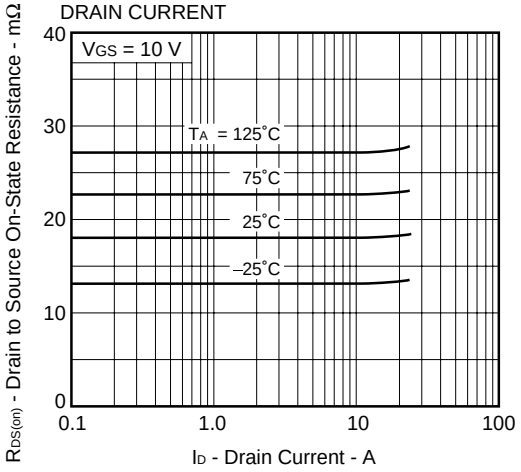
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



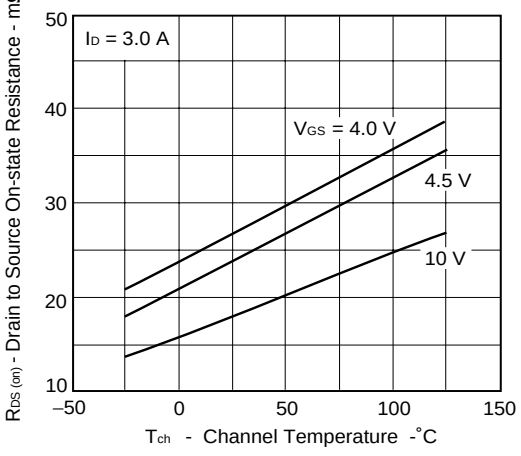
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



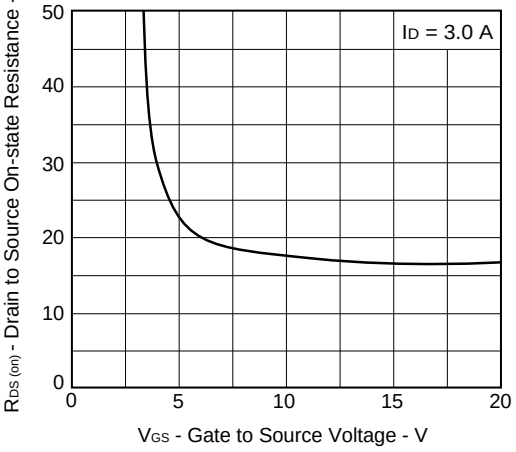
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



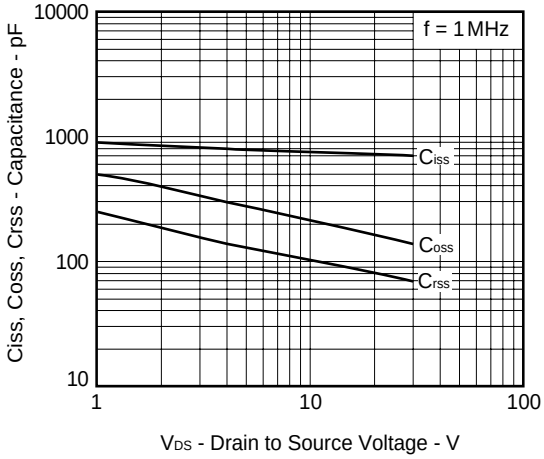
DRAIN TO SOURCE ON STATE RESISTANCE vs. CHANNEL TEMPERATURE



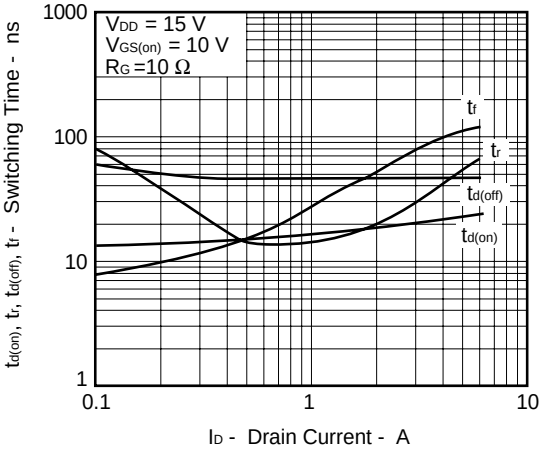
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



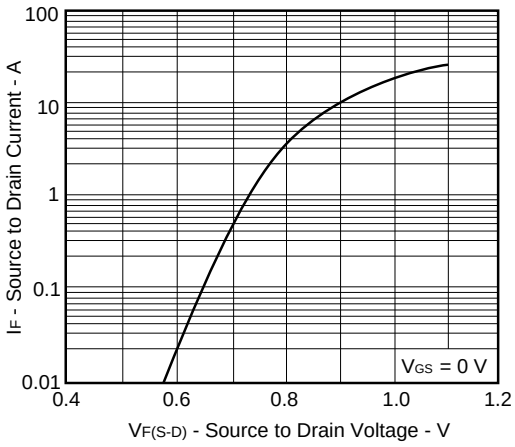
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



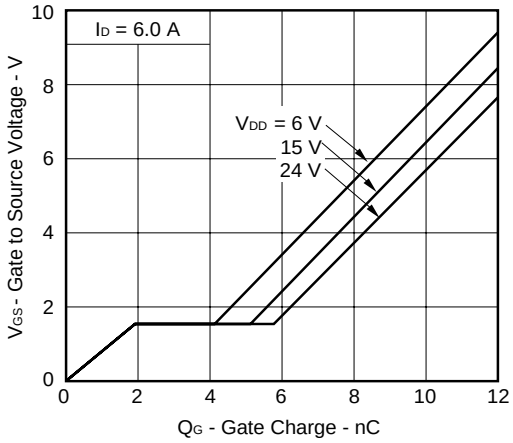
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

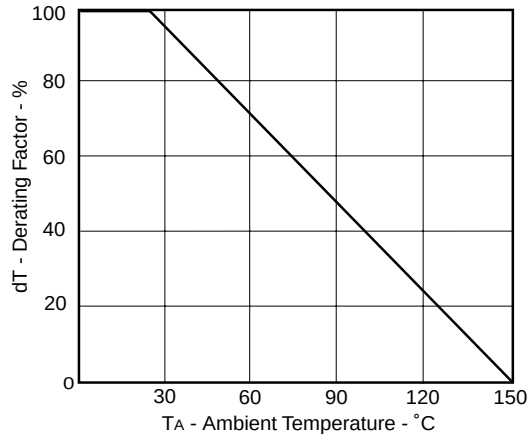


DYNAMIC INPUT CHARACTERISTICS

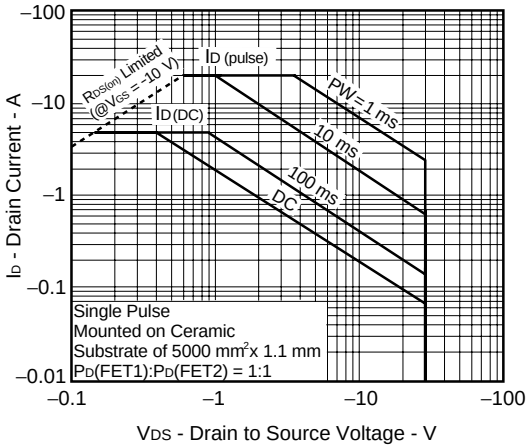


B) P-Channel

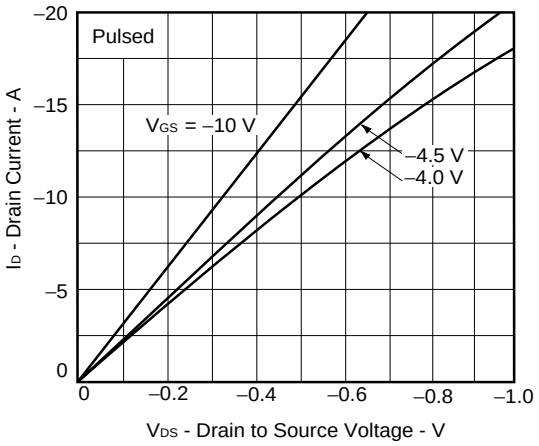
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



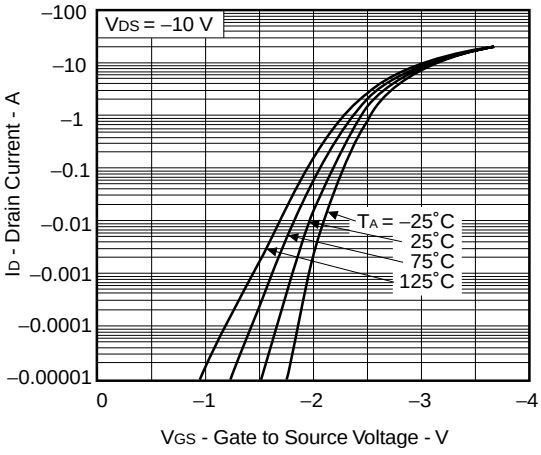
★ FORWARD BIAS SAFE OPERATING AREA



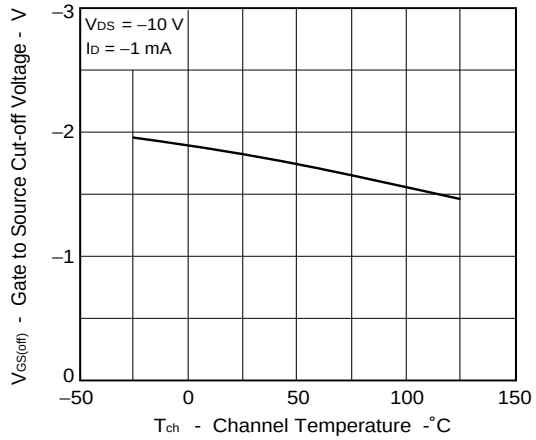
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



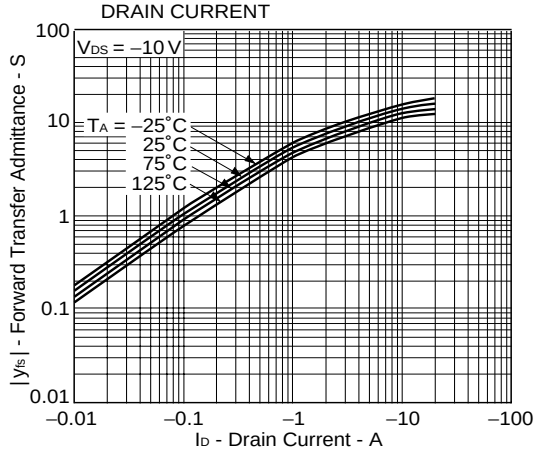
TRANSFER CHARACTERISTICS



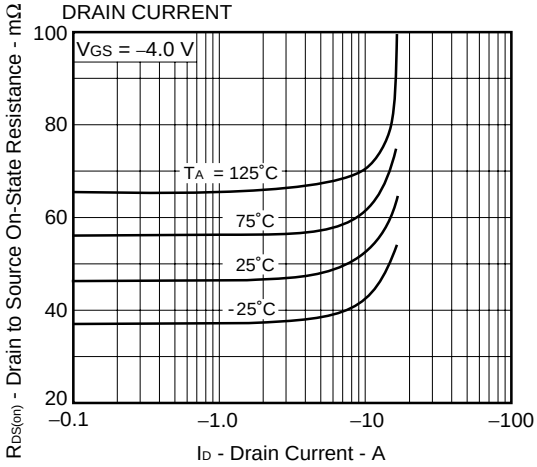
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



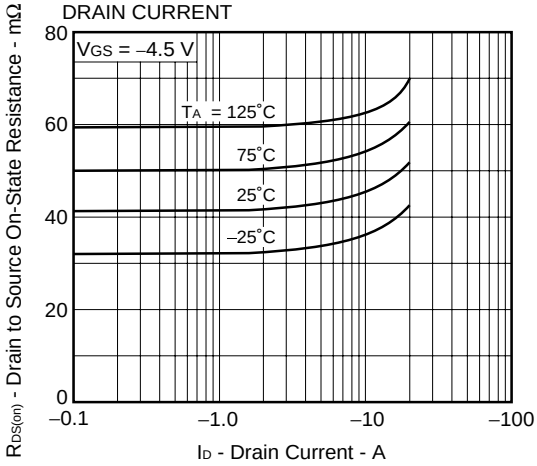
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



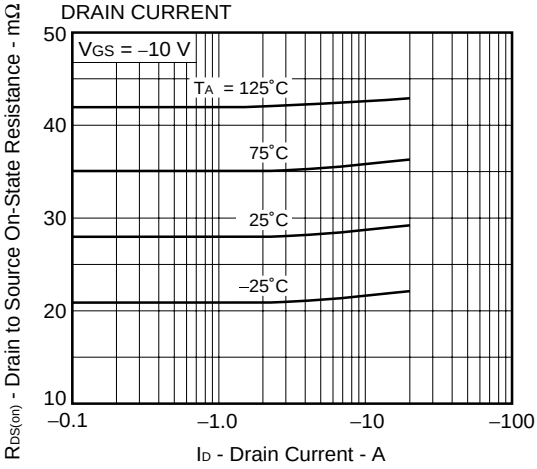
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



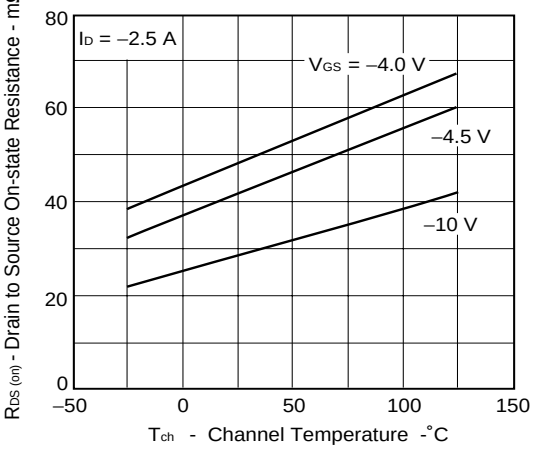
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



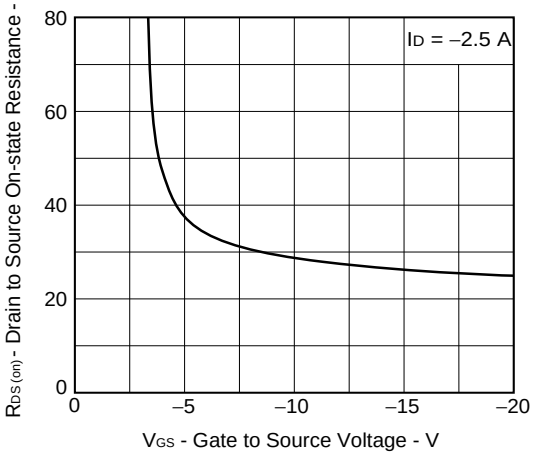
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



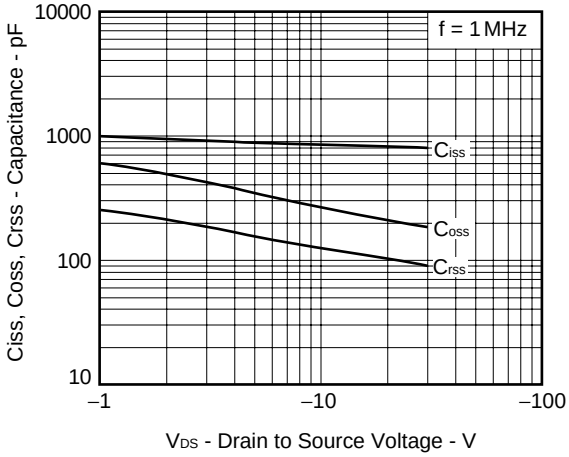
DRAIN TO SOURCE ON STATE RESISTANCE vs. CHANNEL TEMPERATURE



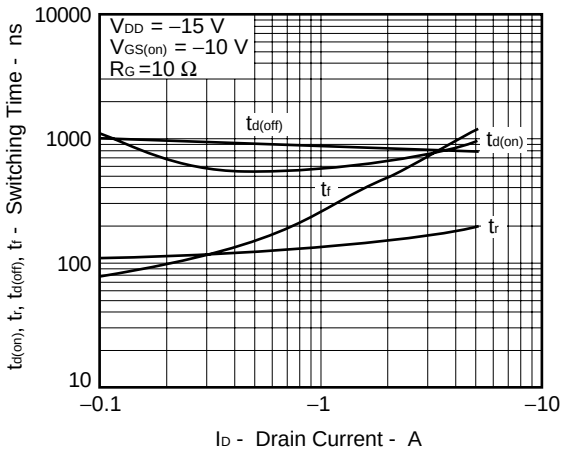
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



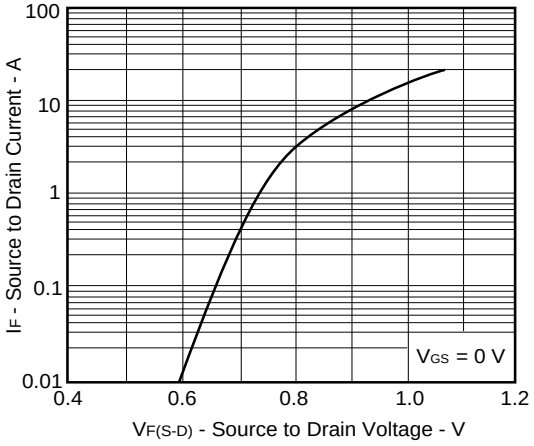
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



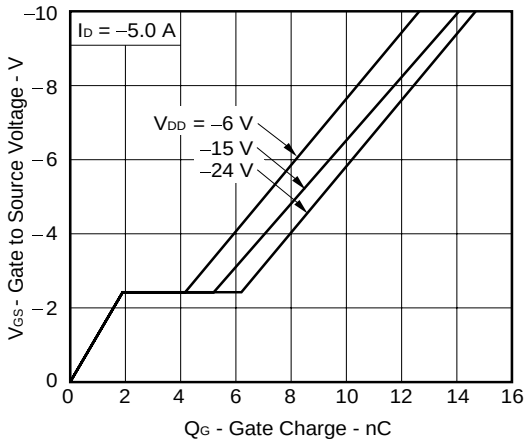
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



C) Common

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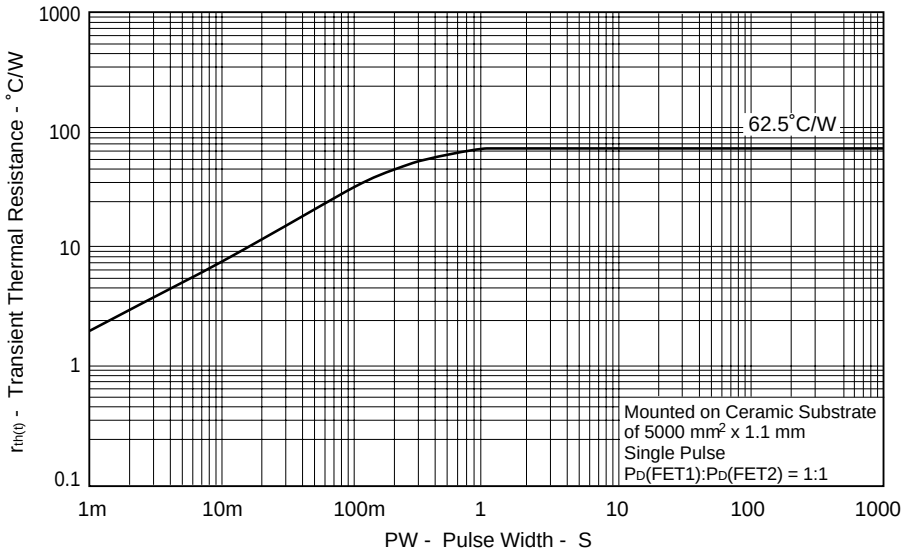
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

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  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
  (Note)
  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4