

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

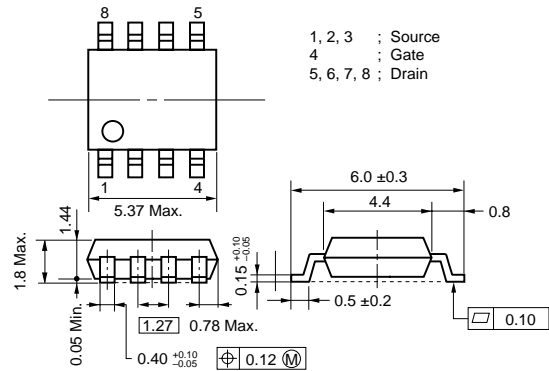
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC Converters and power management application of notebook computers.

FEATURES

- Super low on-state resistance  
 $R_{DS(on)1} = 19.0 \text{ m}\Omega$  TYP. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 4.0 \text{ A}$ )  
 $R_{DS(on)2} = 30.0 \text{ m}\Omega$  TYP. ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 4.0 \text{ A}$ )
- Low  $C_{iss}$  :  $C_{iss} = 750 \text{ pF}$  TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

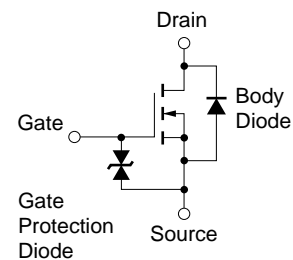
PART NUMBER	PACKAGE
$\mu$ PA1705G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 25$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 8$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 50$	A
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$

- Notes 1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1 \%$   
 2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 1.7 \text{ mm}$

EQUIVALENT CIRCUIT



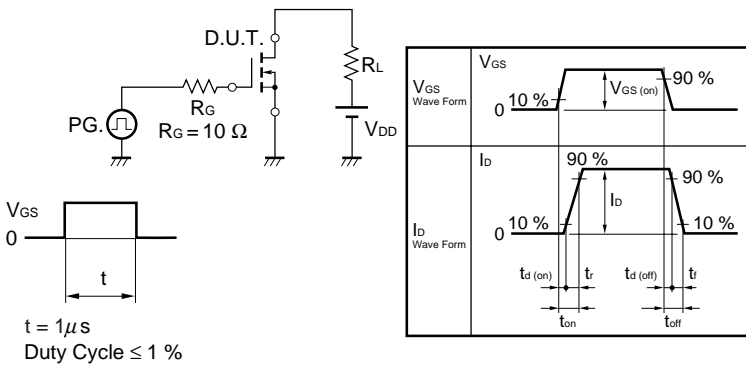
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

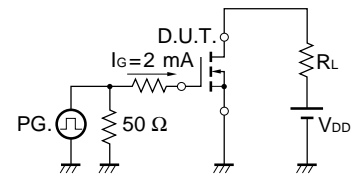
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A		19	27	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A		30	40	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A	4.0	8.4		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		750		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		350		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		160		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 4.0 A		19		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		107		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		50		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		32		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 8.0 A		19		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		2.4		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		6.3		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0 V		33		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs		22		nC

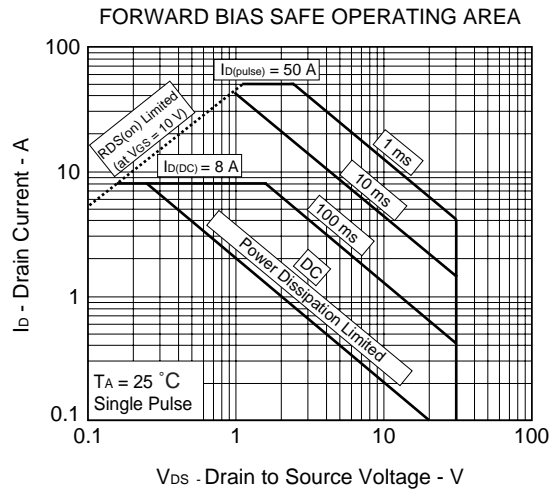
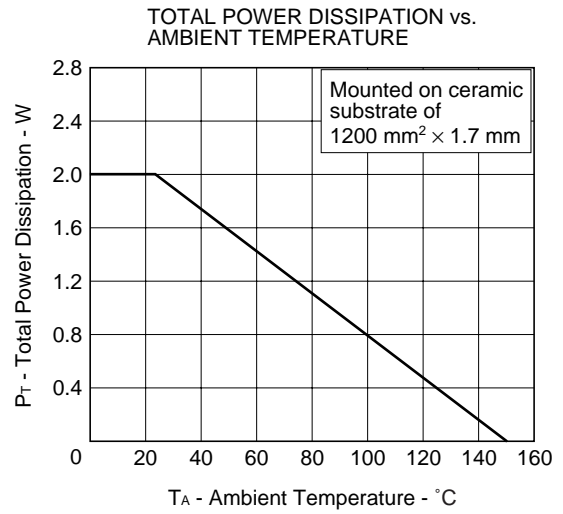
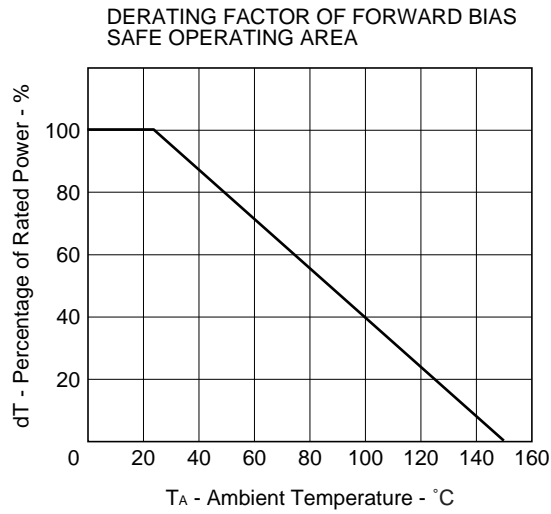
**TEST CIRCUIT 1 SWITCHING TIME**



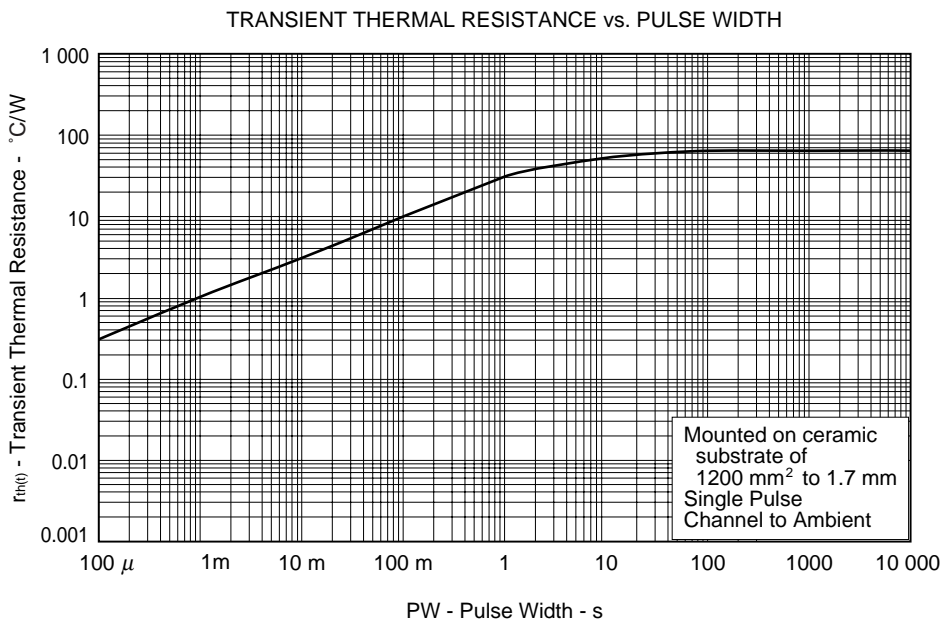
**TEST CIRCUIT 2 GATE CHARGE**

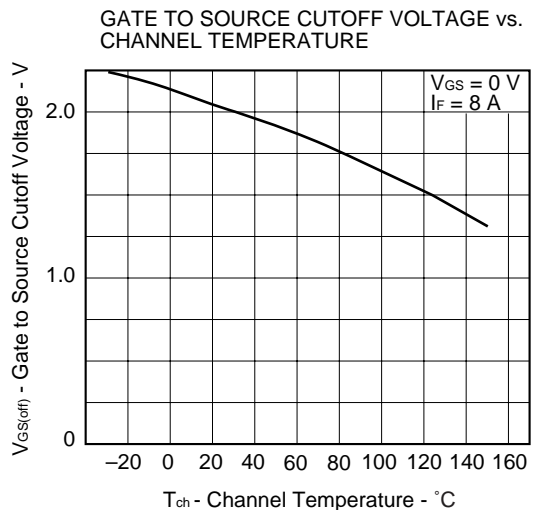
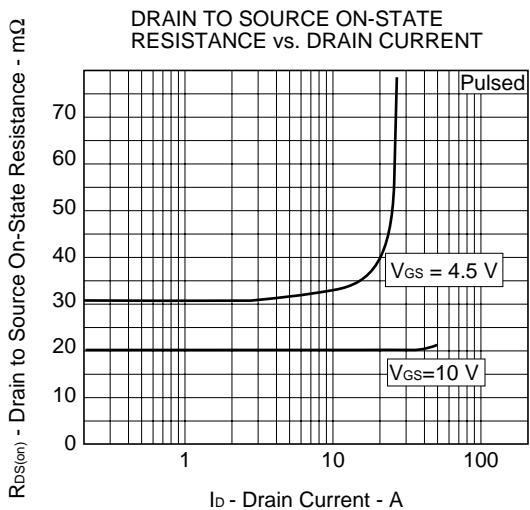
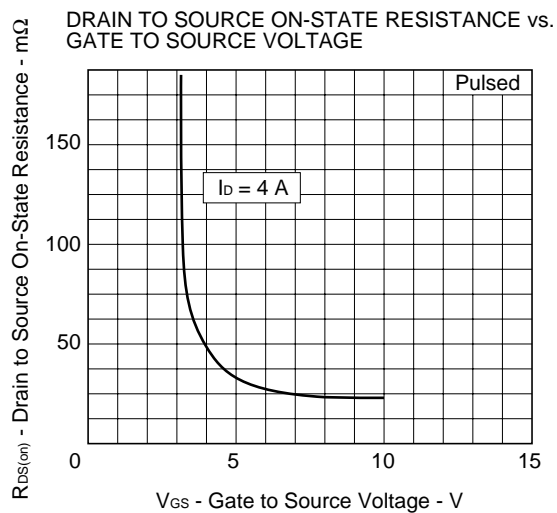
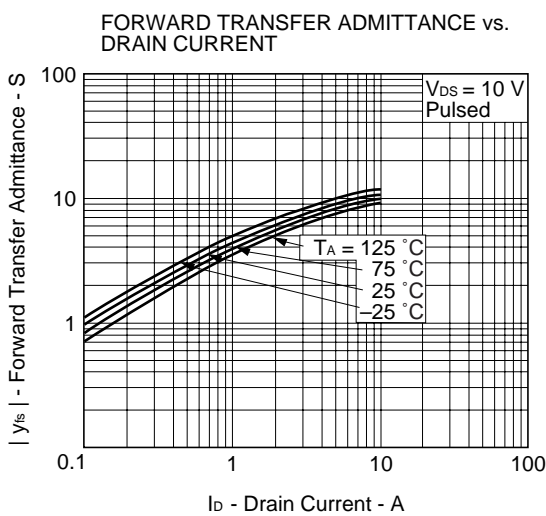
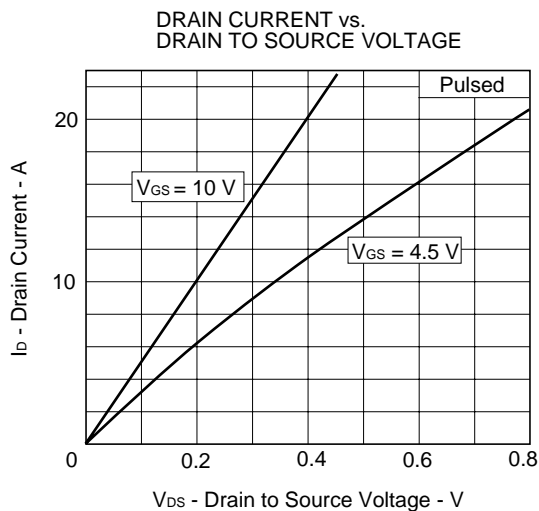
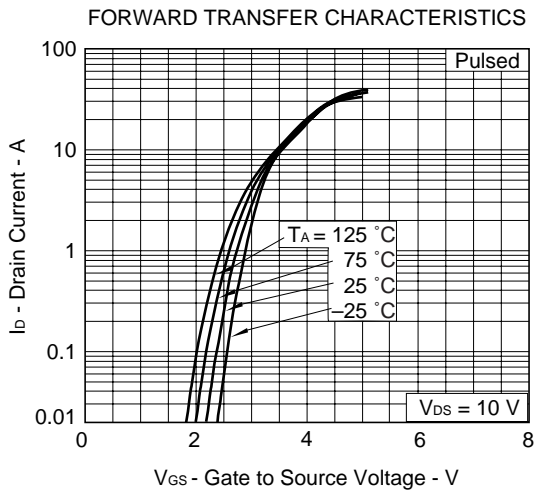


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)

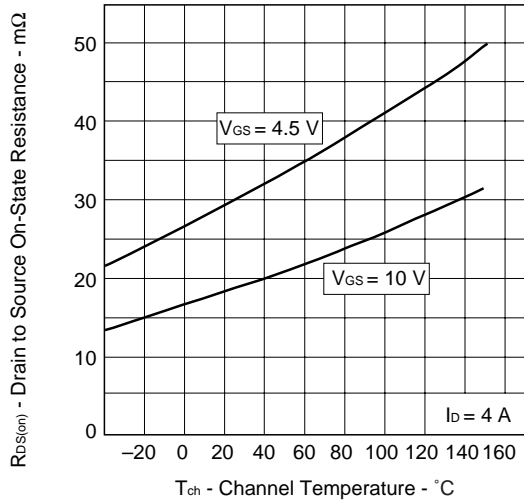


**Remark**  
Mounted on ceramic substrate of 2000 mm<sup>2</sup> × 1.7 mm

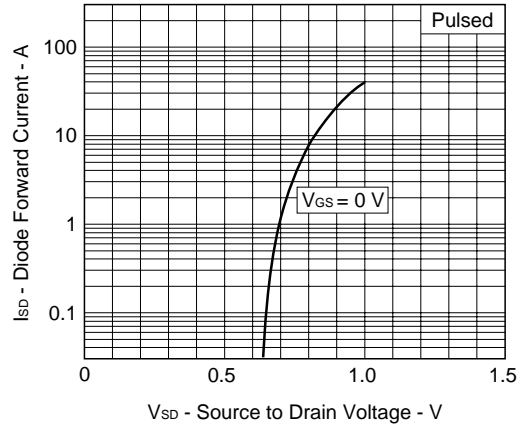




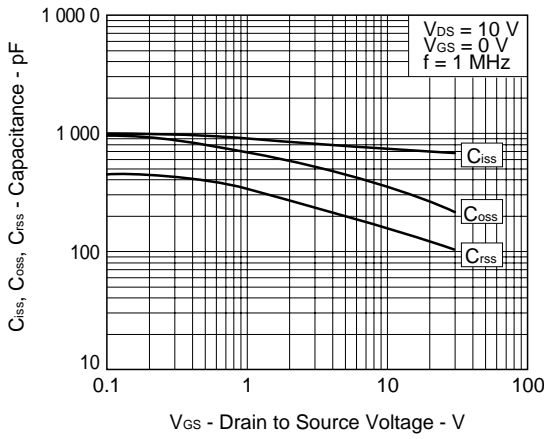
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



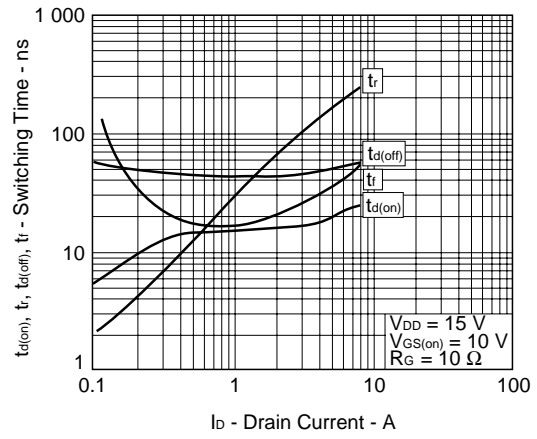
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



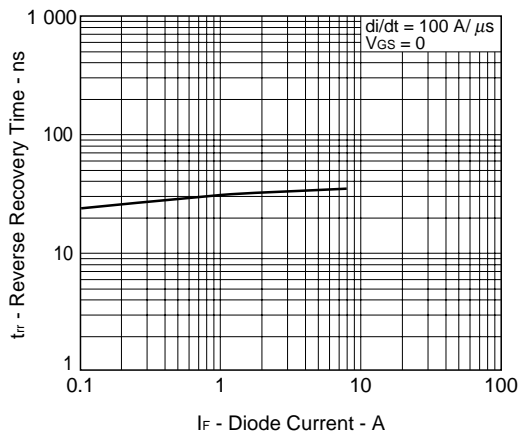
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



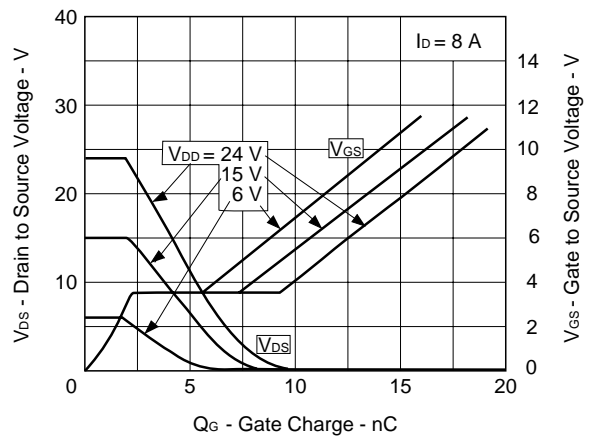
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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