

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of note book computers.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 27 \text{ m}\Omega$ Typ. ($V_{GS} = 10 \text{ V}$, $I_D = 3.5 \text{ A}$)
 $R_{DS(on)2} = 50 \text{ m}\Omega$ Typ. ($V_{GS} = 4 \text{ V}$, $I_D = 3.5 \text{ A}$)
- Low C_{iss} $C_{iss} = 850 \text{ pF}$ Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1700G	Power SOP8

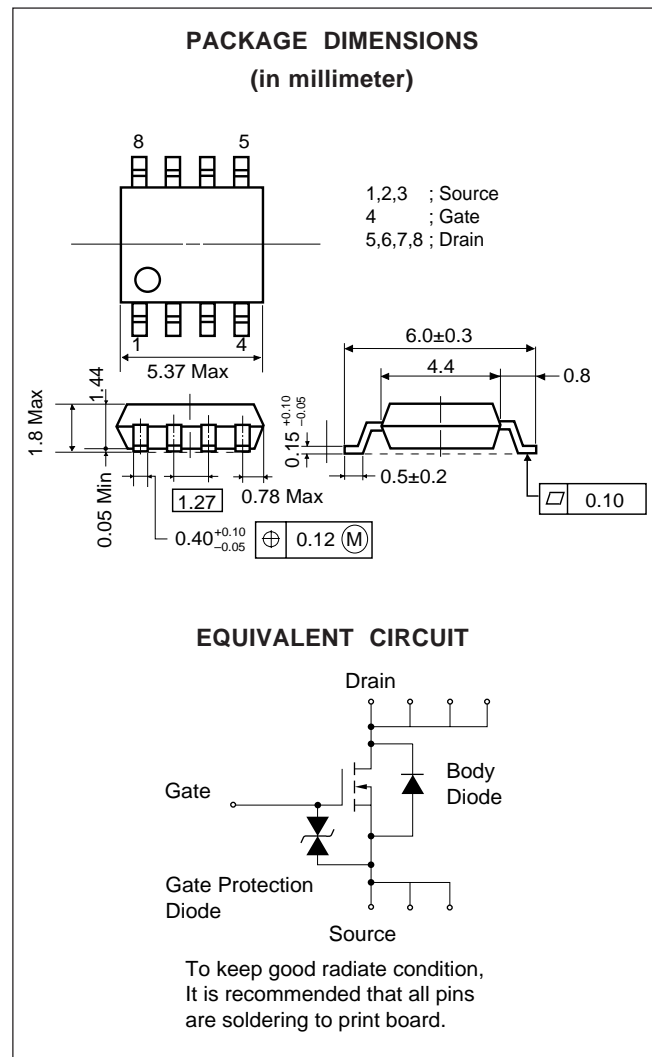
ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GDS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 7.0	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 28	A
Total Power Dissipation	P_T	2.0	W
$(T_A = 25 \text{ }^\circ\text{C})^{**}$			
Channel Temperature	T_{CH}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

** Mounted on ceramic substate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

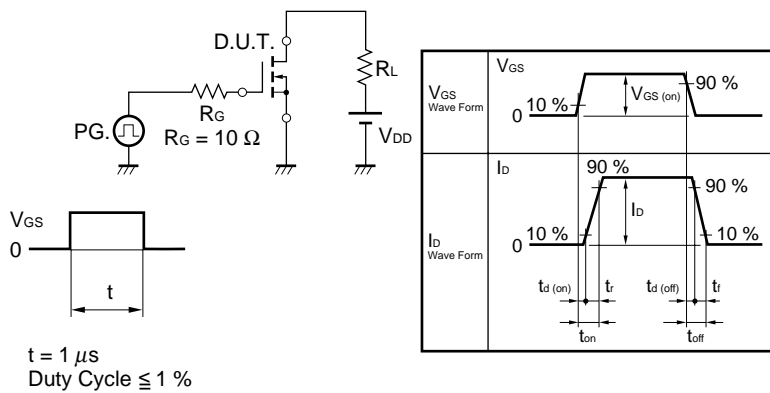
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



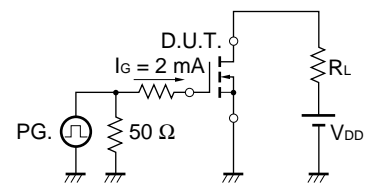
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3.5 A		20	27	mΩ
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 3.5 A		33	50	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	5.0			S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		850		pF
Output Capacitance	C _{oss}	V _{GS} = 0		550		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		270		pF
Turn-On Delay Time	t _{d(on)}	I _D = 3.5 A		20		ns
Rise Time	t _r	V _{GS(on)} = 10 V		105		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = 15 V		90		ns
Fall Time	t _f	R _G = 10 Ω		60		ns
Total Gate Charge	Q _G	I _D = 7.0 A		33		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.4		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		13		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 7.0 A, V _{GS} = 0		0.84		V
Reverse Recovery Time	t _{rr}	I _F = 7.0 A, V _{GS} = 0		60		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		90		nC

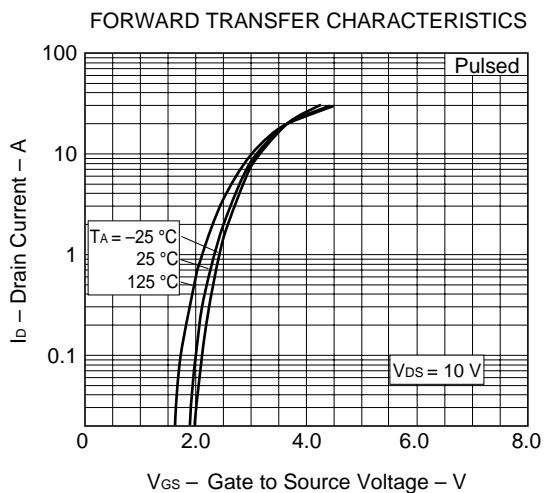
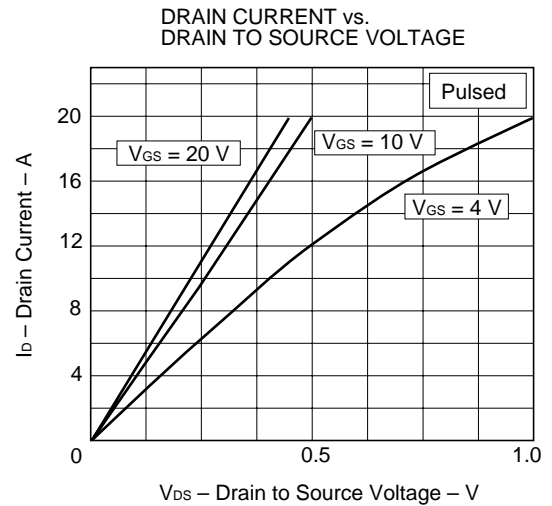
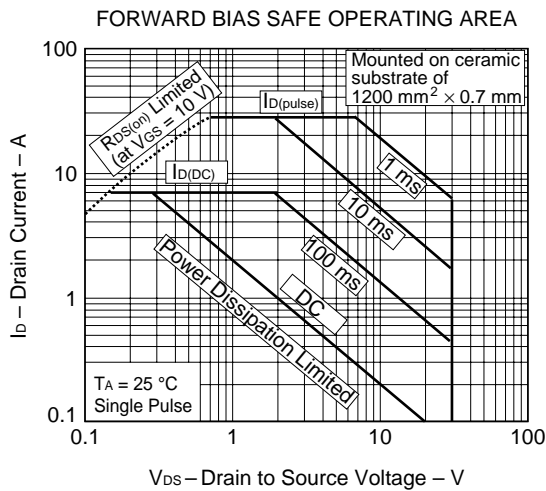
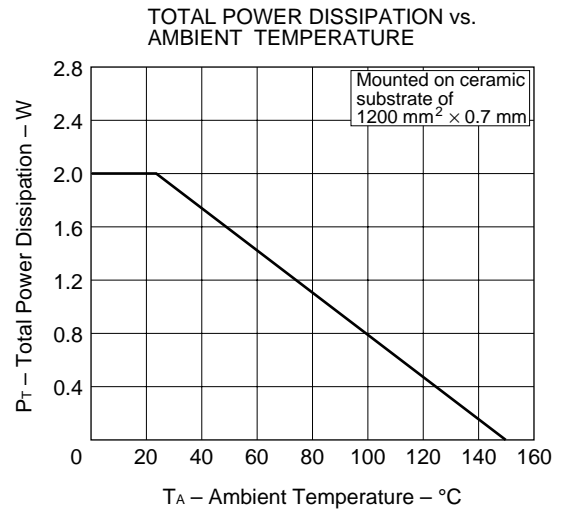
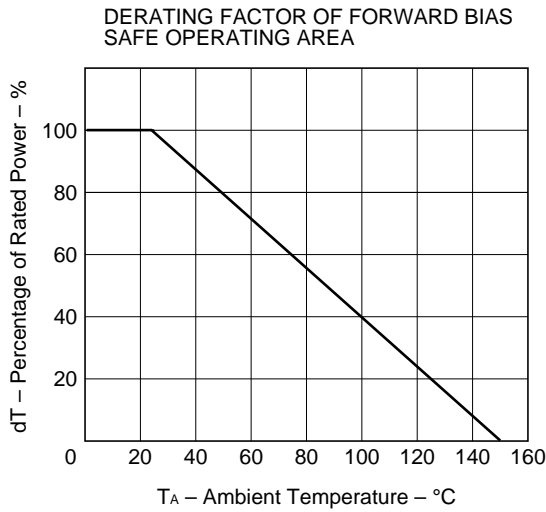
Test Circuit 1 Switching Time



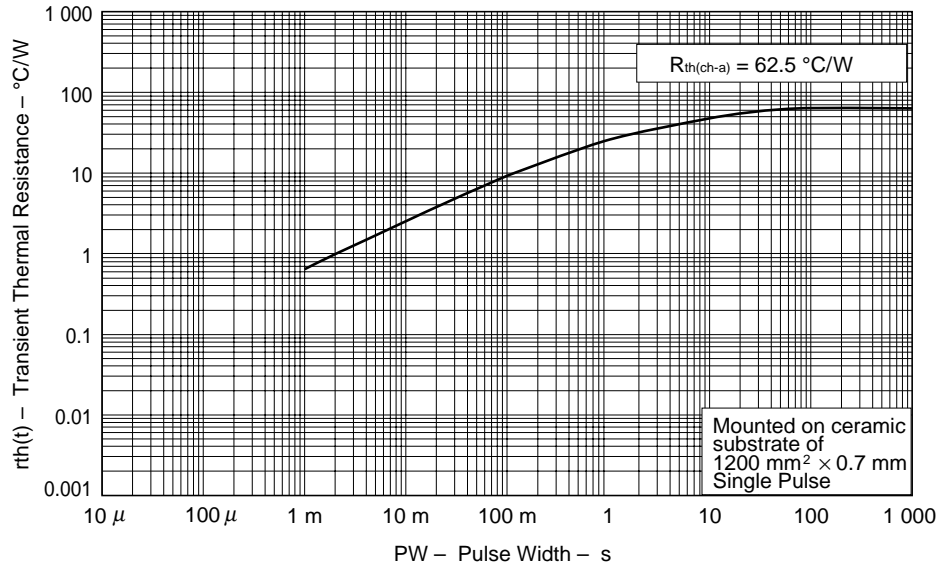
Test Circuit 2 Gate Charge



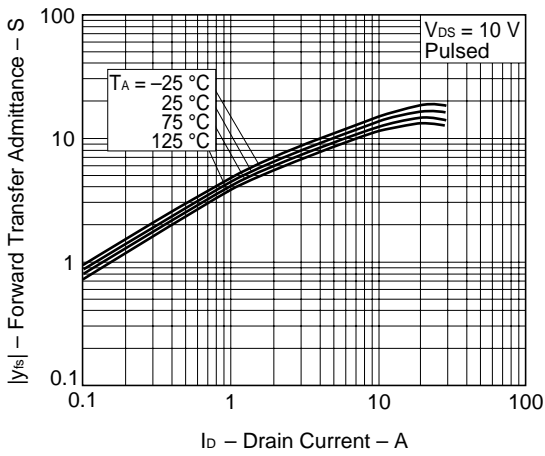
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$)



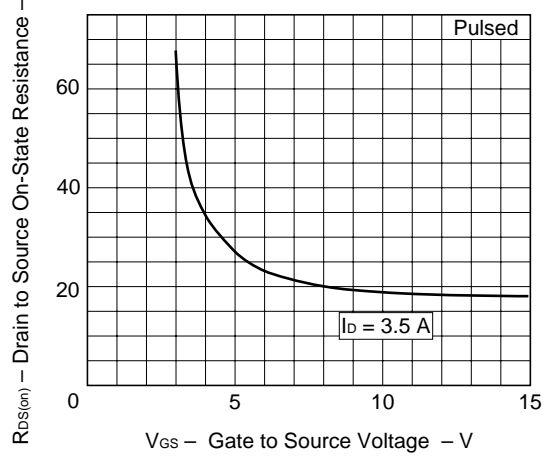
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



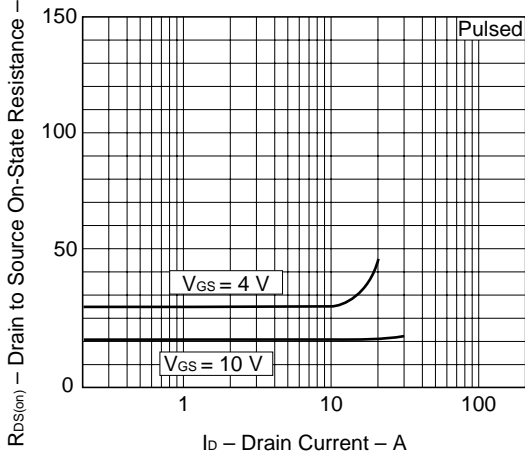
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



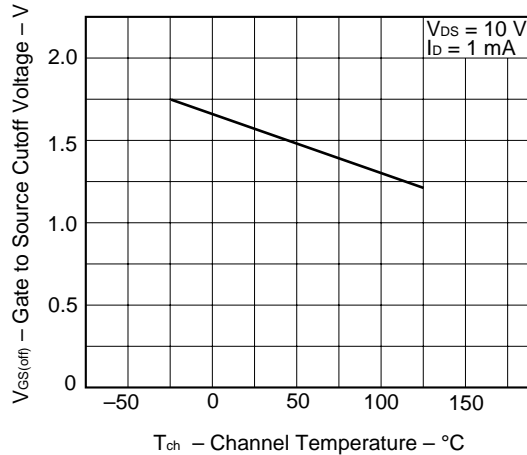
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

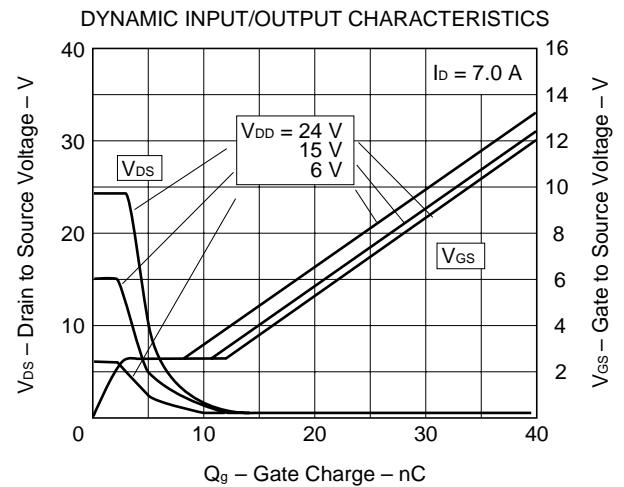
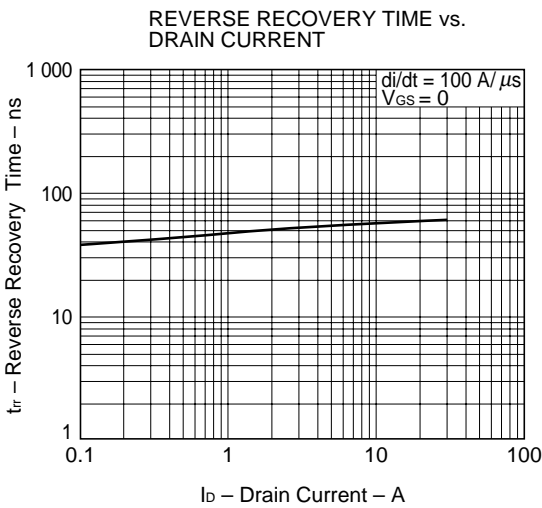
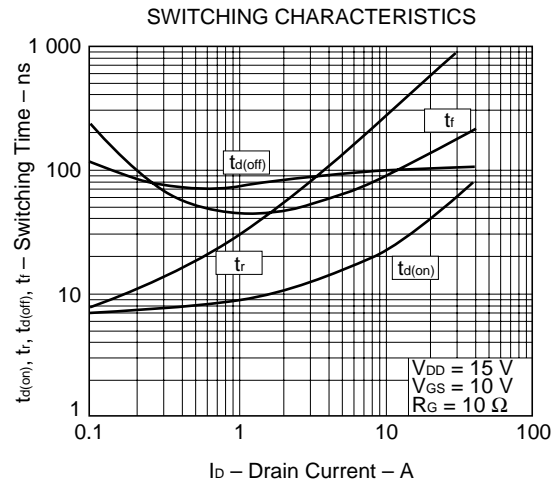
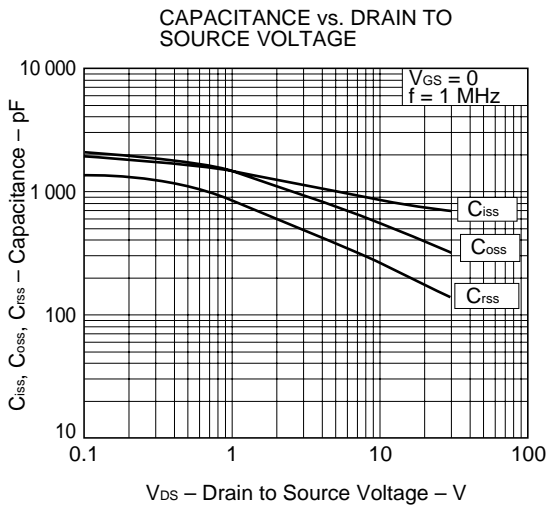
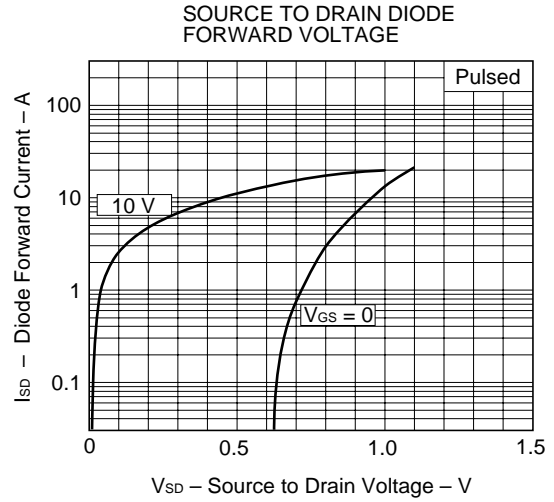
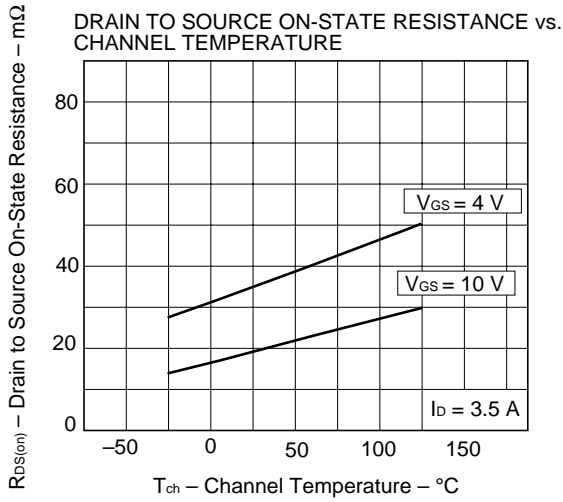


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.