# UM8388

## Single-Chip Floppy Disk Controller

PRELIMINARY

### Features

- IBM PC XT/AT drive system compatible
- Supports 2 drives (MS-DOS support)
- 1.44M/1.2M/360K/720K format selectable
- IBM PC drive system address decoder
- Only 4 components needed for the drive
- Internal write precompensation circuit; precompensation values: 250-125 ns
- Internal data separator circuit
- Supports 8", 5¼", and 3½" drives

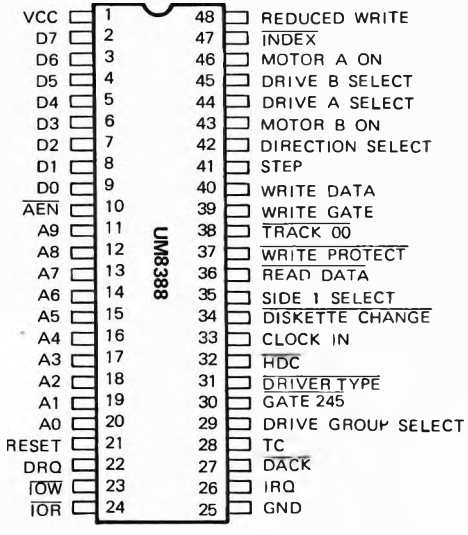
### General Description

The UM8388 is a VLSI Floppy Disk Controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor with up to 2 floppy disk drives. It is capable of supporting 360K Bytes, 1.2M Bytes (in 5¼" diskette drives), 720K Bytes, and 1.44M Bytes, (in 3½" diskette drives) FDDs using MFM coded, and double sided recording. UM8388 includes an internal data separator, write precompensation, circuit address decoder, timing control and other control logics. It simplifies design of a diskette drive system and only 4 components are needed in the IBM PC/AT drive system.

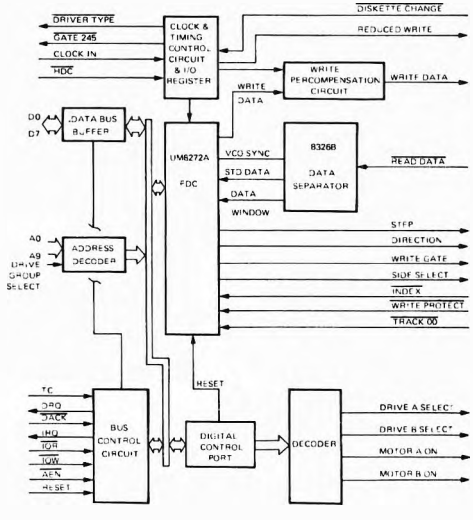
Handshaking signals are provided in UM8388 which makes DMA operation easy to incorporate with the aid of an external DMA control chip. The FDC will operate in either the DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor needs only to load the command into the FDC and all data transfers occur under control of the UM8388 and DMA controller.

Many diskette drive parameters are programmable and a write-protection feature is supported. One interrupt level is used to indicate when an operation is completed, or a status condition requires the microprocessor's attention.

### Pin Configurations

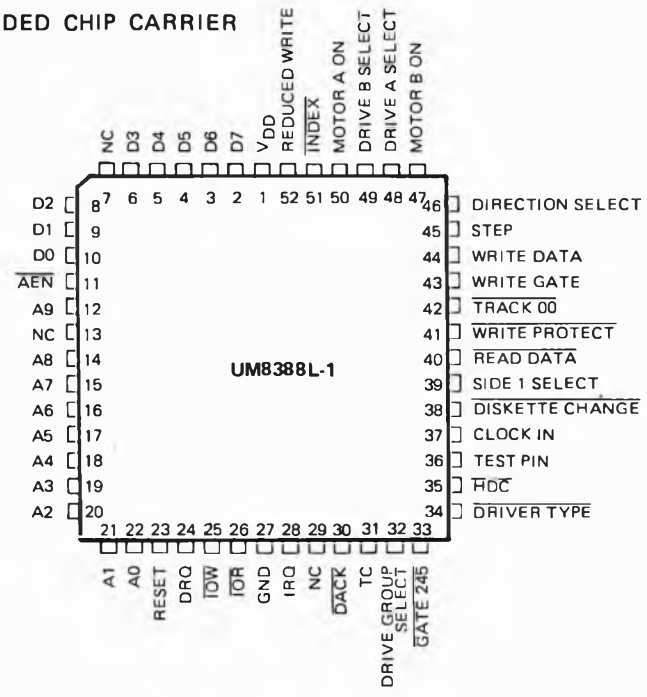



### Block Diagram

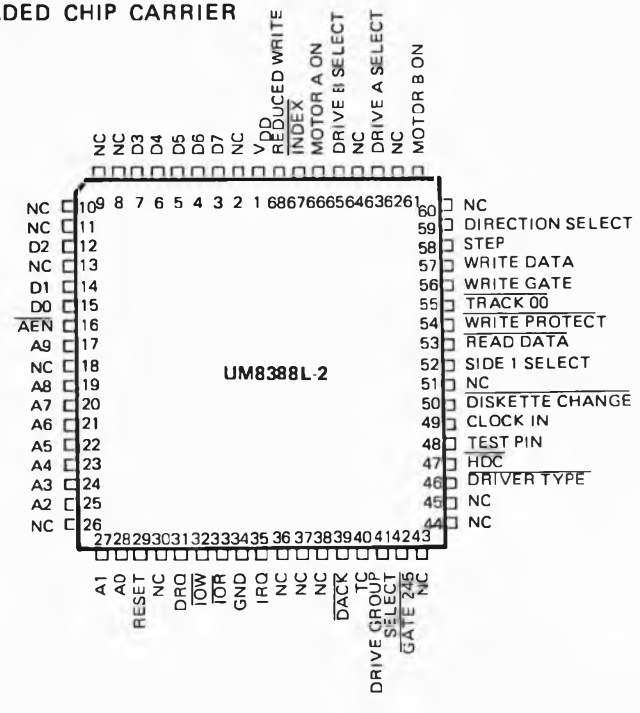


**Pin Configurations**

52 PIN PLASTIC LEADED CHIP CARRIER




68 PIN PLASTIC LEADED CHIP CARRIER



### Absolute Maximum Ratings*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +150°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage $V_{CC}$ . . . . . −0.5 to +7 Volts
Power Dissipation . . . . . 1 Watt

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics ($T_A$ = 0°C to +70°C, $V_{CC}$ = +5V ± 5%)

| Symbol | Parameters | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $V_{IL}$ | Input low voltage | | 0.8 | V | |
| $V_{IH}$ | Input high voltage | 2.0 | | V | |
| $V_{OL}$ | Output low voltage | | 0.4 | V | $I_{OL}$ = 8.0 mA |
| $V_{OH}$ | Output high voltage | 2.4 | $V_{CC}$ | V | $I_{OH}$ = 4.0 mA |
| $I_{CC}$ | $V_{CC}$ supply current | | 200 | mA | |
| $I_{IL}$ | Input leakage current | | 10 | μA | $0 \leqslant V_O \leqslant V_{CC}$ |
| $I_{LOH}$ | High level output leakage current | | 10 | μA | $V_O = V_{CC}$ |
| $I_{OFL}$ | Output float leakage current | | 10 | μA | $0.4V \leqslant V_O \leqslant V_{CC}$ |

### A.C. Characteristics ($T_A$ = 0°C to + 70°C, $V_{CC}$ = +5.0V ± 10%)

PROCESSOR WRITE CYCLE

| Symbol | Parameter | Min. | Max. |
|---|---|---|---|
| $t_{AW}$ | address setup to $\overline{IOW}$ ↓ | 10 ns | |
| $t_{WA}$ | address hold from $\overline{IOW}$ ↑ | 5 ns | |
| $t_{WW}$ | $\overline{IOW}$ pulse width | 250 ns | |
| $t_{DW}$ | data setup to $\overline{IOW}$ ↑ | 150 ns | |
| $t_{WD}$ | data hold from $\overline{IOW}$ ↑ | 10 ns | |
| $t_{WI}$ | IRQ delay from $\overline{IOW}$ ↑ | | 500 ns* |

PROCESSOR READ CYCLE

| Symbol | Parameter | Min. | Max. |
|---|---|---|---|
| $t_{AR}$ | address setup to $\overline{IOR}$ ↓ | 10 ns | |
| $t_{RA}$ | address hold from $\overline{IOR}$ ↑ | 5 ns | |
| $t_{RR}$ | $\overline{IOR}$ pulse width | 250 ns | |
| $t_{RD}$ | data delay from $\overline{IOR}$ ↓ | | 230 ns |
| $t_{DF}$ | output floating delay from $\overline{IOR}$ ↑ | 10 ns | 30 ns |
| $t_{RI}$ | IRQ delay fro $\overline{IOR}$ ↑ | | 500 ns* |

Note: *: The values are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

## DMA OPERATION*

| Symbol | Parameter | Min. | Max. |
|---|---|---|---|
| $t_{ROCY}$ | DRQ cycle period | 13 μs | |
| $t_{AKRO}$ | $\overline{DACK}$ ↓ to DRQ ↓ | | 200 ns |
| $t_{ROR}$ | DRQ ↑ to $\overline{IOR}$ ↓ | 800 ns | |
| $t_{ROW}$ | DRQ ↑ to $\overline{IOW}$ ↓ | 250 ns | |
| $t_{RORW}$ | DRQ ↑ to $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ | | 12 μs |

### Terminal Count, Reset, Index

| Symbol | Parameter | Min. | Typ. | Max. |
|---|---|---|---|---|
| $t_{IDX}$ | index pulse width | | $10t_{CY}$** | |
| $t_{TC}$ | terminal count width | $1t_{CY}$ | | |
| $t_{RST}$ | reset width | $14t_{CY}$ | | |

Notes:
* : The values listed for DMA operation are for 8 MHz clock rate, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.
**: $t_{CY}$ is the clock rate of Drive System.

## FDD INTERFACE

| Symbol | Parameter | Min. | Typ. | Max. |
|---|---|---|---|---|
| $t_{WDD}$ | write data width | | 125/208/250 ns* | |
| $t_{WCY}$ | write data cycle time | | 1/1.67/2 μs* | |
| $t_{RDD}$ | read data active time (low) | 40 ns | 125/208/250 ns* | |
| $t_{RCY}$ | read data cycle time | | 1/1.67/2 μs* | |

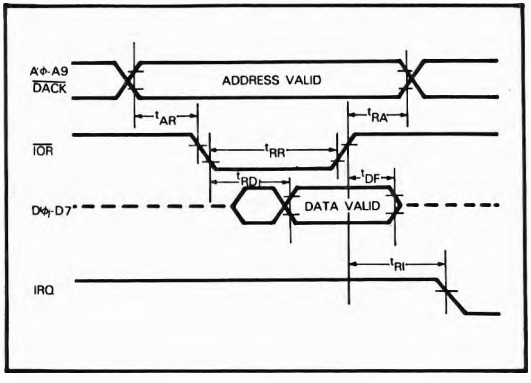
## SEEK OPERATION***

| Symbol | Parameter | Min. | Typ. | Max. |
|---|---|---|---|---|
| $t_{STP}$ | step active time | | 5 μs | |
| $t_{SC}$ | step cycle time | 33 μs | | |
| $t_{DST}$ | DIR setup to step ↑ | 1 μs | | |
| $t_{STD}$ | DIR hold from step ↓ | 24 μs | | |

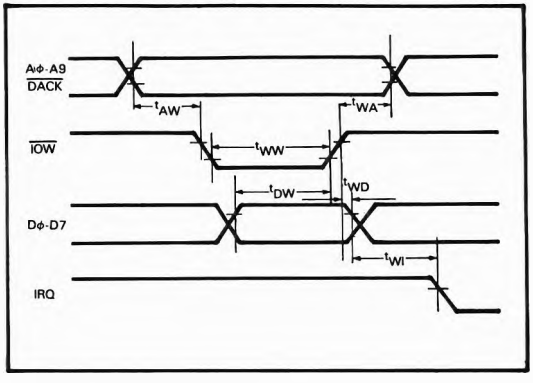
Notes:
* : The specified values are for 8/4.8/4 MHz respectively.
***: The values listed for seek operation are for 8 MHz clock period, multiply timings by 2/1.67 when using 4/4.8 MHz clock rates.

## Timing Waveforms

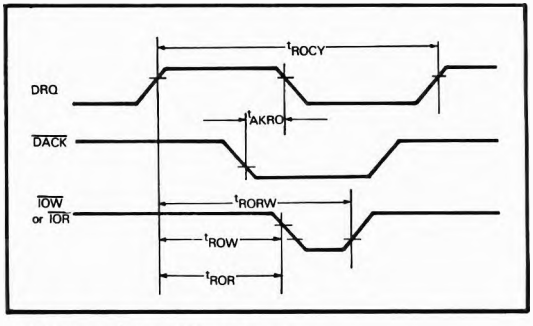
### Processor Read Operation



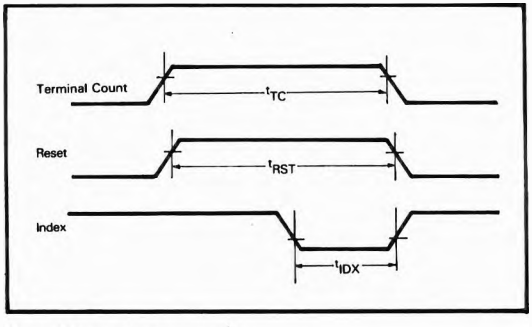

### Processor Write Operation



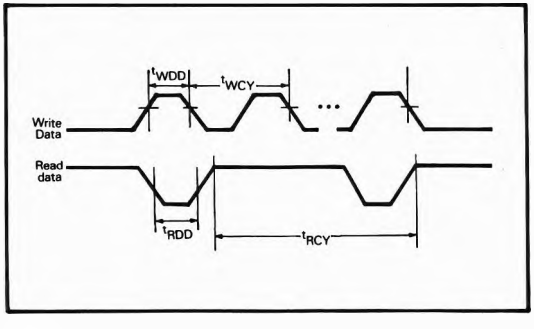

### DMA Operation



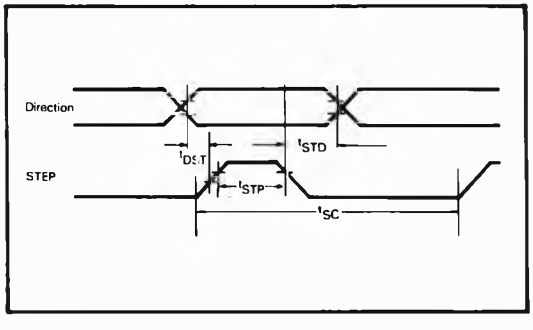

### Terminal Count, Reset, Index




### FDD Write/Read Operation




### Seek Operation



**Pin Description**

| Pin | Symbol | I/O | Description |
|---|---|---|---|
| 1 | $V_{CC}$ | I | Power supply, connected to +5V power supply. |
| 2~9 | D7 ~ D0 | I/O | Bi-directional – 8-bit data bus |
| 10 | $\overline{AEN}$ | I | Input from DMA – Address Enable. When this line is active (low) the DMA controller has control of the address bus. |
| 11~20 | A9 ~ A0 | I | Input from processor – 10-bit Address Bus. |
| 21 | RESET | I | Input from processor – places FDC in idle state. Resets output lines to FDD to "0" (low). Does not affect SRT, HUT or HLT in Specify command. |
| 22 | DRQ | O | Output to DMA – DMA Request is being made by FDC when DRQ = "1". |
| 23 | $\overline{IOW}$ | I | Input from processor – Control signal for transfer of data to FDC via Data Bus, when "0". |
| 24 | $\overline{IOR}$ | I | Input from processor – Control signal for transfer of data from FDC to Data Bus, when "0". |
| 25 | GND | I | Ground. Normally connected to +0V ground |
| 26 | IRQ | O | Output to processor – Interrupt request generated by FDC. |
| 27 | $\overline{DACK}$ | I | Input from DMA – DMA cycle is active when "0" (low) and controller is performing DMA transfer. |
| 28 | TC | I | Input from DMA – Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode. |
| 29 | DRIVE GROUP SELECT | I | The primary address will be applied when this signal is active high (3FX)<br>The secondary address will be applied when this signal is low (37X) |
| 30 | $\overline{GATE\ 245}$ | O | Output low to enable the extra 74LS245 Buffer on data bus. |
| 31 | $\overline{DRIVER\ TYPE}$ | O | Output low to enable the extra disk drive type port. It's address is 3F1. |
| 32 | $\overline{HDC}$ | I | Set this input to low, when your system has a hard disk control card. Otherwise, set this input to high. |
| 33 | CLOCK IN | I | 24 MHz clock input. |
| 34 | $\overline{DISKETTE\ CHANGE}$ | I | Input from FDD – This input is high when a diskette is present again and a step pulse is issued from FDC. |

**Pin Description (Continued)**

| Pin | Symbol | I/O | Description |
|---|---|---|---|
| 35 | SIDE 1 SELECT | O | Output to FDD – This output is active (high) for the upper head. Otherwise, the lower head is selected. |
| 36 | $\overline{\text{READ DATA}}$ | I | Input from FDD – Each bit detected provides a 250 ns (4 MHz), 208 ns (4.8 MHz), 125 ns (8 MHz) active (low) pulse on this line. |
| 37 | $\overline{\text{WRITE PROTECT}}$ | I | Input from FDD – This input is active low when a diskette with a write protect notch is inserted. |
| 38 | $\overline{\text{TRACK 00}}$ | I | Input from FDD – This signal is low when the upper head is on Track 00 (the outermost track). |
| 39 | WRITE GATE | O | Output to FDD – An active high level of this output enables the write current circuits, and the Write Data output controls the writing of information. |
| 40 | WRITE DATA | O | Output to FDD – A 125 ns (8 MHz), 208 ns (4.8 MHz), 250 ns (4 MHz) pulse on this output causes a bit to be written on the disk if Write Gate is active. |
| 41 | STEP | O | Output to FDD – An active high pulse causes the read/write heads to move in the direction determined by the "direction select" signal. Motion is started each time the signal changes from an active to inactive level (at the trailing edge of the pulse). |
| 42 | DIRECTION SELECT | O | Output to FDD – This signal determines the direction the read/write head moves when the step signal is pulsed. A low level indicates away from the center of the diskette (out); a high level indicates toward the center of the diskette (in). |
| 43 | MOTOR B ON | O | Output to FDD – The spindle motor B runs when this input is active. The drive requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the step pulse. |
| 44 | DRIVE A SELECT | O | Output to FDD – When "Drive A Select" is at the active level, drive A is enabled. When it is at the inactive level, all drive A outputs are disabled. |
| 45 | DRIVE B SELECT | O | Output to FDD – When "Drive B Select" is at the active level, drive B is enabled. When it is at the inactive level, all drive B outputs are disabled. |
| 46 | MOTOR A ON | O | Output to FDD – The spindle motor A runs when this input is active. Drive A requires a 1 sec (high density)/750 ms (double density) delay after "motor on" becomes active before and after the trailing edge of the read or write operation. |
| 47 | $\overline{\text{INDEX}}$ | I | Input from FDD – A low pulse appears on this line to indicate the beginning of a disk track when the drive senses the index hole in the diskette. |
| 48 | REDUCED WRITE | O | Output to FDD – The inactive state low of this signal indicates that high-density media is present, requiring normal write currents, and the active state high indicates low-density media is present, requiring a reduced write current. |

## Register Description

### 1. Digital Output Register (IO write 3F2, 372)

The digital output register (DOR) is an output-only register controlling drive motors, drive selection, and feature enable. All bits are cleared by the I/O interface reset line. The bit definitions are as follows.

| | |
|---|---|
| Bit 7 | Reserved |
| Bit 6 | Reserved |
| Bit 5 | Drive B Motor Enable |
| Bit 4 | Drive A Motor Enable |
| Bit 3 | Enable Diskette Interrupts and DMA |
| Bit 2 | Diskette Function Reset – Diskette function reset when this bit is low ('0'). |
| Bit 1 | Reserved |
| Bit 0 | Drive Select – A"0"on this bit indicates that drive A is selected. |

### 2. Digital Input Register (IO read 3F7, 377)

The digital input register is an 8-bit, read-only register used for diagnostic purposes. The following are bit definitions for this register.

| | |
|---|---|
| Bit 7 | Diskette Change |
| Bits 0 ~ 6 | Apply to the currently selected fixed disk drive |

### 3. Transfer Rate Register (Diskette Control Register) (IO write 3F7, 377)

The transfer rate register is a 2-bit, output-only register which controls a programmable divider and provides 8M/4.8M/4M Hz clocks for three different data transfer rates. The definition is given as follows:

| Bit 0 | Bit 1 | Transfer Rates | Clock Rates | Reduce write |
|---|---|---|---|---|
| 0 | 0 | 500K bps | 8 MHz | 0 |
| 1 | 0 | 300K bps | 4.8 MHz | 1 |
| 0 | 1 | 250K bps | 4 MHz | 1 |
| 1 | 1 | reserved | reserved | 1 |

### 4. Main Status Register (IO read 3F4, 374)

Those bits in the main status register are defined as follows:

| | |
|---|---|
| Bit 7 | Request for master (RQM) – The data register is ready to send or receive data to or from the processor. |
| Bit 6 | Data Input/Output (DIO) – The direction of data transfer between the diskette control and the processor. |
| Bit 5 | Non-DMA Mode (NDM) – The diskette controller is in the non-DMA mode. |
| Bit 4 | Diskette Control Busy (CB) – A Read or Write command is being executed. |
| Bit 3 | Reserved |
| Bit 2 | Reserved |
| Bit 1 | Diskette Drive B Busy (DBB) – Diskette drive B is in the seek mode. |
| Bit 0 | Diskette Drive A Busy (DAB) – Diskette drive A is in the seek mode. |

**5. Diskette Data Register (IO read IO write 3F5 375)**

This 8-bit data register actually consists of several registers in a stack and only one register is presented to the data bus at a time when storing data commands, and parameters, or providing diskette-drive status information.

**6. Fixed Disk Status Register (IO read 1F7, 177)**

The contents of this 8-bit fixed disk status register are checked when system BIOS executes self-test. This register is enabled when PC system has no Hard Disk Control card and bit 7 is of this register is fixed to 1 (high). This register shall be disabled when PC system has a Hard Disk Control card.

Table A-1 The I/O addresses of these five registers mentioned above are given in the following:

| Primary | Secondary | Read | Write |
|---|---|---|---|
| 3F2 | 372 | | Digital output register |
| 3F4 | 374 | Main status register | |
| 3F5 | 375 | Diskette data register | Diskette data register |
| 3F7 | 377 | Digital input register | Transfer rate register |
| 1F7 | 177 | Fixed Disk Status register* | |

*: Fixed disk function

## Application Notes

**A: General Description**

The UM8388 can be easily implemented into a FDC card or a main board and only 4 components (UM8388, 7406*2 74LS245*1) are needed in the IBM PC/AT drive system. The address decoder of UM8388 is switchable by setting pin 29 (Drive group select) of UM8388. If pin 29 is set to 1 (high), then the I/O address of the UM8388 is selected in the primary drive group address (3F1 ~ 3F7, 1F7). The contents of the UM8388 Hard Disk Status Register will be checked when system BIOS executes selftest. This register's bit 7 should be high by setting pin 32 to high when the PC system has no Hard Disk Control card, otherwise the register's bit 7 should be low by setting pin 32 to low.

**B: PC/AT Application**

The UM8388 registers are the same as the PC/AT floppy disk controller's. Therefore, the UM8388 can be directly implemented into the FDC card of the PC/AT to support 1.2M, 720K, 360K 1.44M Bytes FDD and only 4 components (UM8388*1, 7406*2 74LS245) are needed. The application circuit is shown as Figure A-1.

**C: PC/XT Application**

If the UM8388 is used to support 1.44M, 1.2M, 720K, 360K Byte FDD in the PC/XT an additional FDC program is needed to control the 1.44M, 1.2M Bytes FDD since the PC/XT BIOS doesn't support the 1.2M, 1.44M Byte FDD. During the FDD operation, this additional BIOS reads the contents of the UM8388 Drive Type Register set by pin 31, thus selects the drive to be 1.44M, 1.2M, 360K or 720K.

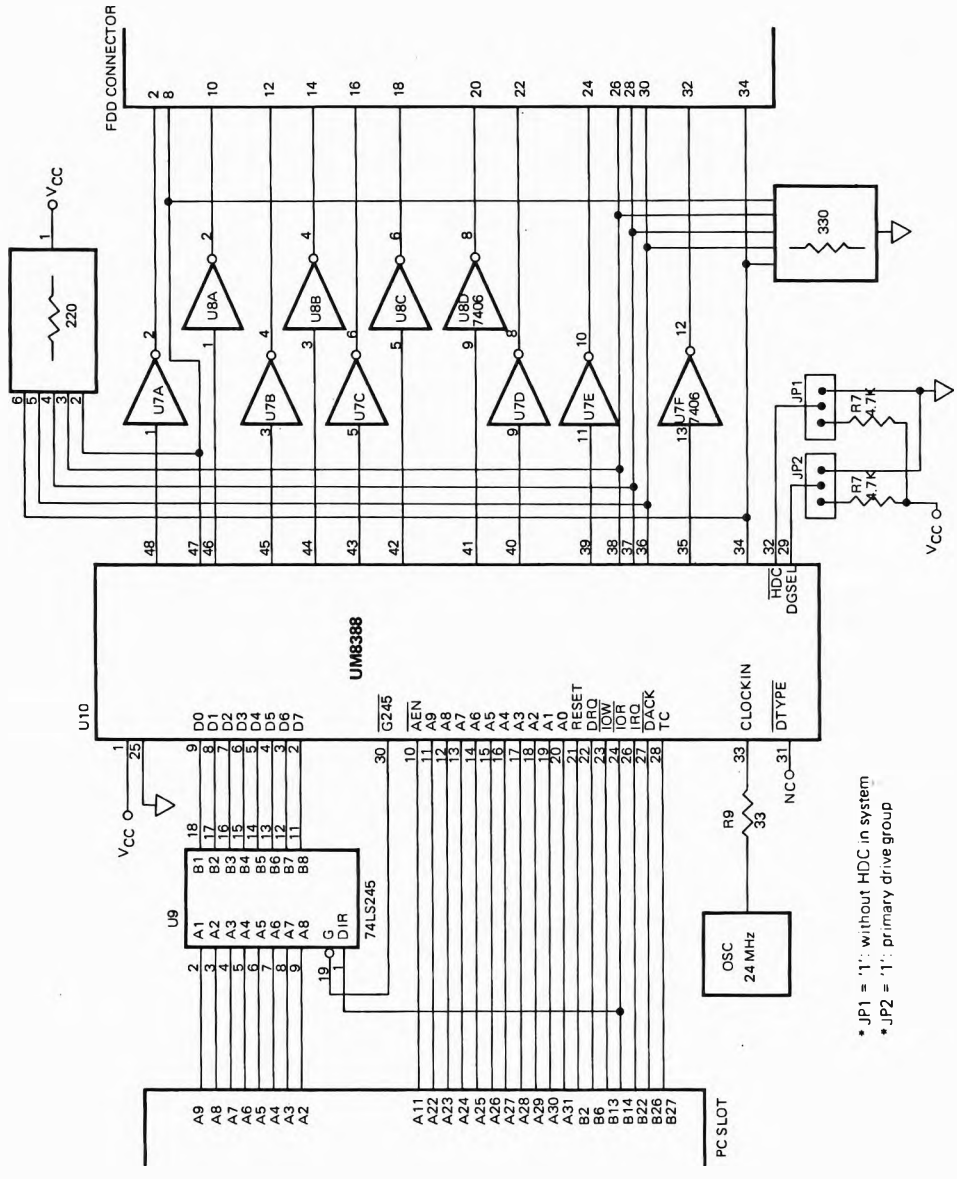



Figure A-1 PC/AT (1.44M, 1.2M, 720K, 360K FDD) Application Circuit

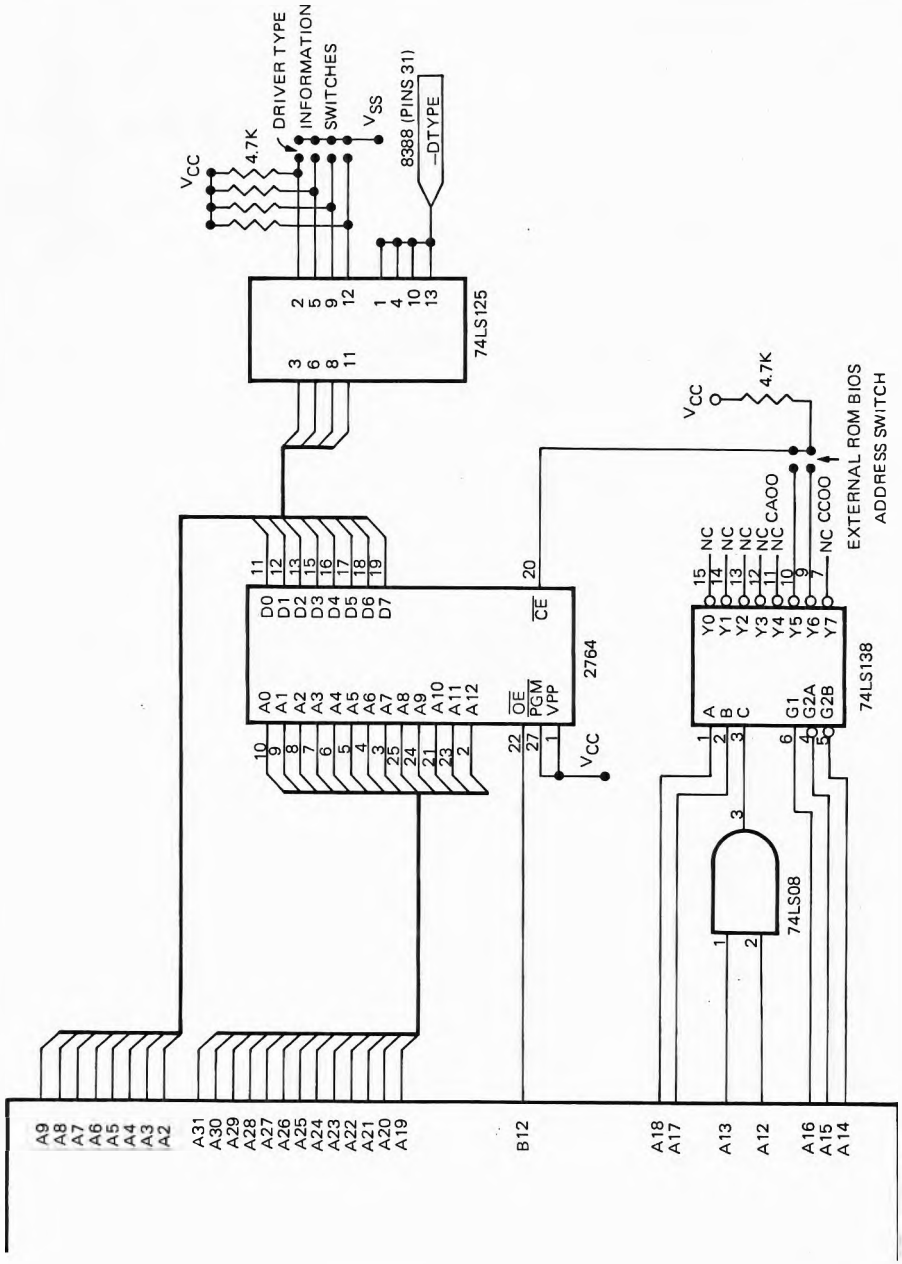



Figure A-2 PC/XT BIOS ROM Circuit

## Ordering Information

| Part Number | Operating Current (Max.) | Package Type |
|---|---|---|
| UM8388 | 200 mA | 48L DIP |
| UM8388L-*1 | 200 mA | 52L PLCC |
| UM8388L-*2 | 200 mA | 68L PLCC |