UMC

UM8326/B

Floppy Disk Data Separator (FDDS)

Features

- Performs complete data separation for floppy disk drives
- Separates FM or MFM-encoded data from any magnetic media
- Eliminates several SSI and MSI devices normally used for data separation
- No critical adjustments required
- Compatible with Standard Microsystems' FDC 1791, FDC 1793 and other floppy disk controllers
- Small 8-pin dual-in-line package
- +5 Volt only power supply
- TTL-compatible inputs and outputs

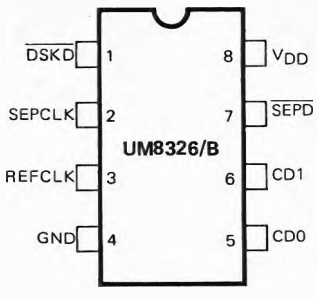
General Description

The Floppy Disk Data Separator provides a low-cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate clock and data inputs for a floppy disk controller.

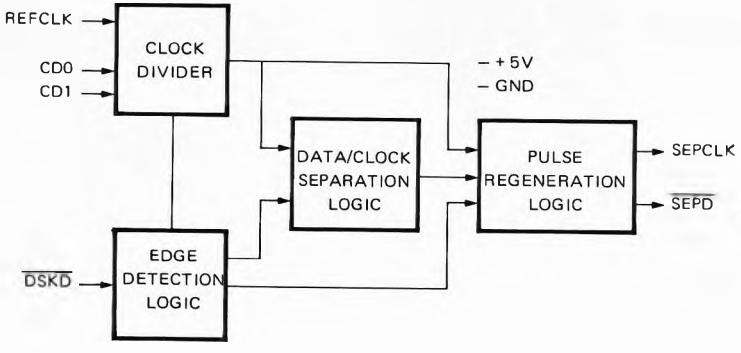
The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and a re-clocking circuitry. Supplied in an 8-pin dual-in-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL-compatible on all inputs and outputs.

The UM8326/B is available in two versions: The UM8326, which is intended for 5¼" disks, and the UM8326B for both 5¼" and 8" disks.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Positive Voltage on any Pin, with respect to ground
. . . . . + 8.0V
Negative Voltage on any Pin, with respect to ground
. . . . . − 0.3V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{DD} = +5V ± 5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level V_{OH}	2.4			V	I_{OH} = −100μA
INPUT CURRENT					
Leakage I_{IL}			10	μA	$0 \leqslant V_{IN} \leqslant V_{DD}$
INPUT CAPACITANCE					
All Inputs			10	pF	
POWER SUPPLY CURRENT					
I_{DD}			60	mA	

A.C. CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CY}	REFCLK Frequency	0.2		4.3	MHz	UM8326
f_{CY}	REFCLK Frequency	0.2		8.3	MHz	UM8326B
t_{CKH}	REFCLK High	50		2500	ns	
t_{CKL}	REFCLK Low	50		2500	ns	
t_{SDON}	REFCLK to SEPD "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to SEPD "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	35			ns	
t_{DLL}	DSKD Active Low	0.1		100	μs	
t_{DLH}	DSKD Active High	0.2		100	μs	

Pin Description

Pin No.	Symbol	Designation	Description
1	$\overline{DSKD}$	$\overline{Disk\ Data}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	SEPCLK	Separated Clock	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	REFCLK	Reference Clock	Reference clock input
4	GND	Ground	Ground
5, 6	CD0 CD1	Clock Divisor	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{SEPD}$	$\overline{Separated\ Data}$	$\overline{SEPD}$ is the data output of the FDDS
8	V_{DD}	Power Supply	+5 volt power supply

Operational Description

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long-term timing correctors assure accurate clock separation.

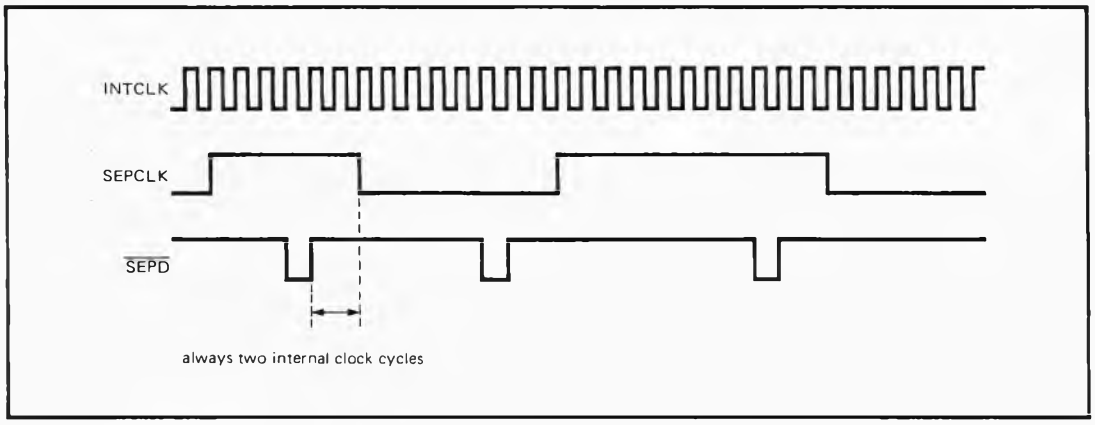
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

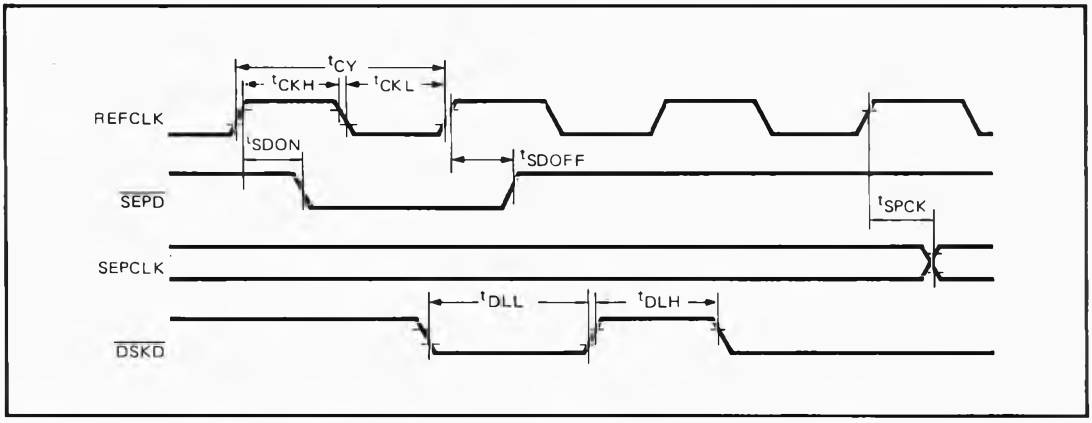
Table 1. Clock Divider Selection Table

Drive (8" or 5¼")	Density (DD or SD)	REFCLK MHz	CD1	CD0	Remarks
8	DD	8	0	0	All selectable
8	SD	8	0	1	
8	SD	4	0	0	
5¼	DD	8	0	1	
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	
5¼	SD	2	0	0	

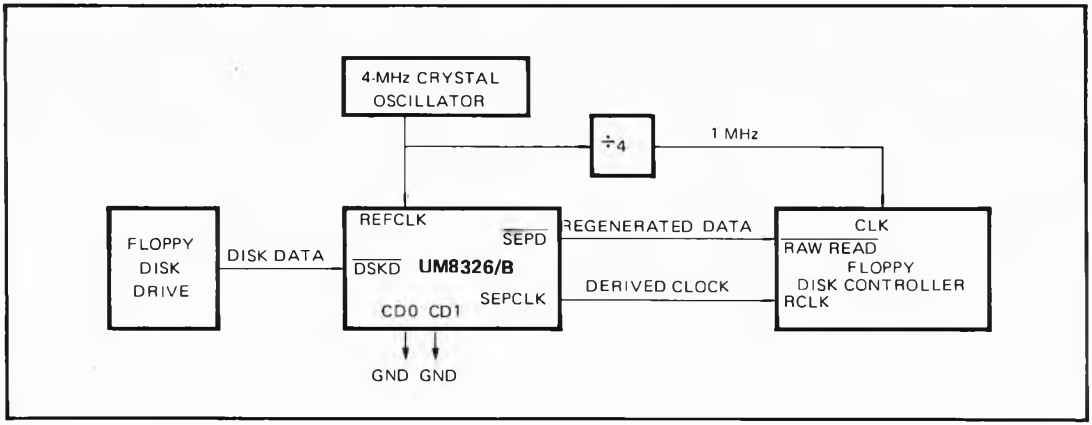
Timing Diagram (1)



Timing Diagram (2)



Typical System Configuration (5¼" Drive, Double Density)



Ordering Information

Part Number	Frequency Option	Drives	Package Type
UM8236B	4 MHz	5¼"	8L DIP
UM8326B	8 MHz	5¼", 8"	8L DIP