UM82C84AE

CMOS Clock Generator and Driver

Features

- Generates the system clock for CMOS or NMOS microprocessors
- Up to 25 MHz operation
- Uses a parallel mode crystal circuit or external frequency source
- Provides ready synchronization
- Generates system reset output from Schmitt Trigger input
- Capable of clock synchronization with other 8284A
- TTL compatible inputs/outputs
- Very low power consumption
- Single +5V power supply

General Description

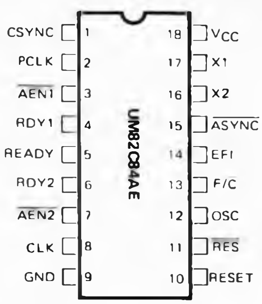
The UM82C84AE is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, X2 and $\overline{RES}$) are TTL compatible with a V_{IH} of 2.0 volts over the industrial temperature and voltage ranges.

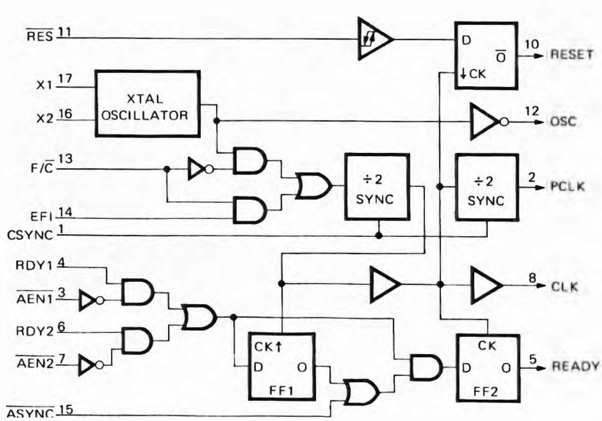
Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

Pin Configuration



Control Pin	Logic 1	Logic 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus not Ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enabled
$\overline{ASYNC}$	2 Stage Ready Synchronization	1 Stage Ready Synchronization

Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . +8.0 Volts
Operating Voltage Range . . . . +4V to +7V
Applied Voltage on Any Pin
V_{IN} . . . . GND −0.3V to V_{CC}0.3V
Ambient Temperature Under Bias T_A . . . . . 0°C to +70°C
Storage Temperature Range
T_{STG} . . . . −65°C to +150°C
Maximum Power Dissipation . . . . 1 Watt

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

V_{CC} = 5.0V ± 10% T_A = 0°C to +70°C

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IH}	Logic One Input Voltage	2.0		V	
V_{IL}	Logic Zero Input Voltage		0.8	V	
V_{T+}	Reset Input High Voltage	0.7 V_{CC}		V	
V_{T+}-V_{T-}	Reset Input Hysteresis	0.2 V_{CC}			
V_{OH}	Logic One Output Voltage	V_{CC}-0.4		V	I_{OH} = -4.0mA for CLK output I_{OH} = -2.5mA for all others
V_{OL}	Logic Zero Output Voltage		0.4	V	I_{OL} = +4.0mA for CLK output I_{OL} = +2.5mA for for others
I_{CL}	Input Leakage Current	−1.0	1.0	μA	$0V < V_{IN} < V_{CC}$ except $\overline{ASYNC}$, X1-see note 1
I_{CC}	Power S Supply Current		40	mA	Crystal Frequency = 25MHz Outputs Open

Notes:
ASYNC pin includes an internal 17.5KΩ nominal pull-up resistor. For $\overline{ASYNC}$ input at GND, $\overline{ASYNC}$ input leakage current= 130μA nominal.
X1-crystal feedback input.

Capacitance

(T_A = 25°C. V_{CC}=GND=0V; V_{IN}=+5V or GND)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		5	pf	Freq. = 1 MHz

*This parameter is guaranteed and sampled, but not 100% tested

A.C. Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tEHEL	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
tELEH	External Frequency LOW Time	13		ns	10%–10% V_{IN}
tELEL	EFI Period	36		ns	
	XTAL Frequency	2.4	25	MHz	
tR1VCL	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = HIGH
tR1VCH	RDY1, RDY2 Inactive Setup to CLK	35		ns	ASYNC= LOW
tR1VCL	RDY1, RDY2 Inactive Setup to CLK	35		ns	
tCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
tAYVCL	ASYNC Setup to CLK	50		ns	
tCLAYX	ASYNC Hold to CLK	0		ns	
tA1VR1V	AEN1, AEN2 Setup to RDY1, RDY2	15		ns	
tCLA1X	AEN1, AEN2 Hold to CLK	0		ns	
tYHEN	CSYNC Setup to EFI	20		ns	
tEHYL	CSYNC Hold to EFI	20		ns	
tYHYL	CSYNC Width	2.tELEL		ns	
tI1HCL	RES Setup to CLK	65		ns	(Note 2)
tCLI1H	RES Hold to CLK	20		ns	(Note 2)

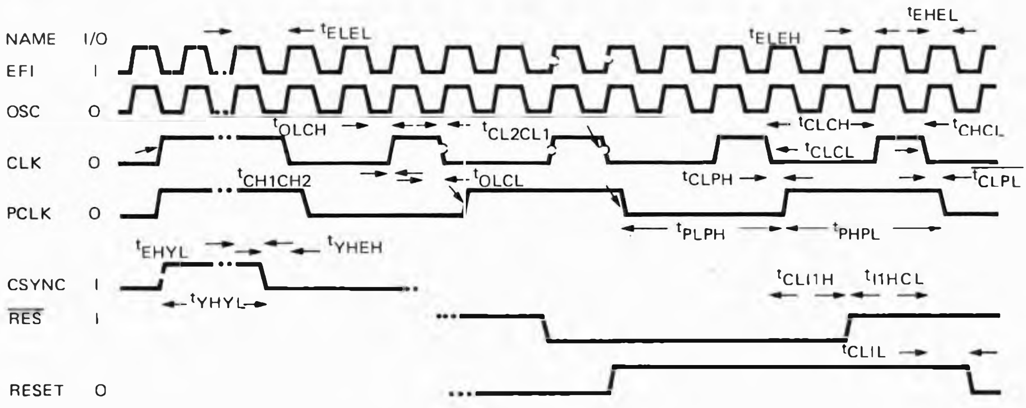
TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
tCLCL	CLK Cycle Period	125		ns	
tCHCL	CLK HIGH Time	(1/3 tCLCL)+2.0		ns	Fig. 7 & Fig. 8
tCLCH	CLK LOW Time	(2/3 tCLCL)215.0		ns	Fig. 7 & Fig. 8
tCH1CH2	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
tCL2CL1					
tPHPL	PCLK HIGH Time	tCLCL−20		ns	
tPLPH	PCLK LOW Time	tCLCL−20		ns	
tRYLCL	Ready Inactive to CLK (See note 4)	−8		ns	Fig. 8 & Fig. 10
tRYHCH	Ready Active to CLK (See note 3)	(2/3 tCLCL)−15.0		ns	Fig. 9 & Fig. 10
tCLIL	CLK to Reset Delay		40	ns	
tCLPH	CLK to PCLK HIGH Delay		22	ns	
tCLPL	CLK to PCLK LOW Delay		22	ns	
tOLCH	OSC to CLK HIGH Delay	−5	22	ns	
tOLCL	OSC to CLK LOW Delay	2	35	ns	

Notes:

1. Output signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between V_{IL} max−.4 V_{OH} and V_{IH} min +.4 volts in 15ns unless otherwise specified.

Timing Waveforms



Note: All timing measurements are made at 1.5 volts. Unless otherwise noted.

Figure 2. Waveforms for Clocks and Reset Signals

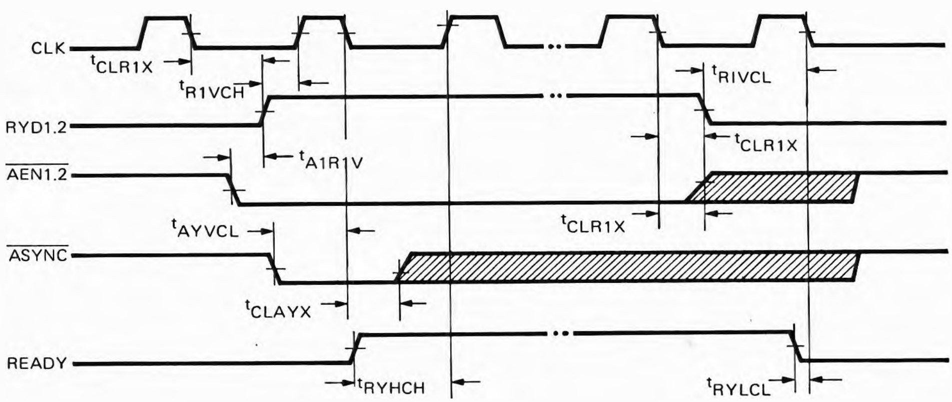


Figure 3. Waveforms for Ready Signals (For Asynchronous Devices)

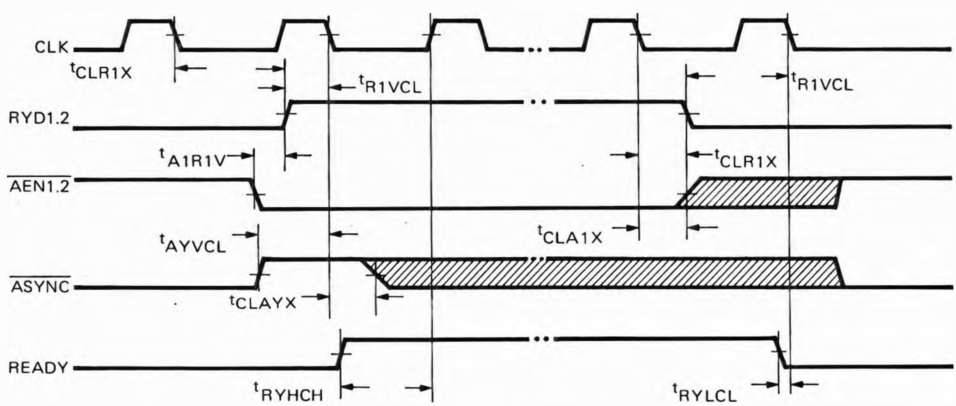


Figure 4. Waveforms for Ready Signals (For Synchronous Devices)

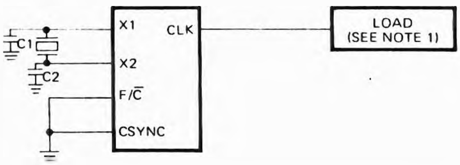


Figure 5. Clock High and Low Time (Using X1, X2)

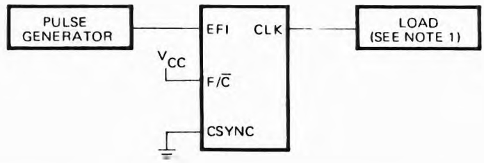


Figure 6. Clock High and Low Time (Using EFI)

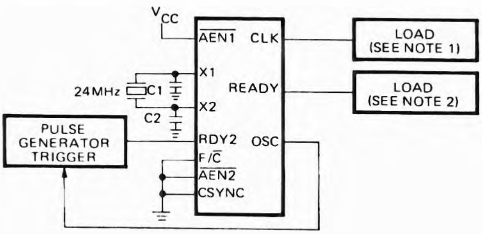


Figure 7. Ready to Clock (Using X1, X2)

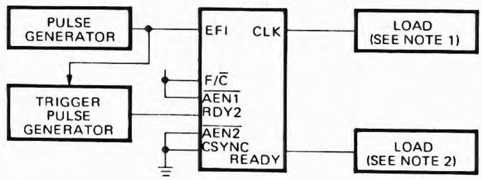
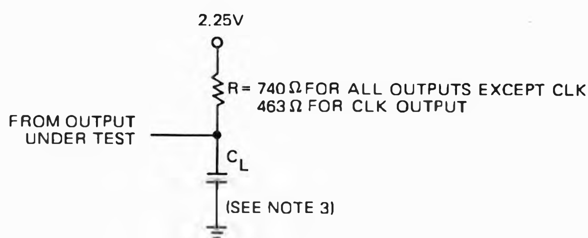


Figure 8. Ready to Clock (Using EFI)



Notes:
1. C_L = 100pF
2. C_L = 30pF
3. C_L INCLUDES PROBE AND JIG CAPACITANCE

Figure 9. Test Load Measurement Conditions

Table 1. Crystal Specifications

Parameter	Typical Crystal
Frequency	2.4–25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	−6db (Min)
Load Capacitance	18–32pf

Pin Description

Symbol	I/O	Description
$\overline{AEN1}$, $\overline{AEN2}$	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RYD1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal of EFI input frequency and a 1/3 duty cycle.
PCLK	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The UM82C84AE provides a Schmitt Trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determinded by $\overline{RES}$.
CSYNC	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple UM82C84AEs to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND		Ground
V_{CC}		+5V supply

Functional Description

Oscillator

The oscillator circuit of the UM82C84AE is designed primarily for use with an external parallel resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source. Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1 + C2} \quad \text{(Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another UM82C84AE clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the UM82C84AE. This is accomplished with two flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/C input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the –3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source*. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt Trigger input (RES) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the UM82C84AE. Wave-forms for clocks and reset signals are illustrated in Fig. 2.

Ready Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each input has a qualifier ($\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$, respectively). The $\overline{\text{AEN}}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{\text{AEN}}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{\text{ASYNC}}$ input defines two modes of READY synchronization operation.

When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop, one at the rising edge of CLK (requiring a setup time tR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, tR1VCL, on each bus cycle.

When $\overline{\text{ASYNC}}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{\text{ASYNC}}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

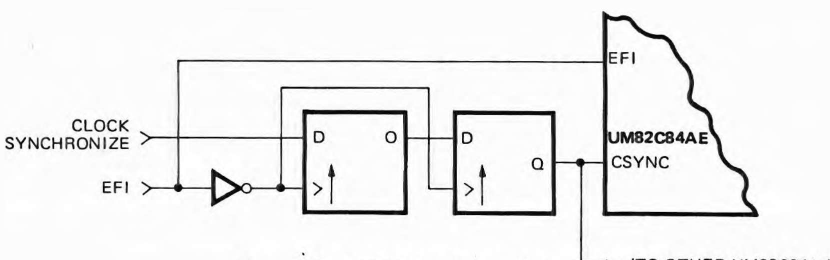


Figure 10. CSYNC Synchronization

*Note: If EFI input is used, then crystal input X1 must be tied to V_{CC} or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to V_{CC} or GND.