UMC

UM82C550

Asynchronous Communications Element with FIFOs

PRELIMINARY

Features:

- Capable of running all existing UM82C450 software
- Pin for pin compatible with the existing UM82C450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins will be TXRDY and RXRDY, respectively
- After reset, all registers are identical to the UM82C450 register set
- In the FIFO mode, transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data
- Full double buffering in the CHARACTER mode eliminates need for precise synchronization
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to $(2^{16} - 1)$ and generates the 16x clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully progrmmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 256K baud)
- False start bit detection
- Complete status reporting capabilities
- TRI-STATE TTL drive for the data and control buses
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break parity overrun framing error simulation
- Fully prioritized interrupt system controls

General Description

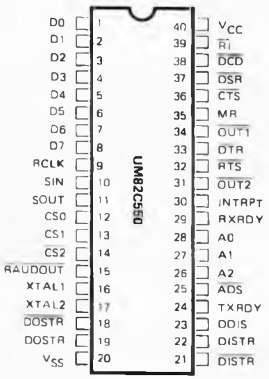
The UM82C550 is an improved version of the UM82C450 Asynchronous Communications Element (ACE). The improved specifications ensure compatibility with any of state-of-the-art CPUs. Functionally identical to the UM82C450 on power up (CHARACTER mode) the UM82C550 can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive overhead when the data rate is high. In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits per byte of error data in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been added to allow signalling of DMA transfers.

The ACE performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the ACE, as well as any error conditions (parity, overrun, framing, or break interrupt).

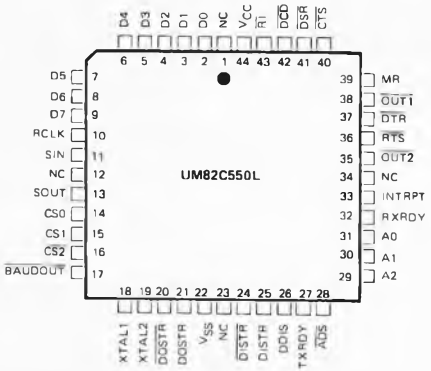
The ACE includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The ACE has complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements, minimizing the computing required to handle the communications link.

Pin Configurations

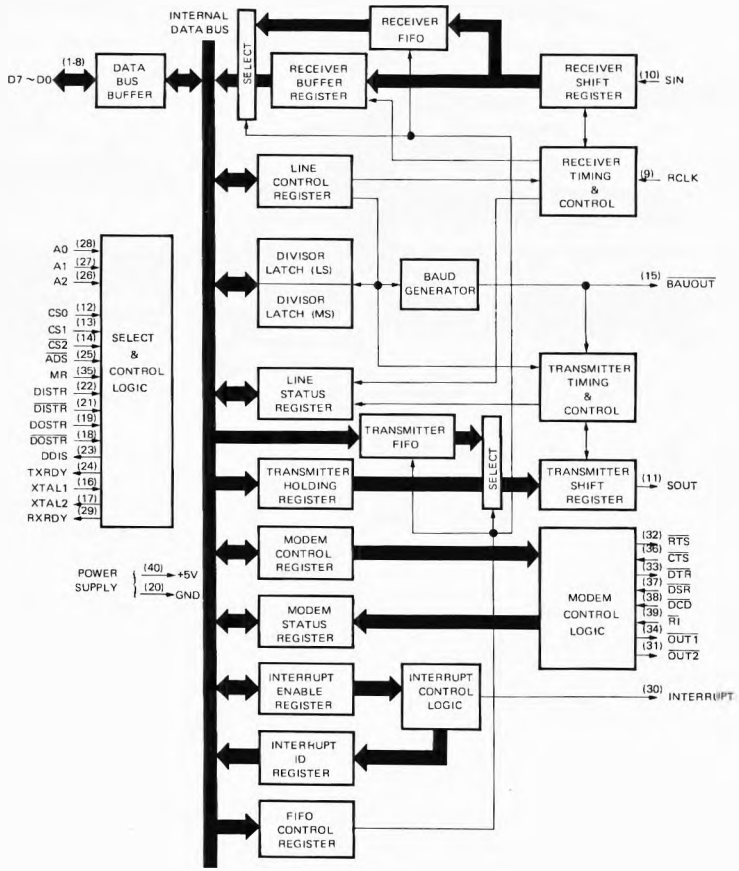
Dual-In-Line Package



Chip Carrier Package



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1 ~ 8	Data Bus D7 ~ D0	I/O	This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data control words, and status information are transferred via the D7 ~ D0 Data Bus.
9	RCLK	I	This input is the 16X baud rate clock for the receiver section of the chip.
10	SIN	I	Serial data input forms the communications link (peripheral device, MODEM, or data set).
11	SOUT	O	Composite serial data output to the communications link (perherial, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.
12 ~ 14	CS0 ~ $\overline{CS2}$	I	When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the ACE and the CPU.
15	$\overline{BAUDOUT}$	O	16X clock signal for the transmitter section of the ACE. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.
16 ~ 17	XTAL1 XTAL2	I O	These two pins connect the main timing reference (crystal or signal clock) to the ACE.
18	$\overline{DOSTR}$ DOSTR	I I	When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to write data or control words into a selected register of the ACE. Note: Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the ACE during a write operation. Therefore tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high if not used.
20	GND		Ground
21 22	$\overline{DISTR}$ DISTR	I I	When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, it allows the CPU to read status information or data from a selected register of the ACE. Note: Only an active DISTR or $\overline{DISTR}$ input is required to transfer data to the ACE during a read operation. Therefore tie either the DISTR input permanently low or the $\overline{DOSTR}$ input permanently high if not used.
23	DDIS	O	Goes low whenever the CPU is reading data from the ACE. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and ACE on the D7 ~ D0 Data Bus at all times except when the CPU is reading data.)

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
24	TXRDY	O	Transmitter DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling per pin can be selected via FCR3 when operating as in the Character Mode only DMA mode 0 is allowed. Mode 0 supports interleaved DMA where a transfer is made between CPU bus cycles. Mode 1 supports burst DMA where multiple transfers are made continuously until the XMIT FIFO has been filled. TXRDY Mode 0: In the Character Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) and there are no characters in the XMIT FIFO or XMIT holding register, the TXRDY pin (24) will be low active. Once It is activated the TXRDY pin will go inactive after the first character is loaded into the XMIT FIFO. TXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when FCR3 = 1 and there is at least one unfilled position in the XMIT FIFO. It will go low active. This pin will become inactive when the XMIT FIFO is completely full.
25	$\overline{ADS}$	I	When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals. Note: An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required tie the $\overline{ADS}$ input permanently low.
26 ~ 28	A0 ~ A2	I	These three inputs are used during a read or write operation to select an ACE register to read from or write operation to select an ACE register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain ACE registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read) Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
29	RXRDY	O	Receiver DMA signalling is available through this pin. When operating in the FIFO mode, one of two types of DMA signalling can be selected via FCR3. When operating as in the Character Mode only DMA mode 0 is allowed. Mode 0 supports interleaved DMA where a transfer is made between CPU bus cycles. Mode 1 supports burst DMA where multiple transfers are made continuously until the RCVR FIFO has been emptied. RXRDY Mode 0: When in the Character Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 1) and there is at least 1 character in the RCVR FIFO or RCVR HOLD register, the RXRDY pin (29) will be low active. Once it is activated the RXRDY pin will go inactive when there are no more characters in the FIFO or HOLD register. RXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when the FCR3 = 1 and the trigger level or the timeout has been reached, the RXRDY pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO or hold register.
30	INTRPT	O	Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available timeout (FIFO Mode only), Transmitter Holding Register Empty and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a master Reset operation.
31	$\overline{\text{OUT 2}}$	O	User-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM Control Register to high level. The $\overline{\text{OUT 2}}$ signal is set high upon a Master Reset Operation. The $\overline{\text{OUT 2}}$ signal is forced to its inactive state (high) during loop mode operation.
32	$\overline{\text{RTS}}$	O	When low, informs the MODEM or data set that the ACE is ready to transmit data. The $\overline{\text{RTS}}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{\text{RTS}}$ signal is set high upon a Master Reset operation. The $\overline{\text{RTS}}$ signal is forced to its inactive state (high) during loop mode operation.
33	$\overline{\text{DTR}}$	O	When low, informs the MODEM or data set that the ACE is ready to communicate. The $\overline{\text{DTR}}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{\text{DTR}}$ signal is set high upon a Master Reset operation. The $\overline{\text{DTR}}$ signal is forced to its inactive state (high) during loop mode operation.
34	$\overline{\text{OUT 1}}$	O	User-designated output that can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to high level. The $\overline{\text{OUT 1}}$ signal is set high upon a Master Reset Operation. The $\overline{\text{OUT 1}}$ signal is forced to its inactive state (high) during loop mode operation.

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
35	MR	I	This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis when high, it clears all the registers and FIFOs (except the Receiver Buffer, Transmitter Holding, Scratch Pad Register and Divisor Latches), and the control logic of the ACE. Also the state of various output signals (SOUT, INTRPT, $\overline{OUT\ 1}$, $\overline{OUT\ 2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input (Refer to Table 1)
36	$\overline{CTS}$	I	The $\overline{CTS}$ signal is a MODEM control function input whose conditions can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. Note: Whenever the $\overline{CTS}$ bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
37	$\overline{DSR}$	I	When low, this indicates that the MODEM or data set is ready to establish the communications link and transfer data with the ACE, the $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
38	$\overline{DCD}$	I	When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MODEM Status Register. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. Note: Whenever the $\overline{DCD}$ bit of the MODEM Status Register changes state, an interrupt is generated if the Modem Status interrupt is enabled.
39	$\overline{RI}$	I	When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register. Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Register is enabled.
40	V_{CC}		+5V Power Supply.

Table I. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3 forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1–3, 7 forced low Bits 4–6 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 – 3 Low Bits 4–7 – Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
RCVR FIFO	MR/FCR1 • FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1 • FCR0/ΔFCR0	All Bits Low
FIFO Control	Master Reset	All Bits Low

Register Descriptions

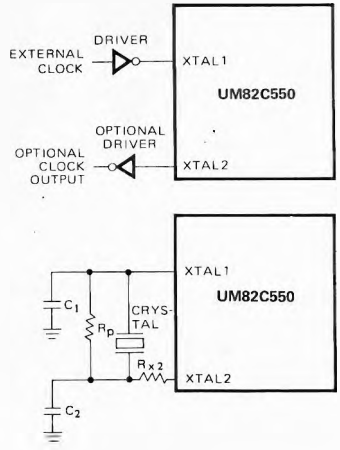
The system programmer may access or control any of the ACE registers summarized in Table II via the CPU. These registers are used to control ACE operations and to transmit and receive data.

Programmable Baud Generator

The ACE contains a programmable Baud Generator that is capable of taking any clock input (DC to 8.0 MHz) and dividing it by any divisor from 2 to $2^{16} - 1$). 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-digit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables III, IV and V illustrate the divisors for use with crystal frequencies of 1.8432 MHz, 3.072 MHz and 8 MHz, respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Typical Oscillator Applications



Typical Crystal Oscillator Network

Crystal	R_p	R_{x2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

Bit No.	Register Address											
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" If Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFO Enable (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error In RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the Character mode.

Table 11 Summary of Registers

Table III. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

Table IV. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Table V. Baud Rates Using 8 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
	2	2.344

Interrupt Enable Register

This 8-bit register enables the four types of interrupts of the ACE to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table II and are described below.

Bit 0: This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table II and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send $\overline{RTS}$ output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-desigated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the ACE. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state: the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs, and the MODEM Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the ACE.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7: These bits are permanently set to logic 0.

Interrupt Identification Register

The ACE has an on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Timeout (priority 2, FIFO Mode only); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip-select time the IIR freezes the highest priority interrupt pending and no other interrupts change the IIR even though they are recorded, until that particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table II and are described below.

Bit 0: This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table VI.

Bit 3: In the Character mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 through 6: These three bits of the IIR are always logic 0.

Bit 7: This bit is set when FCR0 = 1.

Table VI. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	–	None	None	–
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO During the Last 4 Char. Times and There is at Least 1 Char. in it During This Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table II and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty, it is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the Character mode this is a 0. In the FIFO mode LSR7 is set when there is at least one parity error framing error or break indication in the FIFO LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

FIFO Control Register

This is a write only register at the same location as the IIR the IIR is a read only register. This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO Mode to Character Mode and vice versa data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Setting FCR3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR0 = 1 (see description of RXRDY and TXRDY pins.)

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents

of the Line Control Register are indicated in Table II and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) on checked (received data) between the last data word bit and Stop bit of the serial data (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1.

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load in all Os. a pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generater during a Read or write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Modem Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table II and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to $\overline{OUT\ 1}$ in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR0 = 1, IER0 = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.
D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When the XMIT FIFO and transmitter interrupts are enabled (FCR0 = 1, IER1 = 1). XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed character time minus the last stop bit time whenever the following occurs. THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist
   - at least one character is in the FIFO
   - the most recent character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay)
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 16 ms at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
C. When a timeout interrupt has occurred it is cleared and the time reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

With FCR0 = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the ACE in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check RCVR and XMITTER status via the LSR as stated previously.

LSR0 will be set as long as there is one byte in the RCVR FIFO.
LSR1 to LSR4 will specify which error(s) has occured.
Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER2 = 0.
LSR5 will indicate when the XMIT FIFO is empty.
LSR6 will indicate that both the XMIT FIFO and shift register are empty.
LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All input or Output Voltages with Respect to V_{SS}
. . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 60 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0 V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	V
V_{IHX}	Clock Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Clock Input High Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA on all*		0.4	V
V_{OH}	Output High Voltage	I_{OL} = −1.0 mA*	2.4		V
I_{CC} (AV)	Avg Power Supply Current (V_{CC})	V_{CC} = 5.25V, T_A = 25°C No Loads on output SIN, DSR, RLSD, CTS, RI = 2.0V All other inputs = 0.8 V		10	mA
I_{IL}	Input Leakage	V_{CC} = 5.25V, V_{SS} = 0 V All other pins floating. VIN = 0V, 5.25V		± 10	μA
I_{CL}	Clock Leakage			± 10	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 5.25V, V_{SS} = 0 V V_{OUT} = 0V, 5.25V 1) Chip deselected 2) WRITE Mode, chip selected		± 20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		V

*Does not apply to XTAL 2

Capacitance (T_A = 25°C, V_{CC} = V_{SS} = 0V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$C_{XTAL\,2}$	Clock Input Capacitance	f_c = 1 MHz Unmeasured pins returned to V_{SS}		15	20	pF
$C_{XTAL\,1}$	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

AC Characteristics ($T_A = 0°C$ to $-70°C$, $V_{CC} = +5V \pm 5\%$)

Symbol	Parameter	Conditions	Min.	Max.	Units
t_{AH}	Address Hold Time		0		ns
t_{AR}	$\overline{DISTR}$/DISTR Delay from Address	(Note 1)	30		ns
t_{AS}	Address Setup Time		60		ns
t_{AW}	Address Strobe Width		60		ns
t_{CH}	Chip Select Hold Time		0		ns
t_{CS}	Chip Select Setup Time		60		ns
t_{CSR}	$\overline{DISTR}$/DISTR Delay from Chip Select	(Note 1)	50		ns
t_{CSW}	$\overline{DOSTR}$/DOSTR Delay from Select	(Note 1)	50		ns
t_{DD}	$\overline{DISTR}$/DISTR to Driver Enable/Disable	@100 pF loading (Note 3)		60	ns
t_{DDA}	$\overline{DOSTR}$/DOSTR Delay from Address	(Note 1)	30		ns
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	@100 pF loading		125	ns
t_{DH}	Data Hold Time		30		ns
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width		125		ns
t_{DOW}	DOSTR/DOSTR Strobe Width		100		ns
t_{DS}	Data Setup Time		30		ns
t_{HZ}	DISTR/DISTR to Floating Data Delay	@100 pF loading (Note 3)	0	100	ns
t_{MRW}	Master Reset Pulse Width		5		μs
t_{RA}	Address Hold Time from $\overline{DISTR}$/DISTR	(Note 1)	20		ns
t_{RC}	Read Cycle Delay		125		ns
t_{RCS}	Chip Select Hold Time from $\overline{DISTR}$/DISTR	(Note 1)	20		ns
t_{WA}	Address Hold Time from $\overline{DOSTR}$/DOSTR	(Note 1)	20		ns
t_{WC}	Write Cycle Delay		150		ns
t_{WCS}	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	(Note 1)	20		ns
t_{XH}	Duration of Clock High Pulse	External Clock (8.0 MHz Max.)	55		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (8.0 MHz Max.)	55		ns
RC	Read Cycle = $t_{AR} + t_{DIW} + t_{RC}$		280		ns
WC	Write Cycle = $t_{DDA} + t_{DOW} + t_{WC}$		280		ns
Baud Generator					
N	Baud Divisor		1	$2^{16}-1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		175	ns

Note 1: Applicable only when $\overline{ADS}$ is tied low.

AC Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Max.	Units
t_{BLD}	Baud Output Negative Edge Delay	100 pF Load		175	ns
t_{HW}	Baud Output Up Time	f_x = 8.0MHz ÷ 2,100pF Load	75		ns
t_{LW}	Baud Output Down Time	f_x = 8.0MHz ÷ 2,100pF Load	100		ns
Receiver					
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	100 pF Load		1	μs
t_{SCD}	Delay from RCLK to Sample Time			2	μs
t_{SINT}	Delay from Stop to Set Interrupt	(Note 2)	1	1	RCLK Cycles
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	100 pF Load		175	ns
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	100 pF Load		250	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	RCLK Cycles
t_{SI}	Delay from Initial Write to Interrupt	(Note 4)	16	32	RCLK Cycles
t_{STI}	Delay from Stop to Interrupt (THRE)	(Note 4)	8	8	RCLK Cycles
t_{SXA}	Delay from Start to TXRDY active	100 pF Load		8	RCLK Cycles
t_{WXI}	Delay from Write to TXRDY inactive	100 pF Load		195	ns
Modem Control					
t_{MDO}	Delay from $\overline{DOSTR}$/DOSTR (WR MCR) to Output	100 pF Load		200	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/ DISTR (RD MSR)	100 pF Load		250	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		250	ns

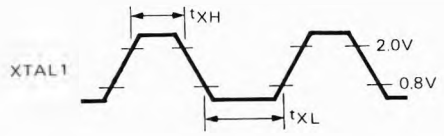
Note 2: In the FIFO mode (FCR0 = 1) the trigger level and timeout interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 9 RCLKs. Status indicators (PE, FE, BI) will be delayed 9 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive.

Notes 3: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 4: This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO Interrupt Mode Operation).

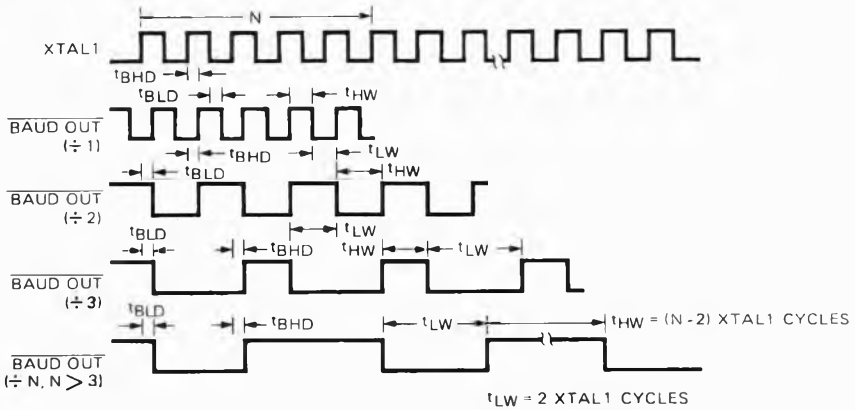
Timing Waveforms

EXTERNAL CLOCK INPUT (8.0 MHz MAX.)

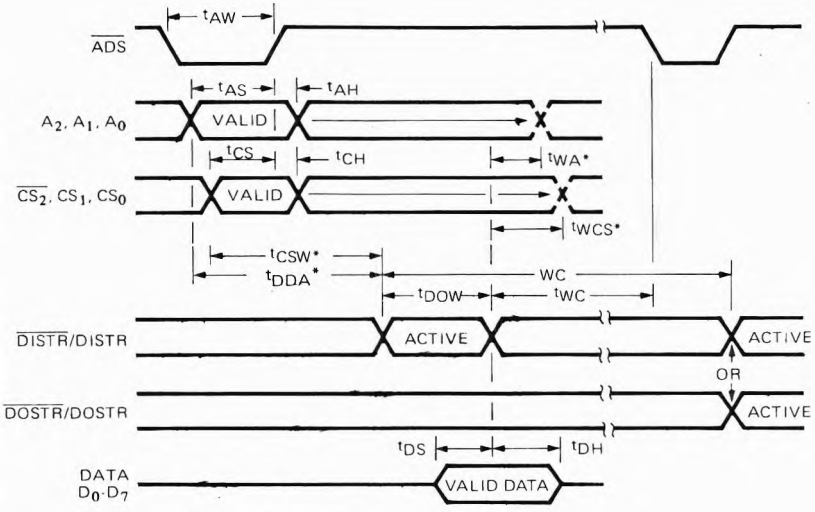


AC TEST POINTS

$\overline{\text{BAUDOUT}}$ TIMING



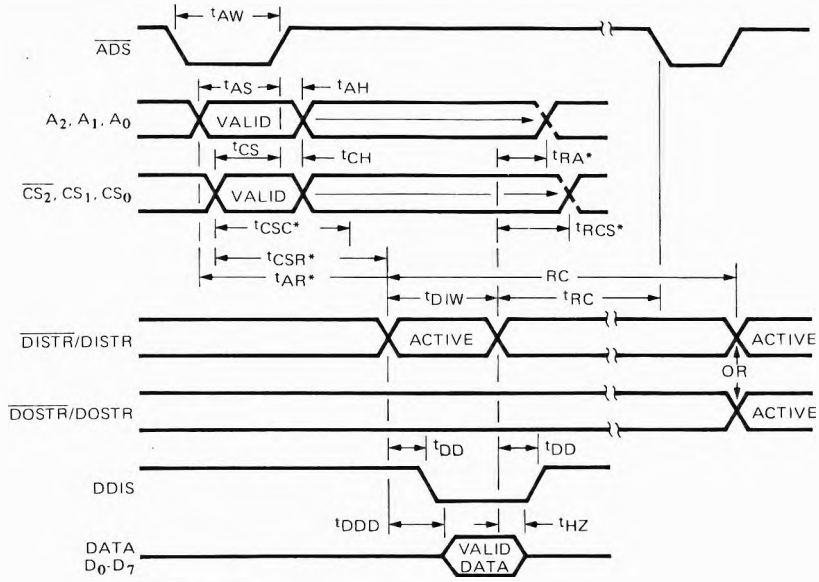
WRITE CYCLE



* Applicable Only When $\overline{\text{ADS}}$ is Tied Low.

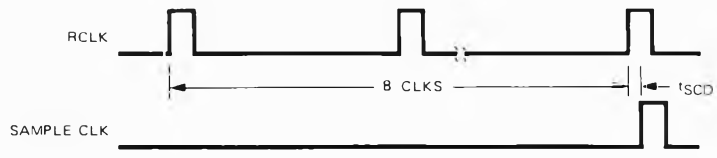
Timing Waveforms (Continued)

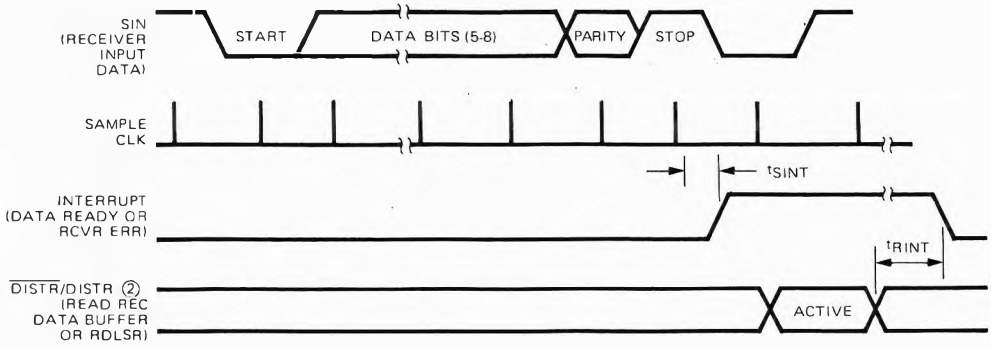
READ CYCLE



* Applicable Only When $\overline{ADS}$ is Tied Low.

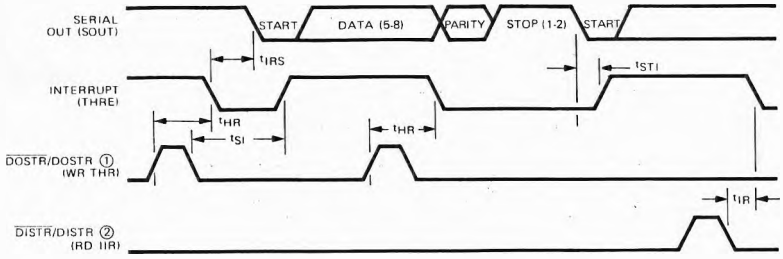
RECEIVER TIMING



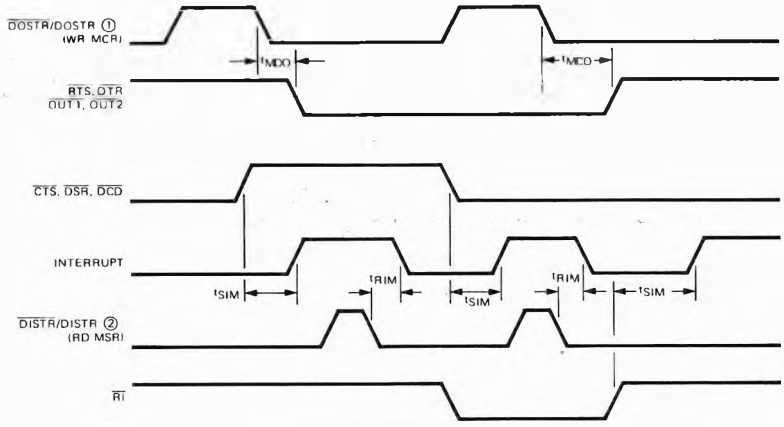


Timing Waveforms (Continued)

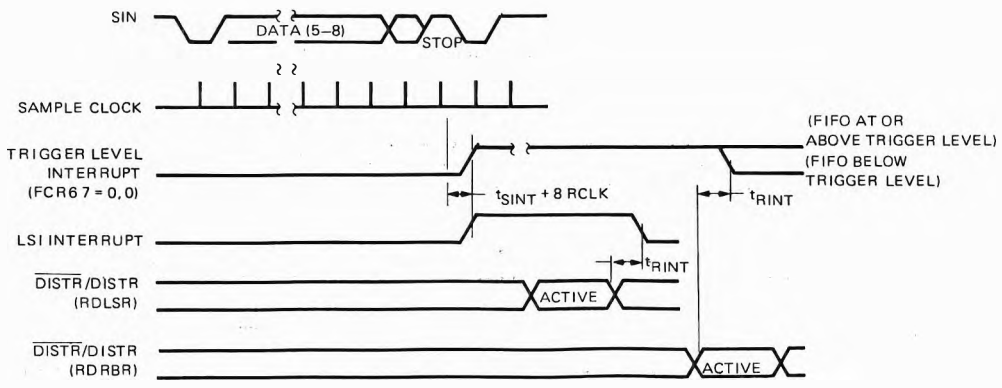
TRANSMITTER TIMING



MODEM CONTROL TIMING

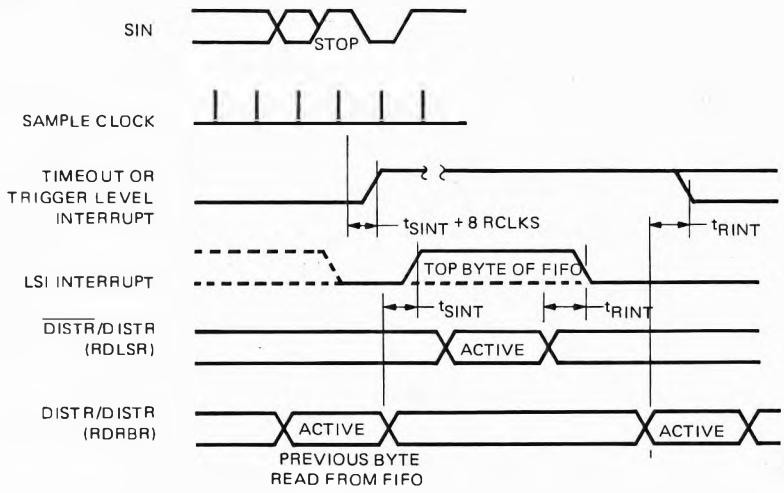


RCVR FIFO First Byte (This Sets RDR)

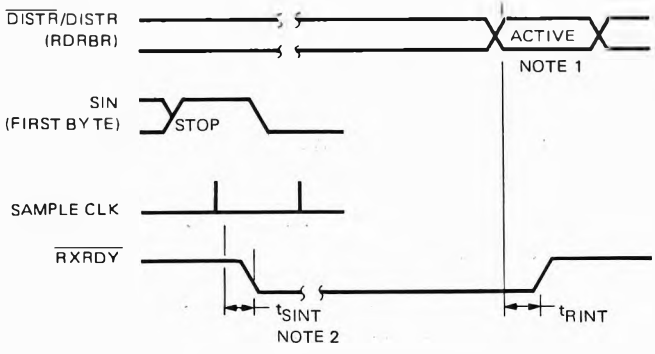


Timing Waveforms (Continued)

RCVR FIFO Bytes Other Than The First Byte (RDR is Already Set)



Receiver Ready (Pin 29) FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)

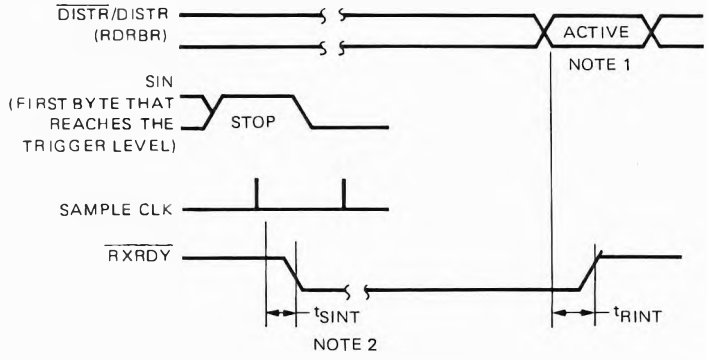


Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, t_{SINT} = 8 RCLKs

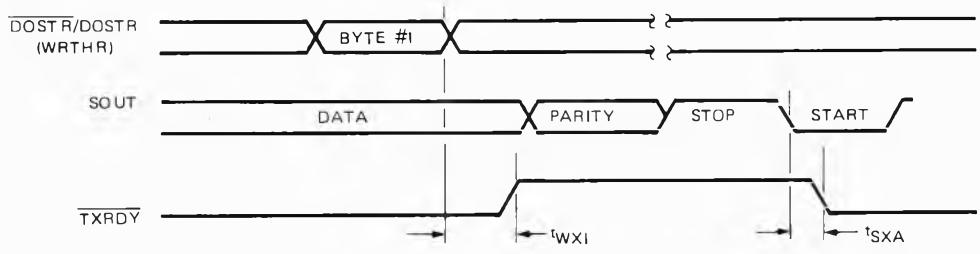
Timing Waveforms (Continued)

Receiver Ready (Pin 29) FCR0 = 1 and FCR3 = 1 (Mode 1)

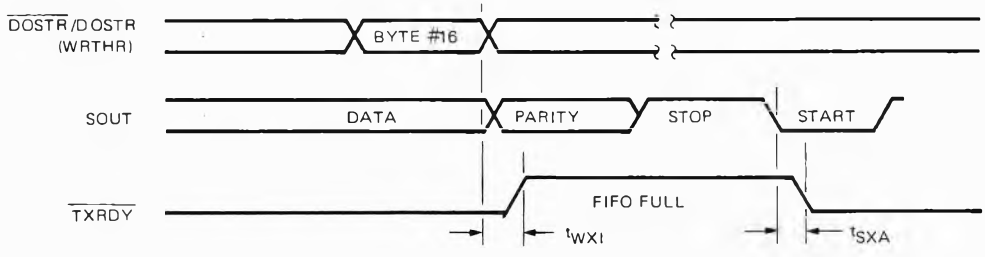


Note 1: This is the reading of the last byte in the FIFO.
Note 2: If FCR0 = 1, t_{SINT} = 9 RCLKS

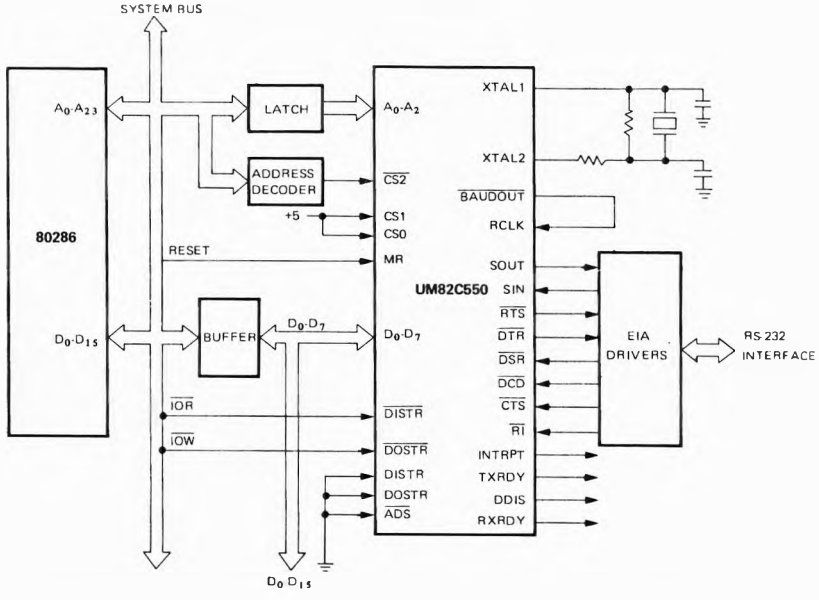
Transmitter Ready (Pin 24) FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



Transmitter Ready (Pin 24) FCR0 = 1 and FCR3 = 1 (Mode 1)



Application Circuit



Ordering Information

Part Number	Package
UM82C550	40L DIP
UM82C550L	44L PLCC