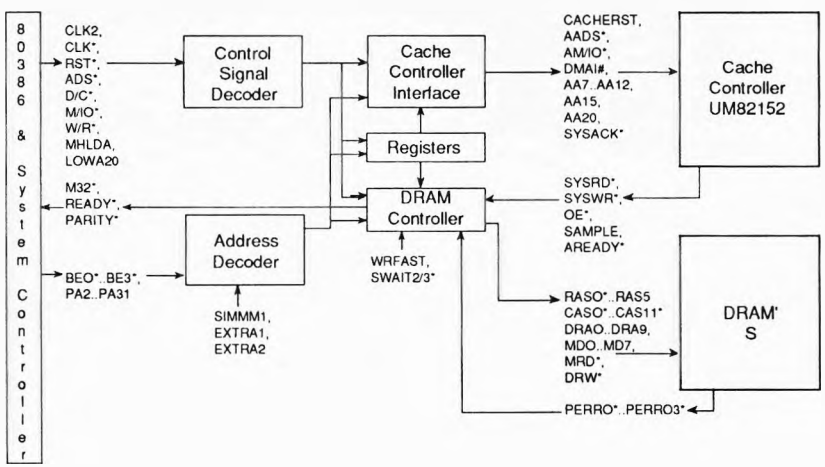
I General Description

The UM82C389 Cache Interface Chip is one of the UMC UM82C380 series High End AT (HEAT) chip set. As a DRAM controller, UM82C389 works in tandem with UM82152 Cache Controller to form an efficient cache memory subsystem. This highly integrated Cache Interface chip contains all necessary glue logic components to interface UM82152 directly to UM80386 CPU. It is also carefully tailored to be directly pin replaceable with the UM82C384 Page Memory Controller: one motherboard is sufficient for both Page/Cache modes.

II Features

- Supports a flexible system memory configuration:
  a) 1M, 2M or 3M using 256Kx1 DRAM
  b) 4M, 8M or 12M using 1Mx1 DRAM
- Uses normal page DRAM (Static column is unnecessary)
- Handles 80ns/100ns DRAM speed at 25MHz system speed
- Accepts short precharge time DRAM to boost system performance
- 120 pin flat package in 1.2μ CMOS technology

III Block Diagram



IV Pin Configuration

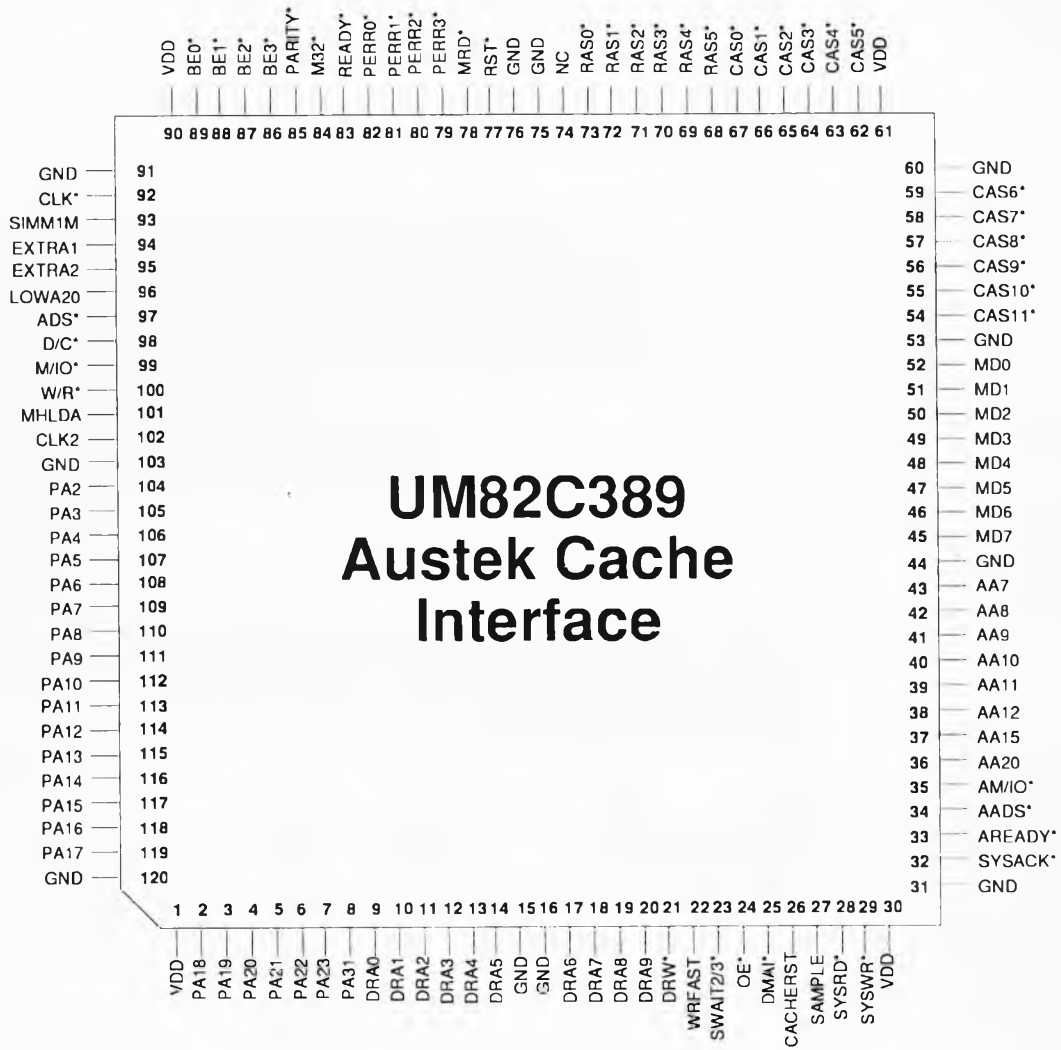


Figure 1. Pin Configuration

VI Functional Description

The Cache Interface has two major functions:

1) Intercepting and modifying all control signals between UM80386 CPU and the Cache Controller UM82152 for different bus cycles (Reset, Memory, I/O, DMA)

2) Working as DRAM controller underneath the Cache Controller

Following is the operation of Cache Interface in different bus cycles:

1) Reset: upon receiving active RST*, Cache Interface generates CACHERST signal correctly synchronized with CLK* for the Cache Controller.
   The internal flip-flops of Cache Interface are also forced to initial known states.

2) I/O: Cache Interface converts all I/O cycles from UM80386 to memory cycles to Cache Controller.

3) Memory:

   a) Normal Memory: all control signals are passed directly to Cache Controller. If a miss occurs, DRAM Controller will be activated to transfer data from DRAM's to UM80386.
   b) Memory-Mapped I/O: only 2 devices are mapped; they are the Cache Controller and the Register of Cache Interface.
   c) Non-Existing Memory Locations: these cycles will be terminated and the corresponding entries in tag RAM will be invalidated to avoid data stalling.

4) D(irect) M(emory) A(ccess): during the DMA read cycles (i.e. data coming from DRAM), Cache controller is forced idle. However, during the DMA Write cycles, Cache Controller will watch over the address bus; if anyaddresses match any entries of tag RAM, the corresponding entries will be invalidated.

Cache Interface can be divided into 5 logic blocks: Control Signal Decoder, Address Decoder, Registers, Cache Controller Interface and DRAM Controller.

1) Control Signal Decoder: decodes all incoming control signals from 80386 to activate either Cache Controller or DRAM Controller depending on bus cycle (Reset, Memory, I/O, or DMA bus cycles).

2) Address Decoder: maps all incoming addresses to actual physical on board memory; activates M32* if existing memory locations are referred to.

3) Registers: store various options to program the Cache Controller Interface as well as the DRAM Controller.

4) Cache Controller Interface: provides all necessary signals to control Cache Controller.

5) DRAM Controller: generates all necessary signals to control DRAM such as R(ow) A(ddress) S(elect) C(olumn) A(dress) S(elect), transceiver direction control, parity generation & detection.

Memory Configurations

Because 24 bit address is used, only 16MB can be addressed. The minimum memory requirement is 1MB. This first 1MB is mapped into two regions: 640KB of base memory and 384KB located at the high end of the 16M address place. More memory can be added incrementally provided the following jumpers are setup correctly

SIMM1M	EXTRA 1	EXTRA 2	System Memory	DRAM Type
0	0	0	1M	
0	1	0	2M	256K
0	1	1	3M	
1	0	0	4M	
1	1	0	8M	1M
1	1	1	12M	
0	0	1	*Illegal	
1	0	1		

Figure 2. Memory Configuration Set Up

Different Memory Configurations are illustrated by Figures 3 & 4.

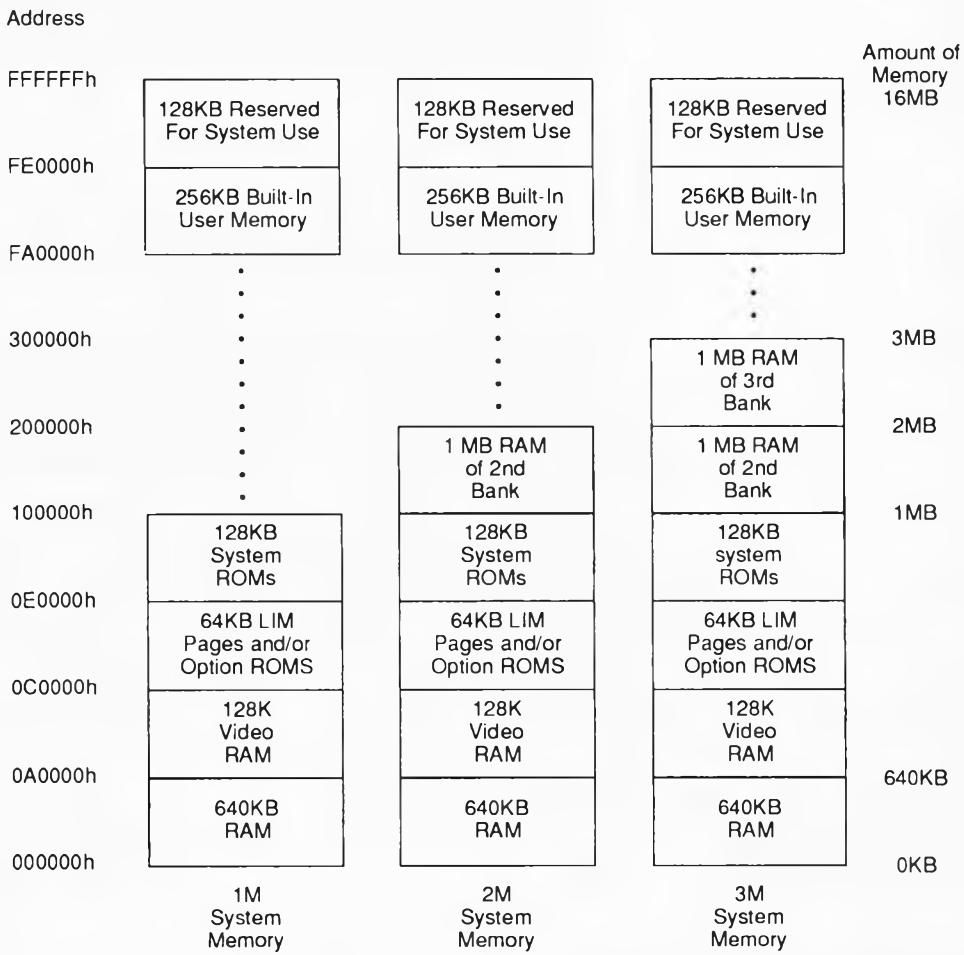


Figure 3. Memory Configuration Using 256Kx1 DRAM

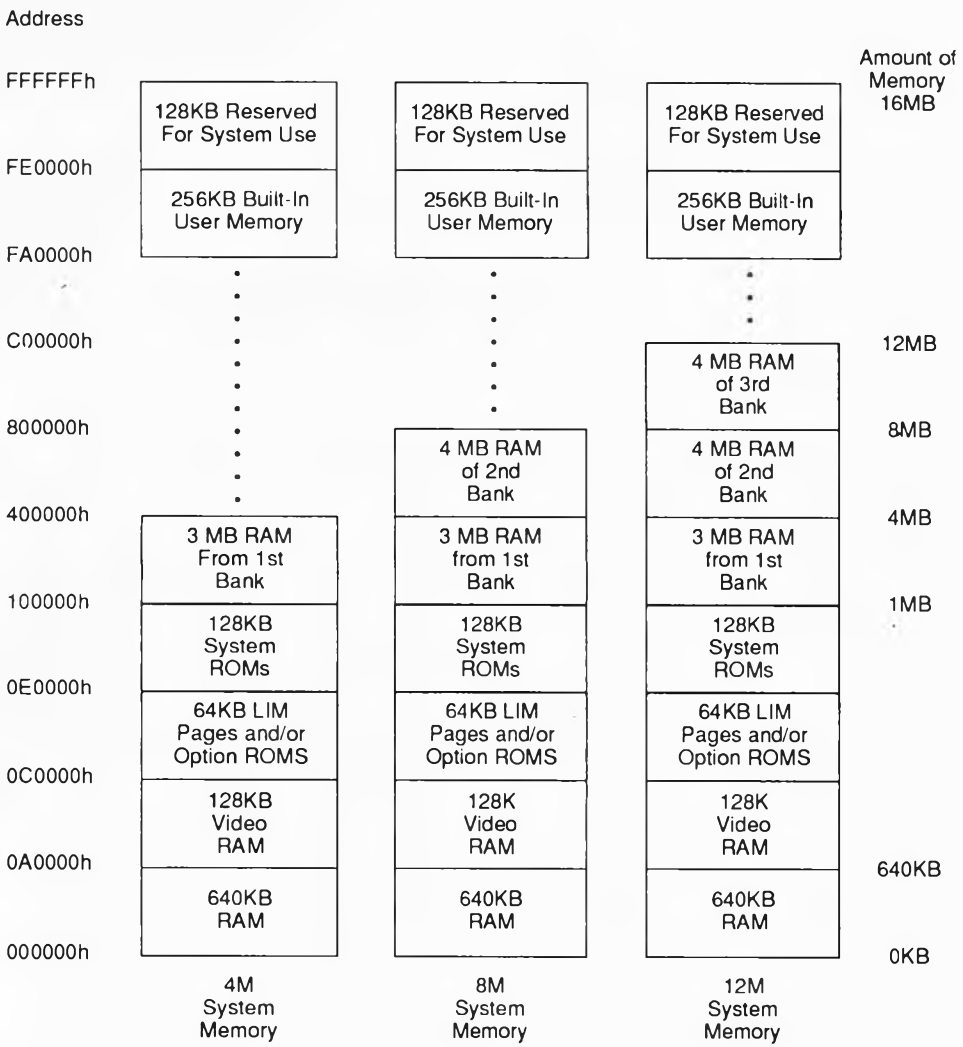


Figure 4. Memory Configuration Using 1Mx1 DRAM

ROM Mapping

Of the 384KB memory located at the end of the 16M address space, the bottom 128KB starting at FE0000h is called Shadow RAM. The Shadow RAM has 2 special features:

- Write-protected by controlling a special hardware register named CONTROL.
- Relocated via hardware register CONTROL to the system ROM's location (0E0000h - OFFFFFh); when mapped, this Shadow RAM can be addressed at locations FE0000h - FFFFFFh or 0E0000h - 0FFFh. The system ROM cannot be accessed any longer.

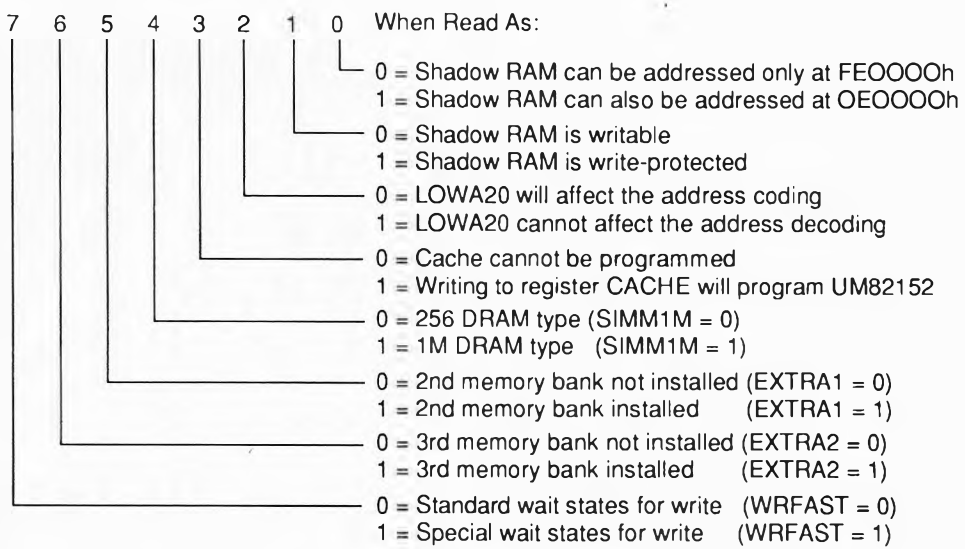
The relocation and write-protected capabilities allow the system ROM to be replaced with high speed RAM having the same contents (Shadow RAM)

Memory-Mapped Hardware Registers

There are 2 registers: CONTROL for diagnostics and control, CACHE for programming the cache controller.

- CONTROL register (address 80C00000h): is partitioned into 2 segments: low nibble is read/write while the high nibble is read only.

IMPORTANT: When writing to CONTROL register, all the bits of low nibble will be complemented (i.e. writing 1 will be read later as 0 and vice versa)



- CACHE register (address 8030xxxxh): actually spreads out 64K memory block starting at 80300000h. When bit 3 of CONTROL register is 1, writing to these locations will be interpreted by the UM82152 as a programming command (check UM82152 data sheet)

Operation

Because the UM82152 always tries to operate the CPU in pipeline mode, the actual length of a bus cycle varies. Here is the summary of wait states for different configurations and situations:

SWAIT 2/3#	WRFAST	Read/ Write	Hit/ Miss	Single/ Pipeline	Wait States	Number of CLK2 Cycles	Notes:
0/1	0/1	Read	Hit	Single	0	6	
0	0/1	Read	Miss	Single	3	12	
0	0	Write	Hit/Miss	Single	3	12	
0	1	Write	Hit/Miss	Single	3/2	12/10	10 if previous cycle is read
1	0/1	Read	Miss	Single	2	10	
1	0	Write	Hit/Miss	Single	2	10	
1	1	Write	Hit/Miss	Single	2/1	10/8	8 if previous cycle is read

Note: For pipeline mode, subtract 2 from the number of CLK2 cycles of the corresponding bus cycle since ADS# is hidden from previous bus cycle (i.e., Read Hit in pipeline mode is 0 wait states and lasts 4 CLK2 cycles).

Figure 5. Wait State Summary