I General Description

The UM82C383 Data Buffer is one of UMC's High End AT (HEAT) Chip Set, It is an interface between 32-bit processor data bus, 16-bit system data bus and 8-bit peripheral data bus.

II Features

- 32-bit data bus buffer
- 16-bit or 8-bit data-bus buffer for PC/AT bus
- 8-bit I/O port data bus buffer
- Word swap logic
- Advanced 1.2μ CMOS Technology
- 120 Pin Flat Package

III Block Diagram

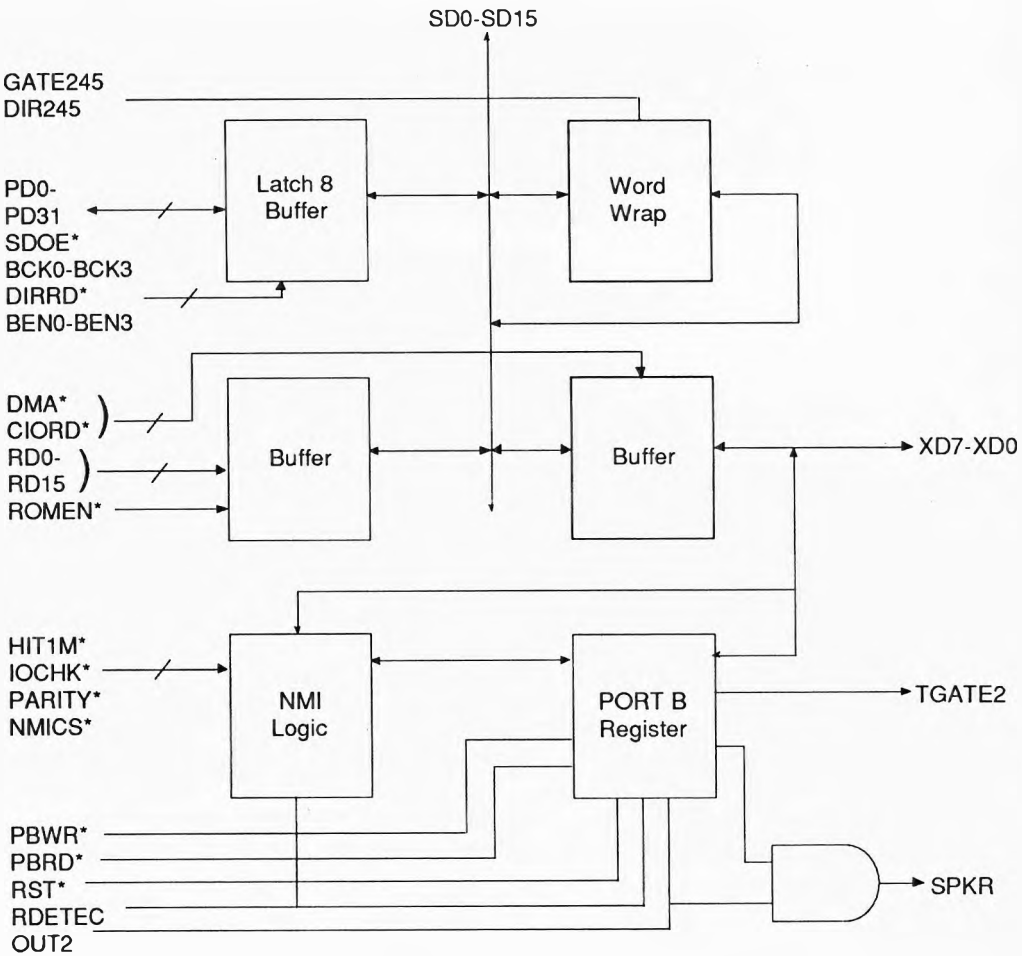

Figure 1. UM82C383 Block Diagram

IV Pin Configuration

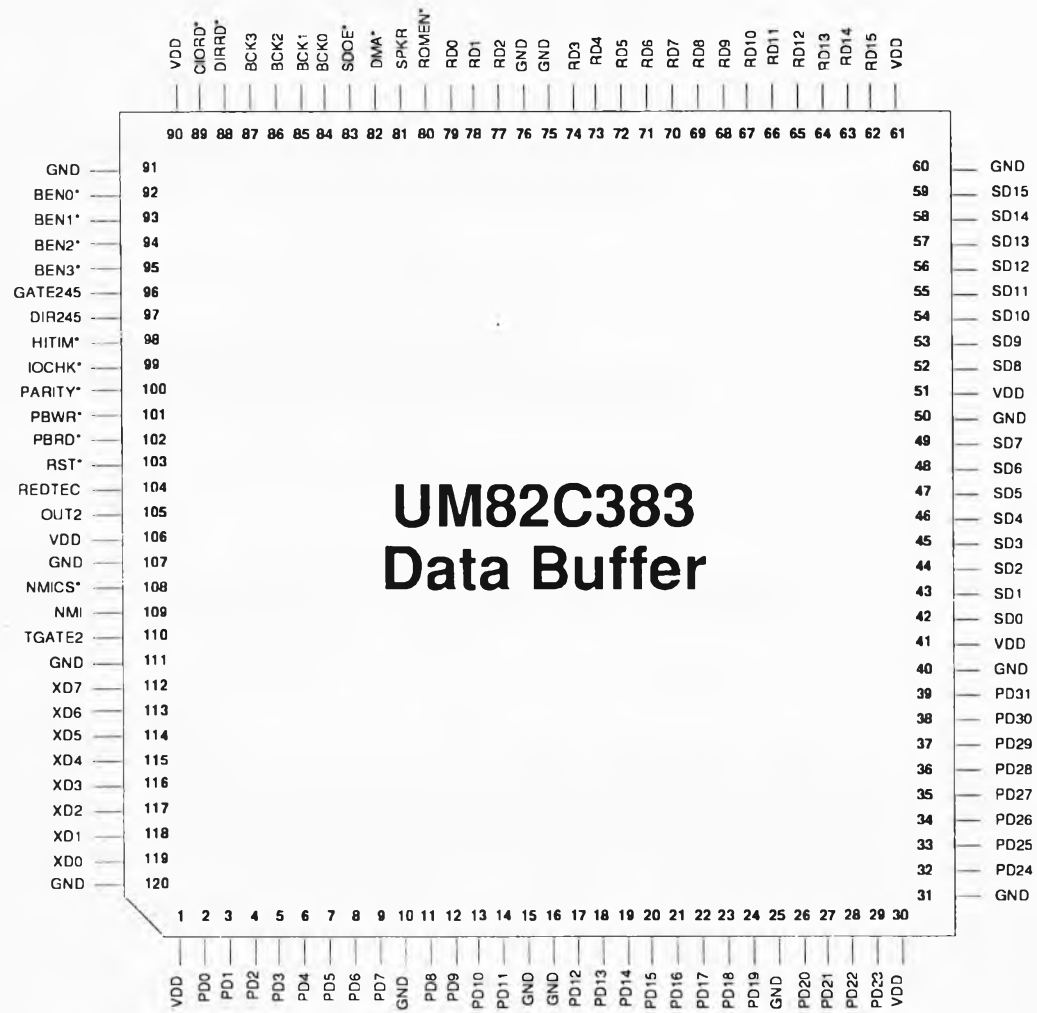

Figure 2. Pin Configuration

VI Functional Description

The UM82C383 Data Buffer contains a 32-bit 80386 data bus buffer, 16-bit PC/AT slot data buffer, 8-bit I/O port data bus buffer, and one internal port 61H. A word-swap logic circuit is also built to facilitate 80386 read or write 32-bit data through PC/AT 16-bit data bus.

During the CPU read cycle, the system bus data can be latched by controlling the signals BCK0-BCK3 and SDOE*. During the CPU write cycle, the processor data can be written to the system bus through data buffer by controlling the signals DIRRD* ,BEN0*-BEN3*. The GATE245 and DIR245 should be asserted to initiate the word wrap circuit to transfer 32-bit data into 8-bit data.

During the DMA cycle, the data transfer between processor bus and system bus is controlled by asserted DIRRD*, BEN0*-BEN3* signals. When the DIRRD* is low, the system bus will be transferred to processor bus. When the DIRRD* is high, the processor bus will be transferred to system bus. The signals GATE245, DIR245 should be asserted to initiate the word wrap circuit if the data transfer is 8-bit only.

UM82C383 also generates NMI signals, which can be enabled by Port B Bit 7. Whenever IOCHK* or PARITY* is low, an NMI error signal will be generated, and can be checked by reading Port B, Bit 6. When a positive transition occurs in HITIM*, NMI will be forced High, which can be checked by reading Port B,Bit 7.

The register descriptions are illustrated as follows:

WRITE PORT B:

BIT 7		: Not defined
BIT 6		: Not defined
BIT 5		: Not defined
BIT 4		: Not defined
BIT 3	-->1	: Clear hit timer register
BIT 2	-->1	: Clear parity check error
BIT 1	-->1	: Enable speaker output
BIT 0		: Trigger 8254 timer 2

READ PORT B:

BIT 7	: Hit timer register status
BIT 6	: Parity check status
BIT 5	: 8254 timer 2 output
BIT 4	: Read RDETEC input to check if refresh counter is active
BIT 3	: Read back written data
BIT 2	: Read back written data
BIT 1	: Read back written data
BIT 0	: Read back written data