UMC

UM74HCT590

8-bit Binary Counter with Output Registers

Features

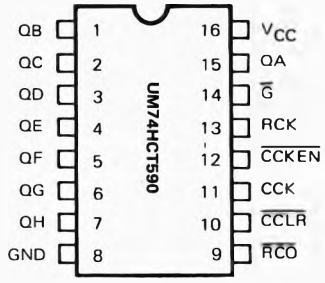
- 8-bit binary counter with parallel register output.
- 3-state register output.
- Direct clear to counter.
- High speed counter with guaranteed frequency: DC to 20 MHz.
- High driving capability (I_{OL} = 24 mA, V_{OL} = 0.5V) for direct interface with TTL, NMOS and CMOS devices.
- Can drive up to 20 TTL loads.

General Description

This is an 8-bit binary counter that feeds an 8-bit storage register. The register has parallel Tri-state outputs QA ~ QH enabled by $\overline{G}$ = 0. Two separate clocks, CCK and RCK, are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

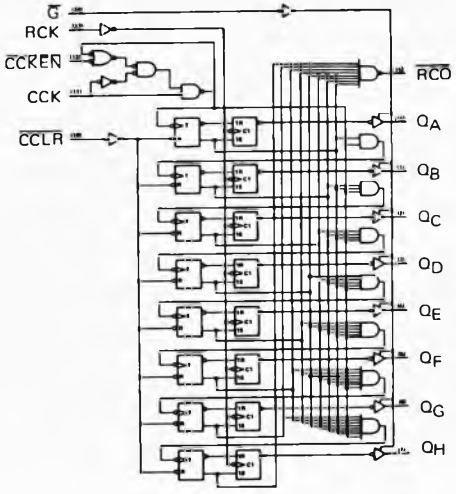
Both the counter and register clocks are positive-edge. When connecting both clocks together, the counter state will always be one count ahead of the register.

Pin Configuration



QA~QH : Register Output.
RCK : Register Clock, Positive Trigger.
CCK : Counter Clock, Positive Trigger.
$\overline{RCO}$: Ripple Carry Output.
$\overline{G}$: Output Enable, $\overline{G}$ = 1 ⇒ Output = High-Z.
$\overline{CCKEN}$: Counter Clock Enable, Active Low.
$\overline{CCLR}$: Counter Clear, Active Low.

Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.5 to 7V

Input Voltage V_I . . . . . −0.5V to +7V

Operating Free-Air Temperature Range . . . −40°C to 85°C

Storage Temperature Range . . . . . −55°C to 125°C

Maximum Power Dissipation . . . . . 0.55 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Electrical Characteristics: (V_{DD} = 5V, T_A = 0°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply	4.5	5	5.5	V	
V_{IH}	Input High-Level Voltage	2.0	–	–	V	
V_{IL}	Input Low-Level Voltage	–	–	0.8	V	
I_{OH}	High-Level Output Current On QA ~ QH	–	–	−4	mA	V_{OH} = 3.0V
I_{OL}	Low-Level Output Current On QA ~ QH	–	–	24	mA	V_{OL} = 0.5V
I_{OHR}	High-Level Output Current On $\overline{RCO}$	–	–	0.4	mA	$V_{\overline{RCO}}$ = 3.4V
I_{OLR}	Low-Level Output Current On $\overline{RCO}$	–	–	8	mA	$V_{\overline{RCO}}$ = 0.5V
V_{OH}	High-Level Output Voltage	3.0	3.8	–	V	$\lvert I_{OH} \rvert$ or $\lvert I_{OHR} \rvert$ = Max.
V_{OL}	Low-Level Output Voltage	–	0.4	0.5	V	I_{OL} or I_{OLR} = Max.
I_{IN}	Input Current	−1.0	–	+1.0	μA	V_{IN} = 5V ~ 0V
I_{OZ}	OFF-State Output Current	−8	–	+8	μA	V_O = 5V ~ 0V.
I_{CC}	Operating Supply Current	–	–	100	μA	

Timing Requirement and Switching Characteristics:

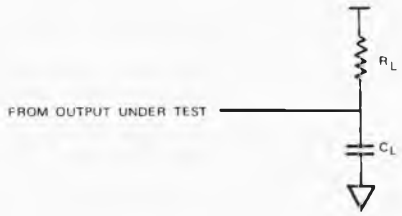
(V_{DD} = 5V, T_A = 0°C to 85°C)

Parameter		Min.	Typ.	Max.	Unit	Condition
Clock Frequency CCK or CCR: $F_{max.}$		20	35	–	MHz	
Pulse Width of CCK or RCK: T_W		20	–	–	ns	Recommended Value
Pulse Width of $\overline{CCLR}$: T_W		20	–	–	ns	Recommended Value
Count enable time: $\overline{CCKEN}$ Low before CCK ↑		20	–	–	ns	Recommended Value
Clear inactive set-up time: T_{SU} $\overline{CCLR}$ Low go High before CCK ↑		20	–	–	ns	Recommended Value
Time Delay from CCK ↑ to $\overline{RCO}$ ↑: T_{PLH}		–	15	25	ns	C_L = 15 pf. R_L = 2KΩ
Time Delay from CCK ↑ to $\overline{RCO}$ ↓: T_{PHL}		–	20	25	ns	
Time Delay from $\overline{CCLR}$ ↓ to $\overline{RCO}$ ↑: T_{PLH}		–	20	25	ns	
Time Delay from RCK ↑ to Q ↑: T_{PLH}		–	15	25	ns	C_L = 45 PF R_L = 667Ω
Time Delay from RCK ↑ to Q ↓: T_{PHL}		–	20	25	ns	
Time Delay when $\overline{G}$ ↓	Q Floating to Q Low: T_{PZL}	–	15	20	ns	
	Q Floating to Q High: T_{PZH}	–	–	20	ns	
Time Delay when $\overline{G}$ ↑	Q High to Q Floating: T_{PHZ}	–	15	20	ns	C_L = 5 PF R_L = 667Ω
	Q Low to Q Floating: T_{PLZ}	–	–	15	ns	

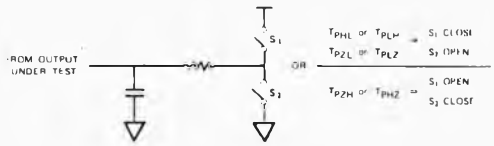
Note: The Parameter Symbol, Voltage Waveform and Measurement Information is Shown on the Next Page.

Parameter Measurement: (Conditions under V_{DD} = 5V, T_A = 25°C)

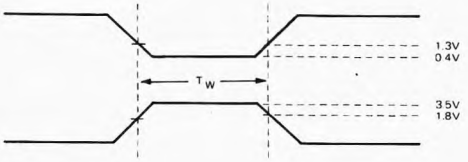
Totem Pole Outputs:



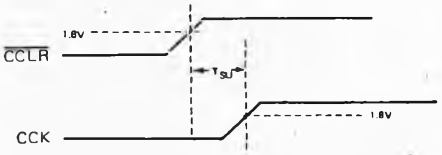
Tri-State Outputs: (QA ~ QH)



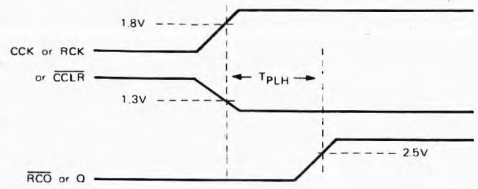
T_W:



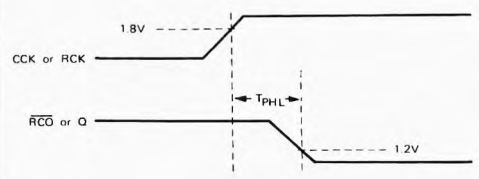
T_{SU}:



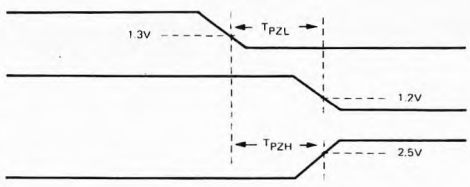
T_{PLH}:



T_{PHL}:



T_{PZL}, T_{PZH}: $\overline{G}$



T_{PHZ}, T_{PLZ}: $\overline{G}$