UMC

UM6845R/RA/RB

CRT Controller

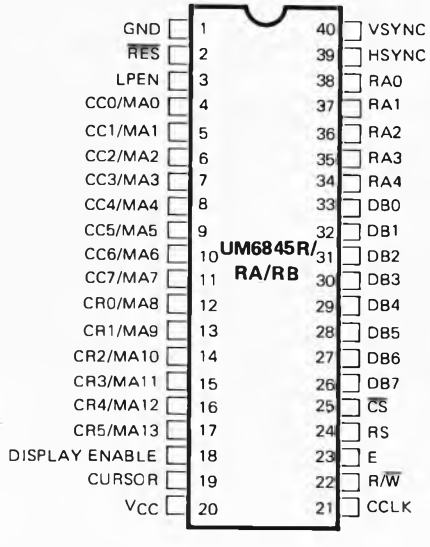
Features

- Single + 5 volt (±5%) power supply
- Alphanumeric and limited graphics capabilities
- Fully programmable display (rows, columns, blanking, etc.)
- Interlaced or non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- External light pen capability
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required
- Straight-binary addressing for Video Display RAM

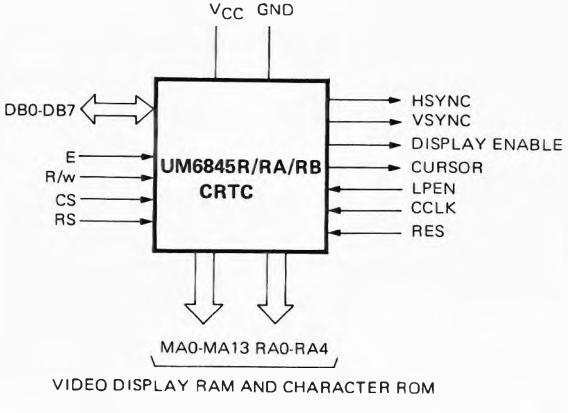
General Description

The UM6845R/RA/RB is a CRT Controller intended to provide capability for interfacing any microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} . . . . . −0.3V to + 7.0V
Input/Output Voltage, V_{IN} . . . . . −0.3V to + 7.0V
Operating Temperature, T_{OP} . . . . . 0°C to 70°C
Storage Temperature, T_{STG} . . . . . −55°C to 150°C
Notice:
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

*Comments

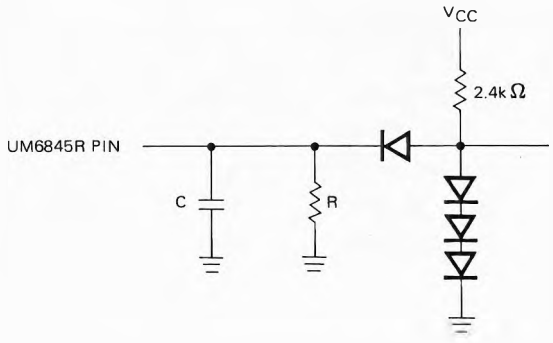
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0 − 70°C, unless otherwise noted)

Symbol	Characteristics	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	−0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	−10.0		+10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205 μA (DB0-DB7) I_{LOAD} = −100 μA (all others)	2.4		–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–		0.4	V
P_D	Power Dissipation	–	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–		10.0	pF

TEST LOAD

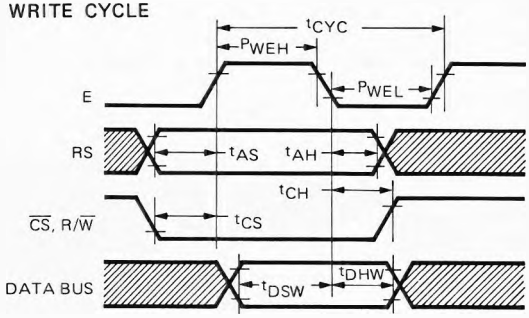


R = 11KΩ FOR DB0–DB7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130pF TOTAL FOR DB0–DB7
C = 30 pF ALL OTHER OUTPUTS

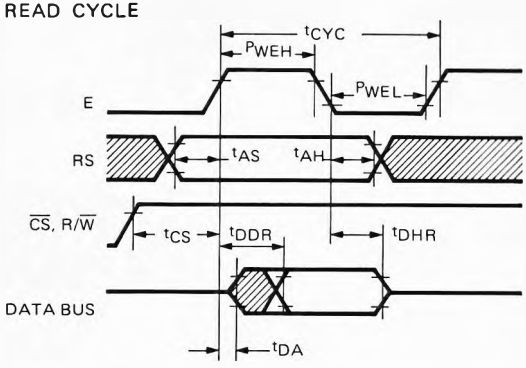
A. C. Characteristics

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{CH}	R/$\overline{W}$, $\overline{CS}$ Hold Time	0	–	0	–	0	–	ns
t_{DSW}	Data Bus Set-Up Time	165	–	60	–	60	–	ns
t_{DHW}	Data Bus Hold Time	10	–	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

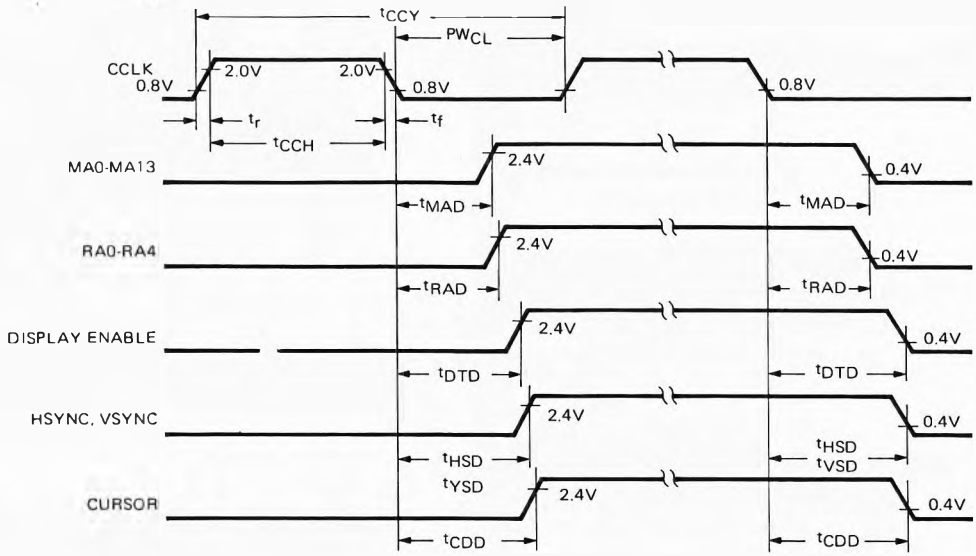
READ TIMING CHARACTERISTICS . (V_{CC} = 5.0V ± 5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	0.33	–	μs
P_{WEH}	E Pulse Width, High	440	–	200	–	150	–	ns
P_{WEL}	E Pulse Width, Low	420	–	190	–	140	–	ns
t_{AS}	Address Set-Up Time	80	–	40	–	30	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	–	40	–	30	–	ns
t_{DDR}	Read Access Time (Valid Data)	–	290	–	150	–	100	ns
t_{DHR}	Read Hold Time	20	60	20	60	20	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	40	–	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

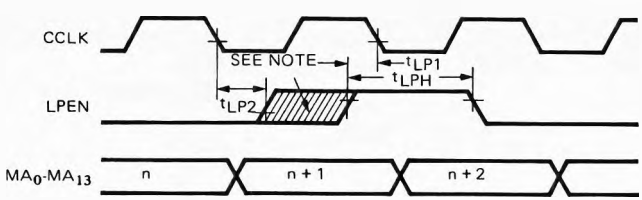
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



Symbol	Parameter	Min.	Typ.	Max.	Units
T_{CCH}	Minimum Clock Pulse Width, High	200			ns
T_{CCY}	Clock Frequency			2.5	MHz
T_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		160	300	ns
t_{VSD}	Vertical Sync Delay Time		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		160	300	ns

LIGHT PEN STROBE TIMING

NOTE:
"Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.



Symbol	Characteristics	UM6845R		UM6845RA		UM6845RB		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	–	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	–	120	–	120	–	120	ns
t_{LP2}	CCLK to LPEN Delay	–	0	–	0	–	0	ns

t_r and t_f = 20 ns (max.)

Pin Description

MPU INTERFACE SIGNAL DESCRIPTION

E (Enable)
The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the UM6845R/RA/RB. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the UM6845R/RA/RB to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6845R/RA/RB. A low on the R/$\overline{W}$ pin allows a write to the UM6845R/RA/RB.

$\overline{CS}$ (Chip Select)
The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The UM6845R/RA/RB is selected when $\overline{CS}$ is low.

RS (Register Select)
The Register Select input is used to access internal registers, A low on this pin permits writes into the Address Register and reads from the Status Register. The content of the Address Register is the identity of the register accessed when RS is high.

DB0–DB7 (Data Bus)
The DB0–DB7 pins are the eight data lines used for transfer of data between the processor and the UM6845R/RA/RB. These lines are bi-directional and are normally high-impedance except during read/write cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)
The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)
The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE
The DISPLAY ENABLE signal is an active-high output and is used to indicate when the UM6845R/RA/RB is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal.

CURSOR
The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthemore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable.

LPEN
The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK
The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$
The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When the $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. The $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when the $\overline{RES}$ goes high. In this way, the $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0–MA13 (Video Display RAM Address Lines)
These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

- **Binary Addressing**
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.

RA0-RA4 (Raster Address Lines)
These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

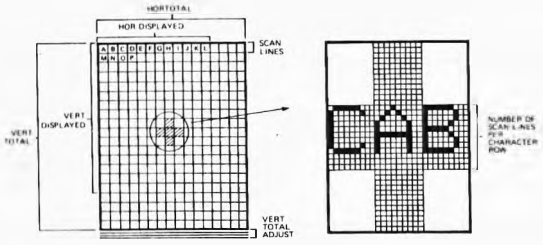


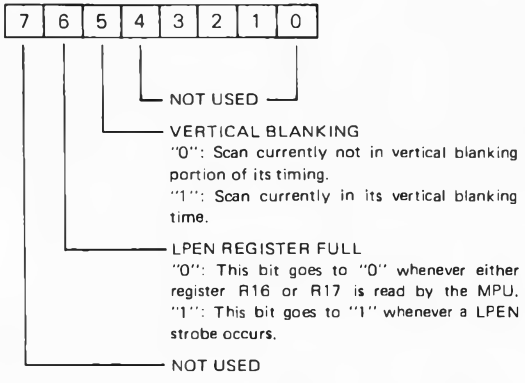
Figure 1. Video Display Format

Description of Internal Registers

Figure 1 illustrates the format of a typical video display and shows the functions of the various UM6845R/RA/RB internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address-selection and read/write capabilities.

Address Register
This is a 5-bit register which is used as a "pointer" to direct UM6845R/RA/RB data transfers to and from the system MPU using the number of the desired register (0-31). When RS is low, this register may be loaded; when RS is high, the register selected is the one whose identity is stored in this register.

Status Register
This 2-bit register is used to monitor the status of the CRTC, as follows:

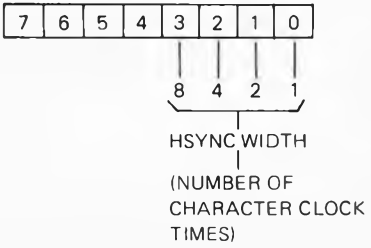


Horizontal Total (R0)
This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)
This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)
This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

Horizontal and Vertical SYNC Widths (R3)
This 4-bit register programs the width of HSYNC.



VSYNC width is set to 16 scan line times.

Vertical Total (R4)
The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronization.

Vertical Total Adjust (R5)
The Vertical Total Adjust Register is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)
This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text vertically.

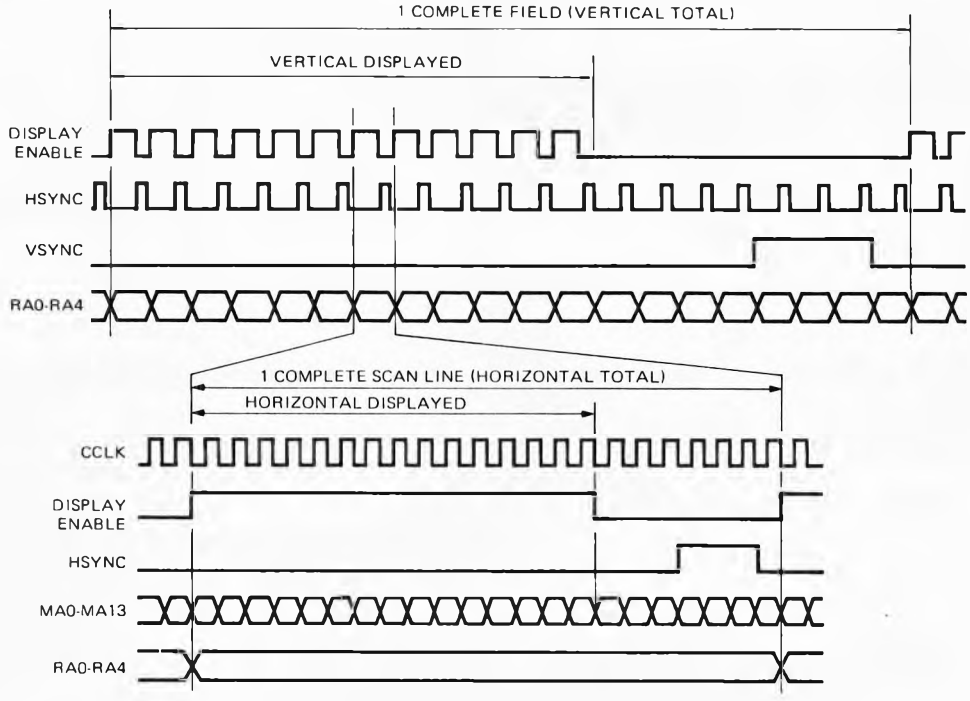
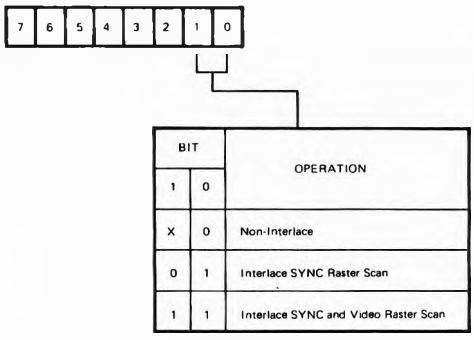


Figure 2. Vertical and Horizontal Timing

Mode Control (R8)

This register is used to select the operating modes of the UM6845R/RA/RB and is configured as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16 x field period
1	1	Blink at 32 x field period

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register containing the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 4). Subsequent memory addresses are generated by the UM6845R/RA/RB as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register containing the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, on the next negative-going edge of CCLK the contents of the internal scan counter are stored in registers R16 and R17.

CS	RS	Address Reg.					Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit.							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√			L	V_s					
0	1	0	0	0	0	0	R0	Horiz. Total	#Charac, -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	#Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	#Scan Lines and #Char. Times		√					H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	#Char. Rows -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert, Total Adjust	#Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert, Displayed	#Char. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	#Char Rows.		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√							I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	#Scan Lines-1		√					●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●

Notes: ● Designates binary bit

▨ Designates unused bit. These bits are always "0", except for $\overline{CS}$ = 1, which does not drive the data bus at all.

Figure 3. Internal Register Summary

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Starting Address = 0) for 80 x 24 Example

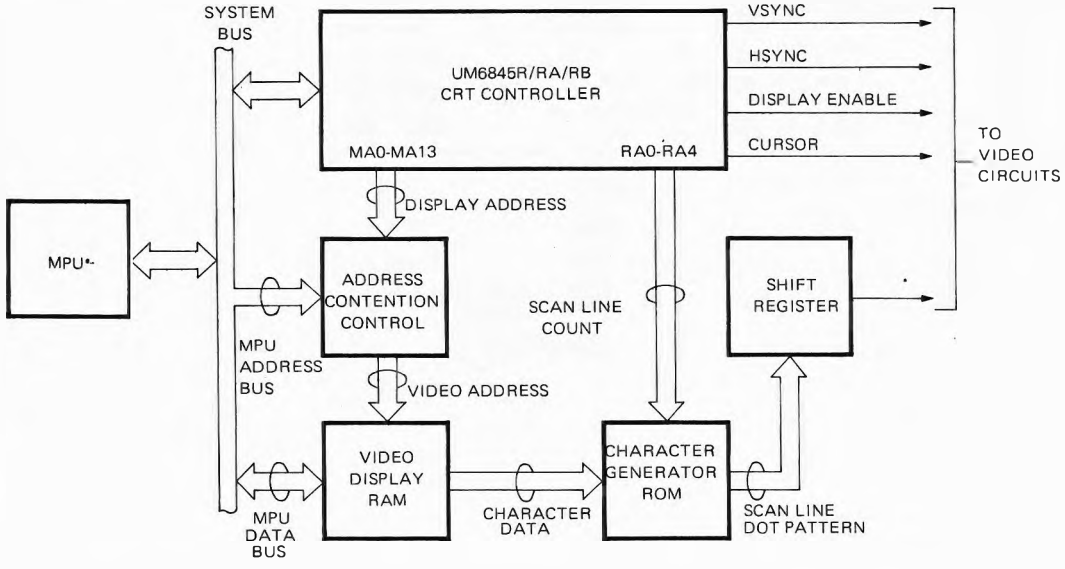


Figure 5. Shared Memory System Configuration

Memory Contention Schemes for Shared Memory Addressing

From Figure 5, it is clear that both the UM6845R/RA/RB and the system MPU must be capable of addressing the video display memory. The UM6845R/RA/RB repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. There are three ways of resolving this dual contention:

MPU PRIORITY

With this method, the address lines to the video display memory are normally driven by the UM6845R/RA/RB unless the MPU needs access, in which case the MPU addresses immediately override those from the UM6845R/RA/RB and the MPU has immediate access.

$\phi 1/\phi 2$ MEMORY INTERLEAVING

This method permits both the UM6845R/RA/RB and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the UM6845R/RA/RB address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the UM6845R/RA/RB and the MPU have periods of unimpeded access to the memory. Figure 6 illustrates the timings.

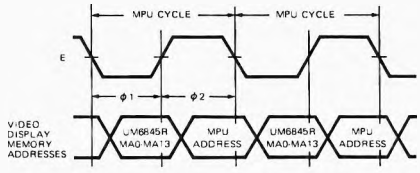


Figure 6. $\phi 1/\phi 2$ Interleaving

INTERLACED MODES

There are three raster-scan display modes (see Figure 7).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlaced Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 8 and is the only difference in the UM6845R/RA/RB operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlaced Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

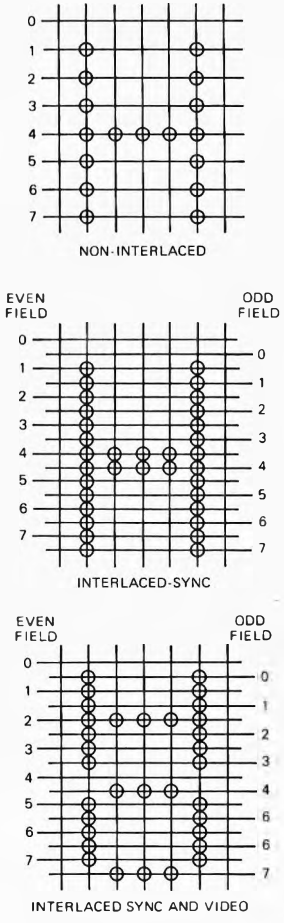


Figure 7. Comparison of Display Modes

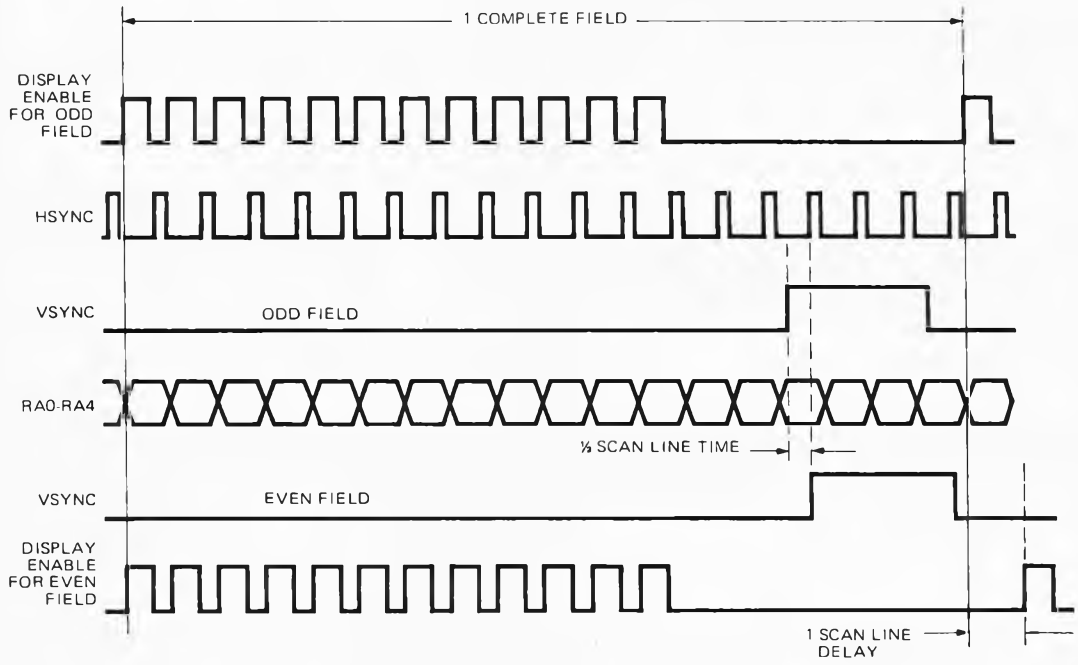


Figure 8. Interlaced Sync Mode and Interlaced Sync & Video Mode Timing

CRTC Register Comparison Table

NON-INTERLACED

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1	Total-1	Total-1	Total-1
R1 Hdisp	Actual	Actual	Actual	Actual
R2 Hsync	Actual	Actual	Actual	Actual
R3 Sync Width	Horizontal (& Vertical *1)	Horizontal	Horizontal & Vertical	Horizontal & Vertical
R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R5 Vtotal Adjustment	Any Value	Any Value	Any Value	Any Value
R6 Vdisp	Any Value <R4	Any Value <R4	Any Value <R4	Any Value <R4
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R8 B0-1	Interlace	Interlace	Interlace	Interlace
Mode Select B2	–	–	–	Row/Column or Binary Addr.
B3	–	–	–	Shared or Transparent Addr.
B4	(Display Enable Skew *1)	–	Display Enable Skew	Display Enable Skew
B5	(Display Enable Skew *1)	–	Display Enable Skew	Cursor Skew
B6	(Cursor Skew *1)	–	Cursor Skew	RA4/
B7	(Cursor Skew *1)	–	Cursor Skew	Transparent
R9 Scan Lines	Total-1	Total-1	Total-1	Total-1
R10 Cursor Start	Actual	Actual	Actual	Actual
R11 Cursor End	Actual	Actual	Actual	Actual
R12/R13 Display Addr.	Write-only Read/Write (MC6845 & *1)	Read/Write	Read/Write	Write-only
R14/R15 Cursor Position	Read/Write	Read/Write	Read/Write	Read/Write
R16/R17 Position	Read-only	Read-only	Read-only	Read-only
R18/R19 Update Addr. Register	N/A	N/A	N/A	Transparent Mode Only
R31 Dummy Register	N/A	N/A	N/A	Transparent Mode Only
Status Register	Yes (UM6845R)	No	No	Yes

CRTC Register Comparison Table (Continued)

INTERLACED SYNC

Register	UM6845R/RA/RB MC6845 MC6845*1	MC6845R HD6845R	UM6845/A/B HD6845S	UM6845E/EA/EB
R0 Htotal	Total-1 = Odd or Even	Total-1 = Odd	Total-1 = Odd	Total-1 = Odd or Even

INTERLACED SYNC AND VIDEO

R4 Vtotal	Total-1	Total-1	Total-1	Total-1
R6 Vdisp	Total	Total/2	Total	Total
R7 Vsync	Actual-1	Actual-1	Actual-1	Actual-1
R9 Scan Lines	Total-1 Odd/Even	Total-1 Only Even	Total-1 Odd/Even	Total-1 Odd/Even
R10 Cursor Start	Odd/Even	Both Odd	Odd/Even	Odd/Even
R11 Cursor End	Odd/Even	Both Even	Odd/Even	Odd/Even
I_{CCLK}	2.5 MHz	2.5 MHz	3.7 MHz	3.7 MHz

Ordering Information

Part Number	CPU Clock Rate	Package
UM6845R	1 MHz	40L DIP
UM6845RA	2 MHz	40L DIP
UM6845RB	3 MHz	40L DIP