UM6551

Asynchronous Communication Interface Adapter (ACIA)

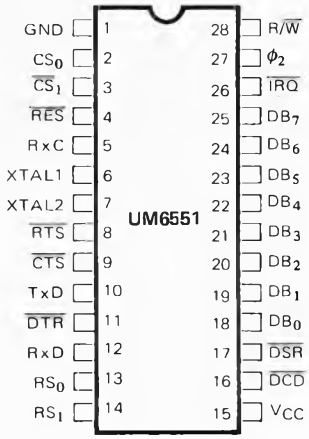
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud)
- Programmable interrupt and status register to simplify software design
- Single +5 volt power supply
- Serial echo mode
- False start bit detection
- 8-bit, bi-directional data bus for direct communication with the microprocessor
- External 16x clock input for non-standard baud rates (up to 125k baud)
- Programmable: word lengths; number of stop bits; parity bit generation and detection
- Data set and modem control signals provided
- Parity: (odd, even, none, mark, space)
- Full-duplex or half-duplex operation
- 5, 6, 7, 8, and 9 bit transmission

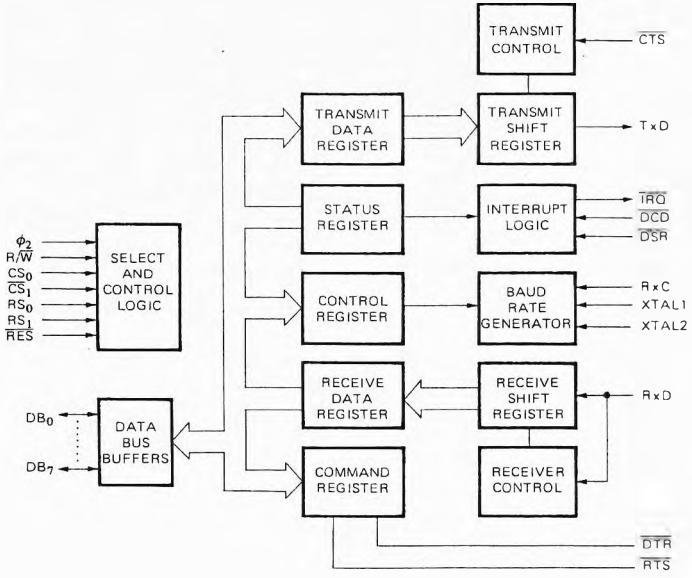
General Description

The UM6551 is an Asynchronous Communication Adapter (ACIA) intended for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud-rate generator, with a crystal being the only external component required.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage ..... −0.3V to +7.0V
Input/Output Voltage ..... −0.3V to +7.0V
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −55°C to 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0−70°C, unless otherwise noted)

Characteristics	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	−100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0-DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance (ϕ2)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL 1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	170	300	mW

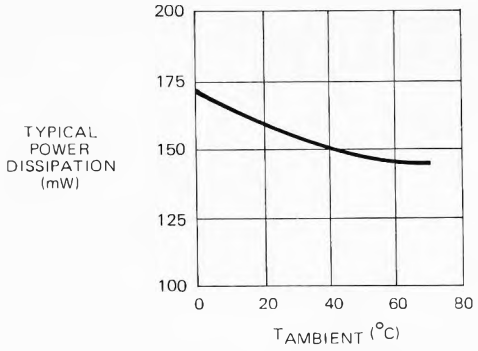


Figure 1. Power Dissipation vs. Temperature

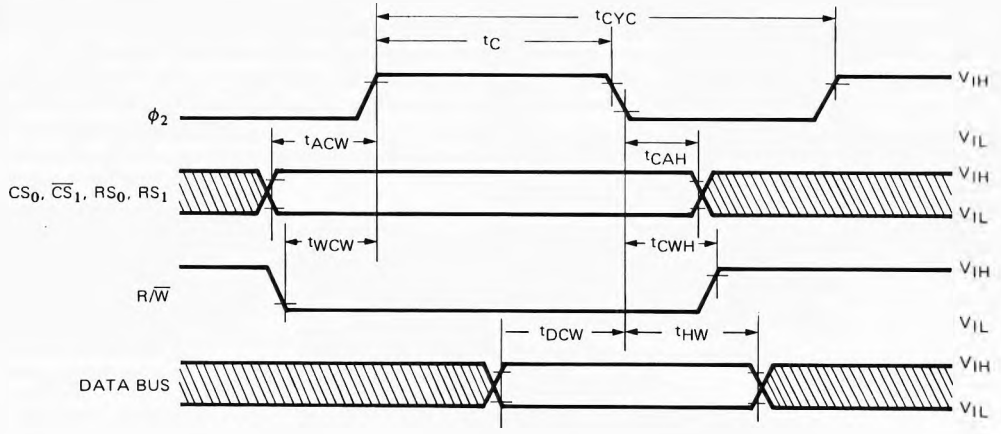


Figure 2. "Write" Timing Characteristics

Write Cycle

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	UM6551		UM6551A		Units
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
φ2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

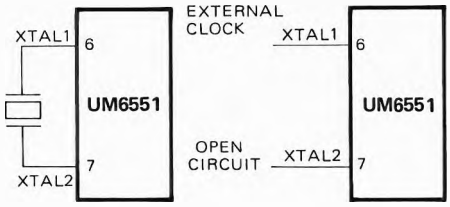
(t_r and t_f = 10 to 30 ns)

Crystal Specification

1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (±%) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level mW 2
   f. Shunt capacitance pF 7 max.
   g. Oscillation mode Fundamental

No external components should be in the crystal circuit

Clock Generation



INTERNAL CLOCK EXTERNAL CLOCK

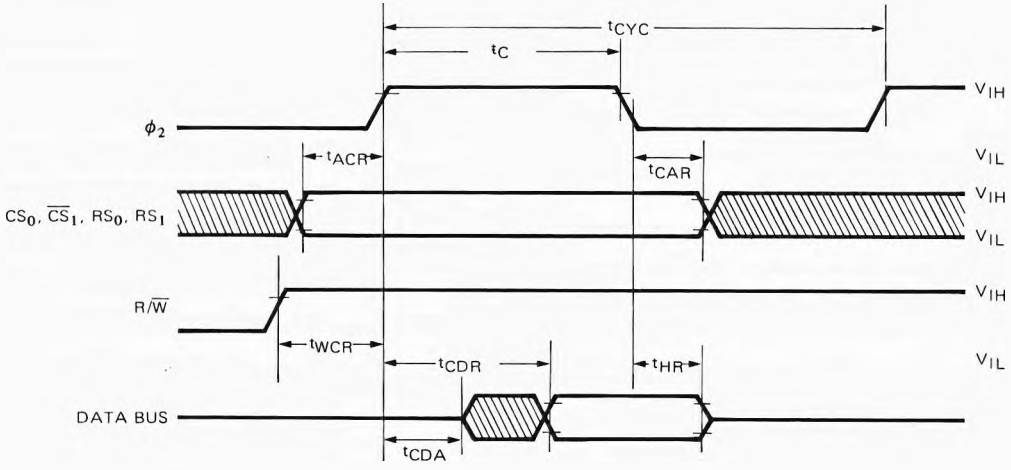


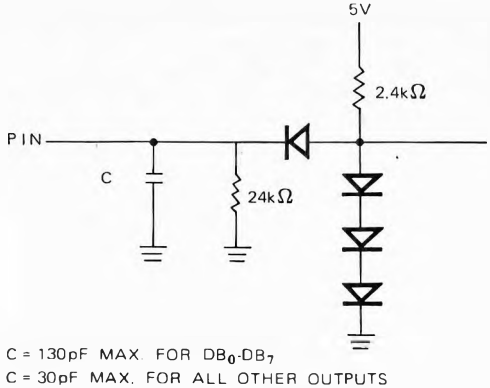
Figure 3. "Read" Timing Characteristics

Read Cycle

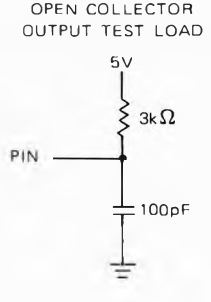
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	UM6551		UM6551A		Units
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (φ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/W Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

Test Load



C = 130pF MAX. FOR DB_0-DB_7
C = 30pF MAX. FOR ALL OTHER OUTPUTS



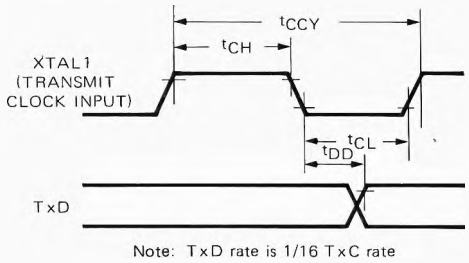


Figure 4a. "Transmit" Timing with External Clock

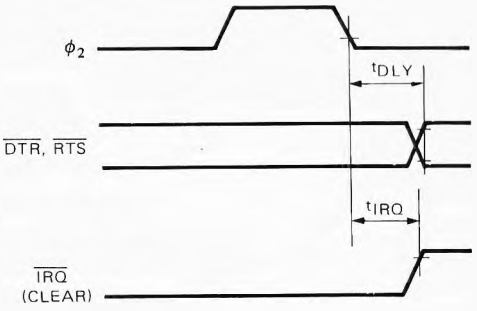


Figure 4b. "Interrupt" and "Output' Timing

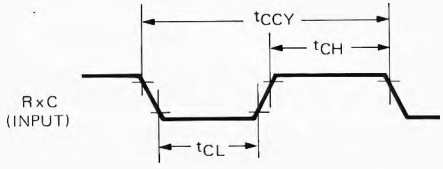


Figure 4c. "Receive" External Clock Timing

Transmit/Receive Characteristics

Characteristics	Symbol	UM6551		UM6551A		Unit
		Min.	Max.	Min.	Max.	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTAL 1 to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

(t_r, t_f = 10 to 30 ns input clocks only)

* The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization, a low on the $\overline{RES}$ input will cause internal registers to be cleared.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfer between the system microprocessor and the UM6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfer. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the UM6551. A low on the R/$\overline{W}$ pin allows a write to the UM6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an "open drain" output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Date Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the UM6551. These lines are bi-directional and are normally high-impedance, except during Read cycles, when selected.

CS_0, CS_1 (Chip Selects)

The two "chip select" inputs are normally connected to the processor address lines either directly or through decoders. The UM6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects)

The two "register select" lines are normally connected to the "processor address" lines to allow the processor to select the various UM6551 internal registers. The following table indicates the internal "register select" coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Register Select Coding

The table shows that only the "Command" and "Control" registers are read/write. The "Programmed Reset" operation does not cause a data transfer, but is used to clear the UM6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$). These differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin; in which case, the XTAL2 pin must "float".

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receive 16x clock input or the receive 16x clock output. The latter mode results if the internal baud rate generator is selected for receive data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

DTR (Data Terminal Ready)

This output pin is used to indicate the status of the UM6551 to the modem. A low on $\overline{DTR}$ indicates the UM6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate the status of the modem to the UM6551. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input and must not be a "no-connect". If unused, it should be driven high or low, but not switched.

Note: if Command Register Bit 0 = "1", and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either "Transmit" or "Receive" operations.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate the status of the carrier detect output of the modem to the UM6551. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a "no-connect".

Note: If Command Register Bit 0 = "1", and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect "Transmit" operation, but must be low for the "Receive" to operate.

Internal Organization

The Transmitter/Receiver sections of the UM6551 are depicted by the block diagram in Figure 5.

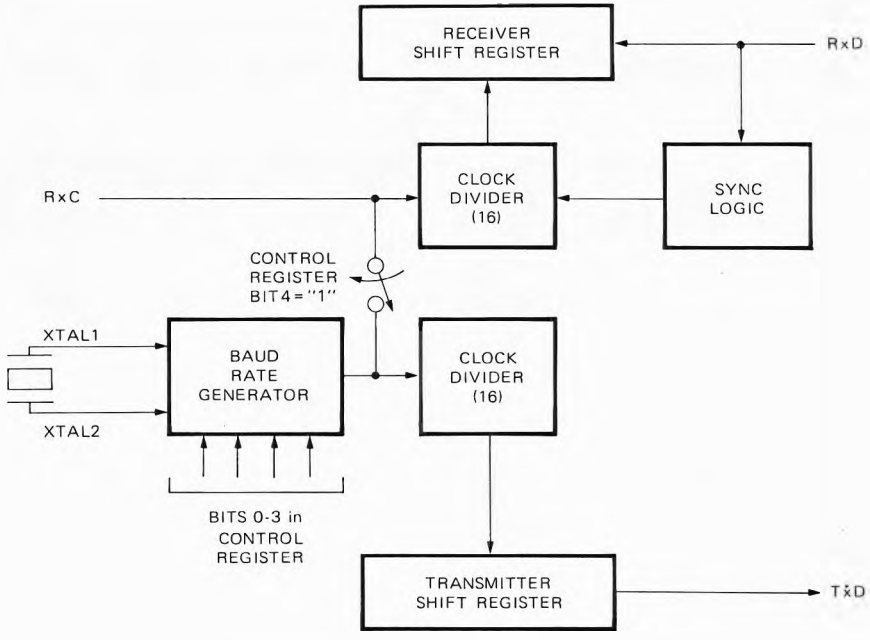


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then R x C becomes an output pin and can be used to slave other circuits to the UM6551.

Control Register

The Control Register is used to select the desired mode for the UM6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

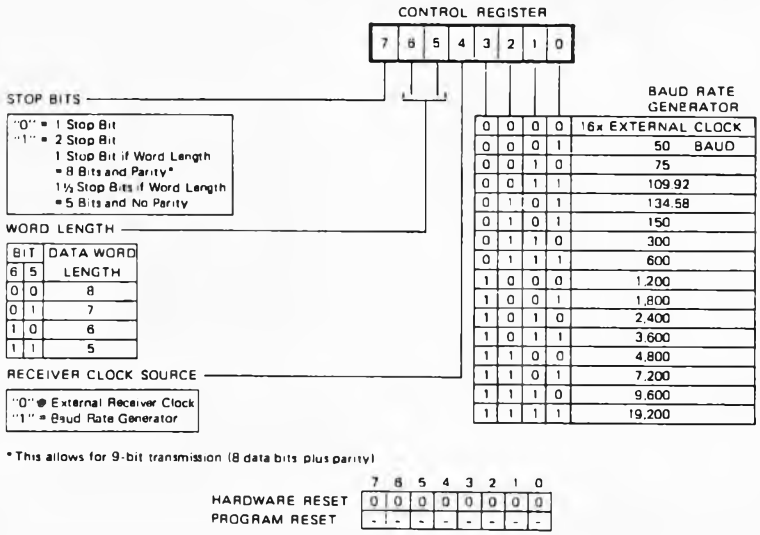


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

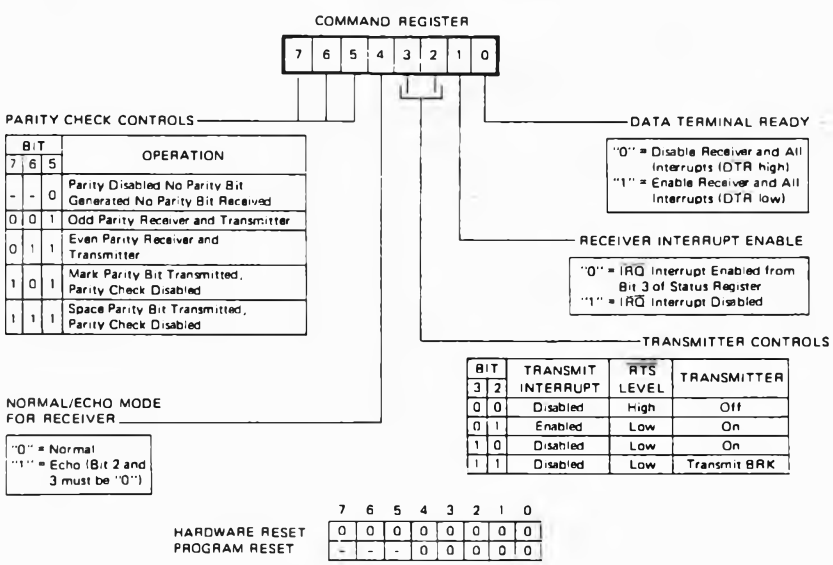


Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various UM6551 functions and is outlined in Figure 8.

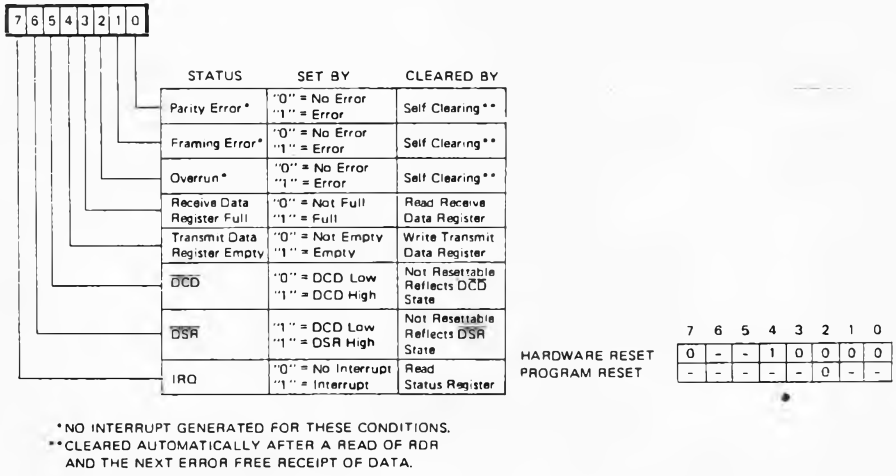


Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the UM6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receiver Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

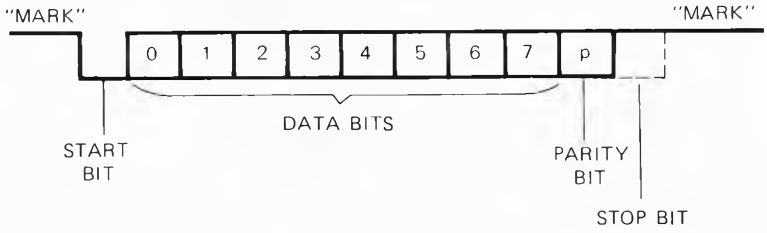


Figure 9. Serial Data Stream Example

Ordering Information

Part Number	Clock Rate	Package
UM6551	1 MHz	28L DIP
UM6551A	2 MHz	28L DIP