

# 205-187

# UMC



## UM6264 Series

### 8K x 8 CMOS SRAM

um 6264-121

#### Features

- Single +5 volt power supply
- Access times: 70/100/120 ns (max.)
- Current:
  - Standard version: Operating: 90 mA (max.)  
Standby: 2 mA (max.)
  - Low power version: Operating: 90 mA (max.)  
Standby: 100  $\mu$ A (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible. All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip select inputs for easy application
- Data retention voltage: 2V (min) for low power version
- UM6264-70/10/12 is the standard version
- UM6264-70L/10L/12L is the low power version
- UM6264-70T/10T/12T is the wide temperature version
- UM6264-70LT/10LT/12LT is the low power, wide temperature version
- Available in 28 pin DIP, SOP, or Skinny DIP packages (See ordering information page 9)

#### General Description

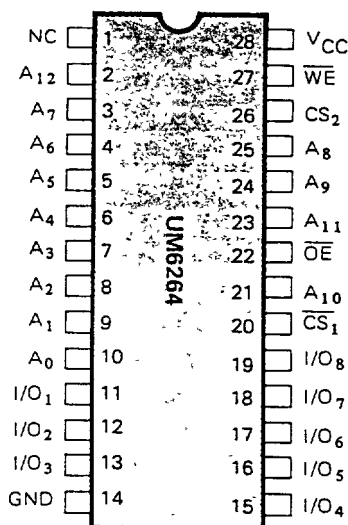
The UM6264 is a high-speed, low-power 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates on a single 5-volt power supply. It is built using UMC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

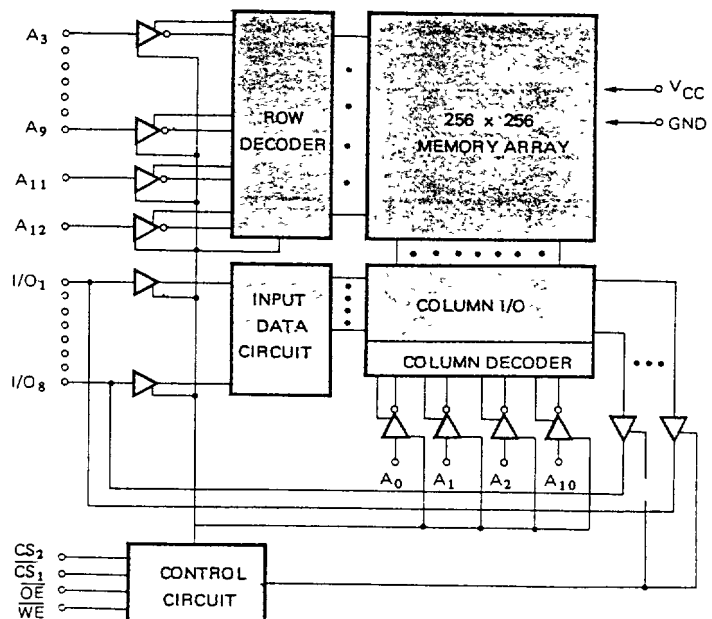
Two chip select inputs are provided for power down and device select, and an output enable input is included for easy interface.

Data retention is guaranteed at a power supply voltage as low as 2V for the low power version

#### Pin Configuration



#### Block Diagram



**Pin Description**

Designation	Description
$A_0 \sim A_{12}$	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}_1$	Chip Select
$CS_2$	Chip Select
NC	No Connection
$I/O_1 \sim I/O_8$	Data Input/Output
$V_{CC}$	Power Supply (+5V)
GND	Ground

**Absolute Maximum Ratings \***

$V_{CC}$  to GND . . . . . -0.5V to +7.0V  
 IN, IN/OUT Volt to GND . . . . . -0.5V to  $V_{CC} + 0.5V$   
 Operating Temperature,  $T_{opr}$  . . . . .  $0^\circ C$  to  $+70^\circ C$  (Note 1)  
 Storage Temperature,  $T_{stg}$  . . . . .  $-55^\circ C$  to  $+125^\circ C$   
 Temperature Under Bias,  $T_{bias}$  . . . . .  $-10^\circ C$  to  $+85^\circ C$  (Note 1)  
 Power Dissipation,  $P_T$  . . . . . 1.0W/SOP 0.7W  
 Soldering temp. & time . . . . .  $260^\circ C$ , 10 sec  
 Note 1. for UM6264-70T/10T/12T, UM6264-70LT/10LT/12LT. ( $T_{opr}$ :  $-40^\circ C$  to  $85^\circ C$ ;  $T_{bias}$ :  $-50^\circ C$  to  $95^\circ C$ )

**Recommended DC Operating Conditions**

$(T_A = 0^\circ C$  to  $70^\circ C$  for UM6264-70/10/12, UM6264-70L/10L/12L,  $T_A = -40^\circ C$  to  $85^\circ C$  for UM6264-70T/10T/12T, UM6264-70LT/10LT/12LT)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
$V_{IH}$	Input High Voltage	2.2	3.5	$V_{CC} + 0.5V$	V
$V_{IL}$	Input Low Voltage	-0.3	0	+0.8	V
$C_L$	Output Load	-	-	100	pF
TTL	Output Load	-	-	1	-

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics**

$(T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5V \pm 10\%$ , GND = 0V,  
 $T_A = -40^\circ C$  to  $85^\circ C$  for T and LT versions)

Symbol	Parameter	UM6264-70/10/12/70T/10T/12T		UM6264-70L/10L/12L/70LT/10LT/12LT		Unit	Conditions
		Min.	Max.	Min.	Max.		
$ I_{LI} $	Input Leakage Current	-	2	-	2	$\mu A$	$V_{IN} = GND$ to $V_{CC}$
$ I_{LO} $	Output Leakage Current	-	2	-	2	$\mu A$	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = GND$ to $V_{CC}$
$I_{CC}$	Active Power Supply Current	-	90	-	90	mA	$\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ $I_{I/O} = 0$ mA
$I_{CC1}$	Dynamic Operating Current	-	90	-	90	mA	Min. Cycle, Duty = 100% $\overline{CS}_1 = V_{IL}$ , $CS_2 = V_{IH}$ $I_{I/O} = 0$ mA
$I_{SB}$	Standby Power Supply Current	-	5	-	3	mA	$\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$
$I_{SB1}$		-	2	-	0.1	mA	$CS_1 \geq V_{CC} - 0.2V$ , $CS_2 \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
$I_{SB2}$		-	2	-	0.1	mA	$CS_1 \leq 0.2V$ , $CS_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ , or $V_{IN} \leq 0.2V$
$V_{OL}$	Output Low Voltage	-	0.4	-	0.4	V	$I_{OL} = 4$ mA
$V_{OH}$	Output High Voltage	2.4	-	2.4	-	V	$I_{OH} = -1.0$ mA

**Truth Table**

Mode	$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O Operation	$V_{CC}$ Current
Standby	H	X	X	X	High Z	$I_{SB}, I_{SB1}$
	X	L	X	X	High Z	$I_{SB}, I_{SB2}$
Output Disabled	L	H	H	H	High Z	$I_{CC}, I_{CC1}$
Read	L	H	L	H	$D_{OUT}$	$I_{CC}, I_{CC1}$
Write	L	H	X	L	$D_{IN}$	$I_{CC}, I_{CC1}$

Note X = H or L

**Capacitance** ( $I_A = 25^\circ C, f = 10 \text{ MHz}$ )

Symbol	Parameter	Min.	Max.	Unit	Conditions
$C_{IN}^*$	Input Capacitance		6	pF	$V_{IN} = 0V$
$C_{I/O}^*$	Input/Output Capacitance		8	pF	$V_{I/O} = 0V$

\* This parameter is sampled and not 100% tested

**AC Characteristics** ( $V_{CC} = 5V \pm 10\%, T_A = 0^\circ$  to  $+70^\circ C$  for UM6264-70/10/12, UM6264-70L/10L/12L  
 $T_A = -40^\circ C$  to  $85^\circ C$  for UM6264-70T/10T/12T, UM6264-70LT/10LT/12LT)

Symbol	Parameter	UM6264-70/70L 70T/70LT		UM6264-10/10L 10T/10LT		UM6264-12/12L 12T/12LT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	

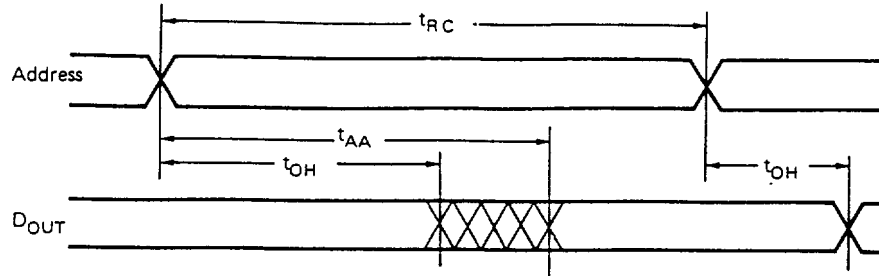
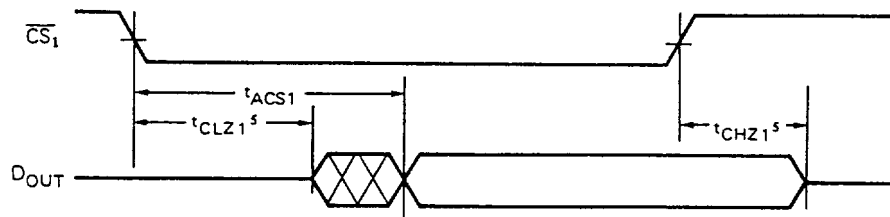
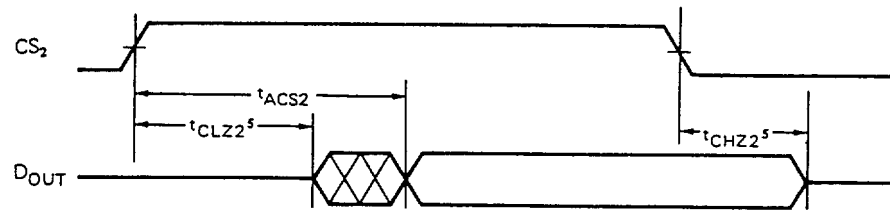
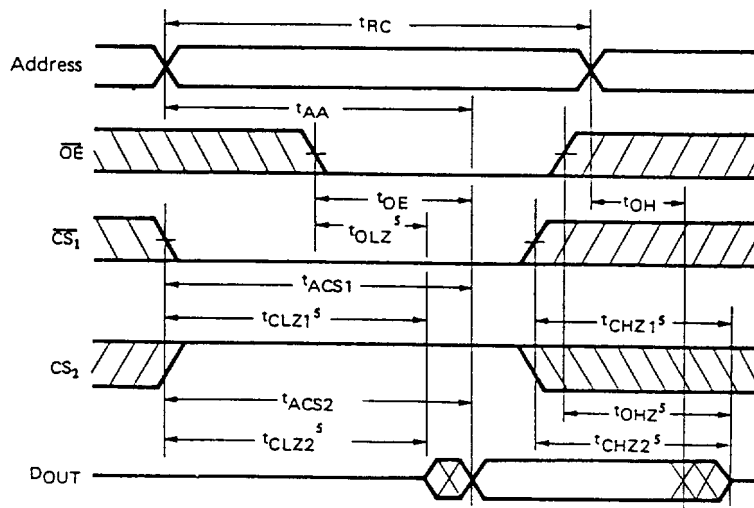
**Read Cycle**

$t_{RC}$	Read Cycle Time	70	—	100	—	120	—	ns
$t_{AA}$	Address Access Time	—	70	—	100	—	120	ns
$t_{ACS1}$	Chip Select Access Time	$CS_1$	—	70	—	100	—	120
$t_{ACS2}$		$CS_2$	—	70	—	100	—	120
$t_{OE}$	Output Enable to Output Valid	—	35	—	50	—	60	ns
$t_{CLZ1}$	Chip Selection to Output in Low Z	$CS_1$	10	—	10	—	10	ns
$t_{CLZ2}$		$CS_2$	10	—	10	—	10	ns
$t_{OLZ}$	Output Enable to Output in Low Z	5	—	5	—	5	—	ns
$t_{CHZ1}$	Chip Deselection to Output in High Z	$CS_1$	0	35	0	35	0	40
$t_{CHZ2}$		$CS_2$	0	35	0	35	0	40
$t_{OHZ}$	Output Disable to Output in High Z	0	30	0	35	0	40	ns
$t_{OH}$	Output Hold from Address Change	10	—	10	—	10	—	ns

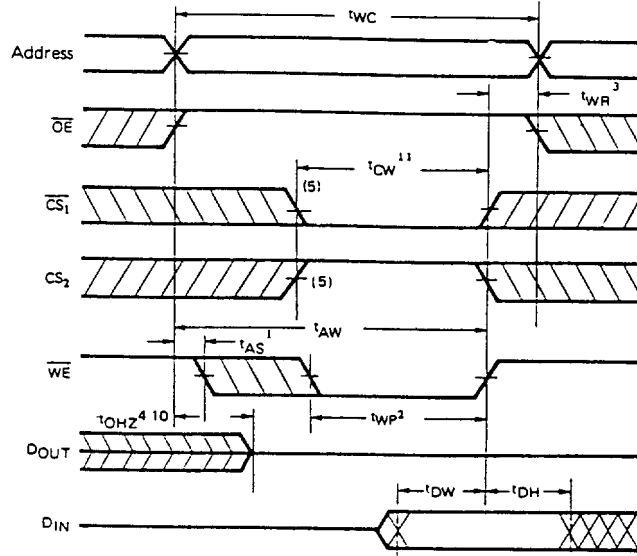
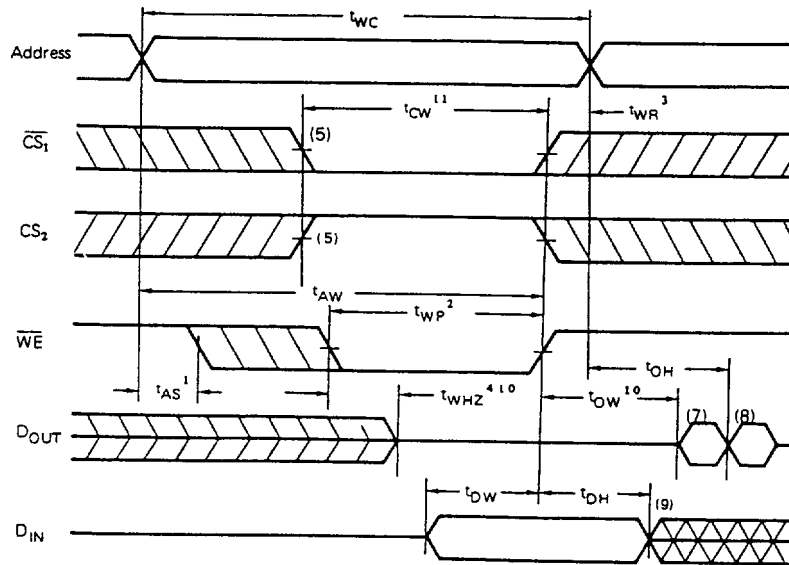
**Write Cycle**

$t_{WC}$	Write Cycle Time	70	—	100	—	120	—	ns
$t_{CW}$	Chip Selection to End of Write	60	—	80	—	85	—	ns
$t_{AS}$	Address Set-up Time	0	—	0	—	0	—	ns
$t_{AW}$	Address Valid to End of Write	60	—	80	—	85	—	ns
$t_{WP}$	Write Pulse Width	50	—	60	—	70	—	ns
$t_{WR}$	Write Recovery Time	0	—	0	—	0	—	ns
$t_{WHZ}$	Write to Output in High Z	0	30	0	35	0	40	ns
$t_{DW}$	Data to Write Time Overlap	30	—	40	—	50	—	ns
$t_{DH}$	Data Hold from Write Time	0	—	0	—	0	—	ns
$t_{OHZ}$	Output Disable to Output in High Z	0	30	0	35	0	40	ns
$t_{OW}$	Output Active from End of Write	5	—	10	—	10	—	ns

Notes  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels

**Timing Waveforms (Continued)**
**Read Cycle 1<sup>(1,2,4)</sup>**

**Read Cycle 2<sup>(1,3,4,6)</sup>**

**Read Cycle 3<sup>(1,4,7,8)</sup>**

**Read Cycle 4<sup>(1)</sup>**


- Notes.
1.  $\overline{WE}$  is high for READ cycle.
  2. Device is continuously selected  $\overline{CS}_1 = V_{IL}$  and  $CS_2 = V_{IH}$ .
  3. Address valid prior to or coincident with  $\overline{CS}_1$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.
  6.  $CS_2$  is high.
  7.  $\overline{CS}_1$  is low.
  8. Address valid prior to or coincident with  $CS_2$  transition high

**Timing Waveforms (Continued)**
**Write Cycle 1**

**Write Cycle 2<sup>(6)</sup>**


- Notes
- $t_{AS}$  is measured from the address valid to the beginning of write
  - A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS_1}$ , a high  $CS_2$  and a low  $\overline{WE}$ .
  - $t_{WR}$  is measured from the earliest of  $\overline{CS_1}$  or  $\overline{WE}$  going high or  $CS_2$  going low to the end of write cycle.
  - During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  - If the  $\overline{CS_1}$  low transition or the  $CS_2$  high transition occur simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  - $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ )
  - $D_{OUT}$  is the same phase of write data of this write cycle.
  - $D_{OUT}$  is the read data of next address.
  - If  $\overline{CS_1}$  is low and  $CS_2$  is high during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to I/O pins
  - Transition is measured  $\pm 500mV$  from steady state. This parameter is sampled and not 100% tested
  - $t_{CW}$  is measured from the later of  $\overline{CS_1}$  going low or  $CS_2$  going high to the end of write.

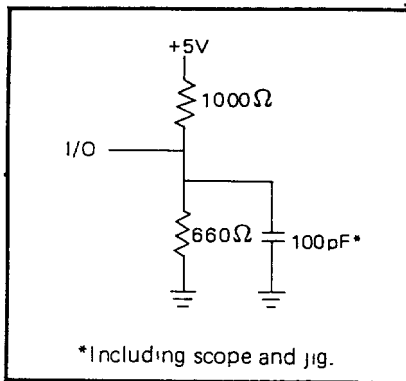
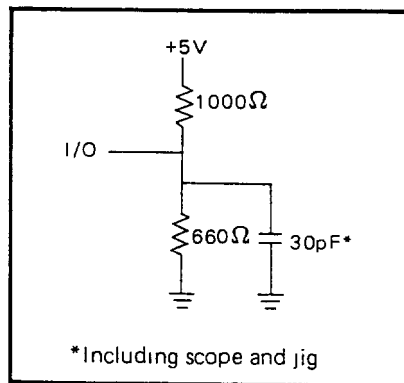
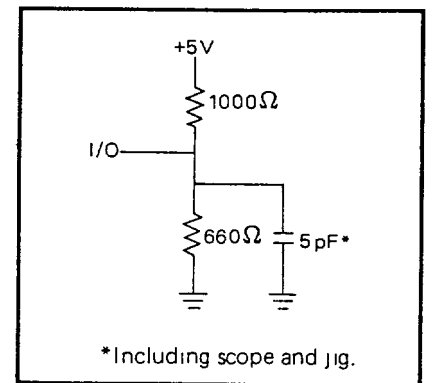
**AC Test Conditions**

For Access Time: 70ns

For Access Times: 100/120 ns

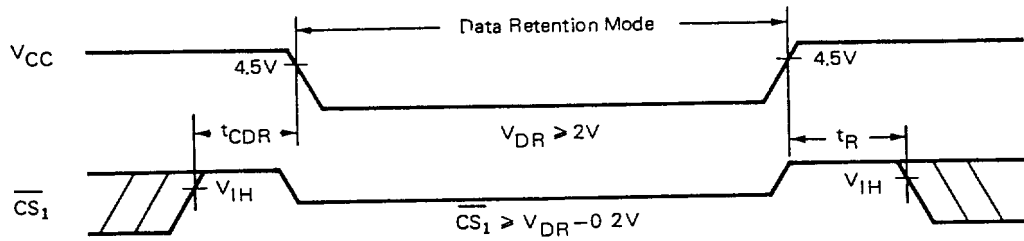
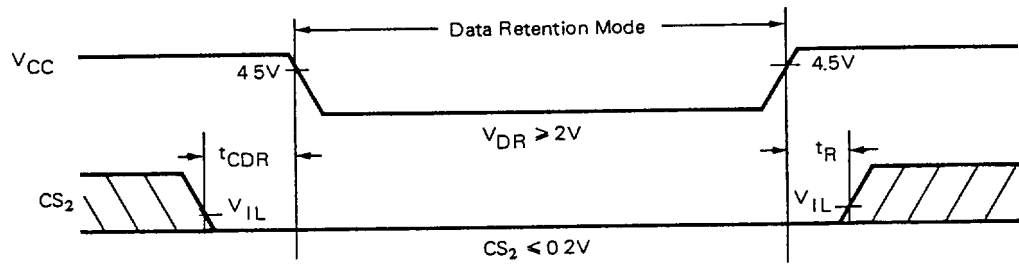
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 2, 3

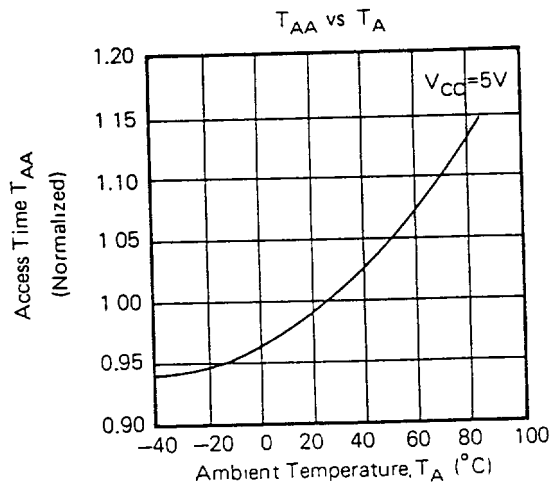
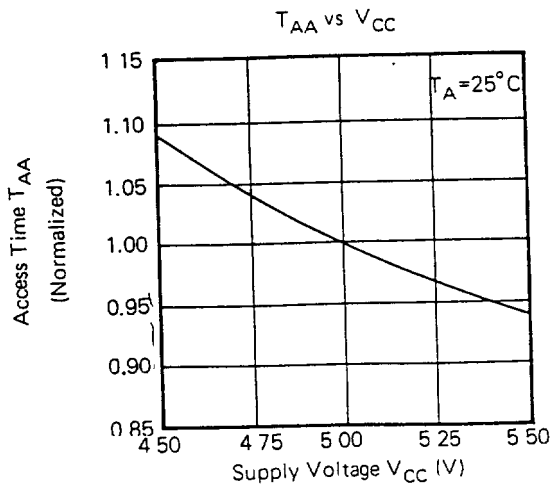
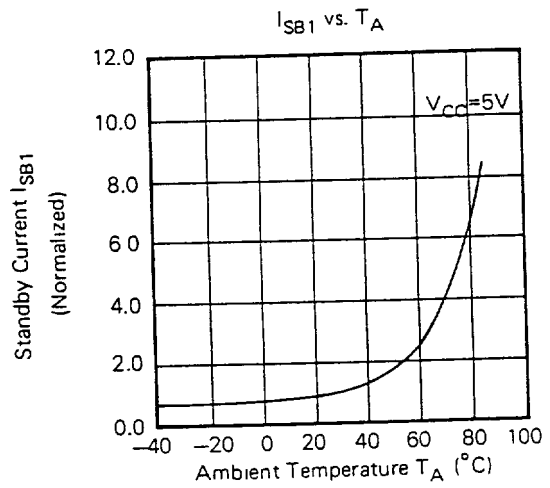
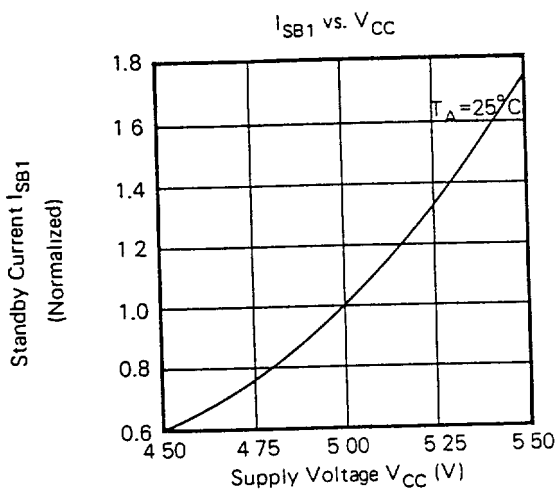
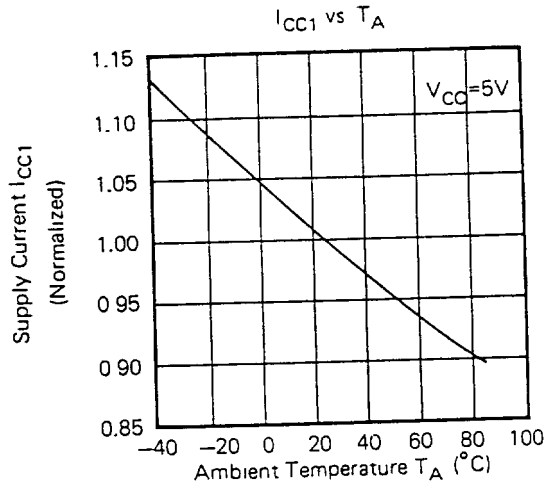
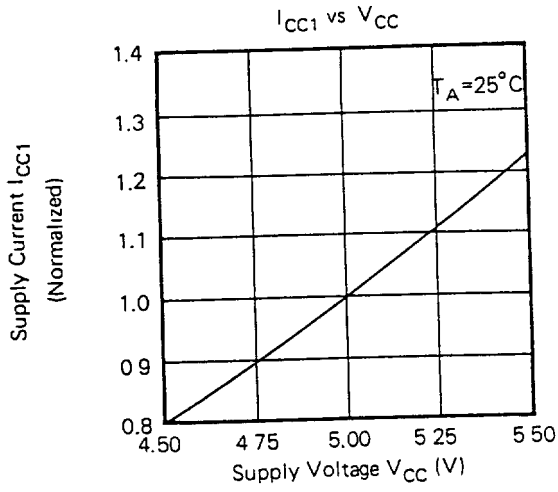
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 3


**Figure 1. Output Load**

**Figure 2. Output Load**

**Figure 3. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** (L version only,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for UM6264-70L/10L/12L;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  for UM6264-70LT/10LT/12LT)

Symbol	Parameter	Min.	Max.	Unit	Conditions
$V_{DR1}$	$V_{CC}$ for Data Retention	2.0	5.5	V	$\overline{CS}_1 \geq V_{CC} - 0.2V$ , $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
$V_{DR2}$		2.0	5.5	V	$CS_2 \leq 0.2V$
$I_{CCDR1}$	Data Retention Current	—	50	$\mu\text{A}$	$V_{CC} = 3.0V$ , $\overline{CS}_1 \geq V_{CC} - 0.2V$ $CS_2 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
$I_{CCDR2}$		—	50	$\mu\text{A}$	$V_{CC} = 3.0V$ , $CS_2 \leq 0.2V$ , $\overline{CS}_1 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
$t_{CDR}$	Chip Deselect to Data Retention Time	0	—	ns	See Retention Waveform
$t_R$	Operation Recovery Time	$t_{RC}^*$	—	ns	

 \* $t_{RC}$  = Read Cycle Time

**Low  $V_{CC}$  Data Retention Waveform (1) ( $\overline{CS}_1$  Controlled)**

**Low  $V_{CC}$  Data Retention Waveform (2) ( $CS_2$  Controlled)**


**Characteristic Curves**


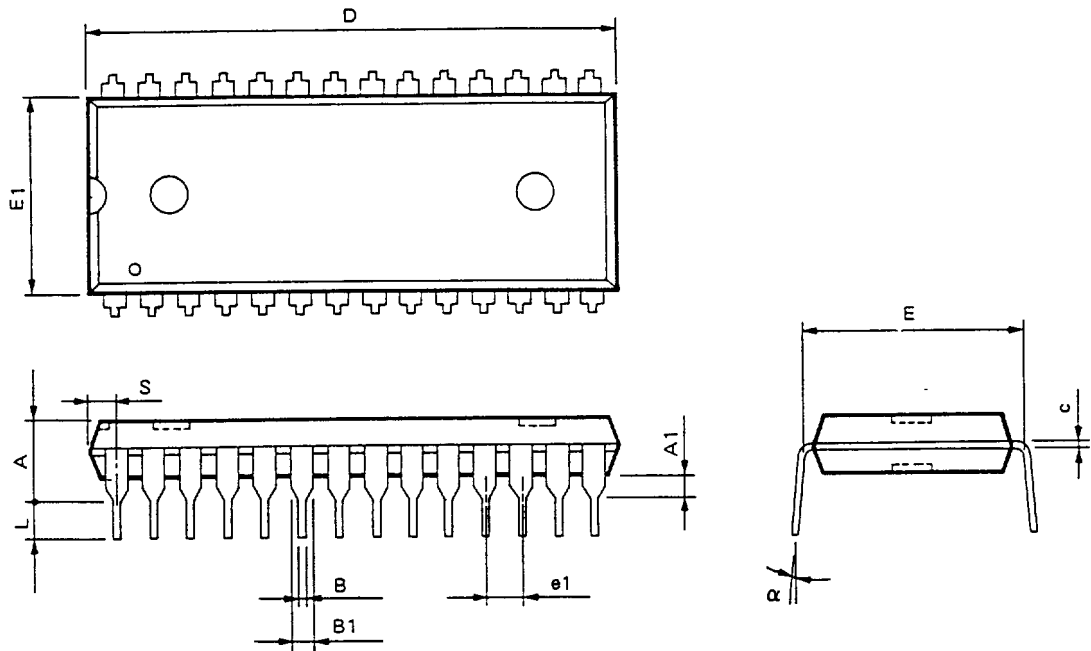


**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Temperature Range	Package
UM6264-70	70	90	2	0°C to 70°C	28L DIP
UM6264-70L		90	0.1	0°C to 70°C	28L DIP
UM6264-70T		90	2	-40°C to 85°C	28L DIP
UM6264-70LT		90	0.1	-40°C to 85°C	28L DIP
UM6264M-70		90	2	0°C to 70°C	28L SOP
UM6264M-70L		90	0.1	0°C to 70°C	28L SOP
UM6264M-70T		90	2	-40°C to 85°C	28L SOP
UM6264M-70LT		90	0.1	-40°C to 85°C	28L SOP
UM6264K-70		90	2	0°C to 70°C	28L Skinny
UM6264K-70L		90	0.1	0°C to 70°C	28L Skinny
UM6264K-70T		90	2	-40°C to 85°C	28L Skinny
UM6264K-70LT		90	0.1	-40°C to 85°C	28L Skinny
UM6264-10		100	90	2	0°C to 70°C
UM6264-10L	90		0.1	0°C to 70°C	28L DIP
UM6264-10T	90		2	-40°C to 85°C	28L DIP
UM6264-10LT	90		0.1	-40°C to 85°C	28L DIP
UM6264M-10	90		2	0°C to 70°C	28L SOP
UM6264M-10L	90		0.1	0°C to 70°C	28L SOP
UM6264M-10T	90		2	-40°C to 85°C	28L SOP
UM6264M-10LT	90		0.1	-40°C to 85°C	28L SOP
UM6264K-10	90		2	0°C to 70°C	28L Skinny
UM6264K-10L	90		0.1	0°C to 70°C	28L Skinny
UM6264K-10T	90		2	-40°C to 85°C	28L Skinny
UM6264K-10LT	90		0.1	-40°C to 85°C	28L Skinny
UM6264-12	120		90	2	0°C to 70°C
UM6264-12L		90	0.1	0°C to 70°C	28L DIP
UM6264-12T		90	2	-40°C to 85°C	28L DIP
UM6264-12LT		90	0.1	-40°C to 85°C	28L DIP
UM6264M-12		90	2	0°C to 70°C	28L SOP
UM6264M-12L		90	0.1	0°C to 70°C	28L SOP
UM6264M-12T		90	2	-40°C to 85°C	28L SOP
UM6264M-12LT		90	0.1	-40°C to 85°C	28L SOP
UM6264K-12		90	2	0°C to 70°C	28L Skinny
UM6264K-12L		90	0.1	0°C to 70°C	28L Skinny
UM6264K-12T		90	2	-40°C to 85°C	28L Skinny
UM6264K-12LT		90	0.1	-40°C to 85°C	28L Skinny

**Package Information**
**28 LEAD DUAL IN-LINE; PLASTIC**

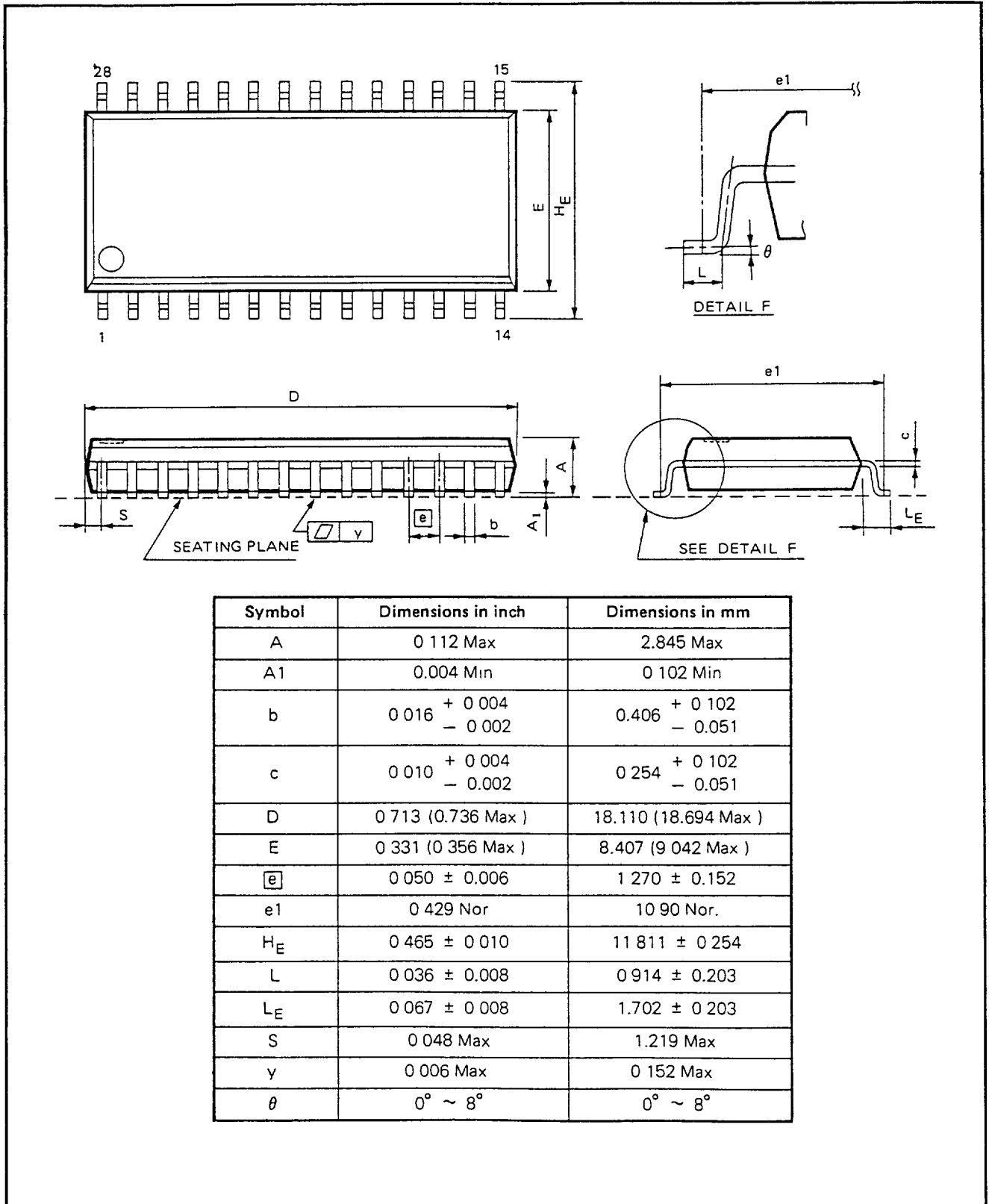
Unit inch/mm



Symbol	Dimensions in inch	Dimensions in mm
A	0.210 Max.	5.334 Max
A1	0.010 Min	0.254 Min.
B	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
B1	0.060 + 0.004 - 0.002	1.524 + 0.102 - 0.051
c	0.010 + 0.004 - 0.002	0.254 + 0.102 - 0.051
D	1.460 (1.470 Max.)	37.084 (37.338 Max.)
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.545 (0.575 Max.)	13.843 (14.605 Max.)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.090 Max.	2.286 Max

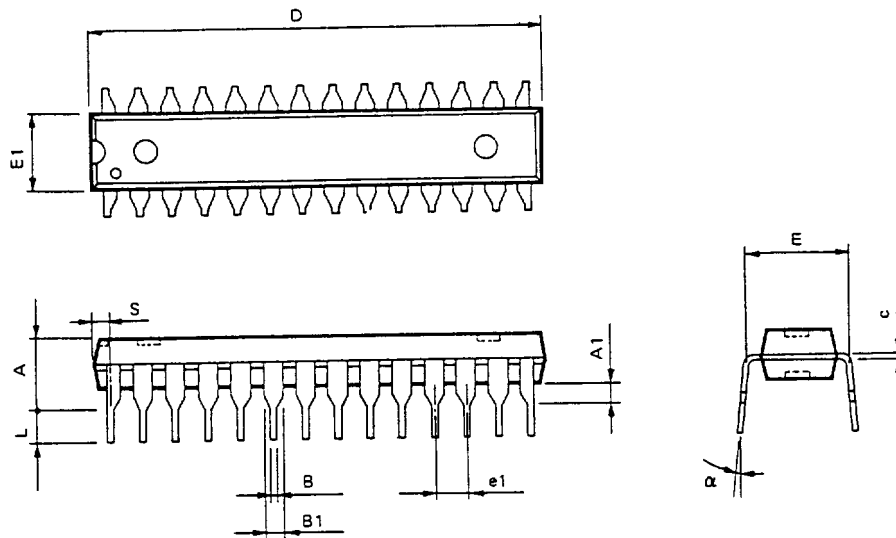
**28 Pin Small Outline**

Unit inch/mm



**28 Pin Skinny Outline**

Unit inch/mm



Symbol	Dimensions in inch	Dimensions in mm
A	0.175 Max	4.445 Max.
A1	0.010 Min.	0.254 Min
B	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
B1	0.060 + 0.004 - 0.002	1.524 + 0.102 - 0.051
c	0.010 + 0.004 - 0.002	0.254 + 0.102 - 0.051
D	1.388 (1.400 Max)	35.255 (35.560 Max)
E	0.310 ± 0.010	7.874 ± 0.254
E1	0.288 (0.310 Max)	7.315 (7.874 Max)
e1	0.100 ± 0.010	2.540 ± 0.254
L	0.130 ± 0.010	3.302 ± 0.254
α	0° ~ 15°	0° ~ 15°
S	0.055 Max	1.397 Max

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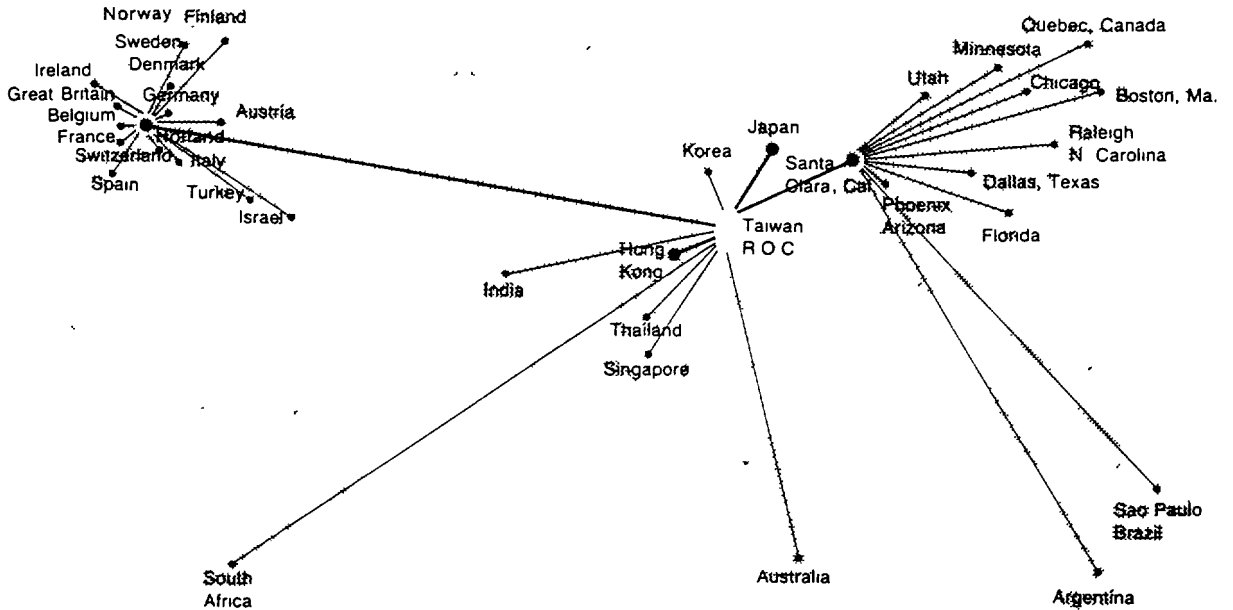
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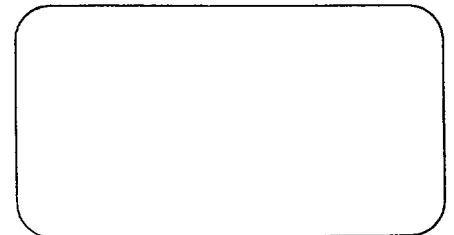
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