UMC

UMC

UM487

PRELIMINARY

HCGA CONTROLLER

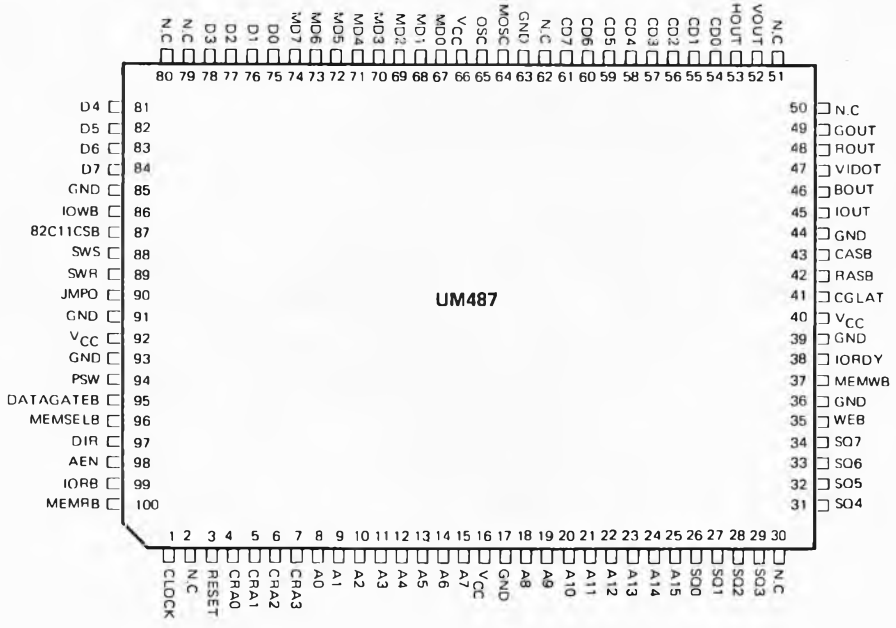
Features

- MGA (Hercules) and CGA compatible
- Built-in 6845 CRTC
- 64K Bytes of video memory
- Flicker-Free operation during CPU read/write
- Minimum circuit board space required
- Display mode changeable using hardware or software
- Optional primary printer port

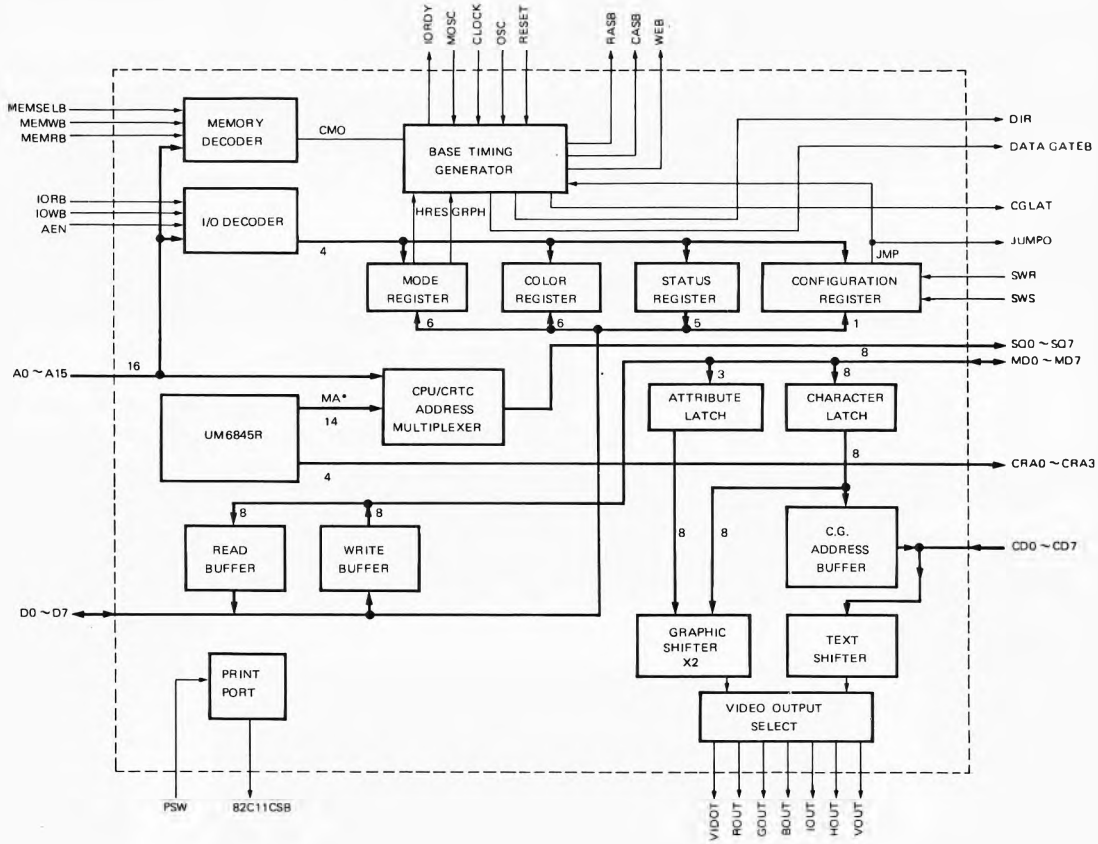
General Description

The UM487 single-chip HCGA controller is an advanced product designed to serve as a combination MGA and CGA through the integration of most of the circuits found on MGA and CGA cards. Built with the UMC 2μm CMOS process, the UM487 incorporates a built-in 6845 CRTC circuit. Thus, for MGA and CGA functions, only a few external components are required to complete the circuits. These include: 64K bytes DRAM; 4 TTLs (74LS374, 74LS245 74LS04 and 74LS20); one character generator (UM2310) and a 16.257 MHz crystal. The UM487 comes packaged in a compact, 100-pin plastic flat pack.

Pin Configuration



Block Diagram



Absolute Maximum Ratings *

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . –55°C to 150°C
All Output Voltages . . . . . –0.5V to +7V
All Input Voltages . . . . . –0.5V to +7V
Supply Voltage V_{CC} . . . . . 0V to +7V
Power Dissipation 0.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input Voltage	2.0			V	
V_{IL}				0.8	V	
V_{OH1}	Output Voltage (for SQ0 ~ SQ7	2.4			V	I_{OH} = –6.0 mA
V_{OL1}	IORDY, RASB, CASB, WEB)			0.4	V	I_{OL} = +6.0 mA
V_{OH2}	Output Voltage (other outputs)	2.4			V	I_{OH} = –3.0 mA
V_{OL2}				0.4	V	I_{OH} = +3.0 mA
I_{IL}	Input Leakage	–10		+10	μA	$0 \leqslant V_{in} \leqslant V_{CC}$
I_{OL}	Output Leakage	–10		+10	μA	
I_{OP}	Operating Current			+12	mA	

AC Characteristics (CGA MODE BASE CLOCK 14.318 MHz, MGA MODE BASE CLOCK 16.257 MHz)

C–1 CPU Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
0	t_{DAC}	DIR, DATAGATEB Active to CPU I/O or Memory Read/Write Cycle			25	ns
1	t_{ASI}	Address Setup Time to IORB, IOWB	30			ns
2	t_{DNC}	DIR, DATAGATEB Non-active to CPU I/O or Memory Read/Write Cycle			20	ns
3	t_{IPW}	IORB, IOWB Active Pulse Width	160			ns
4	t_{DOIR}	Data Output Valid Time to IORB			20	ns
5	t_{DHIR}	Data Output Valid Hold Time to IORB	30			ns
6	t_{DSIW}	Data in Setup Time to IOWB	30			ns
7	t_{DHIW}	Data in Hold Time to IOWB	10			ns
8	t_{ASM}	Address Setup Time to MEMRB, MEMWB	0			ns
9	t_{AMD}	Addr. Valid to MEMCSB Active Delay			15	ns
10	t_{MID}	MEMRB, MEMWB Active to IORDY Low Delay			30	ns
11	t_{MWED}	MEMWB Active to WEB Active Delay	10		2240	ns
12	t_{WDHD}	Memory Write Data Hold Time to WEB	10			ns

C–1 CPU Interface (Continued)

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
13	t_{DORD}	MEMRB Data Output Valid to IORDY	20	30		ns
14	t_{DOMR}	MEMRB Data Output Valid Hold to MEMRB	20			ns

C–2 DRAM Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
15	t_{RL}	RASB Low Time		150		ns
16	t_{RH}	RASB High Time		90		ns
17	t_{CL}	CASB Low Time		90		ns
18	t_{CH}	CASB High Time		60		ns
19	t_{RLCL}	RASB ↓ to CASB ↓		60		ns
20	t_{CLRH}	CASB ↓ to RASB ↑		60		ns
21	t_{CHRL}	CASB ↑ to RASB ↓		60		ns
22	t_{RSU}	Row Address Setup Time to RASB ↓	0			ns
23	t_{RHL}	Row Address Hold Time to RASB ↓	20			ns
24	t_{CSU}	Column Addr. Setup Time to CASB ↓	0			ns
25	t_{CHL}	Column Addr. Hold Time to CASB ↓	25			ns
26	t_{ACR}	Access Time from RASB ↓			150	ns
27	t_{ACC}	Access Time from CASB ↓			90	ns
28	t_{WCL}	WEB Active before CASB ↓		40		ns
29	t_{WPW}	WEB Active Pulse Width		90		ns
30	t_{RLW}	RASB to WEB Active Hold		150		ns
31	t_{CAW}	CASB to WEB Active Hold		60		ns
32	t_{WDSC}	Write Data Setup Time to CASB ↓	0			ns
33	t_{WDHC}	Write Data Hold Time to CASB ↓	45			ns
34	t_{WDHR}	Write Data Hold Time to RASB ↓	110			ns
35	t_{DODC}	Data Output Disable Time to CASB ↑	0			ns
36	t_{PCYC}	Page Mode Read Cycle Time	150			ns

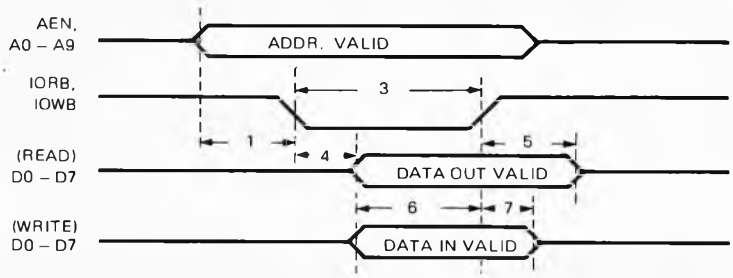
C–3 C. G. Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
39	t_{CGCH}	CGLAT ↑ to CASB ↑	5		10	ns
40	t_{CGAD}	CGLAT to C. G. Address Valid Delay			10	ns
41	t_{ACC}	C. G. Access Time			250	ns
42	t_{DOHA}	Data Output Hold Time from Addr.	0			ns

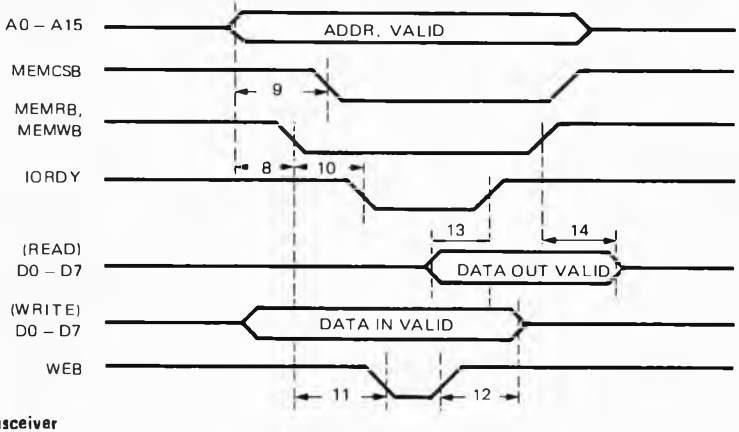
Timing Waveforms

CPU Interface Timing:

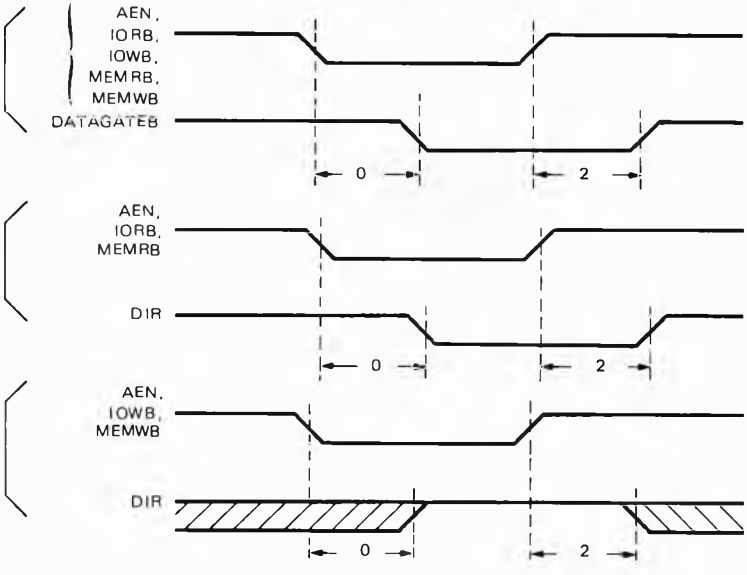
***I/O Cycle**



***Memory Cycle**



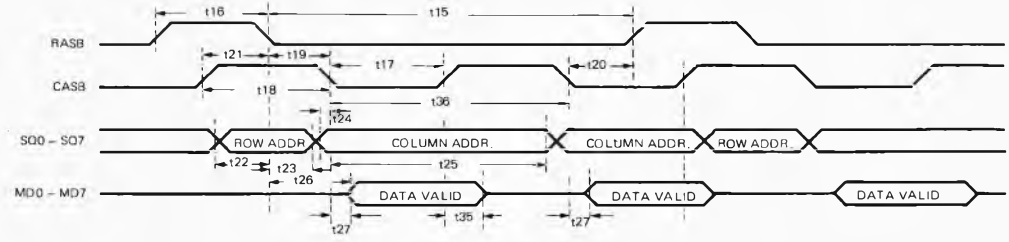
*** Bus Transceiver**



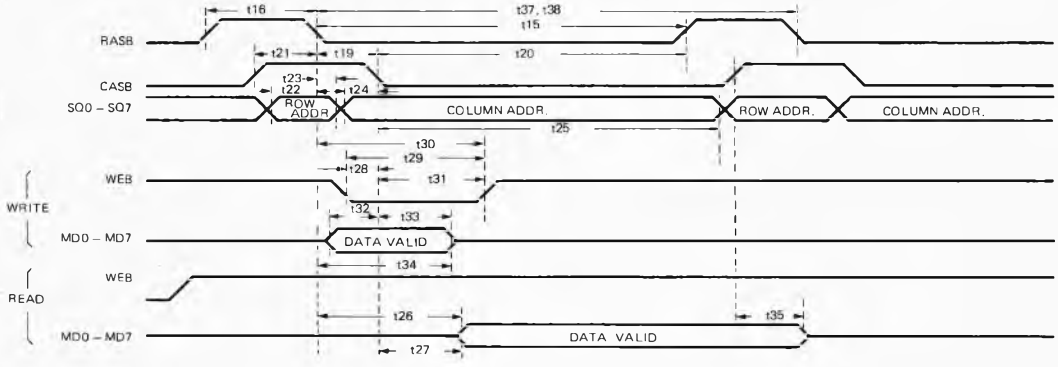
Timing Waveforms (Continued)

DRAM Interface Timing

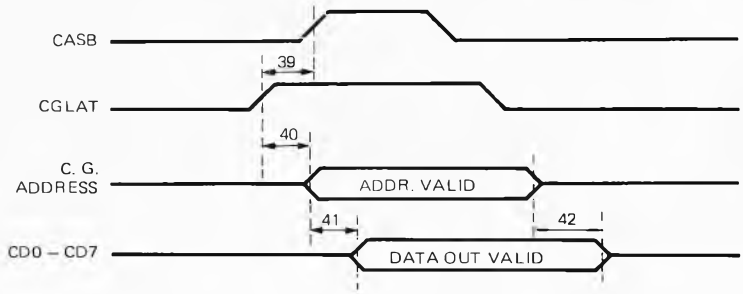
***Page mode Read Cycle**



***Early Write/Read Cycle**



C.G. Interface Timing:



Pin Description

Pin No.	Symbol	I/O	Description
1	CLOCK	I	CPU clock generates built-in 6845 enable signal
3	RESET	I	Chip reset signal, active high
4 ~ 7	CRA0 ~ CRA3	O	Internal 6845 scan line counter, CRA0 is LSB
8 ~ 15 18 ~ 25	A0 ~ A7 A8 ~ A15	I	CPU address bits 0~15, A0 is LSB A15 is MSB
26 ~ 29 31 ~ 34	SQ0 ~ SQ3 SQ4 ~ SQ7	O	Video memory (DRAM) address, SQ0 is LSB
35	WEB	O	Active low, video memory write strobe signal
37	MEMWB	I	Active low, CPU memory write signal
38	IORDY	O	Active high, informs CPU cycle is completed
41	CGLAT	O	Code data latch to C. G. during CGLAT rising edge
42	RASB	O	Video memory row address strobe signal
43	CASB	O	Video memory column address strobe signal
45	IOUT	O	Intensity signal output to RGB monitor
46	BOUT	O	Blue signal output to RGB monitor
47	VIDOT	O	Video dot stream output to monitor
48	ROUT	O	Red signal output to RBG monitor
49	GOUT	O	Green signal output to RBG monitor
52	VOUT	O	Vertical synchronous output to monitor
53	HOUT	O	Horizontal synchronous output to monitor
54 ~ 61	CD0 ~ CD7	I	Character Generator (C. G.) data bus, CD0 is first pixel
64	MOSC	I	MGA mode base clock input (16.257 MHz crystal)
65	OSC	I	CGA mode base clock input (14.318 MHz crystal)
67 ~ 74	MD0 ~ MD7	I/O	Video memory data bus, MD0 is LSB
75 ~ 78 81 ~ 84	D0 ~ D3 D4 ~ D7	I/O	Data bus, D0 is LSB
86	IOWB	I	Active low, CPU I/O write signal
87	82C11CSB	O	Active low, printer controller UM82C11 chip select
88	SWS	I	Active high, to select CGA mode
89	SWR	I	Active high, to select MGA mode
90	JMPO	O	Select CGA/MGA C. G. character font, '0' for MGA
94	PSW	I	Enables primary printer port while PSW is connected to UM82C11 CSB pin
95	DATAGATEB	O	Active low, enables external data transceiver 74LS245

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
96	MEMSELB	I	Active low to select video memory while CPU pins A19 ~ A16 are equal to '1011'
97	DIR	O	Controls external bus transceiver 74LS245 direction '0': from UM487 to CPU during IORB or MEMRB active '1': from CPU to UM487 during IOWB or MEMWB active
98	AEN	I	Active low to enable I/O address
99	IORB	I	Active low, CPU I/O read signal
100	MEMRB	I	Active low, CPU memory read signal
2, 30, 50 51, 62, 79, 80	N. C.	*	No connection
17, 36, 85 39, 44, 93 63, 91	GND	I	Ground
16, 40 66, 92	V_{CC}	I	+5V power supply

* For proper operation, these pins should not be connected.

Register Description

A. Register:

I/O Address		Read/Write	Function	Note
MGA	CGA			
3B4	3D4	W	6845 index register	refer to UM6845R
3B5	3D5	R/W	6845 data register	
3B8	3D8	W	Mode control register	
---	3D9	W	Color select register	
3BA	3DA	R	Status register	
3BB	3DB	W	Light pen reset register	
3B9	3DC	W	Light pen set register	
3BF		W	Configuration register	
3BC		R/W	Primary printer data register	refer to UM82C11
3BD		R	Primary printer status register	
3BE		R/W	Primary printer control word register	

'---' means not used

A-1 Status Register (3?A)

Bit	Logic	MGA (3BA)	CGA (3DA)
0	0 1	Non-horizontal sync. period Horizontal sync. period	Display active period Non-display period
1	0 1	Light pen reset Light pen set	Light pen reset Light pen set
2	0 1	Light pen switch off Light pen switch on	Light pen switch off Light pen switch on
3	0 1	Video dot off Video dot on	Non-vert. sync. period Vertical sync. period
7	0 1	Vertical sync. period Non-vertical sync. period	– – – – – –

Bits 4, 5 and 6 not used

A-2 Mode Controller Register (3?8)

Bit	Logic	MGA (3B8)	CGA (3D8)
0	0 1	– – – – – –	40*25 Text 80*25 Text
1	0 1	Text Graphic (while 3BF bit 0 = 1)	Text Graphic
2	0 1	– – – – – –	Color mode Black/white
3	0 1	Disable video Enable video	Disable video Enable video
4	0 1	– – – – – –	320*200 Graphic 640*200 Graphic
5	0 1	Disable blink Enable blink	Disable blink Enable blink
6	0 1	Disable change mode Enable change mode	Disable change mode Enable change mode
7	0 1	Page 0 Page 1 (while 3BF bit 1 = 1)	– – – – – –

A-3 Color Select Register (3D9 CGA Only)

Bit	Function
0	In 40*25 text, select blue of border color In 320*200 graphic, select blue of background color In 640*200 graphic, select blue of foreground color
1	In 40*25 text, select green of border color In 320*200 graphic, select green of background color In 640*200 graphic, select green of foreground color
2	In 40*25 text, select red of border color In 320*200 graphic, select red of background color In 640*200 graphic, select red of foreground color
3	In 40*25 text, select intensity of border color In 320*200 graphic, select intensity of background color In 640*200 graphic, select intensity of foreground color
4	Text mode background color or Graphic mode foreground color
5	Select foreground color pair (only 320*200 graphic)

Bits 6, 7 not used

A-4 Configuration Register (3BF)

Bit	Logic	Function
0	0 1	Disable MGA graphic Enable MGA graphic
1	0 1	Disable MGA page 1 Enable MGA page 1
6	0 1	Select MGA mode (while 3D8 bit6 = 1) Select CGA mode (while 3B8 bit6 = 1)

Other bit not used

A-5 Internal Registers of 6845 (Refer to UM6845R/RA/RB Data Sheet)

Register No.	Function	Unit	Read/ Write
R0	Horizontal total	Char.	W
R1	Horizontal display	Char.	W
R2	Horizontal sync. position	Char.	W
R3	Sync. pulse width	Char.	W
R4	Vertical total	Row	W
R5	Vertical total adjust	Line	W
R6	Vertical display	Row	W
R7	Vertical sync. position	Row	W
R8	Non-interlace mode	---	W
R9	Max. scan line	Line	W
R10	Cursor start	Line	W
R11	Cursor end	Line	W
R12	Start address (H)	---	W
R13	Start address (L)	---	W
R14	Cursor address (H)	---	R/W
R15	Cursor address (L)	---	R/W
R16	Light pen address (H)	---	R
R17	Light pen address (L)	---	R

Functional Description

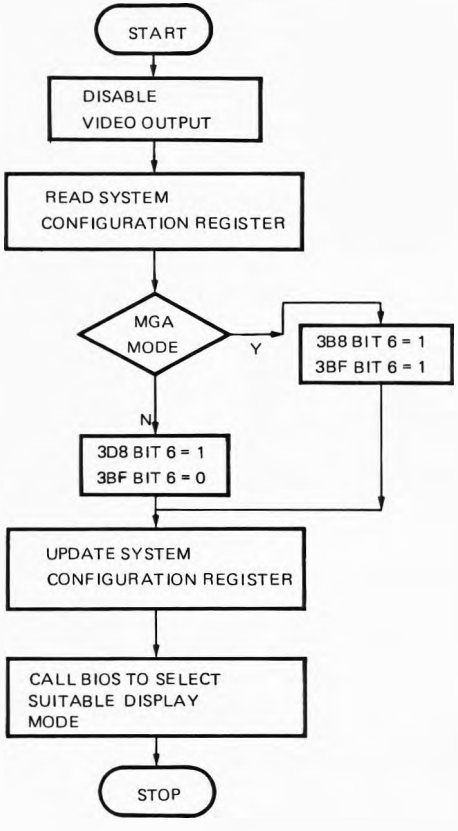
B–1 By HARDWARE

The MGA mode is selected when SW1 pin 2 is connected to pin 3, otherwise CGA mode is active if SW1 pin 2 is connected to pin 1.

B–2 By SOFTWARE

The software changes display mode only if SW3 pin 2 is connected to pin 3 and 3?8 bit 6 is equal to high. (where ? is D or B)

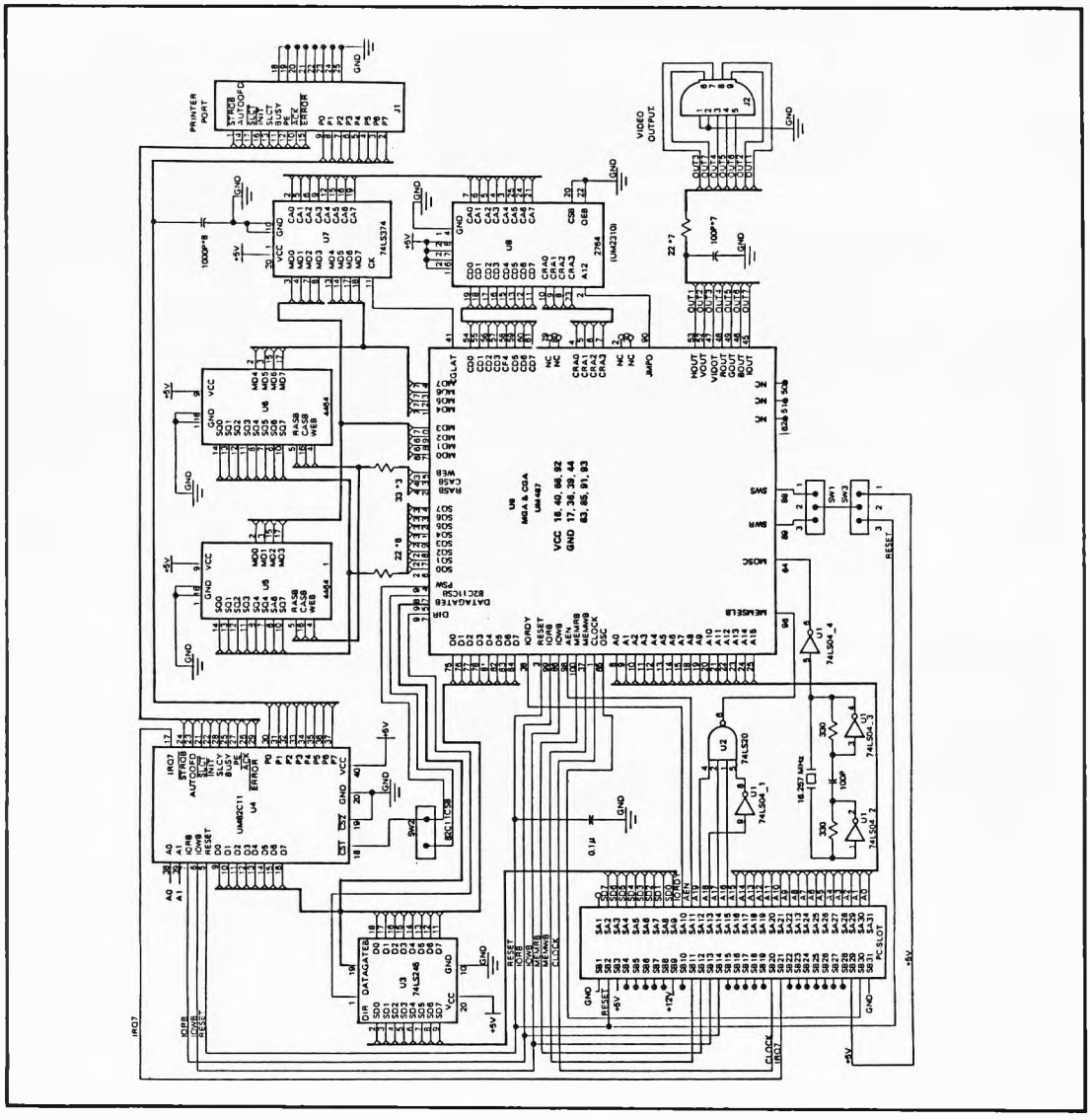
Program Flowchart:



B–3 Program Listing

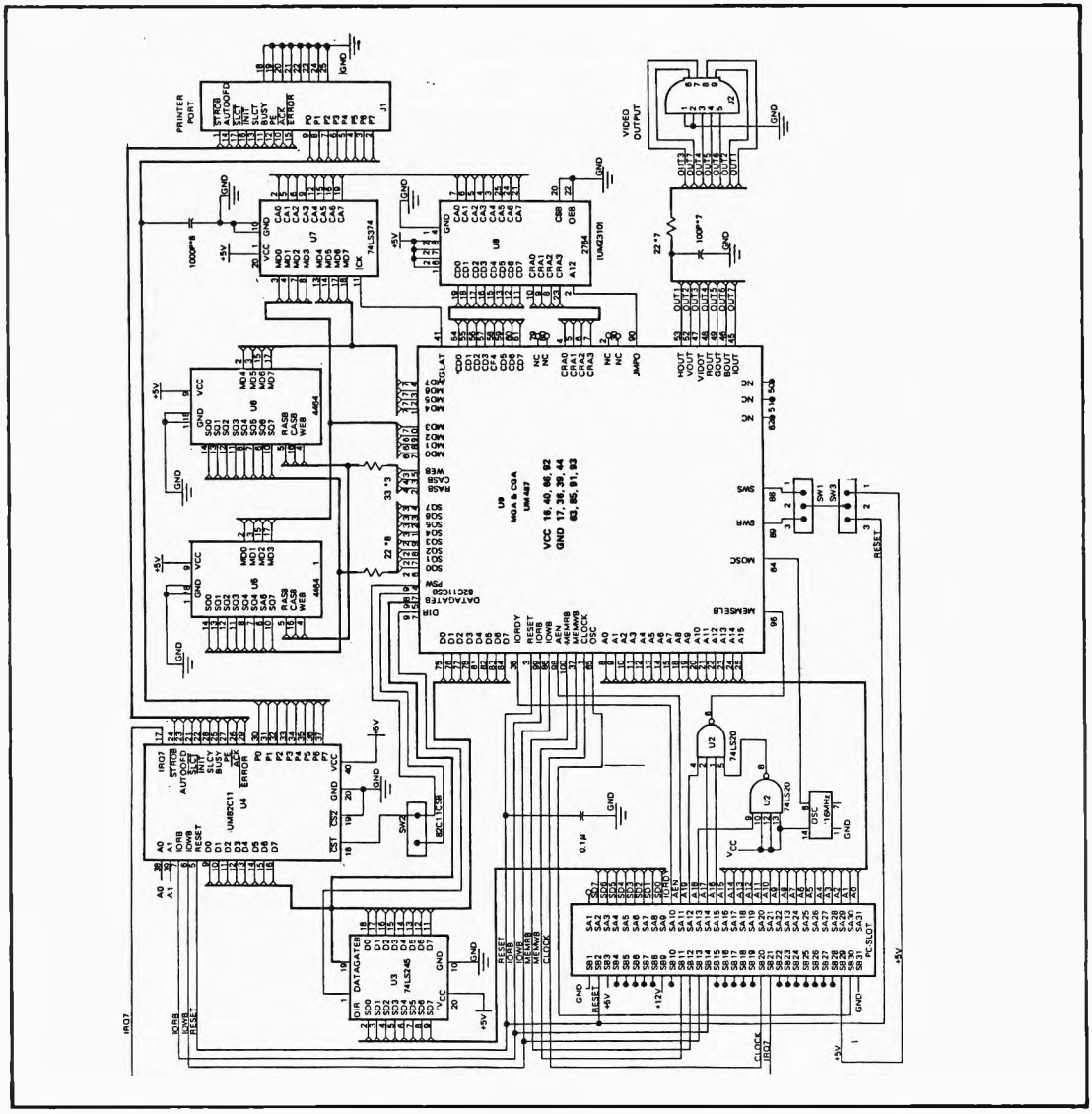
```
NCOMN   PROC    NEAR
        ASSUME  CS: CODE, DS: DATA, SS: STACK
        PUSH    DS
        MOV     AX, 0
        PUSH    AX
        PUSH    CS
        POP     DS
        MOV     AL, 20H
        MOV     CX, 07D0H
        MOV     BH, 0
        MOV     BL, 07
        MOV     AH, 09      ; clear video memory
        INT     10H
        MOV     AH, 0FH     ; read video state
        INT     10H
        CMP     AL, 07      ; MGA mode?
        JZ      MMM
        JMP     CCC
MMM:    MOV     AL, 40H     ; MGA mode
        MOV     DX, 3B8H    ; enable change mode
        OUT     DX, AL
        MOV     DX, 3BFH
        OUT     DX, AL      ; change to CGA mode
        MOV     AX, 0
        MOV     DS, AX
        MOV     AL, [410]   ; read BIOS configura-
                              tion register
        AND     AL, CFH     ; isolate bits 4, 5
        OR      AL, 20H     ; update BIOS con-
                              figuration register
        MOV     [410], AL   ; to CGA mode
        MOV     AH, 0       ; select CGA
        MOV     AL, 3
        INT     10H
        JMP     END
CCC:    MOV     AL, 40H     ; CGA mode
        MOV     DX, 3D8H
        OUT     DX, AL      ; enable change mode
        MOV     AL, 0
        MOV     DX, 3BFH    ; change to MGA mode
        OUT     DX, AL
        MOV     AX, 0
        MOV     DX, AX
        MOV     AL, [410]
        AND     AL, CFH
        OR      AL, 30H     ; update BIOS con-
                              figuration register
        MOV     [410], AL   ; to MGA mode
        MOV     AH, 0       ; select MGA
        MOV     AL, 7
        INT     10H
END:    RET
NCOMN   ENDP
```

Application Circuits



1. The 74LS04 is used for crystal circuit
2. The 74LS20 decodes CPU A19 ~ A16 to generate MEMCSB while MGA or CGA video memory is selected
3. The 74LS245 is data transceiver between CPU and UM487
4. The 74LS374 latches code data to C. G. during text mode
5. SW1 $\overline{3}$ $\overline{2}$ 1 : MGA mode
   SW1 3 $\overline{2}$ $\overline{1}$: CGA mode
6. SW2 is connected while primary printer port is selected
7. SW3 $\overline{3}$ $\overline{2}$ 1 : Enable change mode by software
   SW3 3 $\overline{2}$ $\overline{1}$: Disable change mode by software

Application Circuits



1. 16 MHz osc for MGA mode
2. The 74LS20 decodes CPU A19 ~ A16 to generate MEMCSB while MGA or CGA video memory is selected
3. The 74LS245 is data transceiver between CPU and UM487
4. The 74LS374 latches code data to C. G. during text mode
5. SW1 $\overline{3}21$: MGA mode
   SW1 3$\overline{21}$: CGA mode
6. SW2 is connected while primary printer port is selected
7. SW3 $\overline{3}21$: Enable change mode by software
   SW3 3$\overline{21}$: Disable change mode by software

Ordering Information

Part No.	Package
UM487F	100 Pin QFP