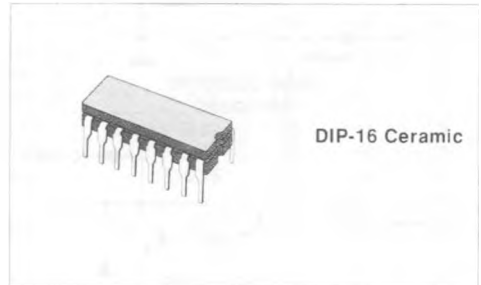


## SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUT CAN BE PARRALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



### DESCRIPTION

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

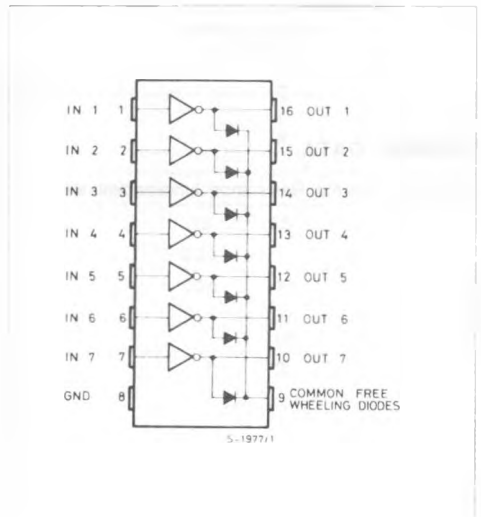
The four versions interface to all common families.

ULQ2001R	General Purpose, DTL, TTL, CMOS
ULQ2002R	15-25 V PMOS
ULQ2003R	5 V TTL, CMOS
ULQ2004R	6-15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal print-heads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are supplied in 16 pin ceramic DIP packages.

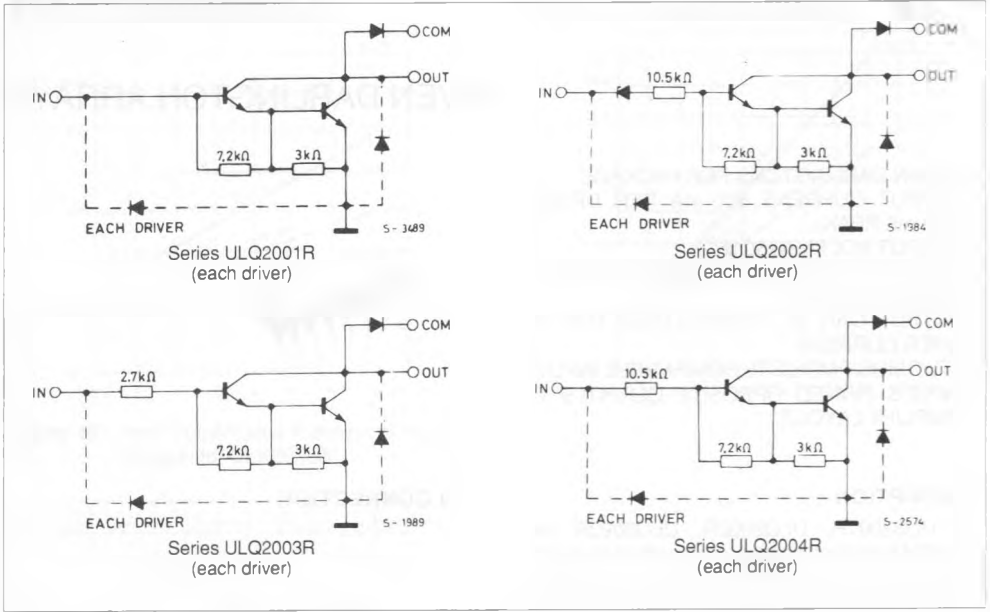
### PIN CONNECTION



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_o$	Output Voltage	50	V
$V_{in}$	Input Voltage (for ULQ2002R/2003R/2004R)	30	V
$I_c$	Continuous Collector Current	500	mA
$I_b$	Continuous Base Current	25	mA
$T_{amb}$	Operating Ambient Temperature Range	- 20 to + 85	C
$T_{stg}$	Storage Temperature Range	- 55 to 150	C

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	150	°C/W
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**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ} \text{C}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.	
$I_{CEX}$	Output Leakage Current	$V_{CE} = 50 \text{ V}$			50	$\mu\text{A}$	1a	
		$T_{amb} = 70^{\circ} \text{C}$	$V_{CE} = 50 \text{ V}$		100	$\mu\text{A}$	1a	
		$T_{amb} = 70^{\circ} \text{C}$ for <b>ULQ2002R</b>	$V_{CE} = 50 \text{ V}$	$V_I = 6 \text{ V}$		500	$\mu\text{A}$	1b
		for <b>ULQ2004R</b>	$V_{CE} = 50 \text{ V}$	$V_I = 1 \text{ V}$		500	$\mu\text{A}$	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 100 \text{ mA}$	$I_B = 250 \mu\text{A}$	0.9	1.1	V	2	
		$I_C = 200 \text{ mA}$	$I_B = 350 \mu\text{A}$	1.1	1.3	V	2	
		$I_C = 350 \text{ mA}$	$I_B = 500 \mu\text{A}$	1.3	1.6	V	2	
$I_{i(on)}$	Input Current	for <b>ULQ2002R</b>	$V_I = 17 \text{ V}$	0.82	1.25	$\text{mA}$	3	
		for <b>ULQ2003R</b>	$V_I = 3.85 \text{ V}$	0.93	1.35	$\text{mA}$	3	
		for <b>ULQ2004R</b>	$V_I = 5 \text{ V}$	0.35	0.5	$\text{mA}$	3	
		$V_I = 12 \text{ V}$	1	1.45	$\text{mA}$	3		
$I_{i(off)}$	Input Current	$T_{amb} = 70^{\circ} \text{C}$	$I_C = 500 \mu\text{A}$	50	65	$\mu\text{A}$	4	
$V_{i(on)}$	Input Voltage	for <b>ULQ2002R</b>	$V_{CE} = 2 \text{ V}$	$I_C = 300 \text{ mA}$		13	V	5
		for <b>ULQ2003R</b>	$V_{CE} = 2 \text{ V}$	$I_C = 200 \text{ mA}$		2.4	V	5
		$V_{CE} = 2 \text{ V}$	$I_C = 250 \text{ mA}$		2.7	V	5	
		$V_{CE} = 2 \text{ V}$	$I_C = 300 \text{ mA}$		3	V	5	
		for <b>ULQ2004R</b>	$V_{CE} = 2 \text{ V}$	$I_C = 125 \text{ mA}$		5	V	5
		$V_{CE} = 2 \text{ V}$	$I_C = 200 \text{ mA}$		6	V	5	
		$V_{CE} = 2 \text{ V}$	$I_C = 275 \text{ mA}$		7	V	5	
$V_{CE} = 2 \text{ V}$	$I_C = 350 \text{ mA}$		8	V	5			
$h_{FE}$	DC Forward Current Gain	for <b>ULQ2001R</b>	$V_{CE} = 2 \text{ V}$	$I_C = 350 \text{ mA}$	1000	-	2	
$C_i$	Input Capacitance			15	25	$\text{pF}$	-	
$t_{PLH}$	Turn-on Delay Time	$0.5 V_I$ to $0.5 V_O$		0.25	1	$\mu\text{s}$	-	
$t_{PHL}$	Turn-off Delay Time	$0.5 V_I$ to $0.5 V_O$		0.25	1	$\mu\text{s}$	-	
$I_R$	Clamp Diode Leakage Current	$V_R = 50 \text{ V}$			50	$\mu\text{A}$	6	
		$T_{amb} = 70^{\circ} \text{C}$	$V_R = 50 \text{ V}$		100	$\mu\text{A}$	6	
$V_F$	Clamp Diode Forward Voltage	$I_F = 350 \text{ mA}$		1.7	2	V	7	

TEST CIRCUITS

Figure 1a.

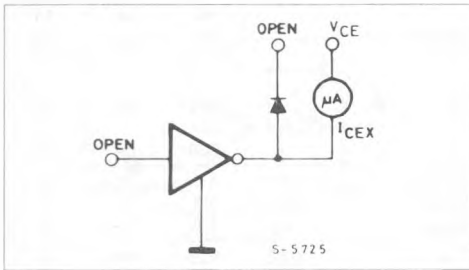


Figure 1b.

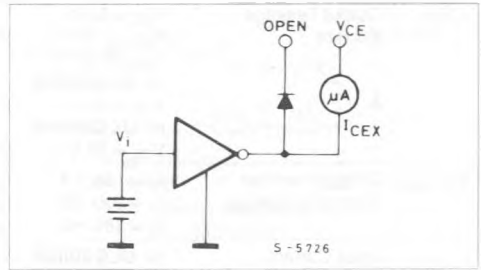


Figure 2.

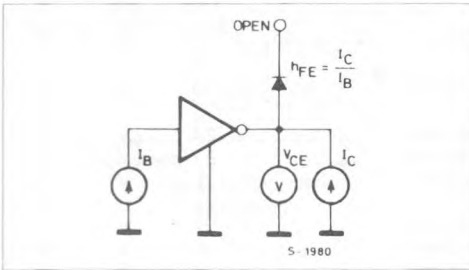


Figure 3.

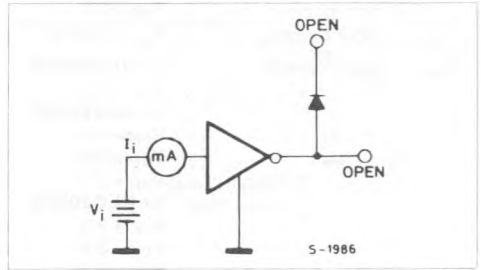


Figure 4.

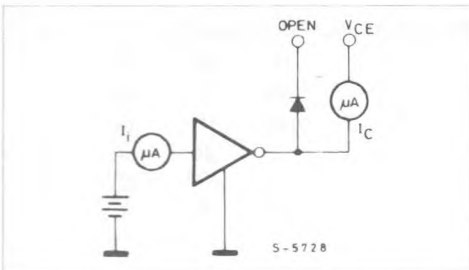


Figure 5.

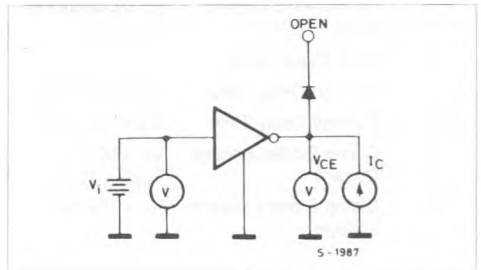


Figure 6.

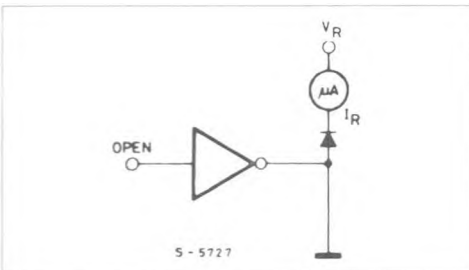


Figure 7.

