

80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

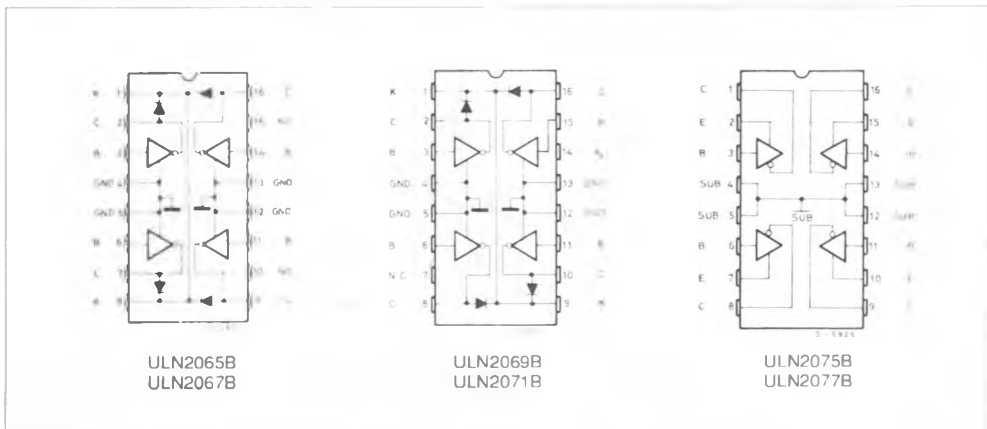
tible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragrain, reducing the load on control logic.

DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compa-



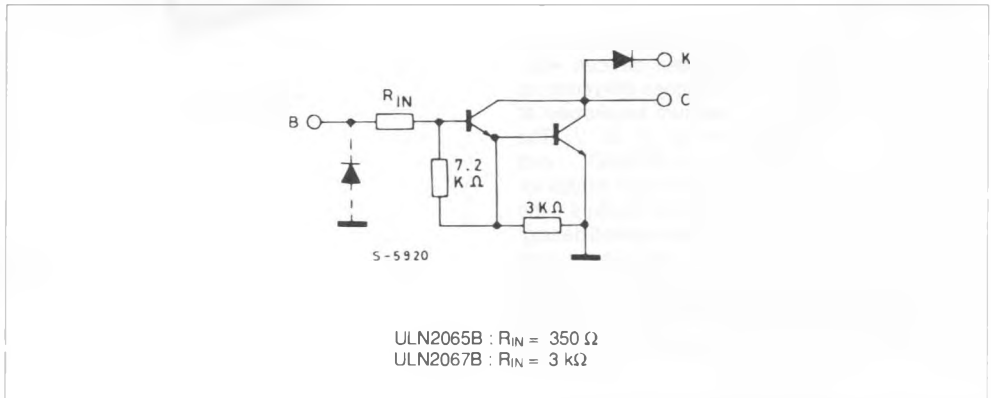
PIN CONNECTIONS AND ORDER CODES



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for ULN2075B – 2077B	60	V
	for ULN2067B – 2071B	30	V
	for ULN2065B – 2069B	15	V
I_i	Input Current	25	mA
V_s	Supply Voltage for ULN2069B	10	V
	for ULN2071B	20	V
P_{Tot}	Power Dissipation : at $T_{pins} = 90\text{ }^\circ\text{C}$	4.3	W
	at $T_{amb} = 70\text{ }^\circ\text{C}$	1	W
T_{amb}	Operating Ambient Temperature Range	- 20 to 85	$^\circ\text{C}$
T_{stg}	Storage Temperature	- 55 to 150	$^\circ\text{C}$

SCHEMATIC DIAGRAM

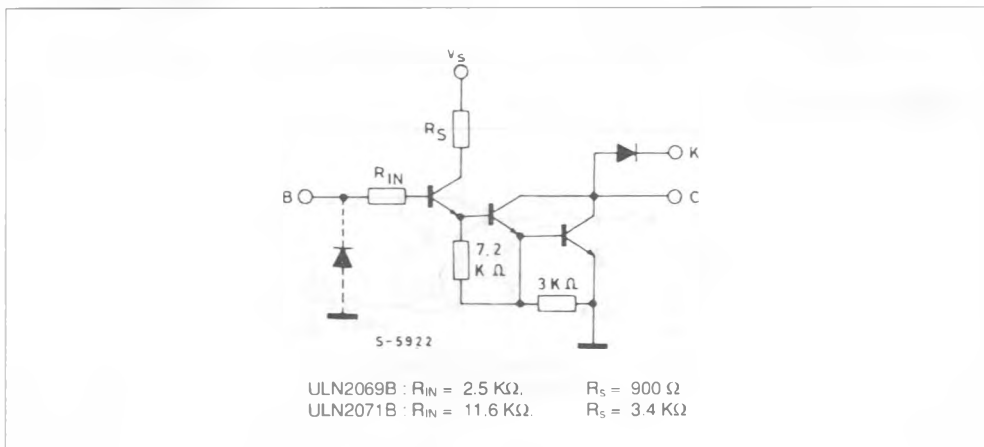


ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for ULN2065B – ULN2067B $V_{CE} = 80\text{ V}$ $V_{CE} = 80\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2065B – ULN2067B $I_C = 100\text{ mA}$ $V_i = 0.4\text{ V}$	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 500\text{ mA}$ $I_B = 625\text{ }\mu\text{A}$ $I_C = 750\text{ mA}$ $I_B = 935\text{ }\mu\text{A}$ $I_C = 1\text{ A}$ $I_B = 1.25\text{ mA}$ $I_C = 1.25\text{ A}$ $I_B = 2\text{ mA}$ for ULN2065B – ULN2067B $I_C = 1.5\text{ A}$ $I_B = 2.25\text{ mA}$			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input Current	for ULN2065B $V_i = 2.4\text{ V}$ for ULN2065B $V_i = 3.75\text{ V}$ for ULN2067B $V_i = 5\text{ V}$ for ULN2067B $V_i = 12\text{ V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input Voltage	for ULN2065B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2067B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$			2 2.5 6.5 10	V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	μs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	μs	
I_R	Clamp Diode Leakage Current	for ULN2065B – ULN2067B $V_R = 80\text{ V}$ $V_R = 80\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			50 100	μA μA	6
V_F	Clamp Diode Forward Voltage	$I_F = 1\text{ A}$ $I_F = 1.5\text{ A}$			1.75 2	V V	7

- Notes :** 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

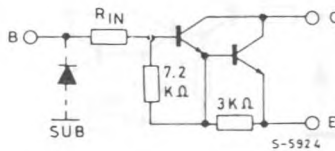
SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($V_s = 5\text{ V}$ for ULN2069B. $V_s = 12\text{ V}$ for ULN2071B. $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for ULN2069B - ULN2071B $V_{CE} = 80\text{ V}$ $V_{CE} = 80\text{ V}$ $T_{amb} = 70\text{ }^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2069B - ULN2071B $I_C = 100\text{ mA}$ $V_i = 0.4\text{ V}$	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for ULN2069B $I_C = 500\text{ mA}$ $V_i = 2.75\text{ V}$ $I_C = 750\text{ mA}$ $V_i = 2.75\text{ V}$ $I_C = 1\text{ A}$ $V_i = 2.75\text{ V}$ $I_C = 1.25\text{ A}$ $V_i = 2.75\text{ V}$ $I_C = 1.5\text{ A}$ $V_i = 2.75\text{ V}$ for ULN2071B $I_C = 500\text{ mA}$ $V_i = 5\text{ V}$ $I_C = 750\text{ mA}$ $V_i = 5\text{ V}$ $I_C = 1\text{ A}$ $V_i = 5\text{ V}$ $I_C = 1.25\text{ A}$ $V_i = 5\text{ V}$ $I_C = 1.5\text{ A}$ $V_i = 5\text{ V}$			1.1 1.2 1.3 1.4 1.5	V V V V V	2
$I_{i(on)}$	Input Current	for ULN2069B $V_i = 2.75\text{ V}$ for ULN2069B $V_i = 3.75\text{ V}$ for ULN2071B $V_i = 5\text{ V}$ for ULN2071B $V_i = 12\text{ V}$			550 1000 400 1250	μA μA μA μA	4
$V_{i(on)}$	Input Voltage	$V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2069B for ULN2071B			2.75 5	V	5
I_s	Supply Current	for ULN2069B $I_C = 500\text{ mA}$ $V_i = 2.75\text{ V}$ for ULN2071B $I_C = 500\text{ mA}$ $V_i = 5\text{ V}$			6 4.5	mA mA	8
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	μs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o $I_C = 1.25\text{ A}$			1.5	μs	
I_R	Clamp Diode Leakage Current	for ULN2069B - ULN2071B $V_R = 80\text{ V}$ $V_R = 80\text{ V}$ $T_{amb} = 70\text{ }^\circ\text{C}$			50 100	μA μA	6
V_F	Clamp Diode Forward Voltage	$I_F = 1\text{ A}$ $I_F = 1.5\text{ A}$			1.75 2	V V	7

SCHEMATIC DIAGRAM



ULN2075B : $R_{IN} = 350\ \Omega$
 ULN2077B : $R_{IN} = 3\ \text{k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for ULN2075B – ULN2077B $V_{CE} = 80\text{ V}$ $V_{CE} = 80\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2075B – ULN2077B $I_C = 100\text{ mA}$ $V_i = 0.4\text{ V}$	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 500\text{ mA}$ $I_B = 625\text{ }\mu\text{A}$ $I_C = 750\text{ mA}$ $I_B = 935\text{ }\mu\text{A}$ $I_C = 1\text{ A}$ $I_B = 1.25\text{ mA}$ $I_C = 1.25\text{ A}$ $I_B = 2\text{ mA}$ for ULN2075B – ULN2077B $I_C = 1.5\text{ A}$ $I_B = 2.25\text{ mA}$			1.1 1.2 1.3 1.4 1.5	V V V V V	3
$I_{i(on)}$	Input Current	for ULN2075B $V_i = 2.4\text{ V}$ for ULN2075B $V_i = 3.75\text{ V}$ for ULN2077B $V_i = 5\text{ V}$ for ULN2077B $V_i = 12\text{ V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input Voltage	for ULN2075B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2077B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$			2 2.5 6.5 10	V V V V	5
t_{PLH}	Turn-on Delay Time	$0.5 V_i$ to $0.5 V_o$			1	μs	
t_{PHL}	Turn-off Delay Time	$0.5 V_i$ to $0.5 V_o$			1.5	μs	

TEST CIRCUITS

Figure 1.

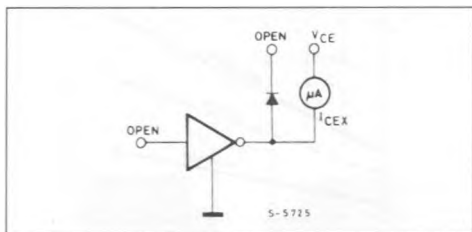


Figure 2.

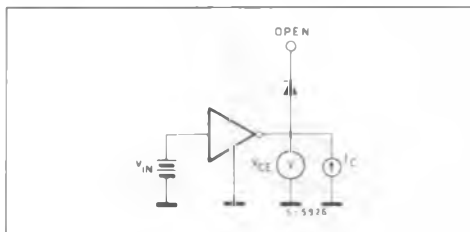


Figure 3.

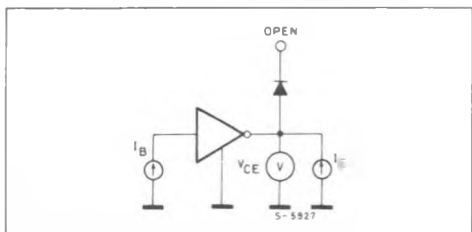


Figure 4.

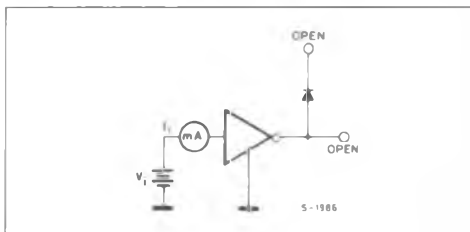


Figure 5.

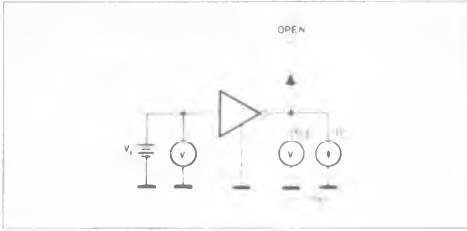


Figure 7.

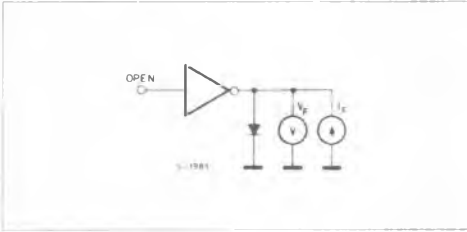


Figure 9 : Input Current as a Function of Input Voltage.

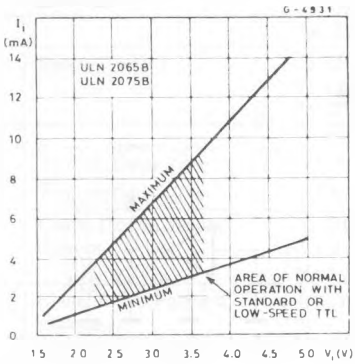


Figure 6.

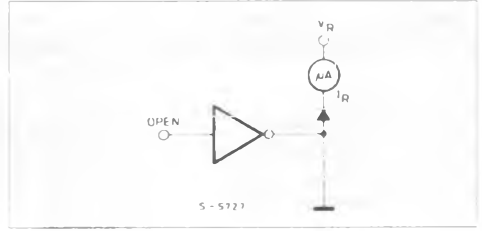


Figure 8.

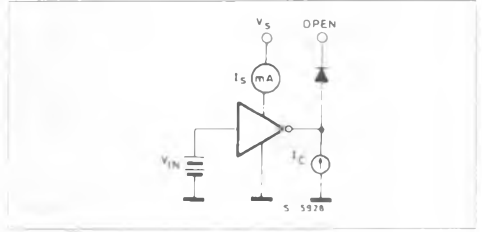


Figure 10 : Input Current as a Function of Input Voltage.

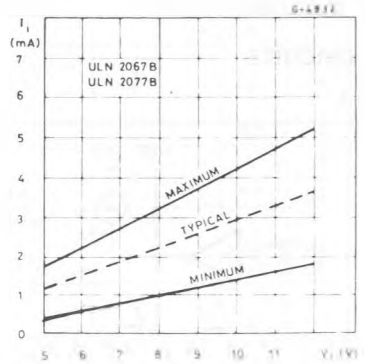
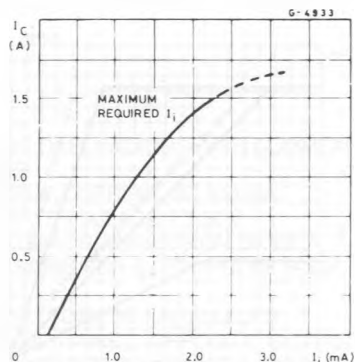


Figure 11 : Collector Current as a Function of Input Current.

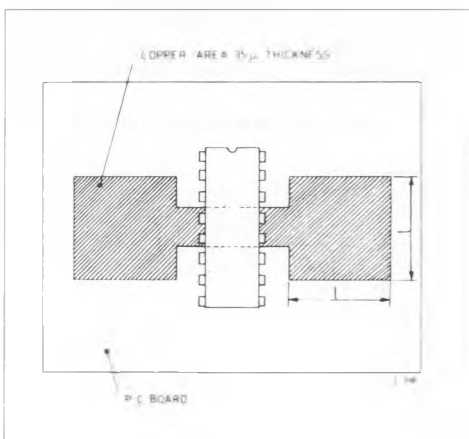


MOUNTING INSTRUCTIONS

The $R_{th\ j-amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j-amb}$ as a function of the side " W_{∞} " of two equal square copper areas having a thickness of $35\ \mu$ (1.4 mils).

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.



During soldering the pins temperature must not exceed $260\ ^\circ\text{C}$ and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 13 : External Heatsink Mounting Example.

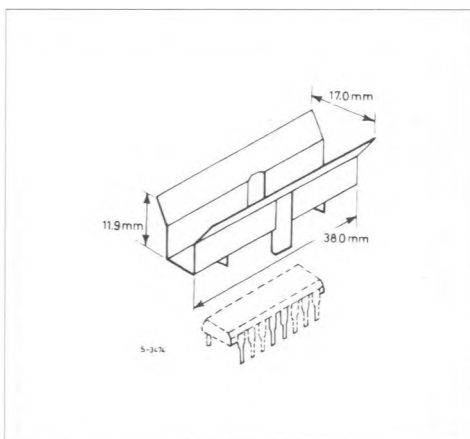


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

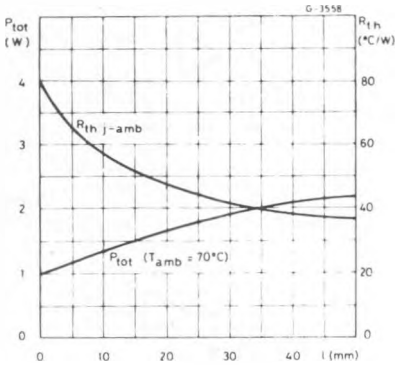


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

