

50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

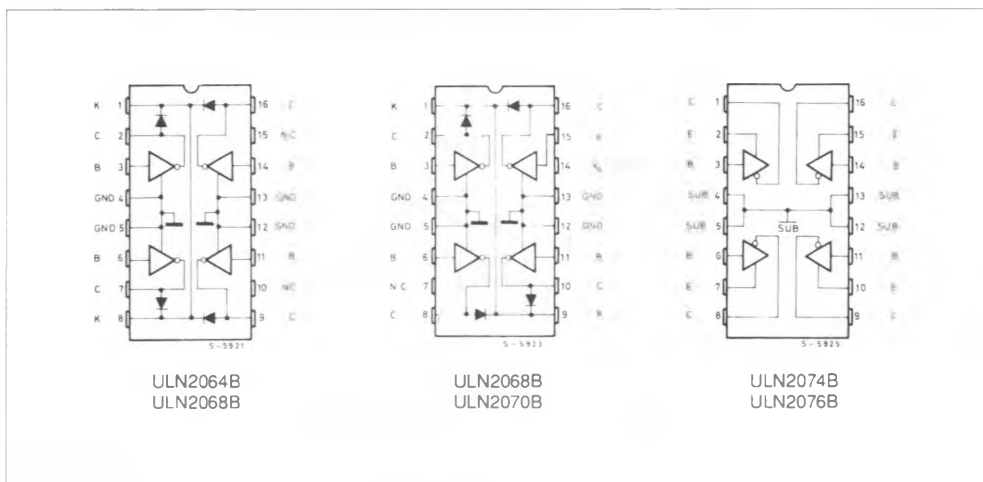
tible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compa-



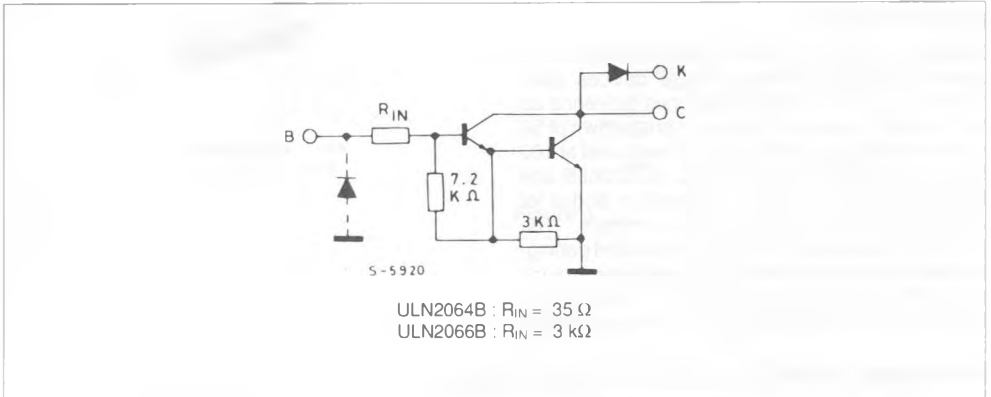
PIN CONNECTIONS (top view) and ORDER CODES



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{OEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_i	Input Voltage for ULN2066B/70B/74B/76B for ULN2064B/68B	30	V
		15	V
I_i	Input Current	25	mA
V_s	Supply Voltage for ULN2068B for ULN2070B	10	V
		20	V
P_{Tot}	Power Dissipation : at $T_{amb} = 90\text{ }^{\circ}\text{C}$ at $T_{amb} = 70\text{ }^{\circ}\text{C}$	4.3	W
		1	W
T_{amb}	Operating Ambient Temperature Range	- 20 to 85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	- 55 to 150	$^{\circ}\text{C}$

SCHEMATIC DIAGRAM

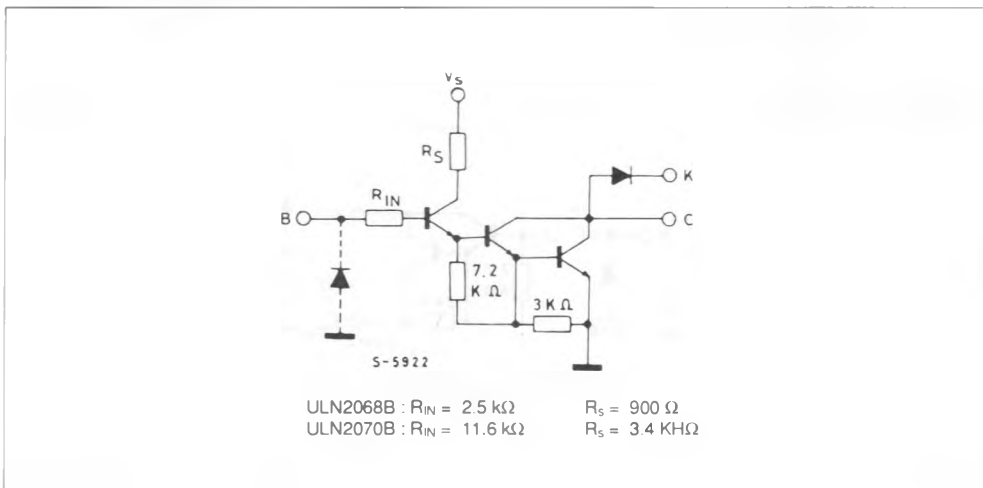


ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for ULN2064B - ULN2066B $V_{CE} = 50\text{ V}$ $V_{CE} = 50\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2064B - ULN2066B $I_C = 100\text{ mA}$ $V_i = 0.4\text{ V}$	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 500\text{ mA}$ $I_B = 625\text{ }\mu\text{A}$ $I_C = 750\text{ mA}$ $I_B = 935\text{ }\mu\text{A}$ $I_C = 1\text{ A}$ $I_B = 1.25\text{ mA}$ $I_C = 1.25\text{ A}$ $I_B = 2\text{ mA}$			1.1 1.2 1.3 1.4	V V V V	3
$I_{i(on)}$	Input Current	for ULN2064B $V_i = 2.4\text{ V}$ for ULN2064B $V_i = 3.75\text{ V}$ for ULN2066B $V_i = 5\text{ V}$ for ULN2066B $V_i = 12\text{ V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input Voltage	for ULN2064B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2066B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$			2 2.5 6.5 10	V V V V	5
t_{PLH}	Turn – on Delay Time	0.5 V_i to 0.5 V_o			1	μs	
t_{PHL}	Turn – off Delay Time	0.5 V_i to 0.5 V_o			1.5	μs	
I_R	Clamp Diode Leakage Current	for ULN2064B - ULN2066B $V_R = 80\text{ V}$ $V_R = 80\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			50 100	μA μA	6
V_F	Clamp Diode Forward Voltage	$I_F = 1\text{ A}$ $I_F = 1.5\text{ A}$			1.75 2	V V	7

- Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types
2. Input current may be limited by maximum allowable input voltage.

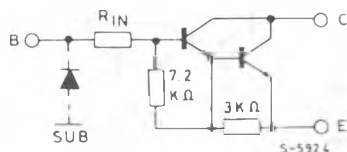
SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS ($V_s = 5\text{ V}$ for ULN2068B. $V_s = 12\text{ V}$ for ULN2070B. $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for ULN2068B - ULN2070B $V_{CE} = 50\text{ V}$ $V_{CE} = 50\text{ V}$ $T_{amb} = 70\text{ }^\circ\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2068B - ULN2070B $I_C = 100\text{ mA}$ $V_i = 0.4\text{ V}$	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for ULN2068B $I_C = 500\text{ mA}$ $V_i = 2.75\text{ V}$ $I_C = 750\text{ mA}$ $V_i = 2.75\text{ V}$ $I_C = 1\text{ A}$ $V_i = 2.75\text{ V}$ $I_C = 1.25\text{ A}$ $V_i = 2.75\text{ V}$ for ULN2070B $I_B = 500\text{ mA}$ $V_i = 5\text{ V}$ $I_B = 750\text{ mA}$ $V_i = 5\text{ V}$ $I_B = 1\text{ A}$ $V_i = 5\text{ V}$ $I_B = 1.25\text{ A}$ $V_i = 5\text{ V}$			1.1 1.2 1.3 1.4	V V V V	2
$I_{I(on)}$	Input Current	for ULN2068B $V_i = 2.75\text{ V}$ for ULN2068B $V_i = 3.75\text{ V}$ for ULN2070B $V_i = 5\text{ V}$ for ULN2070B $V_i = 12\text{ V}$			550 1000 400 1250	μA μA μA μA	4
$V_{I(on)}$	Input Voltage	$V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2068B for ULN2070B			2.75 5	V V	5
I_s	Supply Current	for ULN2068B $I_C = 500\text{ mA}$ $V_i = 2.75\text{ V}$ for ULN2070B $I_C = 500\text{ mA}$ $V_i = 5\text{ V}$			6 4.5	mA mA	8
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	μs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o $I_C = 1.25\text{ A}$			1.5	μs	
I_R	Clamp Diode Leakage Current	for ULN2068B - ULN2070B $V_R = 50\text{ V}$ $V_R = 50\text{ V}$ $T_{amb} = 70\text{ }^\circ\text{C}$			50 100	μA μA	6
V_F	Clamp Diode Forward Voltage	$I_F = 1\text{ A}$ $I_F = 1.5\text{ A}$			1.75 2	V V	7

SCHEMATIC DIAGRAM



ULN2074B : $R_{IN} = 350\ \Omega$
 ULN2076B : $R_{IN} = 3\ \text{k}\Omega$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for ULN2074B – ULN2076B $V_{CE} = 50\text{ V}$ $V_{CE} = 50\text{ V}$ $T_{amb} = 70\text{ }^{\circ}\text{C}$			100 500	μA μA	1
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for ULN2074B – ULN2076B $I_C = 100\text{ mA}$ $V = 0.4\text{ V}$	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 500\text{ mA}$ $I_B = 625\text{ }\mu\text{A}$ $I_C = 750\text{ mA}$ $I_B = 935\text{ }\mu\text{A}$ $I_C = 1\text{ A}$ $I_B = 1.25\text{ mA}$ $I_C = 1.25\text{ A}$ $I_B = 2\text{ mA}$			1.1 1.2 1.3 1.4	V V V V	3
$I_{(IOn)}$	Input Current	for ULN2074B $V_i = 2.4\text{ V}$ for ULN2074B $V_i = 3.75\text{ V}$ for ULN2076B $V_i = 5\text{ V}$ for ULN2076B $V_i = 12\text{ V}$	1.4 3.3 0.6 1.7		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{(IOn)}$	Input Voltage	for ULN2074B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$ for ULN2076B $V_{CE} = 2\text{ V}$ $I_C = 1\text{ A}$ $V_{CE} = 2\text{ V}$ $I_C = 1.5\text{ A}$			2 2.5 6.5 10	V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V _i to 0.5 V _o			1	μs	
t_{PHL}	Turn-off Delay Time	0.5 V _i to 0.5 V _o			1.5	μs	

TEST CIRCUITS

Figure 1.

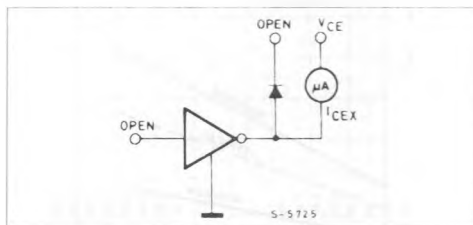


Figure 2.

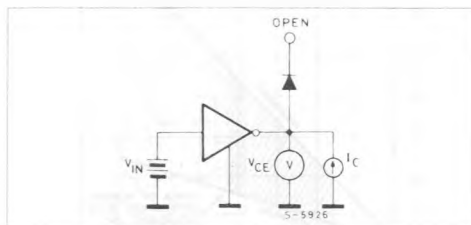


Figure 3.

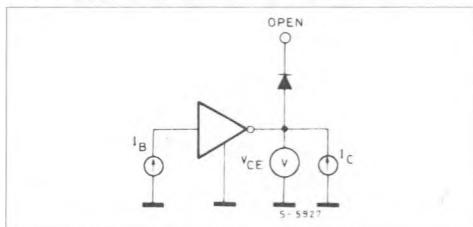


Figure 4.

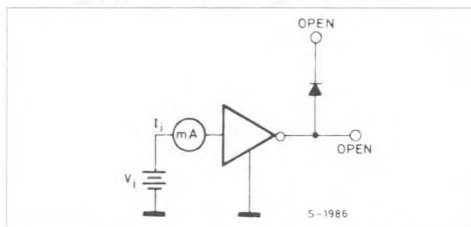


Figure 5.

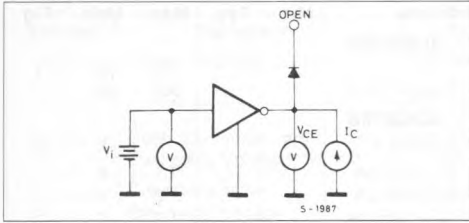


Figure 7.

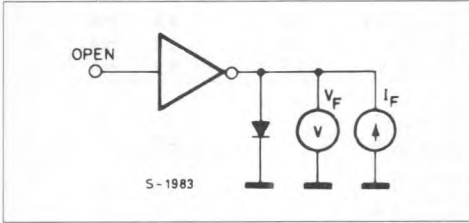


Figure 9 : Input Current as a Function of Input Voltage.

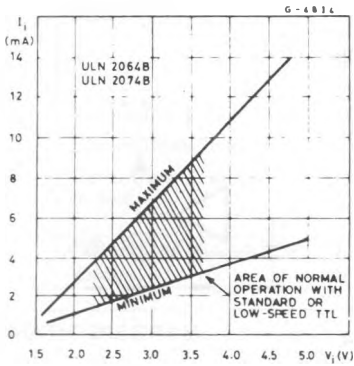


Figure 6.

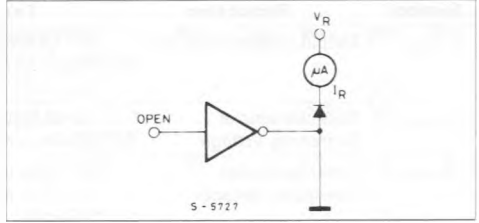


Figure 8.

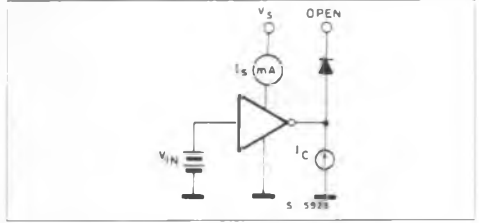


Figure 10 : Input Current as a Function of Input Voltage.

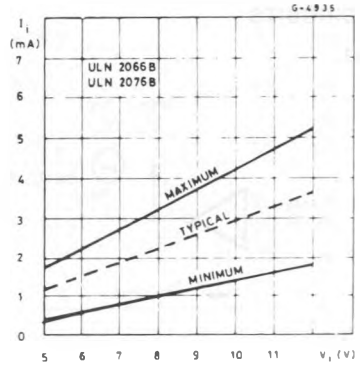
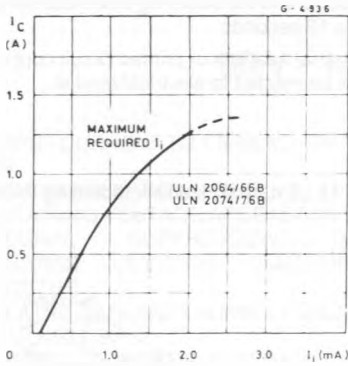


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

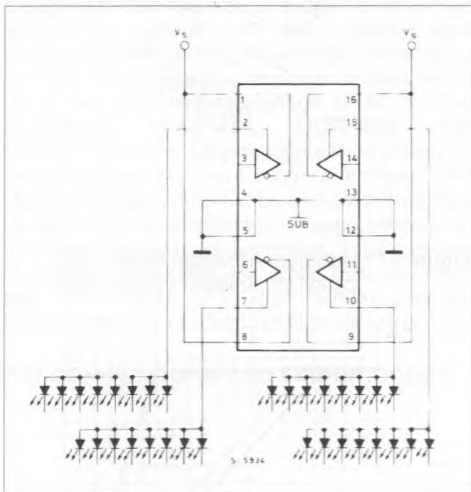
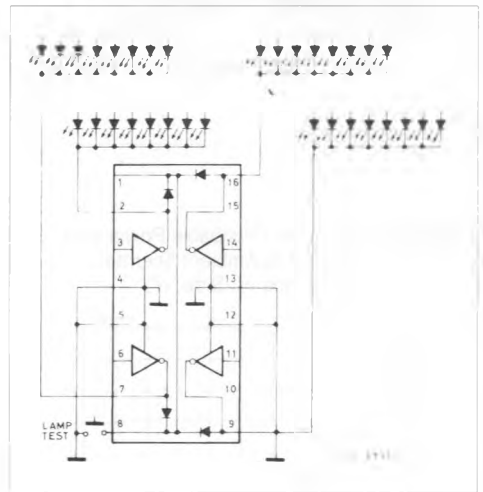


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th j-amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissippable power P_{tot} and the $R_{th j-amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

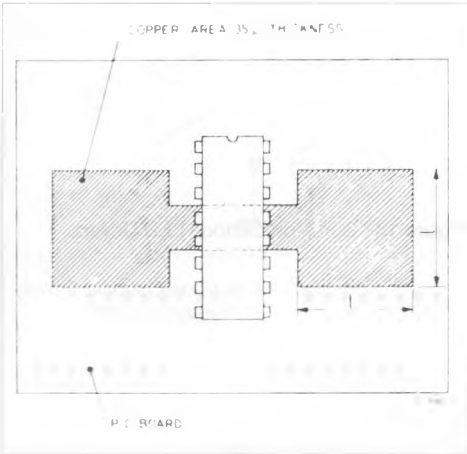
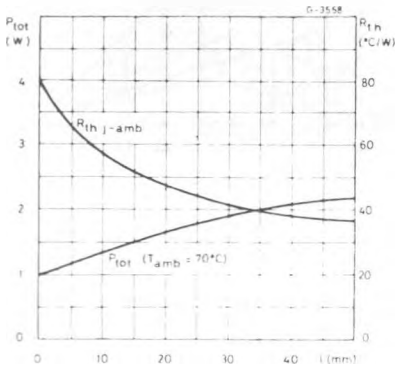


Figure 16 : Maximum Dissippable Power and Junction to Ambient Thermal Resistance vs. Side "α".



During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 15 : External Heatsink Mounting Example.

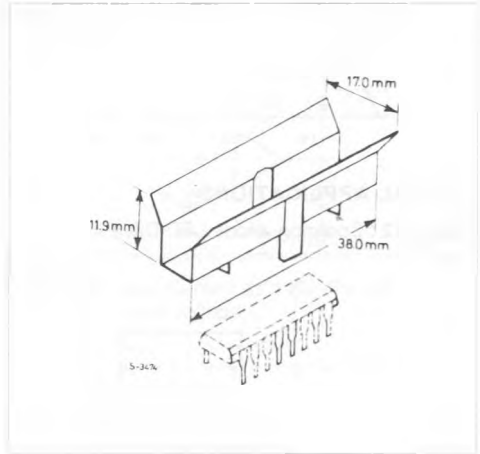


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

