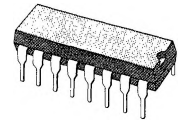
80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

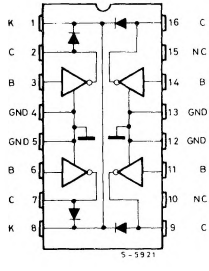
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

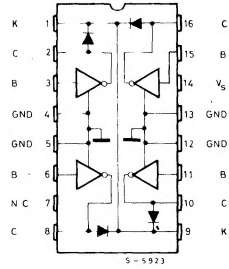


POWERDIP
12 + 2 + 2

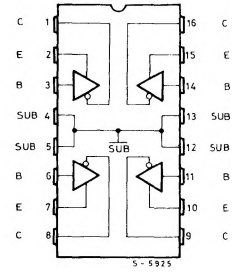
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



ULN2069B
ULN2071B

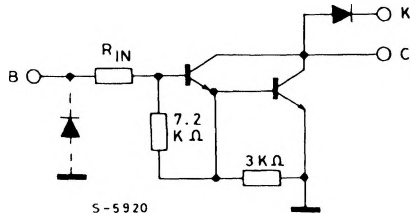


ULN2075B
ULN2077B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for **ULN2075B – 2077B**	60	V
	for **ULN2067B – 2071B**	30	V
	for **ULN2065B – 2069B**	15	V
I_I	Input Current	25	mA
V_s	Supply Voltage for **ULN2069B**	10	V
	for **ULN2071B**	20	V
P_{tot}	Power Dissipation : at T_{pins} = 90 °C	4.3	W
	at T_{amb} = 70 °C	1	W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



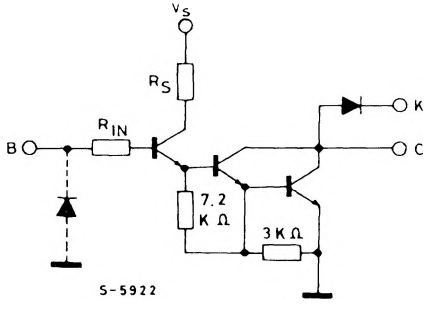
ULN2065B : R_{IN} = 350 Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2065B – ULN2067B**						
		V_{CE} = 80 V				100	µA	1
		V_{CE} = 80 V	T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2065B – ULN2067B**						
		I_C = 100 mA	V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA	I_B = 625 µA			1.1	V	3
		I_C = 750 mA	I_B = 935 µA			1.2	V	
		I_C = 1 A	I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A	I_B = 2 mA			1.4	V	
		for **ULN2065B – ULN2067B**						
		I_C = 1.5 A	I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2065B**	V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2065B**	V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2067B**	V_i = 5 V	0.6		1.8	mA	
		for **ULN2067B**	V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2065B**						5
		V_{CE} = 2 V	I_C = 1 A			2	V	
		V_{CE} = 2 V	I_C = 1.5 A			2.5	V	
		for **ULN2067B**						
		V_{CE} = 2 V	I_C = 1 A			6.5	V	
		V_{CE} = 2 V	I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o				1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o				1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2065B – ULN2067B**						6
		V_R = 80 V				50	µA	
		V_R = 80 V	T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.75	V	7
		I_F = 1.5 A				2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

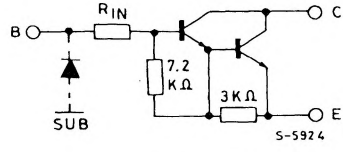


ULN2069B : R_{IN} = 2.5 KΩ, R_s = 900 Ω
ULN2071B : R_{IN} = 11.6 KΩ, R_s = 3.4 KΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2069B, V_s = 12 V for ULN2071B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2069B – ULN2071B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2069B – ULN2071B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2069B**					2
		I_C = 500 mA V_i = 2.75 V			1.1	V	
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		I_C = 1.5 A V_i = 2.75 V			1.5	V	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			1.1	V	
		I_C = 750 mA V_i = 5 V			1.2	V	
		I_C = 1 A V_i = 5 V			1.3	V	
		I_C = 1.25 A V_i = 5 V			1.4	V	
		I_C = 1.5 A V_i = 5 V			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2069B** V_i = 2.75 V			550	µA	4
		for **ULN2069B** V_i = 3.75 V			1000	µA	
		for **ULN2071B** V_i = 5 V			400	µA	
		for **ULN2071B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					5
		for **ULN2069B**			2.75	V	
		for **ULN2071B**			5		
I_s	Supply Current	for **ULN2069B**					8
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2069B – ULN2071B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350 Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2075B – ULN2077B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2075B – ULN2077B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2075B – ULN2077B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2075B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2075B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2077B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2077B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2075B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2077B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

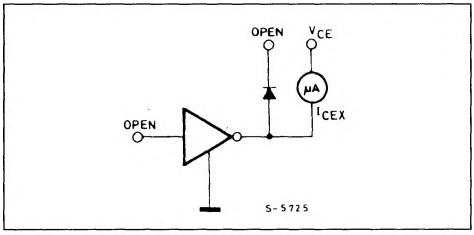


Figure 2.

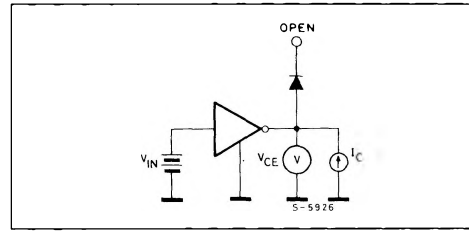


Figure 3.

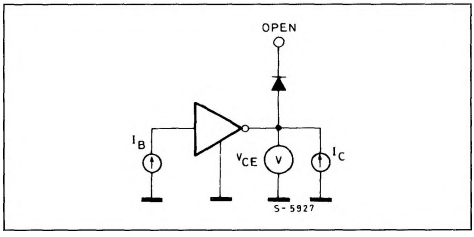


Figure 4.

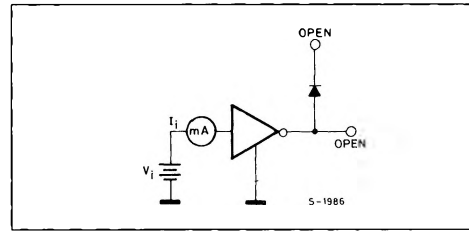


Figure 5.

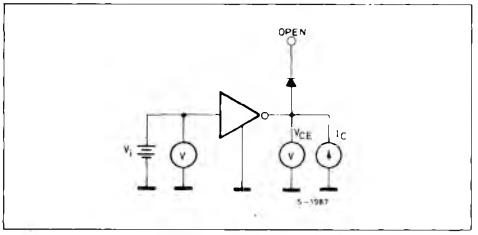


Figure 6.

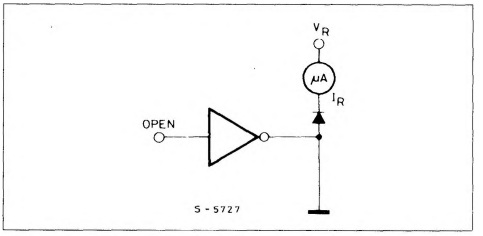


Figure 7.

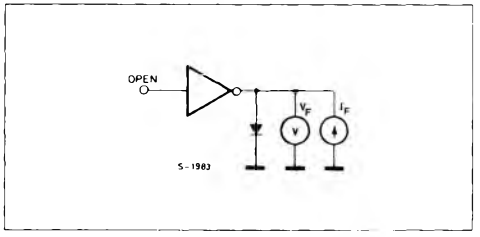


Figure 8.

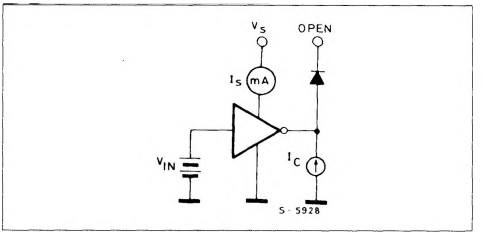


Figure 9 : Input Current as a Function of Input Voltage.

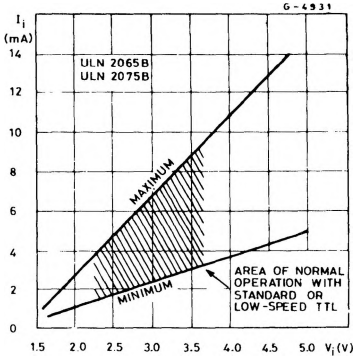


Figure 10 : Input Current as a Function of Input Voltage.

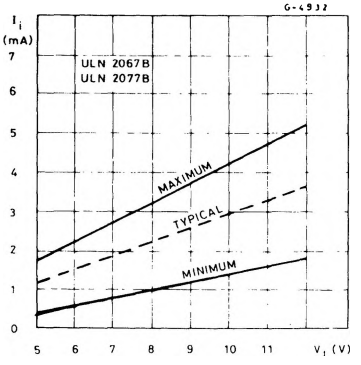
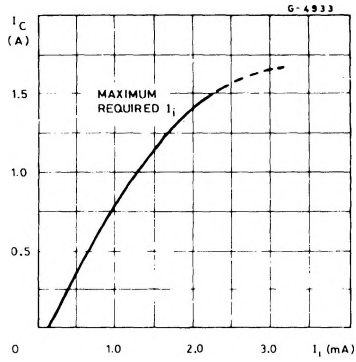


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

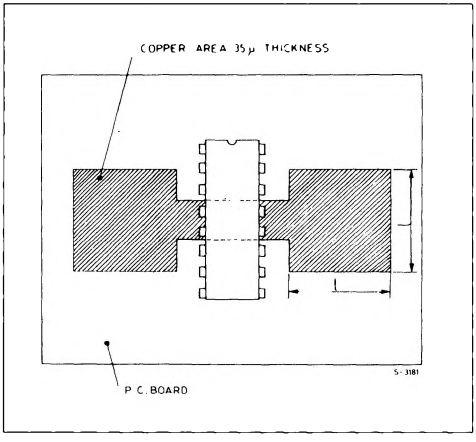


Figure 13 : External Heatsink Mounting Example.

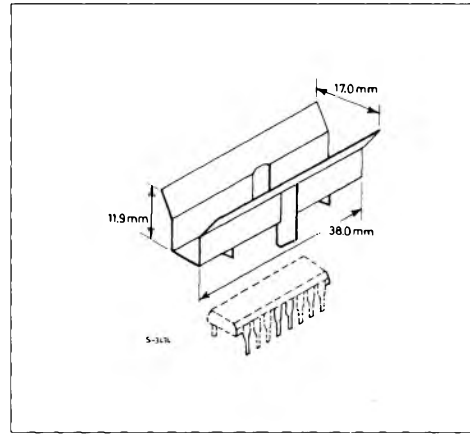


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

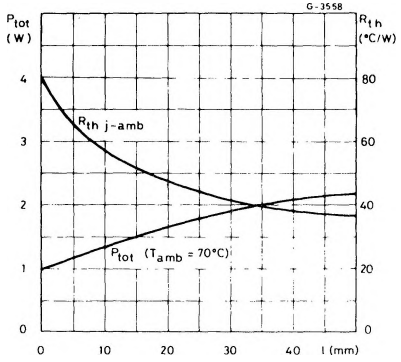


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.