



SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

DESCRIPTION

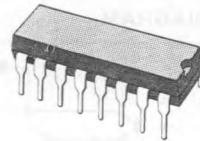
The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

The four versions interface to all common logic families :

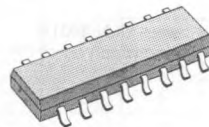
ULN2001A	General Purpose. DTL. TTL. PMOS. CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL. CMOS
ULN2004A	6-15 V CMOS. PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal print-heads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



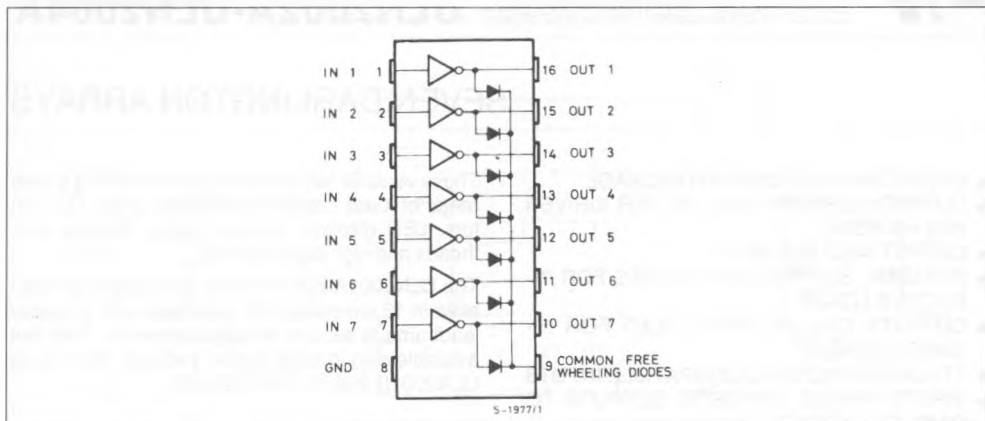
SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

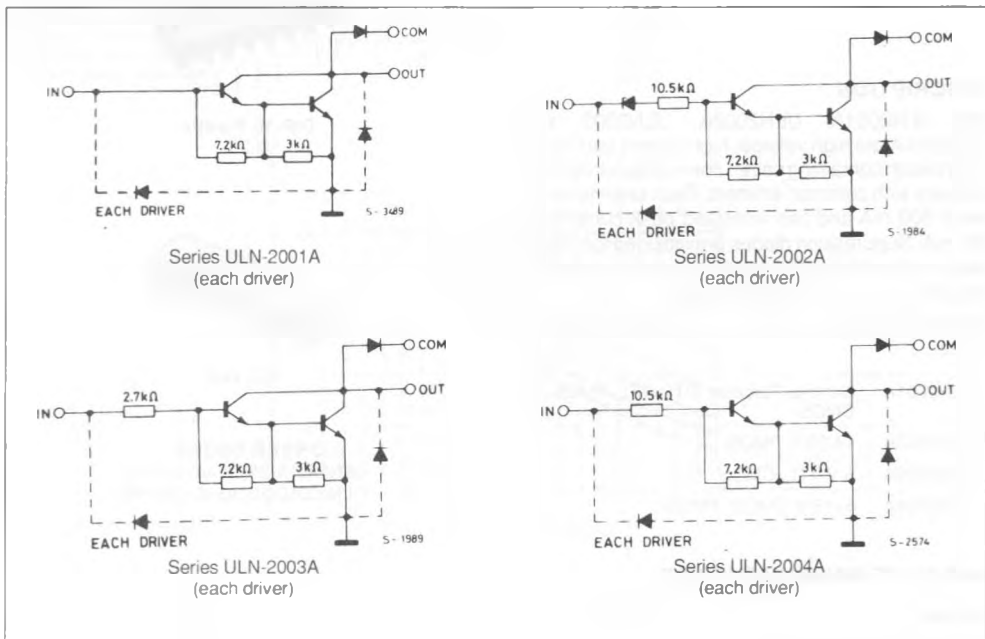
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	- 20 to 85	°C
T_{stg}	Storage Temperature Range	- 55 to 150	°C
T_j	Junction Temperature	150	°C

PIN CONNECTION



SCHEMATIC DIAGRAM



THERMAL DATA

			DIP-16	SO-16
$R_{th(j-c)}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.	
I_{CEX}	Output Leakage Current	$V_{CE} = 50\text{ V}$			50	μA	1a	
		$T_{amb} = 70\text{ }^{\circ}\text{C}$	$V_{CE} = 50\text{ V}$		100	μA	1a	
		$T_{amb} = 70\text{ }^{\circ}\text{C}$ for ULN2002A	$V_{CE} = 50\text{ V}$	$V_i = 6\text{ V}$		500	μA	1b
		for ULN2004A	$V_{CE} = 50\text{ V}$	$V_i = 1\text{ V}$		500	μA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 100\text{ mA}$	$I_B = 250\text{ }\mu\text{A}$	0.9	1.1	V	2	
		$I_C = 200\text{ mA}$	$I_B = 350\text{ }\mu\text{A}$	1.1	1.3	V	2	
		$I_C = 350\text{ mA}$	$I_B = 500\text{ }\mu\text{A}$	1.3	1.6	V	2	
$I_{(ON)}$	Input Current	for ULN2002A	$V_i = 17\text{ V}$	0.82	1.25	mA	3	
		for ULN2003A	$V_i = 3.85\text{ V}$	0.93	1.35	mA	3	
		for ULN2004A	$V_i = 5\text{ V}$	0.35	0.5	mA	3	
		$V_i = 12\text{ V}$	1	1.45	mA	3		
$I_{C(1)}$	Input Current	$T_{amb} = 70\text{ }^{\circ}\text{C}$	$I_C = 500\text{ }\mu\text{A}$	50	65	μA	4	
$V_{I(ON)}$	Input Voltage	for ULN2002A	$V_{CE} = 2\text{ V}$			13	V	5
		for ULN2003A	$V_{CE} = 2\text{ V}$	$I_C = 300\text{ mA}$				
		$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$		2.4	V	5	
		$V_{CE} = 2\text{ V}$	$I_C = 250\text{ mA}$		2.7	V	5	
		$V_{CE} = 2\text{ V}$	$I_C = 300\text{ mA}$		3	V	5	
		for ULN2004A	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$		5	V	5
		$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$		6	V	5	
$V_{CE} = 2\text{ V}$	$I_C = 275\text{ mA}$		7	V	5			
$V_{CE} = 2\text{ V}$	$I_C = 350\text{ mA}$		8	V	5			
h_{FE}	DC Forward Current Gain	for ULN2001A	$V_{CE} = 2\text{ V}$	$I_C = 350\text{ mA}$	1000		—	2
C	Input Capacitance			15	25	pF	—	
t_{PLH}	Turn-on Delay Time	0.5 V to 0.5 V_O		0.25	1	μs	—	
t_{PHL}	Turn-off Delay Time	0.5 V to 0.5 V_O		0.25	1	μs	—	
I_R	Clamp Diode Leakage Current	$V_R = 50\text{ V}$			50	μA	6	
		$T_{amb} = 70\text{ }^{\circ}\text{C}$	$V_R = 50\text{ V}$		100	μA	6	
V_F	Clamp Diode Forward Voltage	$I_F = 350\text{ mA}$		1.7	2	V	7	

TEST CIRCUITS

Figure 1a.

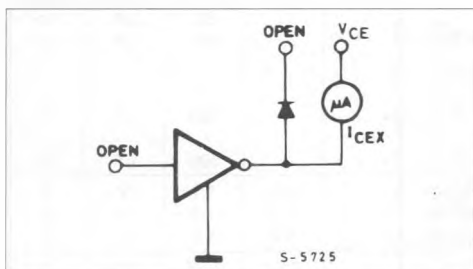


Figure 1b.

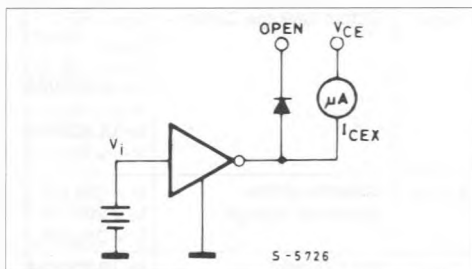


Figure 2.

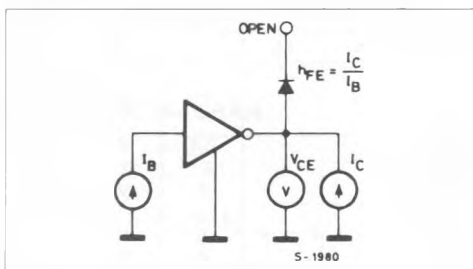


Figure 3.

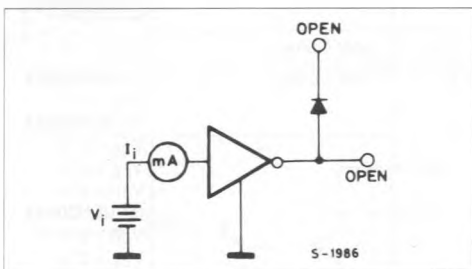


Figure 4.

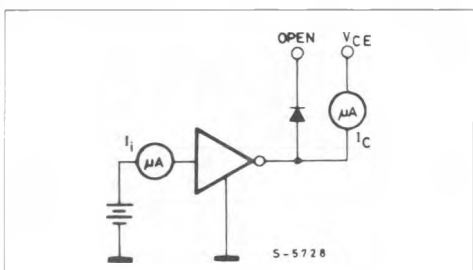


Figure 5.

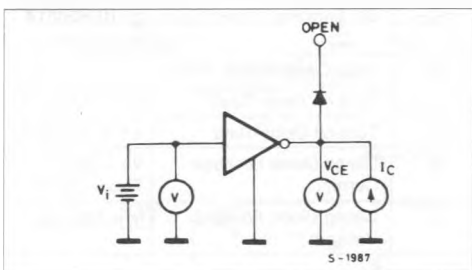


Figure 6.

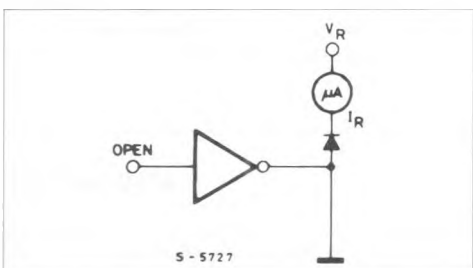


Figure 7.

