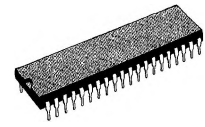
SGS-THOMSON MICROELECTRONICS

UEB4732

A.C. PLASMA PANEL DRIVER

- 32-BIT SHIFT REGISTER WITH LATCHES
- DECODING LOGIC CIRCUIT
- LOW TO HIGH VOLTAGE INTERFACE FOR DIRECT CONNECTION TO 32 ELECTRODES

DIP-40
(Plastic)



ORDER CODE : UEB4732DP

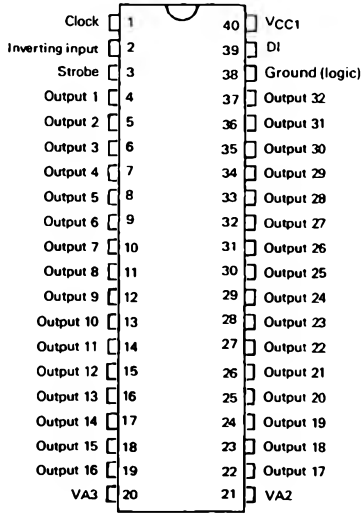
DESCRIPTION

UEB4732 is a BIMOS* IC's especially designed to provide selective and sustain signals needed by the X and Y electrodes of an A.C. plasma panel.

Realizing a complete A.C. plasma panel control system requires only UEB4732 and two high voltage common amplifiers for rows and columns of the panel. The whole network is driven by a few CMOS logical signals.

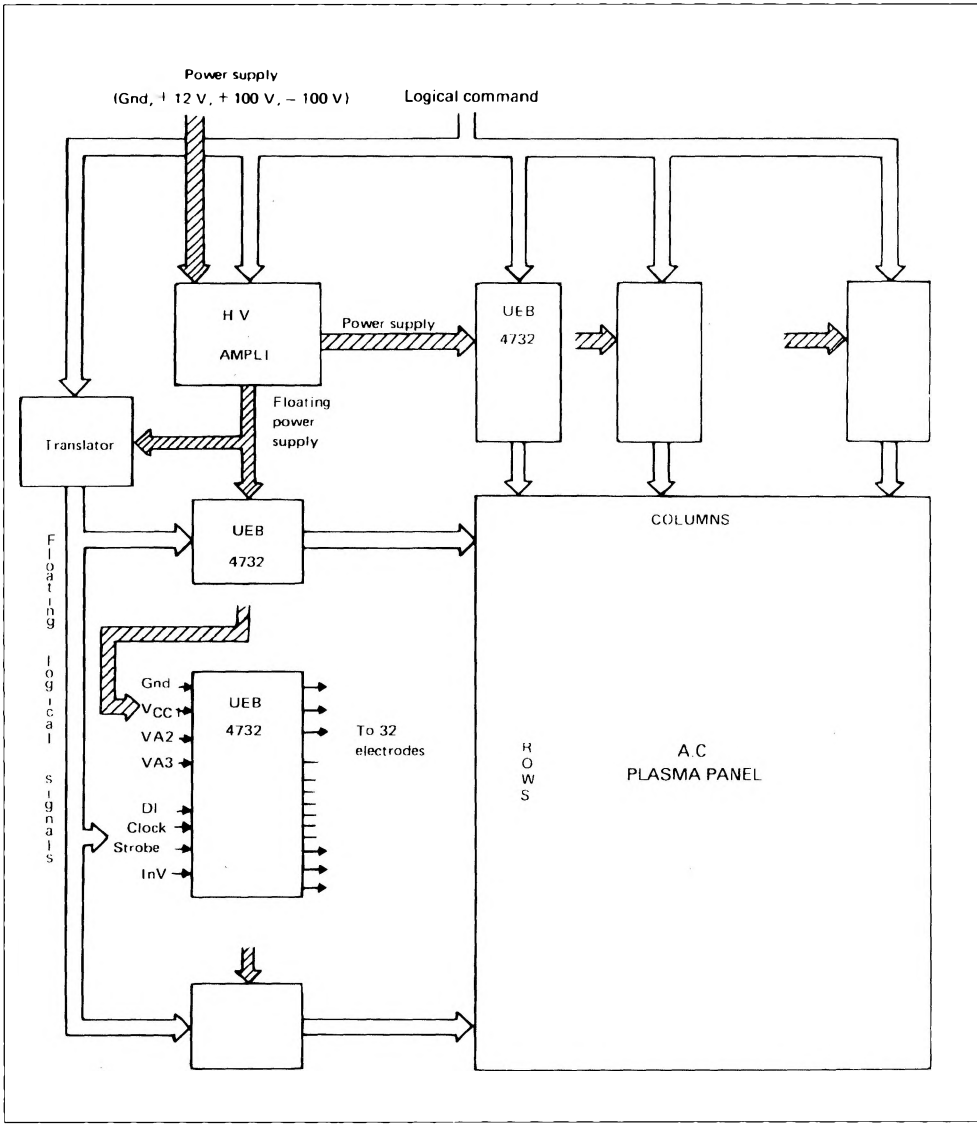
* Bipolar CMOS and complementary DMOS on same chip.

PIN CONNECTION



- 4 CMOS compatible logic inputs : DI, Clock, Strobe, Inv.
- 32 totem pole 100 V outputs, with clamping diodes to the VA2 and VA3 inputs.
- Logic supplies (Ground and V_{CC1}) separated from hight voltage (VA2, VA3) to avoid disturbances.

TYPICAL APPLICATION

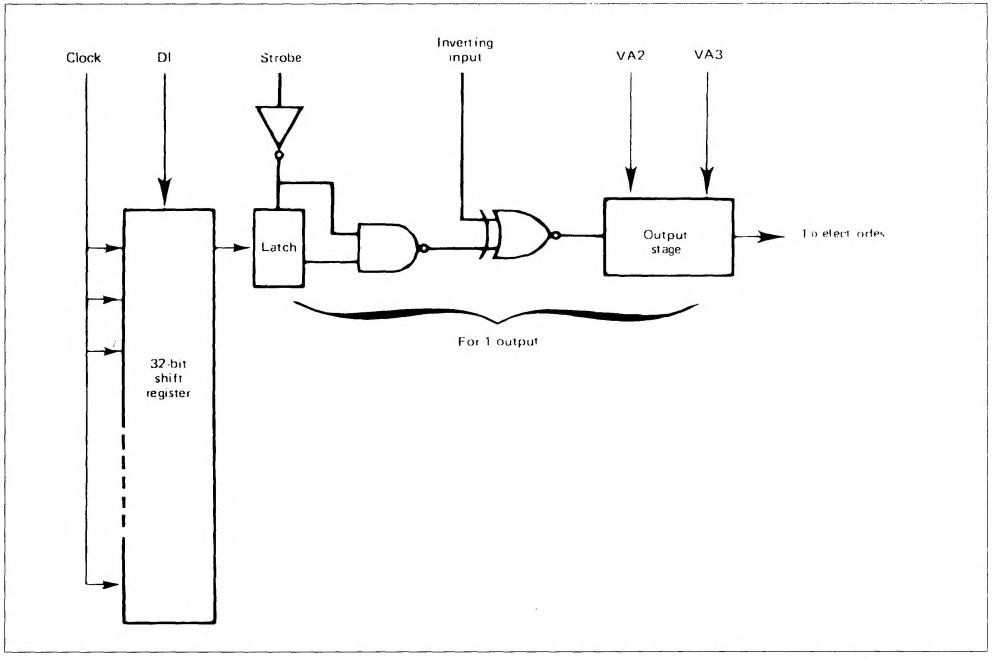


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC1}	Logic Supply Voltage	18	V
V_{A2}	V_{A2} Voltage ($V_{A2} \geq V_{A3}$)	120	V
V_{A3}	V_{A3} Voltage	10	V
V_i	Input Voltage Range	− 0.3 to V_{CC1} + 0.3	V

NOTE: Voltage values are with respect to network ground terminal (ground logic).

SCHEMATIC DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS (over recommended operating range)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	High Level Dropout Voltage (for one output) V_{A2} > 20 V				V
	− I_{OH} = − 10 mA		5	10	
	− I_{OH} = − 20 mA		10	20	
V_{OL}	Low Level Dropout Voltage (for one output) V_{A3} = Ground				V
	− I_{OL} = 10 mA		5	10	
	− I_{OL} = 20 mA		10	20	
V_{OK}	Dropout Clamp Voltage				V
	− I_O = ± 100 mA in One Output			2	
	− I_O = ± 100 mA Simultaneously in the 32 Outputs			3	
f_{clock}	Maximum Clock Pulse Frequency	4	8		MHz

* All typical values are at V_{CC1} = 12 V, T_{amb} = 25 °C.

RECOMMANDED OPERATING CONDITIONS (voltage values are referred to logic ground of the IC)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Logic Supply Voltage	10		15	V
V_{A2}	V_{A2} Voltage ($V_{A2} \geq V_{A3}$)	– 0.6		120	V
V_{A3}	V_{A3} Voltage	– 0.6		10	V
I_O	Peak Current (for one output) – High Level V_{A2} > 20 V – Low Level V_{A3} = Ground		 – 20 20		mA
I_O	Peak Clamp Current (for one output)		± 100		mA
T_{amb}	Operating Free Air Temperature UEB4732	 0		 + 70	°C

FUNCTION TABLE

Functions	Data	Inputs		Strobe	Shift Register			Latchs			Outputs		
		Clock	Inv.		R1	R2	R32	L1	L2	L32	01	02	032
LOAD	H	↑	X	X	H	R1n	R31n	R1s	R2s	R32s	Levels at 01 through 032 depend on Inv. and strobe (see "strobe").		
	L	↑	X	X	L	R1n	R31n	R1s	R2s	R32s			
LATCH	X	H	L	↓	R1n	R2n	R32n	R1n	R2n	R32n	R1n	$\overline{R2n}$	$\overline{R32n}$
	X	H	H	↓	R1n	R2n	R32n	R1n	R2n	R32n	$\overline{R1n}$	R2n	$\overline{R32n}$
STROBE	X	X	L	L	Levels at R1 through R32 depend only on data and clock (see "load").			R1s	R2s	R32s	$\overline{R1s}$	$\overline{R2s}$	$\overline{R32s}$
	X	X	H	L				R1s	R2s	R32s	$\overline{R1s}$	$\overline{R2s}$	$\overline{R32s}$
	X	X	L	H				R1	R2	R32	L	L	L
	X	X	H	H				R1	R2	R32	H	H	H

H = High level L = Low level X = Irrelevant

↑ = Low to high transition ↓ = High to low transition

For the outputs, the high level (H) is V_{A2}, the low level (L) is V_{A3}.

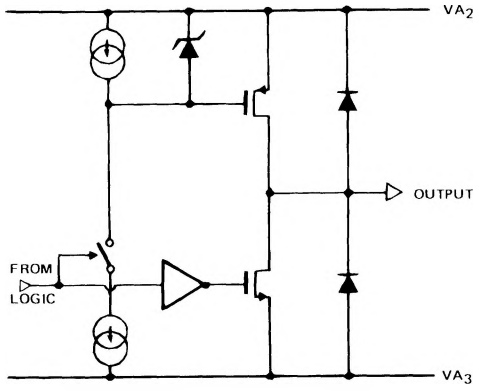
R1.....R32 = Levels currently at internal outputs of shift register.

R1n....R32n = Levels at shift register outputs R1 through R32, respectively, before the most recent ↑ transition of clock.

R1s....R32s = Levels at shift register outputs R1 through R32, respectively, before the most recent ↓ transition of strobe (levels currently stored by the 32 latchs L1 through L32).

$\overline{R1s}$.....$\overline{R32s}$ = Logical inversion of R1s.....R32s.

SCHEMATIC OF ONE OUTPUT STAGE



During the sustaining signal, $V_{A2} = V_{A3}$ and the current flows through the two clamp diodes.

During the selective signals (write and erase on the plasma panel), V_{A2} is at high voltage (typ. 100 V, referred to logic ground) V_{A3} is equal to logic ground, and the output is selectively adressed by complementary by DMOS stage.

DESCRIPTION

The UEB4732 is designed to provide easily the line and the column select operation of a plasma display panel. For an use on the X axis of the panel, the Inv. input is set at a steady low level, the outputs are normally low and are selectively switched high when the strobe input is low. For an use on the Y axis of the panel, the Inv. input is set at a steady high level, the outputs are normally high and are selectively switched low when the strobe input is low (the 32 bit data is inverted).

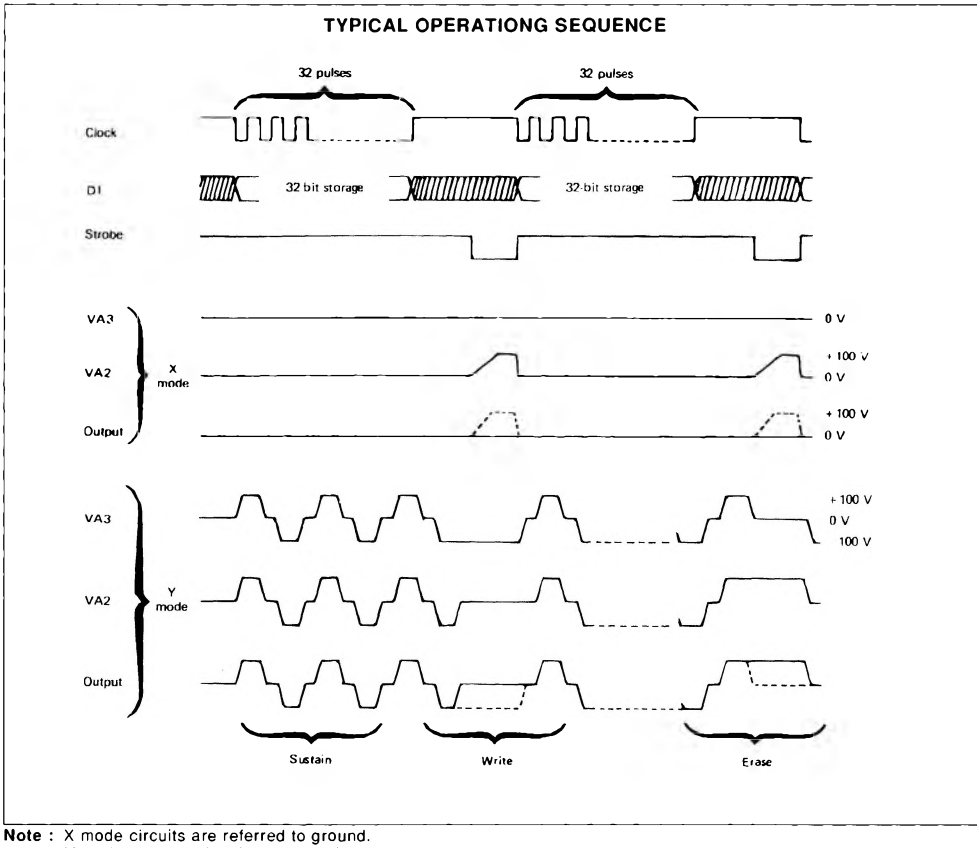
The Inv. input may also be used as a sustain input : when strobe is high, if the Inv. input is switched low, all outputs switch low, if the Inv. input is switched high, all outputs switch high.

Data is enterred serially in the shift register, on the low to high level transition of clock. It is stored in the 32 latchs on the high to low level transition of strobe, so the outputs are stable during the low level of strobe, regradless of the state of clock and data, and a new data can be enterred immediately.

The logical voltage reference (ground logic) and the high voltage reference (V_{A3}) are separated to avoid disturbances.

All output stages are complementary DMOS and contain clamp diodes to the V_{A2} and V_{A3} supply inputs. These diodes are designed to provide the peak current of the sustaining signal (typ. 100 mA/output) without distorsion of the signal.

TIMING DIAGRAM



Note : X mode circuits are referred to ground.
Y mode ones are floating on sustaining voltage.
In X mode, Inv. input is low.
In Y mode, Inv. input is high.