10-Rail Power-Supply Sequencer and Monitor With ACPI Support

Check for Samples: UCD9090-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **Monitor and Sequence 10 Voltage Rails**
  - **All Rails Sampled Every 400 µs**
  - **12-Bit ADC With 2.5-V, 0.5% Internal V_{REF}**
  - **Sequence Based on Time, Rail, and Pin Dependencies**
  - **Four Programmable Undervoltage and Overvoltage Thresholds per Monitor**
- **Nonvolatile Error and Peak-Value Logging per Monitor (up to 30 Fault Detail Entries)**
- **Closed-Loop Margining for 10 Rails**
  - **Margin Output Adjusts Rail Voltage to Match User-Defined Margin Thresholds**
- **Programmable Watchdog Timer and System Reset**
- **Flexible Digital I/O Configuration**
- **Pin-Selected Rail States**
- **Multiphase PWM Clock Generator**
  - **Clock Frequencies From 15.259 kHz to 125 MHz**
  - **Capability to Configure Independent Clock Outputs for Synchronizing Switch-Mode Power Supplies**
- **JTAG, I²C, SMBus, and PMBus™ Interfaces**

APPLICATIONS

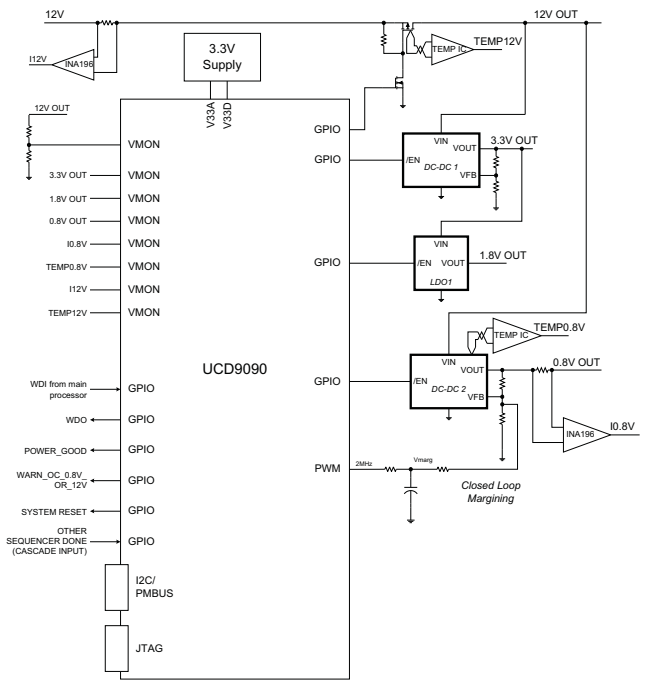
Any System Requiring Sequencing and Monitoring of Multiple Power Rails

DESCRIPTION

The UCD9090-Q1 is a 10-rail PMBus- and I²C-addressable power-supply sequencer and monitor. The device integrates a 12-bit ADC for monitoring up to 10 power-supply voltage inputs. Twenty-three GPIO pins are usable for power-supply enables, power-on reset signals, external interrupts, cascading, or other system functions. Ten of these pins offer PWM functionality. Using these pins, the UCD9090-Q1 offers support for margining and for general-purpose PWM functions.

One can achieve specific power states using the pin-selected rail-states feature. This feature allows enabling or disabling any rail by the use of up to three GPIs. This feature is useful for implementing system low-power modes and the Advanced Configuration and Power Interface (ACPI) specification that is used for hardware devices.

Use of the TI Fusion Digital Power™ designer software assists in device configuration. This PC-based graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.



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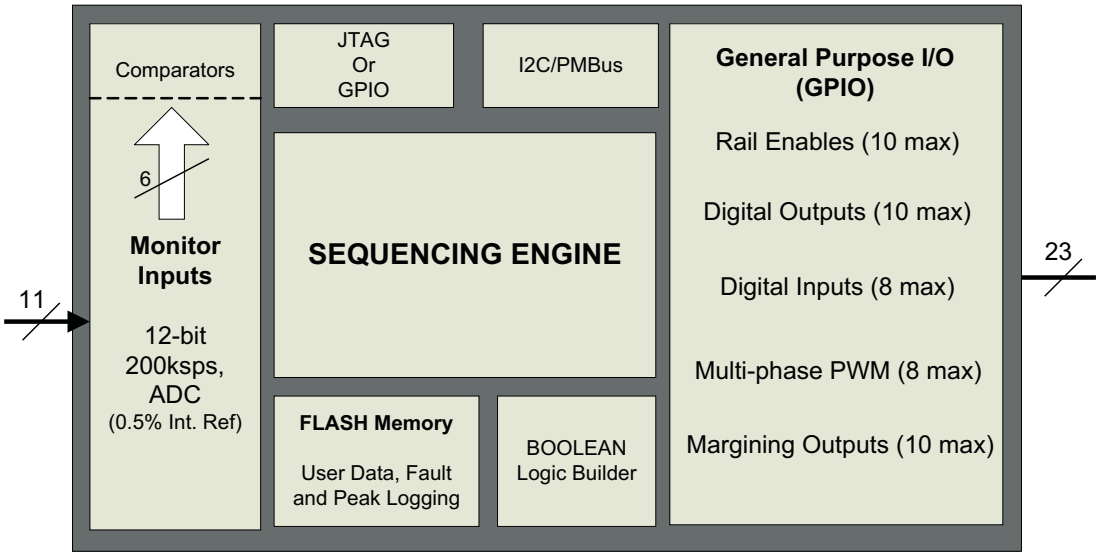
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



48-pin QFN

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Voltage applied at V33D to DV_{SS}		–0.3 to 3.8	V
Voltage applied at V33A to AV_{SS}		–0.3 to 3.8	V
Voltage applied to any other pin(2)		–0.3 to (V33A + 0.3)	V
Storage temperature (T_{stg})		–40 to 150	°C
ESD rating	Human-body model (HBM)	2.5	kV
	Charged-device model (CDM)	750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.

THERMAL INFORMATION

THERMAL METRIC(1)		UCD9090-Q1 RGZ (48 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	25	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	8.9	
θ_{JB}	Junction-to-board thermal resistance	5.5	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	1.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage during operation (V_{33D}, V_{33DIO}, V_{33A})	3	3.3	3.6	V
Operating free-air temperature range, T_A	–40		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current(1)	V_{V33A} = 3.3 V		8		mA
I_{V33DIO}		V_{V33DIO} = 3.3 V		2		mA
I_{V33D}		V_{V33D} = 3.3 V		40		mA
I_{V33D}		V_{V33D} = 3.3 V, storing configuration parameters in flash memory		50		mA
ANALOG INPUTS (MON1–MON13)						
V_{MON}	Input voltage range	MON1–MON10	0		2.5	V
		MON11	0.2		2.5	V
INL	ADC integral nonlinearity		–4		4	LSB
DNL	ADC differential nonlinearity		–2		2	LSB
I_{lkg}	Input leakage current	3 V applied to pin			100	nA
I_{OFFSET}	Input offset current	1-kΩ source impedance	–5		5	µA
R_{IN}	Input impedance	MON1–MON10, ground reference	8			MΩ
		MON11, ground reference	0.5	1.5	3	MΩ
C_{IN}	Input capacitance				10	pF
$t_{CONVERT}$	ADC sample period	12 voltages sampled, 3.89 µs/sample		400		µs
V_{REF}	ADC 2.5 V, internal reference accuracy	0°C to 125°C	–0.5%		0.5%	
		–40°C to 125°C	–1%		1%	
ANALOG INPUT (PMBUS_ADDRx)						
I_{BIAS}	Bias current for PMBus Addr pins		9		11	µA
V_{ADDR_OPEN}	Voltage – open pin	PMBUS_ADDR0, PMBUS_ADDR1 open	2.26			V
V_{ADDR_SHORT}	Voltage – shorted pin	PMBUS_ADDR0, PMBUS_ADDR1 short to ground			0.124	V

(1) Device programmed but not configured, and no peripherals connected to any pins, are the basis for typical supply current values.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DIGITAL INPUTS AND OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(2), V_{33DIO} = 3 V			Dgnd + 0.3	V
V_{OH}	High-level output voltage	I_{OH} = –6 mA(3), V_{33DIO} = 3 V	V_{33DIO} –0.6			V
V_{IH}	High-level input voltage	V_{33DIO} = 3 V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V
MARGINING OUTPUTS						
f_{PWM_FREQ}	MARGINING-PWM frequency	FPWM1-8	15.260		125,000	kHz
		PWM1-2	0.001		7800	
$DUTY_{PWM}$	MARGINING-PWM duty-cycle range		0%		100%	
SYSTEM PERFORMANCE						
V_{DD}Slew	Minimum V_{DD} slew rate	V_{DD} slew rate between 2.3 V and 2.9 V	0.25			V/ms
V_{RESET}	Supply voltage at which device comes out of reset	For power-on reset (POR)			2.4	V
t_{RESET}	Low-pulse duration needed at $\overline{\text{RESET}}$ pin	To reset device during normal operation	2			µs
$f_{(PCLK)}$	Internal oscillator frequency	T_A = 125°C, T_A = 25°C	240	250	260	MHz
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase-and-write cycles	T_J = 25°C	20			K cycles

(2) The maximum total current, I_{OL}max, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(3) The maximum total current, I_{OH}max, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.

PMBus, SMBus, I²C

The following section shows the timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus.

I²C, SMBus, PMBus TIMING REQUIREMENTS

T_A = –40°C to 85°C, 3 V < V_{DD} < 3.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SMB)}$	SMBus or PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		400	kHz
$f_{(I2C)}$	I²C operating frequency	Slave mode, SCL 50% duty cycle	10		400	kHz
$t_{(BUF)}$	Bus free time between start and stop		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.26			µs
$t_{(SU:STA)}$	Repeated-start setup time		0.26			µs
$t_{(SU:STO)}$	Stop setup time		0.26			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		50			ns
$t_{(TIMEOUT)}$	Error signal or detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		0.5			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.26		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock-low slave-extend time	See (3)			25	ms
t_f	Clock or data fall time	See (4)			120	ns
t_r	Clock or data rise time	See (5)			120	ns

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device can extend the clock cycles in one message from initial start to the stop.
(4) Fall time t_f = 0.9 VDD to (V_{IL}MAX – 0.15)
(5) Rise time t_r = (V_{IL}MAX – 0.15) to (V_{IH}MIN + 0.15)

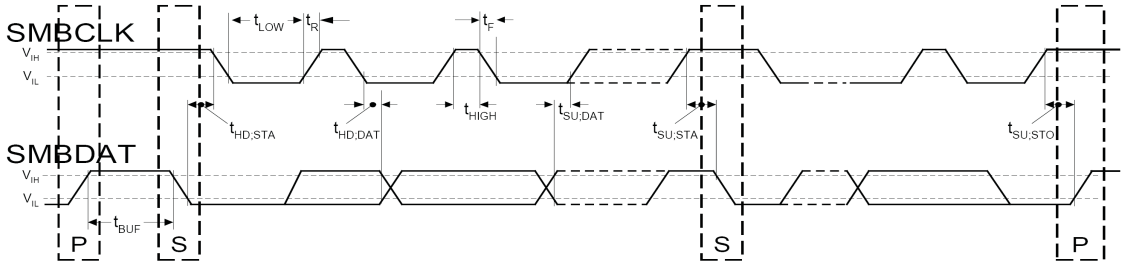


Figure 1. Timing Diagram for I²C and SMBus

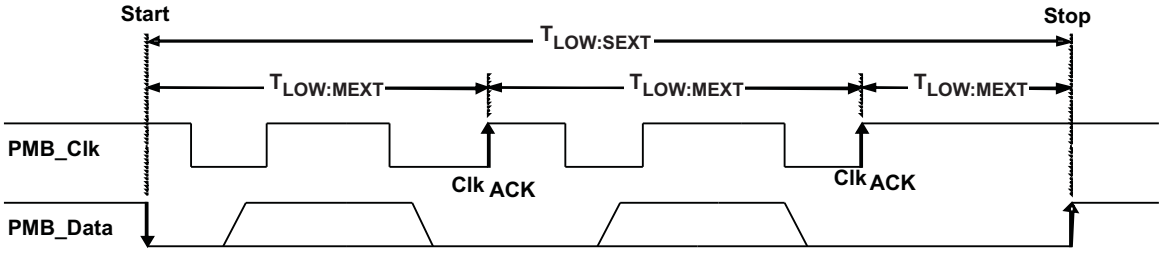


Figure 2. Bus Timing in Extended Mode

DEVICE INFORMATION

Figure 3. UCD9090-Q1 PIN ASSIGNMENT

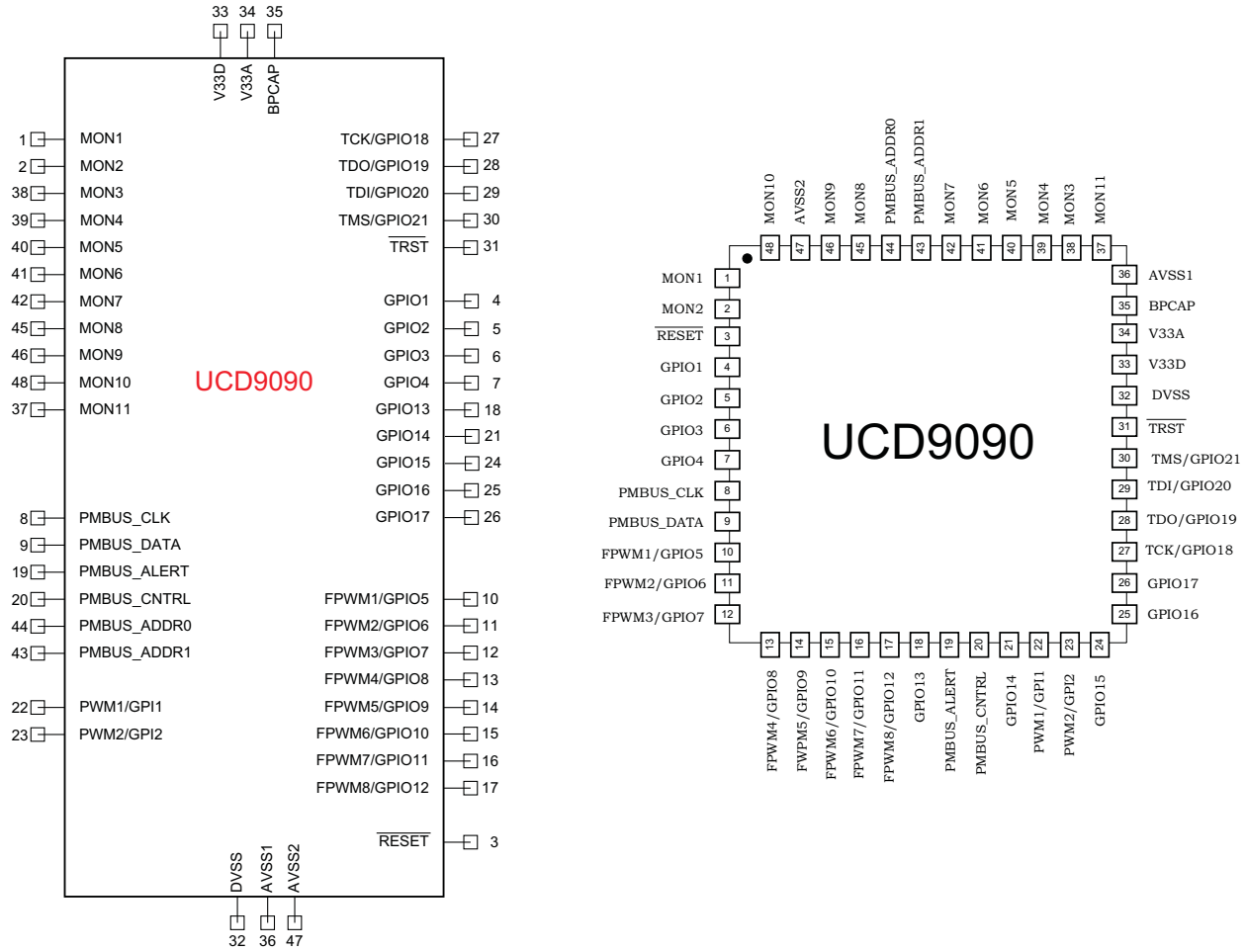


Table 1. PIN FUNCTIONS

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
ANALOG MONITOR INPUTS			
MON1	1	I	Analog input (0 V–2.5 V)
MON2	2	I	Analog input (0 V–2.5 V)
MON3	38	I	Analog input (0 V–2.5 V)
MON4	39	I	Analog input (0 V–2.5 V)
MON5	40	I	Analog input (0 V–2.5 V)
MON6	41	I	Analog input (0 V–2.5 V)
MON7	42	I	Analog input (0 V–2.5 V)
MON8	45	I	Analog input (0 V–2.5 V)
MON9	46	I	Analog input (0 V–2.5 V)
MON10	48	I	Analog input (0 V–2.5 V)
MON11	37	I	Analog input (0.2 V–2.5 V)
GPIO			
GPIO1	4	I/O	General-purpose discrete I/O

Table 1. PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
GPIO2	5	I/O	General-purpose discrete I/O
GPIO3	6	I/O	General-purpose discrete I/O
GPIO4	7	I/O	General-purpose discrete I/O
GPIO13	18	I/O	General-purpose discrete I/O
GPIO14	21	I/O	General-purpose discrete I/O
GPIO15	24	I/O	General-purpose discrete I/O
GPIO16	25	I/O	General-purpose discrete I/O
GPIO17	26	I/O	General-purpose discrete I/O
PWM OUTPUTS			
FPWM1/GPIO5	10	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM2/GPIO6	11	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM3/GPIO7	12	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM4/GPIO8	13	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM5/GPIO9	14	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM6/GPIO10	15	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM7/GPIO11	16	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM8/GPIO12	17	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
PWM1/GPI1	22	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PWM2/GPI2	23	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PMBus COMM INTERFACE			
PMBUS_CLK	8	I/O	PMBus clock (must have pullup to 3.3 V)
PMBUS_DATA	9	I/O	PMBus data (must have pullup to 3.3 V)
PMBUS_ALERT	19	O	PMBus alert, active-low, open-drain output (must have pullup to 3.3 V)
PMBUS_CNTRL	20	I	PMBus control
PMBUS_ADDR0	44	I	PMBus analog address input. Least-significant address bit
PMBUS_ADDR1	43	I	PMBus analog address input. Most-significant address bit
JTAG			
TCK/GPIO18	27	I/O	Test clock or GPIO
TDO/GPIO19	28	I/O	Test data out or GPIO
TDI/GPIO20	29	I/O	Test data in (tie to V_{dd} with 10-kΩ resistor) or GPIO
TMS/GPIO21	30	I/O	Test mode select (tie to V_{dd} with 10-kΩ resistor) or GPIO
$\overline{\text{TRST}}$	31	I	Test reset – tie to ground with 10-kΩ resistor
INPUT POWER AND GROUNDS			
$\overline{\text{RESET}}$	3		Active-low device reset input. Hold low for at least 2 µs to reset the device.
V33A	34		Analog 3.3-V supply. See the *Layout Guidelines* section.
V33D	33		Digital core 3.3-V supply. See the *Layout Guidelines* section.
BPCap	35		1.8-V bypass capacitor. See the *Layout Guidelines* section.
AVSS1	36		Analog ground
AVSS2	47		Analog ground
DVSS	32		Digital ground
QFP ground pad	NA		Thermal pad – tie to ground plane

FUNCTIONAL DESCRIPTION

TI FUSION GUI

The Texas Instruments *Fusion Digital Power Designer* is available for device configuration. This PC-based graphical user interface (GUI) offers an intuitive I^2C or PMBus interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip nonvolatile memory, and observe system status (voltage, and so forth). The data sheet references *Fusion Digital Power Designer* throughout as *Fusion GUI* and many sections include screenshots. Download the *Fusion GUI* from www.ti.com.

PMBUS INTERFACE

The PMBus is a serial interface specifically designed to support power management. Its basis is on the SMBus interface, built on the I^2C physical specification. The UCD9090-Q1 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands support the function of the device. For unique features of the UCD9090-Q1, defined MFR_SPECIFIC commands configure or activate those features. The *UCD90xxx Sequencer and System Health Controller PMBUS Command Reference* (SLVU352) defines these commands. One can find the most-current UCD90xxx PMBus™ Command Reference within the TI Fusion Digital Power Designer software via the Help Menu (Help, Documentation & Help Center, Sequencers tab, Documentation section).

This document makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The Power Management Bus Implementers Forum publishes the specification, which is available from www.pmbus.org.

The UCD9090-Q1 is PMBus compliant, in accordance with the *Compliance* section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support either 100-kHz or 400-kHz PMBus operation.

THEORY OF OPERATION

Modern electronic systems often use numerous microcontrollers, DSPs, FPGAs, and ASICs. Each device can have multiple supply voltages to power the core processor, analog-to-digital converter, or I/O. These devices are typically sensitive to the order and timing of how the voltages are sequenced on and off. The UCD9090-Q1 can sequence supply voltages to prevent malfunctions, intermittent operation, or device damage caused by improper power up or power down. Appropriate handling of under- and overvoltage faults can extend system life and improve long-term reliability. The UCD9090-Q1 stores power supply faults to on-chip nonvolatile flash memory for aid in system failure analysis.

Four-corner testing during system verification can improve system reliability. During four-corner testing, the system operates at the minimum and maximum expected ambient temperature and with each power supply set to the minimum and maximum output voltage, commonly referred to as margining. One use of the UCD9090-Q1 is to implement accurate closed-loop margining of up to 10 power supplies.

The UCD9090-Q1 10-rail sequencer can be used in a PMBus- or pin-based control environment. The TI Fusion GUI provides a powerful but simple interface for configuring sequencing solutions for systems having between one and 10 power supplies by using 10 analog voltage-monitor inputs, two GPIs, and 21 highly configurable GPIOs. A rail includes voltage, a power-supply enable, and a margining output. The rail definition must include at least one of these. After defining how the power-supply rails should operate in a particular system, the user can select analog input pins and GPIOs to monitor and enable each supply (Figure 4).

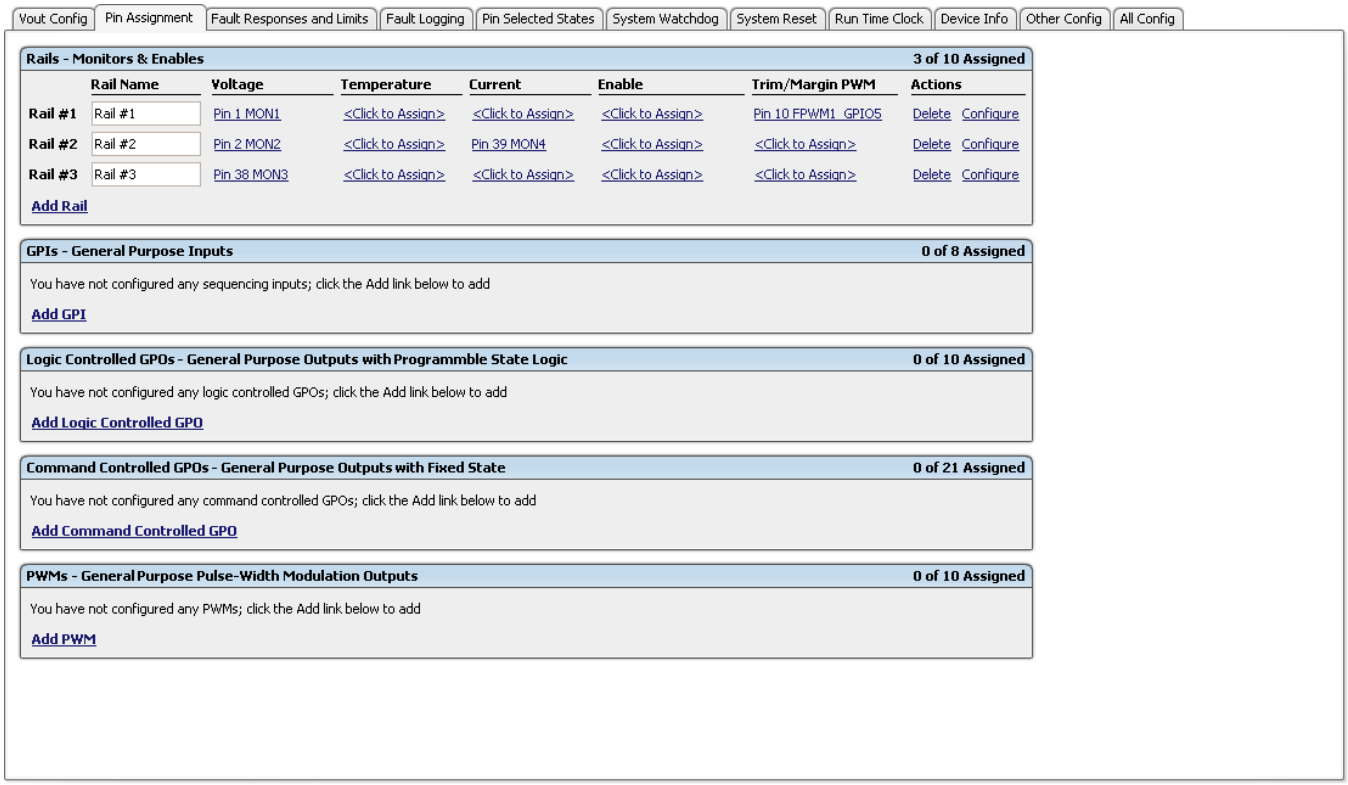


Figure 4. Fusion GUI Pin-Assignment Tab

After configuring the pins, select other key monitoring and sequencing criteria for each rail from the Vout Config tab (Figure 5):

- Nominal operating voltage (Vout)
- Undervoltage (UV) and overvoltage (OV) warning and fault limits
- Margin-low and margin-high values
- Power-good-on and power-good-off limits
- PMBus or pin-based sequencing control (On/Off Config)
- Rails and GPIs for sequence-on dependencies
- Rails and GPIs for sequence-off dependencies
- Turn-on and turn-off delay timing
- Maximum time allowed for a rail to reach POWER_GOOD_ON or POWER_GOOD_OFF after being enabled or disabled
- Other rails to turn off in case of a fault on a rail (fault-shutdown slaves)

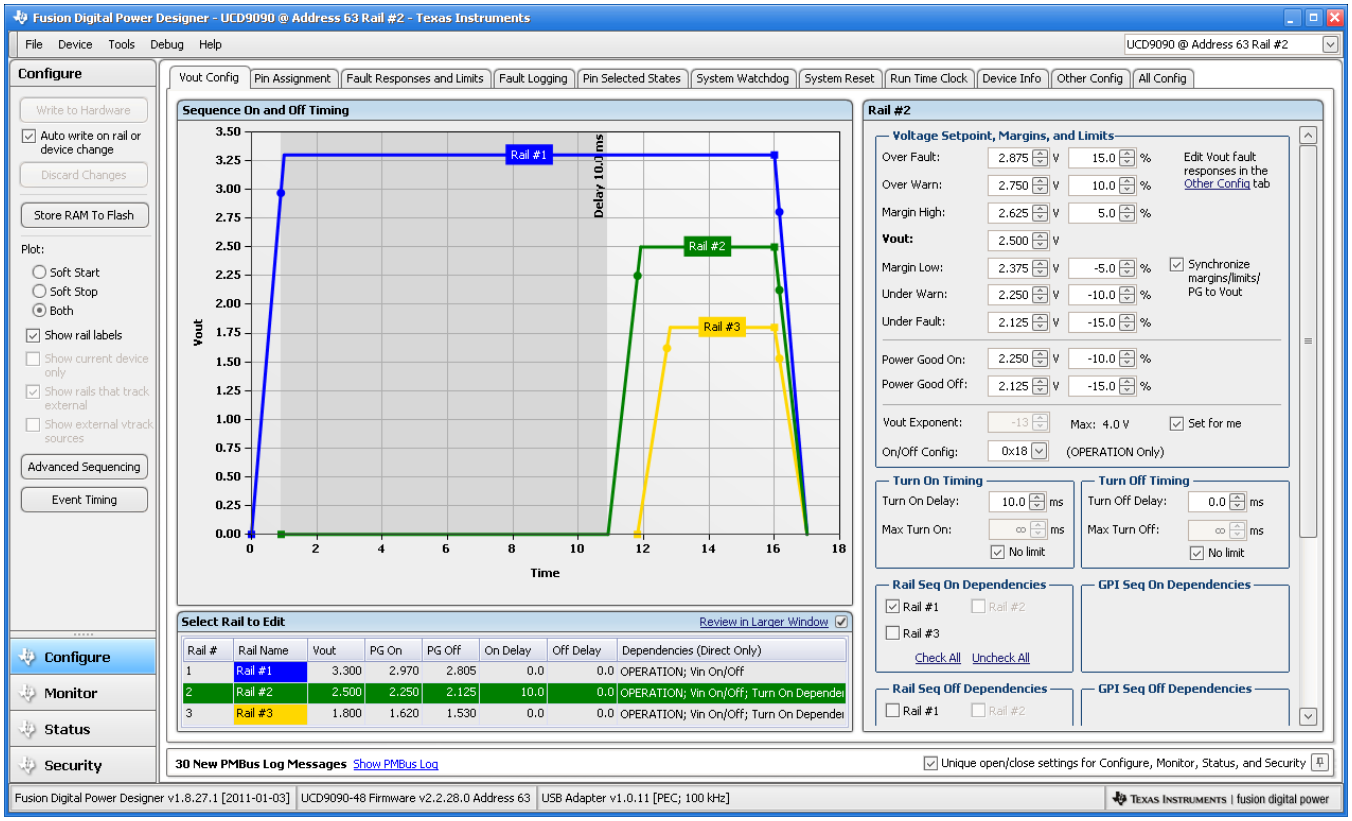


Figure 5. Fusion GUI V_{OUT}-Config Tab

The **Synchronize margins/limits/PG to Vout** checkbox is an easy way to change the nominal operating voltage of a rail and also update all of the other limits associated with that rail according to the percentages shown to the right of each entry.

The plot in the upper left section of Figure 5 shows a simulation of the overall sequence-on and sequence-off configuration, including the nominal voltage, the turnon and turnoff delay times, the power-good-on and power-good-off voltages, and any timing dependencies between the rails.

After a rail voltage has reached its POWER_GOOD_ON voltage and is in regulation, the device compares it against two UV and two OV thresholds in order to determine if it has exceeded a warning or fault limit. In case of a fault detection, the UCD9090-Q1 responds based on a variety of flexible, user-configured options. Faults can cause rails to restart, shut down immediately, sequence off using turnoff delay times, or shut down a group of rails and sequence them back on. Different types of faults can result in different responses.

The user selects fault responses, along with a number of other parameters including user-specific manufacturing information and external scaling and offset values, in the different tabs within the Configure function of the *Fusion GUI*. Once the configuration satisfies the user requirements, a user can write it to device SRAM if an I^2C or PMBus connects the *Fusion GUI* to a UCD9090-Q1. SRAM contents can then be stored to data flash memory so that the configuration remains in the device after a reset or power cycle.

The *Fusion GUI* Monitor page has a number of options, including a device dashboard and a system dashboard, for viewing and controlling device and system status.

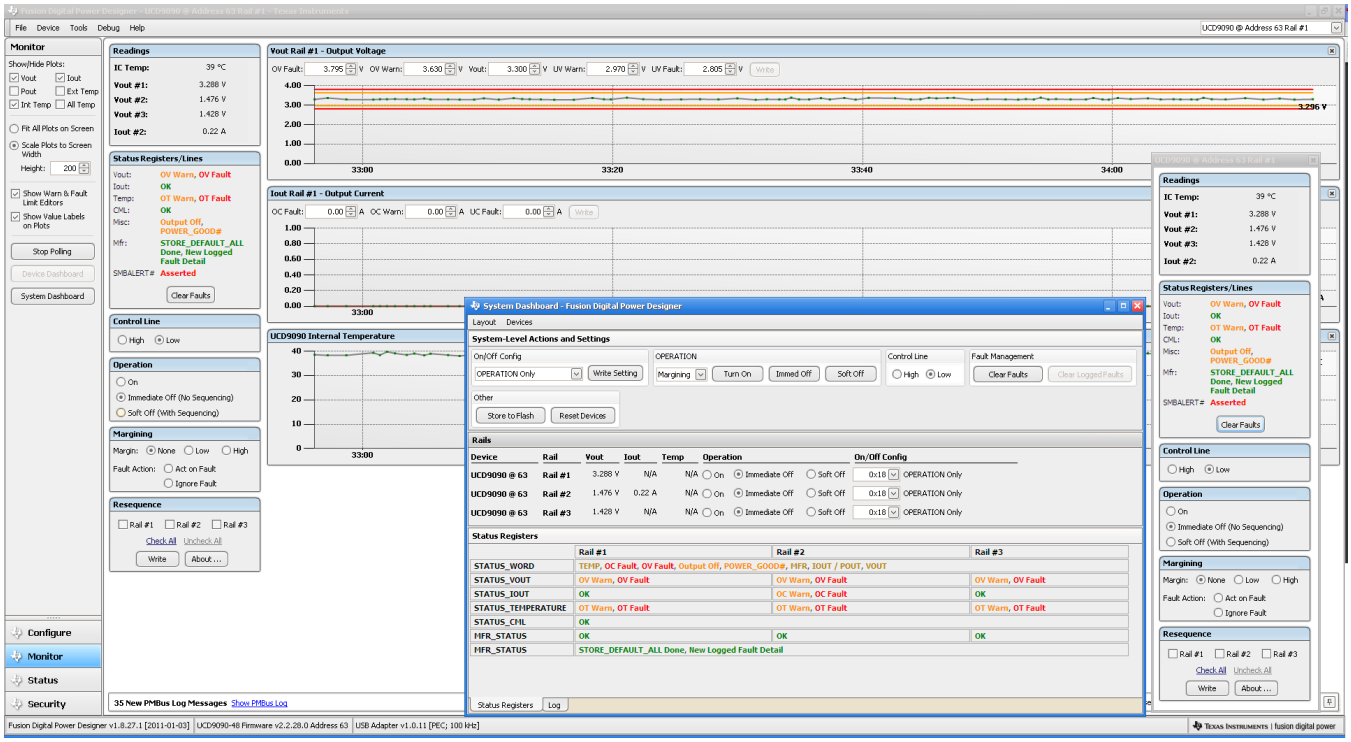


Figure 6. Fusion GUI Monitor Page

The UCD9090-Q1 also has status registers for each rail and the capability to log faults to flash memory for use in system troubleshooting. This is helpful in the event of a power-supply or system failure. The status registers (Figure 7) and the fault log (Figure 8) are available in the *Fusion GUI*. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* (SLVU352) and the PMBus Specification for detailed descriptions of each status register and supported PMBus commands.

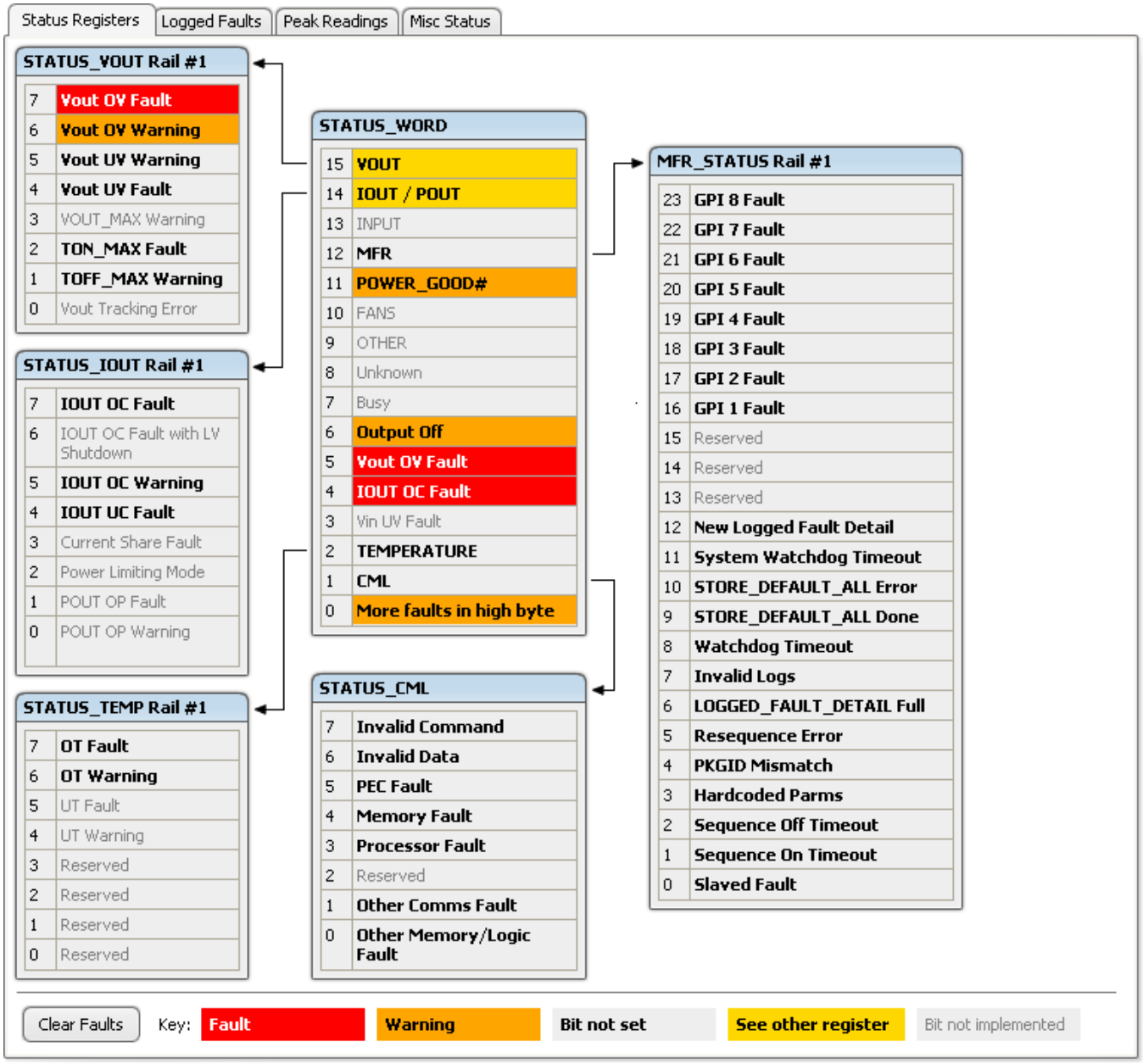


Figure 7. Fusion GUI Rail-Status Register

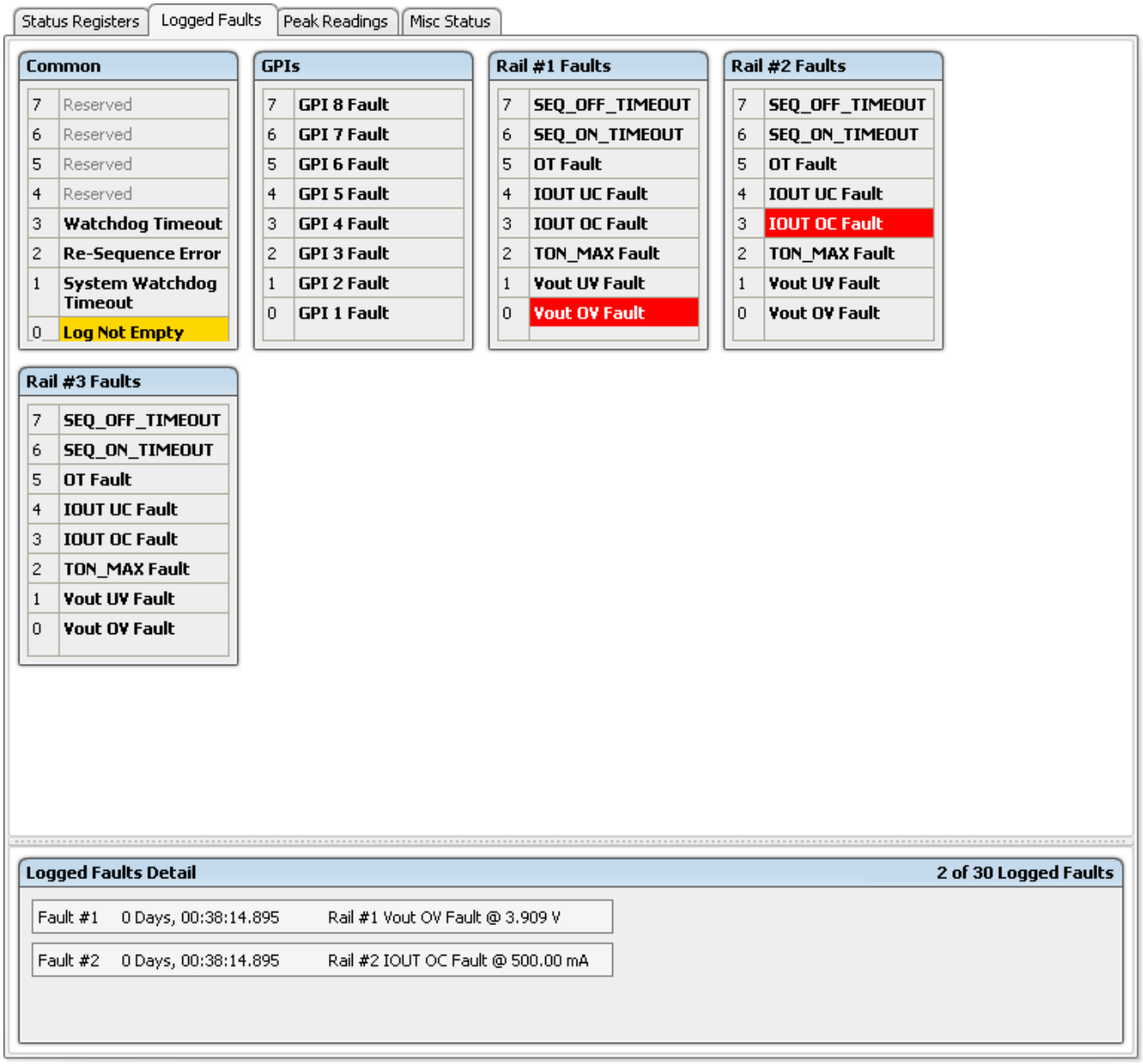


Figure 8. Fusion GUI Flash-Error Log (Logged Faults)

POWER-SUPPLY SEQUENCING

The UCD9090-Q1 can control the turnon and turnoff sequencing of up to 10 voltage rails by using a GPIO to set a power-supply enable pin high or low. In PMBus-based designs, the system PMBus master can initiate a sequence-on event by asserting the PMBUS_CNTRL pin or by sending the OPERATION command over the I^2C serial bus. In pin-based designs, one can also use the PMBUS_CNTRL pin to sequence-on and sequence-off.

The auto-enable setting ignores the OPERATION command and the PMBUS_CNTRL pin. Sequence-on starts at power up after each rail has its dependencies and time delays met. Consider a rail to be on or within regulation when the measured voltage for that rail crosses the power-good-on (POWER_GOOD_ON (1)) limit. The rail is still in regulation until the voltage drops below power-good-off (POWER_GOOD_OFF). Without having the voltage monitoring set for a given rail, that rail is considered ON if an OPERATION command, PMBUS CNTRL pin, or auto-enable commands it on and (TON_DELAY + TON_MAX_FAULT_LIMIT) time passes. Consider a rail OFF when commanded OFF and (TOFF_DELAY + TOFF_MAX_WARN_LIMIT) time passes.

Turnon Sequencing

The UCD9090-Q1 supports the following sequence-on options for each rail:

- Monitor only – do not sequence-on
- Fixed delay time (TON_DELAY) after an OPERATION command to turn on
- Fixed delay time after assertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails achieves regulation (POWER_GOOD_ON)
- Fixed time after a designated GPI has reached a user-specified state
- Any combination of the previous options

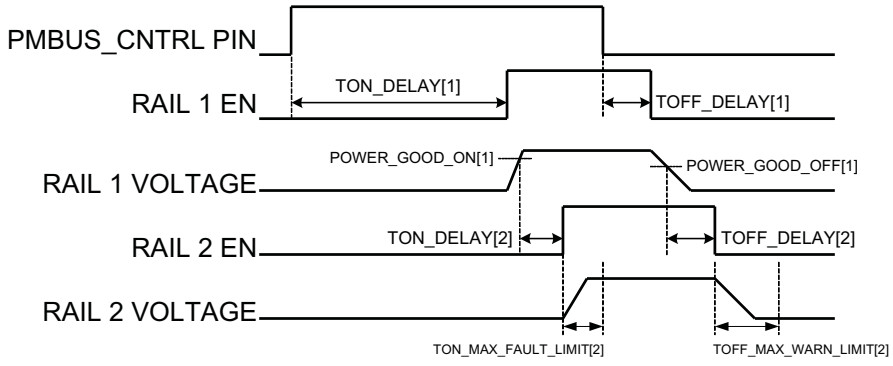
The maximum TON_DELAY time is 3276 ms.

Turnoff Sequencing

The UCD9090-Q1 supports the following sequence-off options for each rail:

- Monitor only – do not sequence-off
- Fixed delay time (TOFF_DELAY) after an OPERATION command to turn off
- Fixed delay time after deassertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails drop below regulation (POWER_GOOD_OFF)
- Fixed delay time in response to an undervoltage, overvoltage, or maximum turn-on fault on the rail
- Fixed delay time in response to a fault on a different rail when set as a fault shutdown slave to the faulted rail
- Fixed delay time in response to a GPI reaching a user-specified state
- Any combination of the previous options

The maximum TOFF_DELAY time is 3276 ms.



- Rail 1 and Rail 2 are both sequenced “ON” and “OFF” by the PMBUS_CNTRL pin only
- Rail 2 has Rail 1 as an “ON” dependency
- Rail 1 has Rail 2 as an “OFF” dependency

Figure 9. Sequence-On and Sequence-Off Timing

(1) In this document, configuration parameters such as Power Good On are referred to using Fusion GUI names. *The UCD90xxx Sequencer and System Health Controller PMBus Command Reference* name is shown in parentheses (POWER_GOOD_ON) the first time the parameter appears.

Sequencing Configuration Options

In addition to the turnon and turnoff sequencing options, the user can configure the time between when a rail is enabled and when the monitored rail voltage must reach its power-good-on setting by using maximum turnon (TON_MAX_FAULT_LIMIT). Maximum turnon can be set in 1-ms increments. A value of 0 ms means that there is no limit and the device can try to turn on the output voltage indefinitely.

Rails can be configured to turn off immediately or to sequence-off according to rail and GPI dependencies and user-defined delay times. Configure a sequenced shutdown by selecting the appropriate rail and GPI dependencies and turnoff delay (TOFF_DELAY) times for each rail. The turnoff delay times begin when the PMBUS_CNTRL pin deasserts, when using the PMBus OPERATION command to give a soft-stop command, or when a fault occurs on a rail that has other rails set as fault-shutdown slaves.

Shutdowns on one rail can initiate shutdowns of other rails or controllers. In systems with multiple UCD9090-Q1s, it is possible for each controller to be both a master and a slave to another controller.

PIN-SELECTED RAIL STATES

This feature allows the use of up to three GPIs to enable or disable any rail. This is useful for implementing system low-power modes and the Advanced Configuration and Power Interface (ACPI) specification that is used for operating system-directed power management in servers and PCs. In up to 8 system states, the power system designer can define which rails are on and which rails are off. If presentation of a new state on the input pins requires a rail to change state, it does so with regard to its sequence-on or sequence-off dependencies.

This function causing a rail to change its state results in a modification of the OPERATION command. This requires setting ON_OFF_CONFIG to use the OPERATION command for a given rail for this function to have any effect on the rail state. The device uses the first three pins configured with the GPI_CONFIG command to select one of eight system states. After a device reset, the sampling of these pins determines the system state, which if enabled is the basis for updating each rail state. When selecting a new system state, changes to the status of the GPIs must not take longer than 1 microsecond. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete configuration settings of PIN_SELECTED_RAIL_STATES.

Table 2. GPI Selection of System States

GPI 2 State	GPI 1 State	GPI 0 State	System State
Not asserted	Not asserted	Not asserted	0
Not asserted	Not asserted	Asserted	1
Not asserted	Asserted	Not asserted	2
Not asserted	Asserted	Asserted	3
Asserted	Not asserted	Not asserted	4
Asserted	Not asserted	Asserted	5
Asserted	Asserted	Not asserted	6
Asserted	Asserted	Asserted	7

MONITORING

The UCD9090-Q1 has 11 monitor input pins (MONx) that are multiplexed into a 12-bit ADC that has a 2.5-V reference. Configuring the monitor pins is possible so that they can measure voltage signals to report voltage-, current-, and temperature-type measurements. A single rail can include all three measurement types, each monitored on a separate MON pin. If a rail has both voltage and current assigned to it, then the user can calculate power for the rail. Digital filtering applied to each MON input depends on the type of signal. Voltage inputs have no filtering. Current and temperature inputs have a low-pass filter.

VOLTAGE MONITORING

The UCD9090-Q1 can monitor up to 12 voltages using the analog input pins. The input voltage range is 0 V–2.5 V for all MONx inputs except MON11 (pin 37), which has a range of 0.2 V–2.5 V. Any voltage between 0 V and 0.2 V on these pins reads as 0.2 V. Use external resistors to attenuate voltages higher than 2.5 V.

The ADC operates continuously, requiring 3.89 µs to convert a single analog input. The sequencing and monitoring algorithm samples each rail every 400 µs. The maximum source impedance of any sampled voltage should be less than 4 kΩ. The source impedance limit is particularly important when using a resistor-divider network to lower the voltage applied to the analog input pins.

Configure MON1–MON6 using digital hardware comparators, if desired, to achieve faster fault responses. Each hardware comparator has four thresholds [two UV (Fault and Warning) and two OV (Fault and Warning)]. The hardware comparators respond to UV or OV conditions in about 80 µs (faster than 400 µs for the ADC inputs) and can disable rails or assert GPOs. The only fault response available for the hardware comparators is to shut down immediately.

The ADC uses an internal 2.5-V reference. The ADC reference has a tolerance of ±0.5% between 0°C and 125°C and a tolerance of ±1% between –40°C and 125°C. Monitoring voltages higher than 2.5 V requires an external voltage divider. Enter the nominal rail voltage and the external scale factor into the *Fusion GUI* to report the actual voltage being monitored instead of the ADC input voltage. The nominal voltage sets the range and precision of the reported voltage according to Table 3.

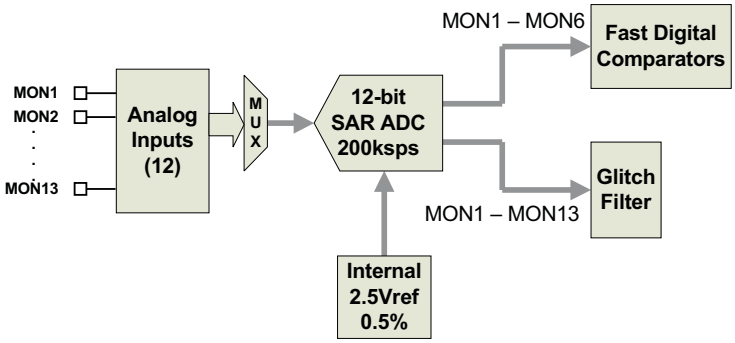


Figure 10. Voltage Monitoring Block Diagram

Table 3. Voltage Range and Resolution

VOLTAGE RANGE (Volts)	RESOLUTION (Millivolts)
0 to 127.99609	3.90625
0 to 63.99805	1.95313
0 to 31.99902	0.97656
0 to 15.99951	0.48824
0 to 7.99976	0.24414
0 to 3.99988	0.12207
0 to 1.99994	0.06104
0 to 0.99997	0.03052

Although the reporting of monitor results can have a resolution of about 15 µV, the 2.5-V reference and the 12-bit ADC determine the real conversion resolution of 610 µV.

CURRENT MONITORING

Monitor current by using the analog inputs. Use external circuitry, see Figure 11, in order to convert the current to a voltage within the range of the UCD9090-Q1 MONx input in use.

For a monitor input configured as a current, a sliding-average digital filter smooths the measurements. The device takes a current measurement for one rail every 200 µs. If programmed to support 10 rails (with or without monitoring current at all rails), then the current measurement for each rail occurs every 2 ms. The current calculation comprises a sliding average using the last four measurements. The filter reduces the probability of false fault detections, and introduces a small delay to the current reading. If a rail definition includes a voltage monitor and a current monitor, then monitoring for undercurrent warnings begins once the rail voltage reaches POWER_GOOD_ON. If the rail does not have a voltage monitor, then current monitoring begins after TON_DELAY.

The device supports multiple PMBus commands related to current, including READ_IOUT, which reads external currents from the MON pins; IOUT_OC_FAULT_LIMIT, which sets the overcurrent fault limit; IOUT_OC_WARN_LIMIT, which sets the overcurrent warning limit; and IOUT_UC_FAULT_LIMIT, which sets the undercurrent fault limit. The *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* contains a detailed description of how to use MBus commands to implement current-fault responses.

IOUT_CAL_GAIN is a PMBus command that allows the user to enter the scale factor of an external current sensor and any amplifiers or attenuators between the current sensor and the MON pin in milliohms. IOUT_CAL_OFFSET is the current that results in 0 V at the MON pin. The combination of these PMBus commands allows the reporting of current in amperes. The following example using the INA196 would require programming IOUT_CAL_GAIN to Rsense(mΩ) × 20.

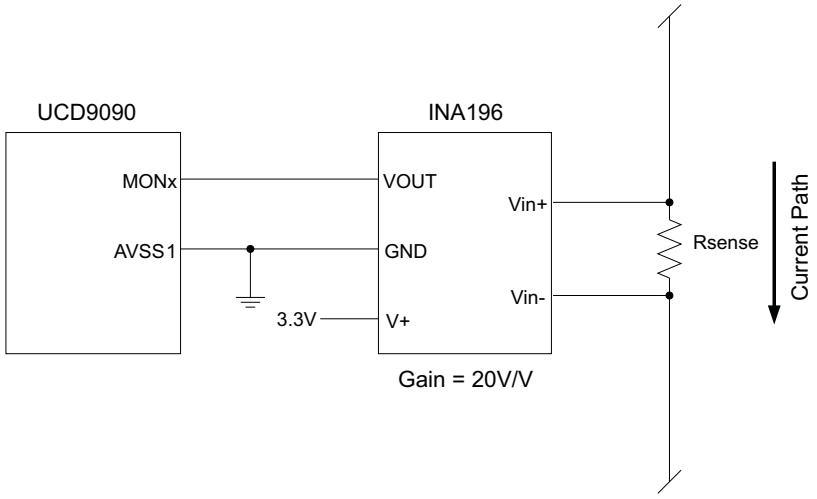


Figure 11. Current Monitoring Circuit Example Using the INA196

REMOTE TEMPERATURE MONITORING AND INTERNAL TEMPERATURE SENSOR

The UCD9090-Q1 has support for internal and remote temperature sensing. The internal temperature sensor requires no calibration and can report the device temperature via the PMBus interface. The remote temperature sensor can report the remote temperature by using a configurable gain and offset for the type of sensor being used in the application, such as a linear temperature sensor (LTS) connected to the analog inputs.

Use external circuitry to convert the temperature to a voltage within the range of the UCD9090-Q1 MONx input being used.

If an input is configured as a temperature, the measurements are smoothed by a sliding-average digital filter. The temperature for one rail is measured every 100 ms. If programmed to support 10 rails (with or without monitoring temperature at all rails), then the current measurement for each rail temperature occurs every 1 s. The temperature calculation comprises a sliding average using the last 16 measurements. The filter reduces the probability of false fault detections, and introduces a small delay to the temperature reading. A silicon diode sensor with an accuracy of ±5°C, monitored using the ADC, measures the internal device temperature. Temperature monitoring begins immediately after reset and initialization.

The device supports multiple PMBus commands related to temperature, including READ_TEMPERATURE_1, which reads the internal temperature; READ_TEMPERATURE_2, which reads external temperatures; and OT_FAULT_LIMIT and OT_WARN_LIMIT, which set the overtemperature fault and warning limit. The *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* contains a detailed description of how to use PMBus commands to implement temperature-fault responses.

TEMPERATURE_CAL_GAIN is a PMBus command that allows the user to enter the scale factor of an external temperature sensor and any amplifiers or attenuators between the temperature sensor and the MON pin in °C/V. TEMPERATURE_CAL_OFFSET is the temperature that results in 0 V at the MON pin. The combination of these PMBus commands allows the reporting of temperature in degrees Celsius.

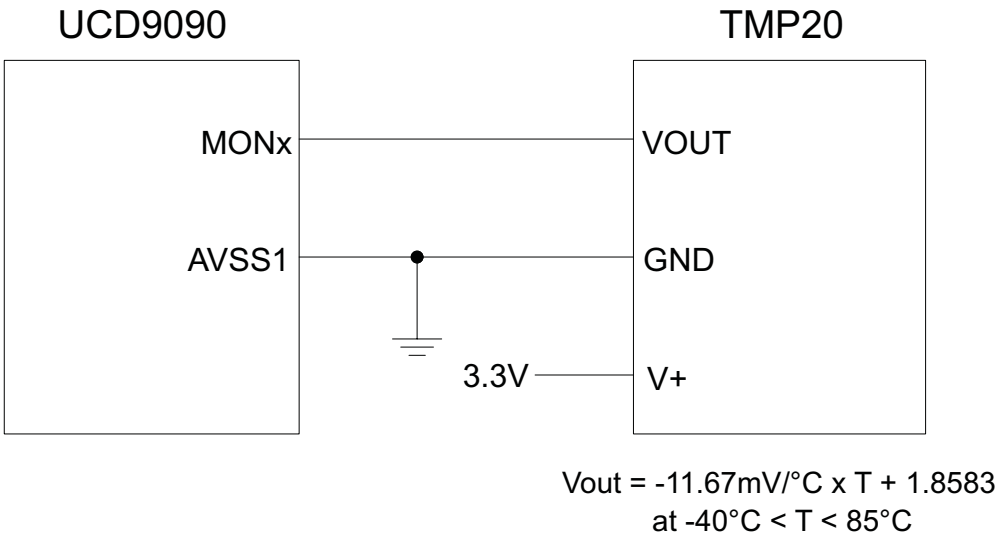


Figure 12. Remote Temperature Monitoring Circuit Example using the TMP20

TEMPERATURE BY HOST INPUT

If the host system has the option of not using the temperature-sensing capability of the UCD9090-Q1, it can still provide the desired temperature to the UCD9090-Q1 through the PMBus. The host may have temperature measurements available through I^2C- or SPI-interfaced temperature sensors. The UCD9090-Q1 would use the temperature given by the host in place of an external temperature measurement for a given rail. The temperature provided by the host would still be used for detecting overtemperature warnings or faults, logging peak temperatures, input to Boolean logic-builder functions, and feedback for the fan-control algorithms. To write a temperature associated with a rail, the PMBus command used is the READ_TEMPERATURE_2 command. If the host writes that command, the value written is used as the temperature until the writing of another value. This is true even if the temperature does not have an assigned monitor pin. When there is a monitor pin associated with the temperature, then after writing READ_TEMPERATURE_2 , there is no further use for the monitor pin until the part is reset. When there is not a monitor pin associated with the temperature, the internal temperature sensor senses the temperature until the writing of the READ_TEMPERATURE_2 command.

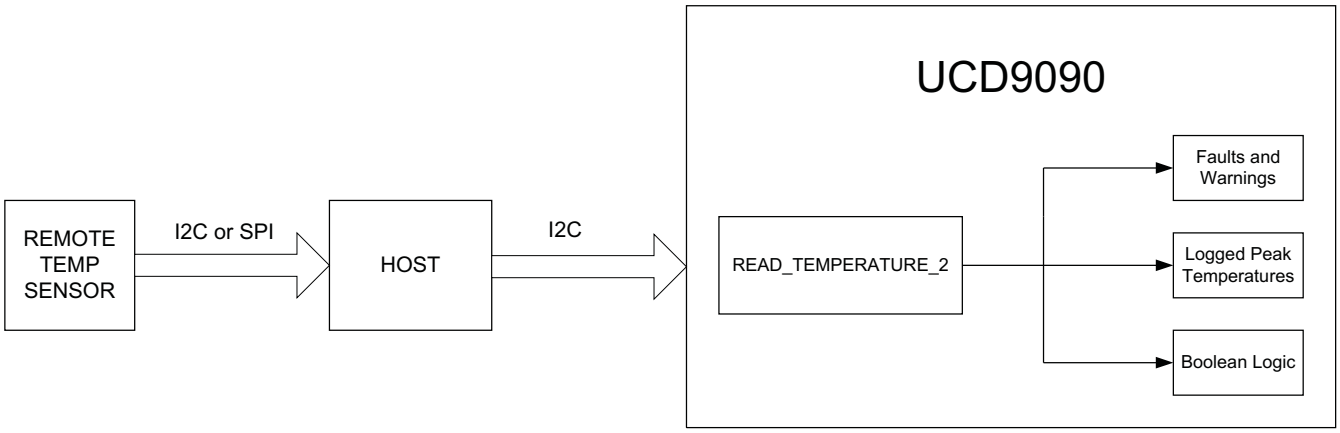


Figure 13. Temperature Provided by Host

FAULT RESPONSES AND ALERT PROCESSING

The UCD9090-Q1 monitors whether the rail stays within a window of normal operation. There are two programmable warning levels (under and over) and two programmable fault levels (under and over). When any monitored voltage goes outside of the warning or fault window, the PMBALERT# pin asserts immediately, and setting of the appropriate bits in the PMBus status registers occurs (see Figure 7). The *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* and the *PMBus Specification* provides detailed descriptions of the status registers.

The user can enable or disable a programmable glitch filter for each MON input and then, on a glitch filter for an input defined as a voltage, set that filter between 0 and 102 ms with 400-µs resolution.

The device bases fault-response decisions on results from the 12-bit ADC. The device cycles through the ADC results and compares them against the programmed limits. Timing of the event within the ADC conversion cycle and the selected fault response determine the time to respond to an individual event.

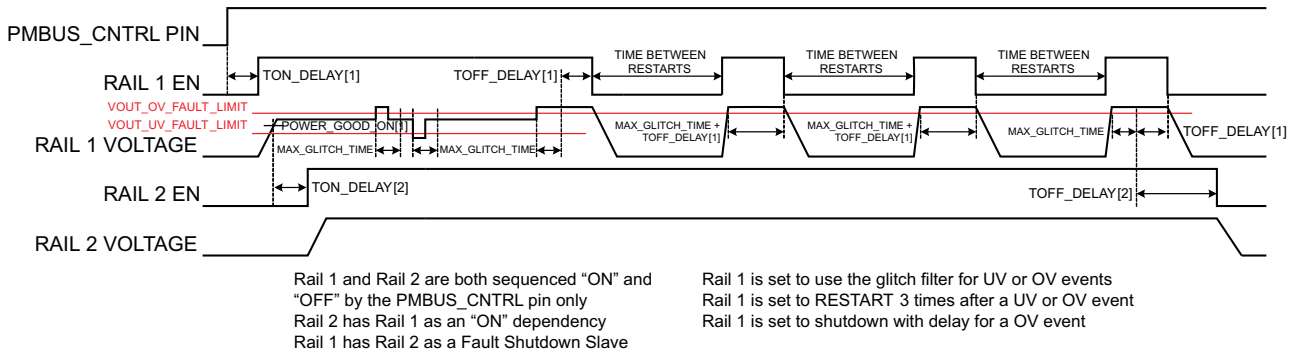


Figure 14. Sequencing and Fault-Response Timing

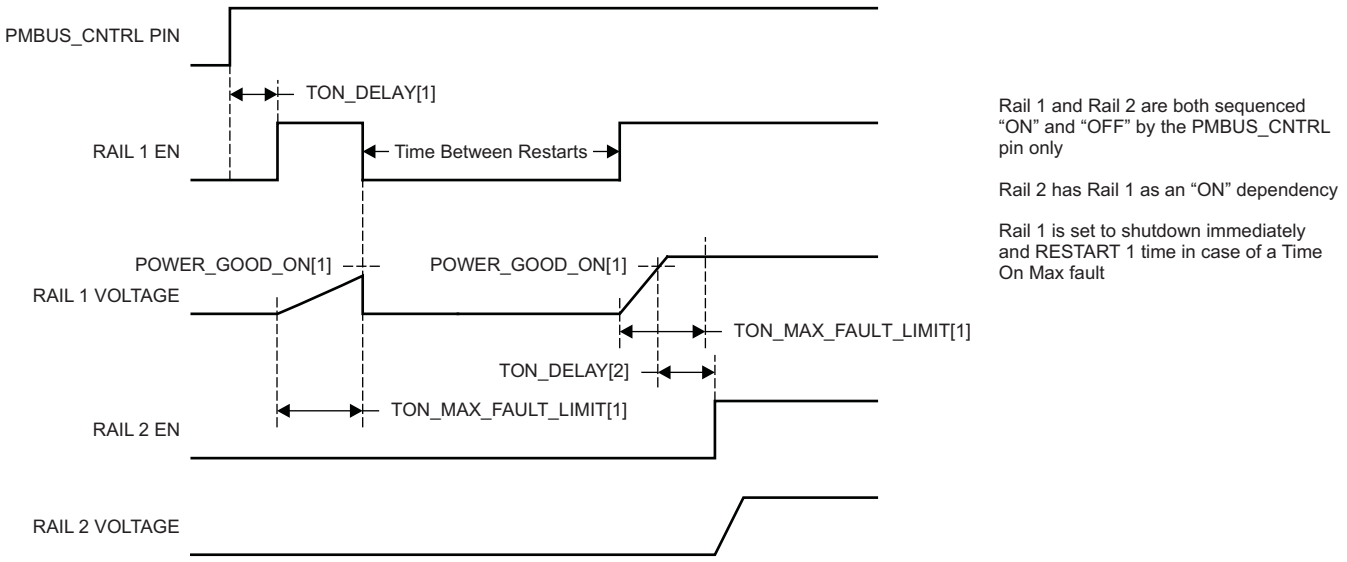


Figure 15. Maximum Turnon Fault

The configurable fault limits are:

TON_MAX_FAULT – Flagged if an enabled rail does not reach the POWER_GOOD_ON limit within the configured time

VOUT_UV_WARN – Flagged if a voltage rail drops below the specified UV warning limit after reaching the POWER_GOOD_ON setting

VOUT_UV_FAULT – Flagged if a rail drops below the specified UV fault limit after reaching the POWER_GOOD_ON setting

VOUT_OV_WARN – Flagged if a rail exceeds the specified OV warning limit at any time during startup or operation

VOUT_OV_FAULT – Flagged if a rail exceeds the specified OV fault limit at any time during startup or operation

MAX_TOFF_WARN – Flagged if a rail not reach 12.5% of the nominal rail voltage within the configured time following a command to shut down

Faults are more serious than warnings. The PMBALERT# pin is always asserted immediately if a warning or fault occurs. If a warning occurs, the following takes place:

Warning Actions

- Immediately assert the PMBALERT# pin
- Flag the status bit
- Assert a GPIO pin (optional)
- Omit logging warnings to flash

Choose from a number of fault-response options:

Fault Responses

- *Continue Without Interruption:* Flag the fault and take no action
- *Shut Down Immediately:* Shut down the faulted rail immediately and restart according to the rail configuration
- *Shut Down using TOFF_DELAY:* If a fault occurs on a rail, exhaust whatever retries are configured. If the rail does not come back, schedule the shutdown of this rail and all fault-shutdown slaves. Sequence all selected rails off, including the faulty rail, according to their sequence-off dependencies and T_OFF_DELAY times. For the Do Not Restart selection, sequence off all selected rails on fault detection.

Restart

- *Do Not Restart:* Do not attempt to restart a faulted rail after it has been shut down.
- *Restart Up To N Times:* Attempt to restart a faulted rail up to 14 times after it has been shut down. The measurement for time between restarts is between the rail enable pin deassertion (after any glitch filtering and turnoff delay times, if configured to observe them) and reassertion. That time setting can be between 0 and 1275 ms in 5-ms increments.
- *Restart Continuously:* Same as *Restart Up To N Times* except that the device continues to restart until the fault goes away, the specified combination of PMBus OPERATION command and PMBUS_CNTRL pin status commands it off, reset of the device, or removal of power from the device.
- *Shut Down Rails and Sequence On (Re-sequence):* Shut down the selected rails immediately or after reaching the continue-operation time, and then sequence-on those rails using sequence-on dependencies and T_ON_DELAY times.

SHUT DOWN ALL RAILS AND SEQUENCE ON (RESEQUENCE)

One can configure the UCD9090-Q1 to turn off a set of rails and then sequence them back on in response to a fault or a RESEQUENCE command. To sequence all rails in the system, select all rails as fault-shutdown slaves of the faulted rail. The rails designated as fault-shutdown slaves do soft shutdowns regardless of whether the setting for the faulted rail is to stop immediately or stop with delay. Only after all retries are exhausted for a given fault does the device perform shut-down-all-rails and sequence-on.

While waiting for the rails to turn off, any of the rails reaching its TOFF_MAX_WARN_LIMIT results in the reporting of an error. There is a configurable option to continue with the resequencing operation if an error report occurs. After the faulted rail and fault-shutdown slaves sequence-off, the UCD9090-Q1 waits for a programmable delay time between 0 and 1275 ms in increments of 5 ms and then sequences-on the faulted rail and fault-shutdown slaves according to the start-up sequence configuration. This repeats until the faulted rail and fault-shutdown slaves successfully achieve regulation, or for a user-selected 1, 2, 3, 4, or unlimited number of times. If the resequence operation is successful, the resequence counter resets if all of the resequenced rails maintain normal operation for one second.

Once shut-down-all-rails and sequence-on begin, the device ignores any faults on the fault-shutdown slave rails. The occurrence of two or more simultaneous faults with different fault-shutdown slaves results in taking the more conservative. For example, if a set of rails is already on its second resequence and the device is configured to resequence three times, and another set of rails enters the resequence state, resequencing that second set of rails only happens once. Another example – if one set of rails is waiting for all of its rails to shut down so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shut down before resequencing.

GPIOs

The UCD9090-Q1 has 21 GPIO pins that can function as either inputs or outputs. Each GPIO has configurable output-mode options, including open-drain or push-pull outputs that it can actively drive to 3.3 V or ground. The device can use an additional two pins as either inputs or PWM outputs but not as GPOs. Table 4 lists possible uses for the GPIO pins and the maximum number of each type for each use. GPIO pins can be dependents in sequencing and alarm processing. Additional uses are for system-level functions such as external interrupts, power-goods, resets, or for the cascading of multiple devices. Configuring a rail without a MON pin but with a GPIO set as an enable can sequence a GPO up or down.

Table 4. GPIO Pin-Configuration Options

PIN NAME	PIN	RAIL EN (10 MAX)	GPI (8 MAX)	GPO (10 MAX)	PWM OUT (10 MAX)	MARGIN PWM (10 MAX)
FPWM1/GPIO5	10	X	X	X	X	X
FPWM2/GPIO6	11	X	X	X	X	X
FPWM3/GPIO7	12	X	X	X	X	X
FPWM4/GPIO8	13	X	X	X	X	X
FPWM5/GPIO9	14	X	X	X	X	X
FPWM6/GPIO10	15	X	X	X	X	X
FPWM7/GPIO11	16	X	X	X	X	X
FPWM8/GPIO12	17	X	X	X	X	X
GPI1/PWM1	22		X		X	X
GPI2/PWM2	23		X		X	X
GPIO1	4	X	X	X		
GPIO2	5	X	X	X		
GPIO3	6	X	X	X		
GPIO4	7	X	X	X		
GPIO13	18	X	X	X		
GPIO14	21	X	X	X		
GPIO15	24	X	X	X		
GPIO16	25	X	X	X		
GPIO17	26	X	X	X		
TCK/GPIO18	27	X	X	X		
TDO/GPIO19	28	X	X	X		
TDI/GPIO20	29	X	X	X		
TMS/GPIO21	30	X	X	X		

GPO Control

PMBus commands or logic defined in internal Boolean function blocks can control the GPIOs when configured as outputs. Controlling GPOs by PMBus commands (GPIO_SELECT and GPIO_CONFIG) can provide control over LEDs, enable switches, and so forth, with the use of an I^2C interface. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for details on controlling a GPO using PMBus commands.

GPO Dependencies

A user can configure GPIOs as outputs that are based on Boolean combinations of up to two ANDs all ORed together (Figure 16). Inputs to the logic blocks can include the first eight defined GPOs, GPIs, and rail-status flags. The user can select one rail-status type as an input for each AND gate in a Boolean block, and for a selected rail status, include the status flags of all active rails as inputs to the AND gate. *_LATCH* rail-status types stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin. Table 5 shows the different rail-status types. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete definitions of rail-status types. The GPO response is configurable to have a delayed assertion or deassertion.

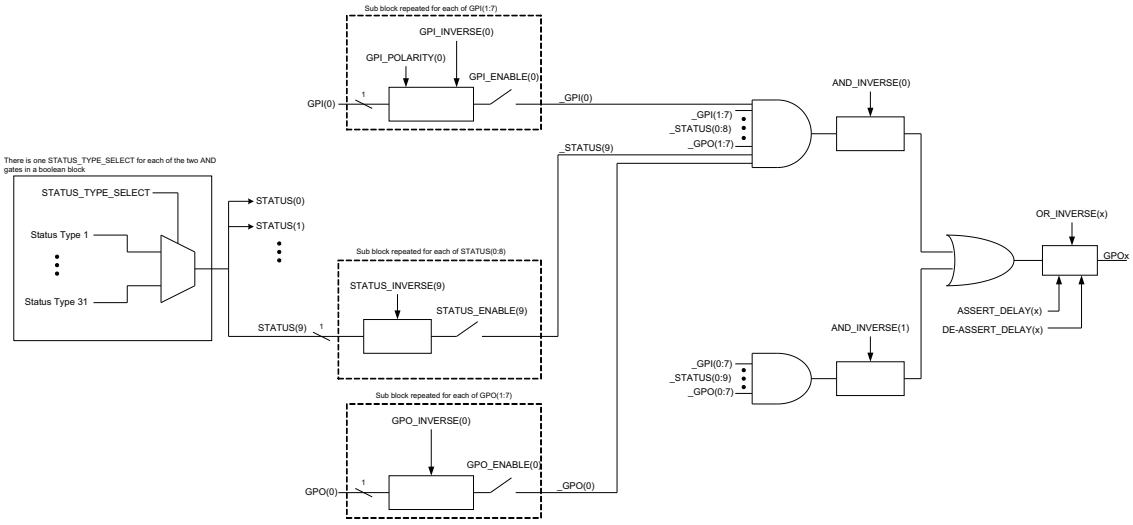


Figure 16. Boolean Logic Combinations

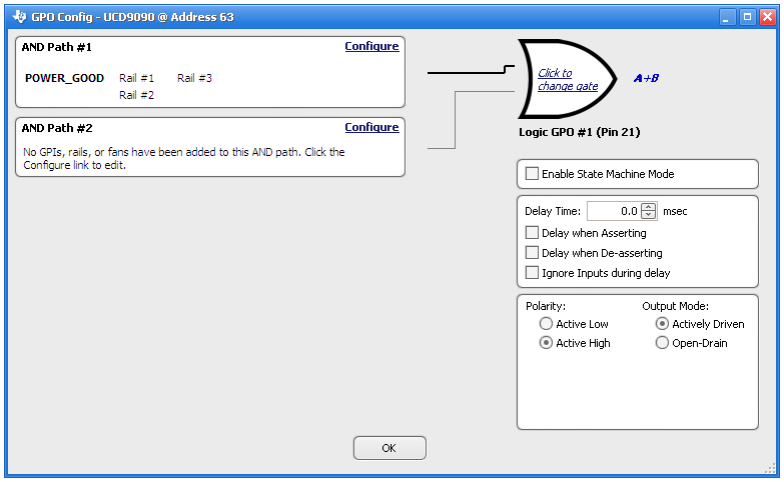


Figure 17. Fusion Boolean Logic Builder

Table 5. Rail-Status Types for Boolean Logic

Rail-Status Types		
POWER_GOOD	IOUT_UC_FAULT	TOFF_MAX_WARN_LATCH
MARGIN_EN	TEMP_OT_FAULT	SEQ_ON_TIMEOUT_LATCH
MRG_LOW_nHIGH	TEMP_OT_WARN	SEQ_OFF_TIMEOUT_LATCH
VOUT_OV_FAULT	SEQ_ON_TIMEOUT	SYSTEM_WATCHDOG_TIMEOUT_LATCH
VOUT_OV_WARN	SEQ_OFF_TIMEOUT	IOUT_OC_FAULT_LATCH
VOUT_UV_WARN	SYSTEM_WATCHDOG_TIMEOUT	IOUT_OC_WARN_LATCH
VOUT_UV_FAULT	VOUT_OV_FAULT_LATCH	IOUT_UC_FAULT_LATCH
TON_MAX_FAULT	VOUT_OV_WARN_LATCH	TEMP_OT_FAULT_LATCH
TOFF_MAX_WARN	VOUT_UV_WARN_LATCH	TEMP_OT_WARN_LATCH
IOUT_OC_FAULT	VOUT_UV_FAULT_LATCH	
IOUT_OC_WARN	TON_MAX_FAULT_LATCH	

GPO Delays

A user can configure the GPOs so that they manifest a change in logic with a delay on assertion, deassertion, both, or none. GPO behavior using delays has different effects depending on whether the logic change occurs at a faster rate than the delay. On a normal delay configuration, if the logic for a GPO changes to a state and reverts back to the previous state within the time of a delay, then the GPO does not manifest the change of state on the pin. In Figure 18, the GPO setting is such that it follows the GPI with a 3-ms delay at assertion and also at de-assertion. When the GPI first changes to a high logic state, the device maintains the state for a time longer than the delay, allowing the GPO to follow with an appropriate logic state. The same goes when the GPI returns to its previous low logic state. The second time that the GPI changes to a high logic state, it returns to a low logic state before the delay time expires. In this case, the GPO does not change state. A delay configured in this manner serves as a glitch filter for the GPO.

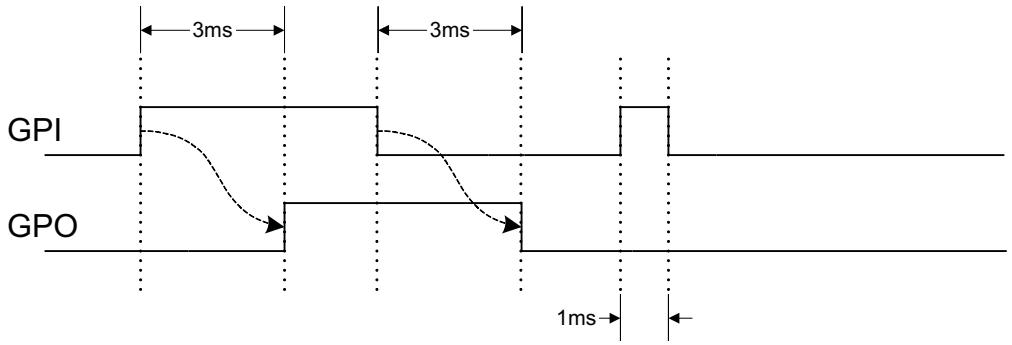


Figure 18. GPO Behavior When Not Ignoring Inputs During Delay

The *Ignore Input During Delay* bit allows the output of a change in GPO even if it occurs for a time shorter than the delay. This configuration setting has the GPO ignore any activity from the triggering event until the delay expires. Figure 19 represents the two cases for ignoring the inputs during a delay. In the case in which the logic changes occur with more time than the delay, the GPO signal looks the same as when not ignoring the input. Then on a GPI pulse shorter than the delay, the GPO still changes state. Any pulse that occurs on the GPO when having the *Ignore Input During Delay* bit set has a duration of at least the time delay.

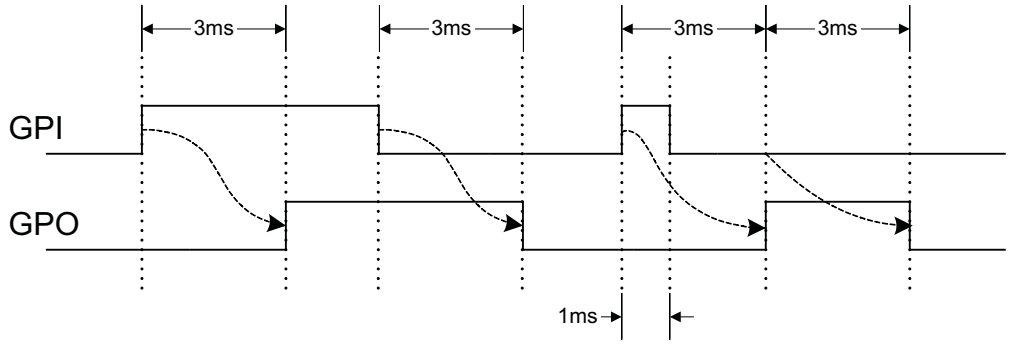


Figure 19. GPO Behavior When Ignoring Inputs During Delay

State Machine Mode Enable

With this bit in the GPO_CONFIG command set, the device uses only one of the AND paths at a given time. When the GPO logic result is currently TRUE, the device uses AND path 0 until the result becomes FALSE. When the GPO logic result is currently FALSE, the device uses AND path 1 until the result becomes TRUE. This provides a very simple state machine and allows for more-complex logical combinations.

GPI Special Functions

There are five special input functions which use GPIs. There can be no more than one pin assigned to each of these functions.

- **GPI Fault Enable** – When set, the device treats de-assertion of the GPI as a fault.
- **Latched Statuses Clear Source** – When a GPO uses a latched status type (_LATCH), one can configure a GPI that clears the latched status.
- **Input Source for Margin Enable** – With this pin asserted, the device puts all rails with margining enabled in a margined state (low or high).
- **Input Source for Margin Low or Not-High** – With this pin asserted, the device sets all margined rails to margin low as long as the input source asserts the margin enable. With this pin deasserted, the device sets the rails to margin high.

The configuration of GPI pin polarity can be either active-low or active-high. The PIN_SELECTED_RAIL_STATES command uses the first three GPIs defined, regardless of their main purpose.

Power-Supply Enables

Configuration of ach GPIO can be as a rail-enable pin with either active-low or active-high polarity. Output mode options include open-drain or push-pull outputs that one can actively drive to 3.3 V or ground. During reset, the GPIO pins are high-impedance except for FPWM/GPIO pins 17–24, which the device drives low. To hold the power supplies off during reset, tie external pulldown or pullup resistors to the enable pins. The UCD9090-Q1 can support a maximum of 10 enable pins.

NOTE

The only use of GPIO pins that have FPWM capability (pins 10–17) should be as power-supply enable signals if the signal is active-high.

Cascading Multiple Devices

One can use a GPIO pin to coordinate multiple controllers by using the pin as a power-good output from one device and connecting it to the PMBUS_CNTRL input pin of another. This imposes a master-slave relationship among multiple devices. During start-up, the slave controllers initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off, it sends the shutdown signal to its slaves.

A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

The PMBus specification implies that the power-good signal is active when all the rails in a controller are regulating at their programmed voltage. The UCD9090-Q1 allows configuring of GPIOs to respond to a desired subset of power-good signals.

PWM Outputs

FPWM1–FPWM8

Pins 10–17 are configurable as fast pulse-width modulators (FPWMs). The frequency range is 15.260 kHz to 125 MHz. FPWMs can be configured as closed-loop margining outputs, fan controllers, or general-purpose PWMs.

Any FPWM pin not used as a PWM output is configurable as a GPIO. A designer can use one FPWM in a pair as a PWM output and the other pin as a GPO. The device actively drives FPWM pins low from reset when used as GPOs.

The frequency settings for the FPWMs apply to pairs of pins:

- FPWM1 and FPWM2 – same frequency
- FPWM3 and FPWM4 – same frequency
- FPWM5 and FPWM6 – same frequency
- FPWM7 and FPWM8 – same frequency

If not using an FPWM pin from a pair while the setting of its companion is to function as a PWM, TI recommends configuring the unused FPWM pin as an active-low open-drain GPO so that it does not disturb the rest of the system. Setting an FPWM automatically enables the other FPWM within the pair if not configured for any other functionality.

Derive the frequency for the FPWM by dividing down a 250-MHz clock. To determine an actual frequency to which an FPWM can be set, divide 250 MHz by any integer between 2 and (2^{14} – 1).

The FPWM duty-cycle resolution depends on the frequency setting for a given FPWM. After determining the frequency, calculate the duty-cycle resolution using Equation 1.

$$\text{Change per Step } (\%)_{FPWM} = \text{frequency} \div (250 \times 10^6 \times 16) \times 100 \quad (1)$$

Take for an example determining the actual frequency and the duty-cycle resolution for a 75-MHz target frequency.

1. Divide 250 MHz by 75 MHz to obtain 3.33.
2. Round off 3.33 to obtain an integer of 3.
3. Divide 250 MHz by 3 to obtain the actual closest frequency of 83.333 MHz.
4. Use Equation 1 to calculate the duty-cycle resolution of 2.0833%.

PWM1-2

Pins 22 and 23 are usable as GPIs or PWM outputs. These PWM outputs have an output frequency of 0.93 Hz to 7.8125 MHz.

Derive the frequency for PWM1 and PWM2 by dividing down a 15.625-MHz clock. To determine a possible frequency setting for these PWMs, one must divide 15.625 MHz by any integer between 2 and (2^{24} – 1). The duty-cycle resolution depends on the set frequency for PWM1 and PWM2.

The PWM1 or PWM2 duty-cycle resolution depends on the frequency set for the given PWM. Knowing the frequency, one can calculate the duty-cycle resolution using Equation 2.

$$\text{Change per Step } (\%)_{PWM1/2} = \text{frequency} \div 15.625 \times 10^6 \times 100 \quad (2)$$

Calculate as follows to determine the PWM1 frequency setting closest 1 MHz:

1. Divide 15.62 5 MHz by 1 MHz to obtain 15.625.
2. Round off 15.625 to obtain an integer of 16.
3. Divide 15.625 MHz by 16 to obtain the actual closest frequency of 976.563 kHz.
4. Use Equation 2 to calculate the duty-cycle resolution of 6.25%.

All frequencies below 238 Hz have a duty-cycle resolution of 0.0015%.

Programmable Multiphase PWMs

The user can align FPWMs with reference to their phase. The phase for each FPWM is configurable from 0° to 360°. This provides flexibility in PWM-based applications such as power-supply controller, digital clock generation, and others. See an example of four FPWMs programmed to have phases at 0°, 90°, 180° and 270° (Figure 20).

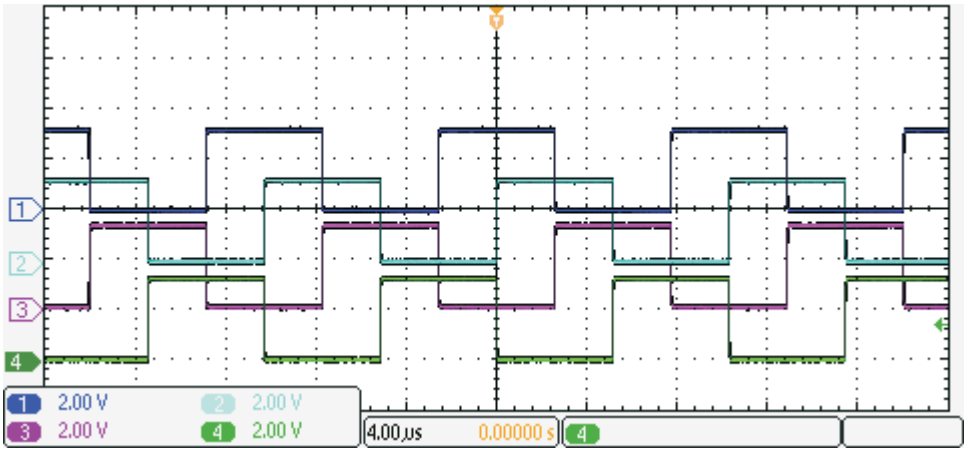


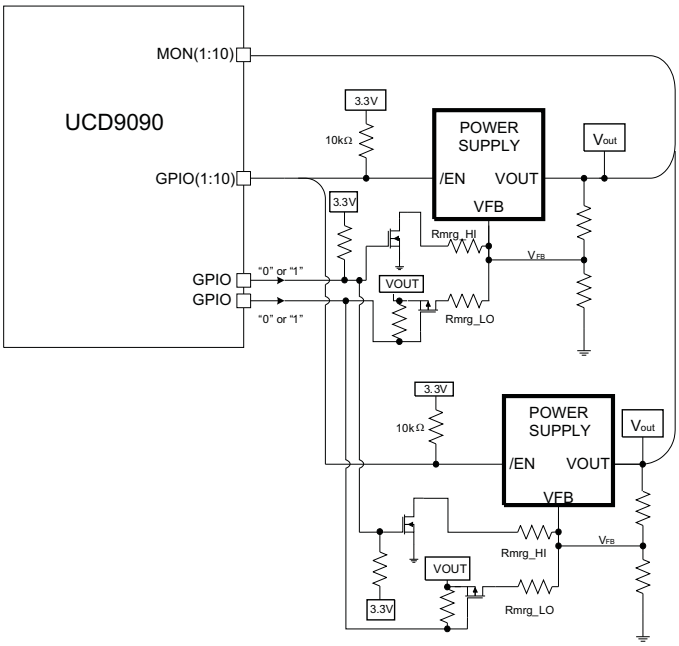
Figure 20. Multiphase PWMs

MARGINING

Product validation testing uses margining to verify that the complete system works properly over all conditions, including minimum and maximum power-supply voltages, load range, ambient temperature range, and other relevant parameter variations. Margining can be controlled over PMBus using the OPERATION command or by configuring two GPIO pins as margin-EN and margin-UP/DOWN inputs. The MARGIN_CONFIG command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* describes different available margining options, including ignoring faults while margining and using closed-loop margining to trim the power-supply output voltage one time at power up.

Open-Loop Margining

To perform open-loop margining, connect a power-supply feedback node to ground through one resistor and to the margined power supply output (V_{OUT}) through another resistor. The power-supply regulation loop responds to the change in feedback-node voltage by increasing or decreasing the power-supply output voltage to return the feedback voltage to the original value. The fixed resistor values and the voltage at V_{OUT} and ground determine the voltage change. It is necessary to configure two GPIO pins as open-drain outputs for connecting resistors from the feedback node of each power supply to V_{OUT} or ground.



Open Loop Margining

Figure 21. Open-Loop Margining

Closed-Loop Margining

Closed-loop margining uses a PWM or FPWM output for each power supply being margined. An external RC network converts the FPWM pulse train into a dc margining voltage. The margining voltage is connected to the appropriate power-supply feedback node through a resistor. The device monitors the power-supply output voltage and controls the margining voltage by adjusting the PWM duty cycle until the power-supply output voltage reaches the margin-low and margin-high voltages set by the user. The voltage setting resolutions are the same that apply to the voltage measurement resolution (Table 3). Closed-loop margining can operate in several modes (Table 6). Given that this closed-loop system has feedback through the ADC, the ADC measurement dominates the closed-loop margining accuracy. The relationship between duty cycle and margined voltage is configurable so that voltage increases when duty cycle increases or decreases. For more details on configuring the UCD9090-Q1 for margining, see the *Voltage Margining Using the UCD9012x* application note (SLVA375).

Table 6. Closed-Loop Margining Modes

Mode	Description
DISABLE	Margining is disabled.
ENABLE_TRI_STATE	When not margining, the PWM pin is in the high-impedance state.
ENABLE_ACTIVE_TRIM	When not margining, continuous adjustment of the PWM duty cycle keeps the voltage at VOUT_COMMAND.
ENABLE_FIXED_DUTY_CYCLE	When not margining, the PWM duty-cycle setting is for a fixed duty cycle.

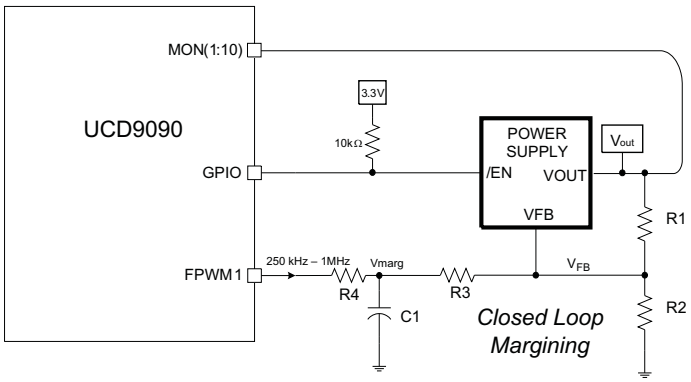


Figure 22. Closed-Loop Margining

RUN-TIME CLOCK

The run-time clock value is in milliseconds and days. Both are 32-bit numbers. Issuing a STORE_DEFAULT_ALL command saves this value in nonvolatile memory. Detection of a power-down condition can also save the value (see BROWNOUT FUNCTION).

The run-time clock is also writable. This allows the host to correct the clock periodically. It also allows initializing the clock to the actual, absolute time in years (for example, March 23, 2010). The user must translate the absolute time to days and milliseconds.

The three usage scenarios for the run-time clock are:

- **Time from restart (reset or power-on)** – the run-time clock starts from 0 each time a restart occurs
- **Absolute run-time, or operating time** – the device preserves the run-time clock setting across restarts, for tracking the total time that the device has been in operation (Note: *Boot time* is not part of this. Only normal operation time is captured here.)
- **Local time** – an external processor sets the run-time clock to real-world time at each time the device restarts.

The run-time clock value is the timestamp for any logged faults.

SYSTEM RESET SIGNAL

The UCD9090-Q1 can generate a programmable system-reset pulse as part of sequence-on. Programming a GPIO to remain deasserted until the voltage of a particular rail or combination of rails reaches its respective POWER_GOOD_ON levels, plus a programmable delay time, creates the pulse. Program the system-reset delay duration as shown in Table 7. See an example of two SYSTEM RESET signals in Figure 23. Configuration of the first SYSTEM RESET signal is such that it becomes de-asserted on Power Good On and asserted on Power Good Off after a given common delay time. Configurationn of the second SYSTEM RESET signal is such that it sends a pulse after a delay time on achieving Power Good On. The pulse duration is configurable between 0.001 s and 32.256 s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for pulse-duration configuration details.

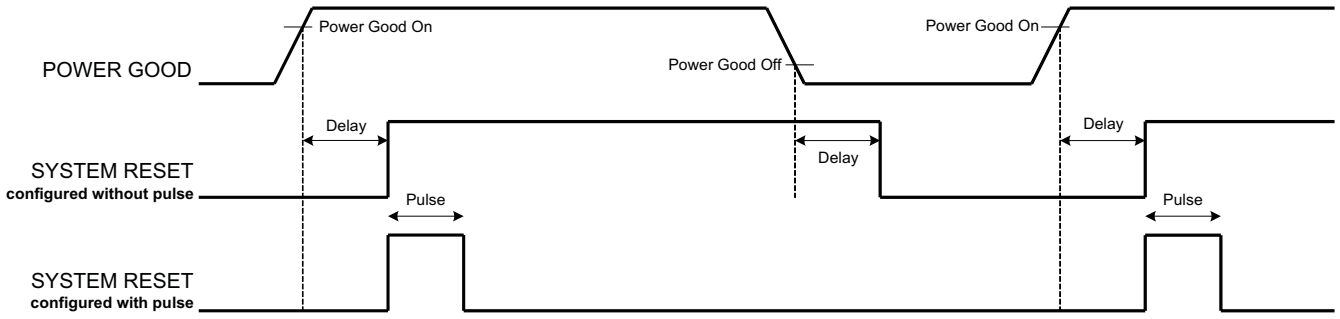


Figure 23. System Reset With and Without Pulse Setting

The system reset can react to watchdog timing. In Figure 24, the first delay on SYSTEM RESET is for the initial reset release that would get a CPU running once all necessary voltage rails are in regulation. The watchdog configuration includes a start time and a reset time. If these times expire without the WDI clearing them, then the expectation is that the CPU providing the watchdog signal is not operating. Either a delay or GPI tracking-release delay toggles the SYSTEM RESET to determine if the CPU recovers.

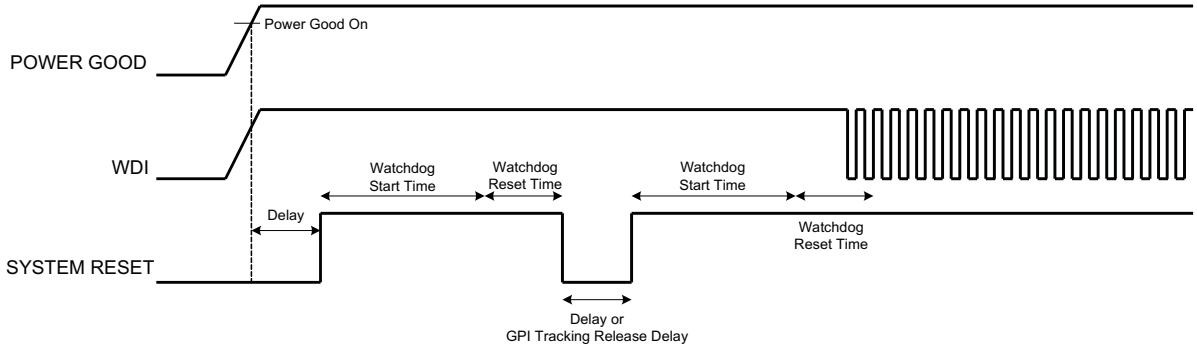


Figure 24. System Reset With Watchdog

Table 7. System-Reset Delay

Delay
0 ms
1 ms
2 ms
4 ms
8 ms
16 ms
32 ms
64 ms
128 ms
256 ms
512 ms
1.02 s
2.05 s
4.10 s
8.19 s
16.38 s
32.8 s

WATCHDOG TIMER

The user can configure a GPI and GPO as a watchdog timer (WDT). The WDT can be independent of power-supply sequencing or tied to a GPIO functioning as a watchdog output (WDO) configured to provide a system-reset signal. One can reset the WDT by toggling a watchdog input (WDI) pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C. The WDI and WDO pins are optional when using the watchdog timer. The SYSTEM_WATCHDOG_RESET command can replace the WDI and the Boolean-logic-defined GPOs or the system-reset function can manifest the WDO.

The WDT can be active immediately at power up or set to wait while the system initializes. Table 8 lists the programmable wait times before the initial time-out sequence begins.

Table 8. WDT Initial Wait Time

WDT INITIAL WAIT TIME
0 ms
100 ms
200 ms
400 ms
800 ms
1.6 s
3.2 s
6.4 s
12.8 s
25.6 s
51.2 s
102 s
205 s
410 s
819 s
1638 s

The watchdog time-out is programmable from 0.001s to 32.256 s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for details on configuring the watchdog time-out. If the WDT times out, the UCD9090-Q1 can assert a GPIO pin configured as WDO that is separate from a GPIO defined as system-reset pin, or it can generate a system-reset pulse. After a time-out, toggling the WDI pin or writing to SYSTEM_WATCHDOG_RESET over I^2C restarts the WDT.

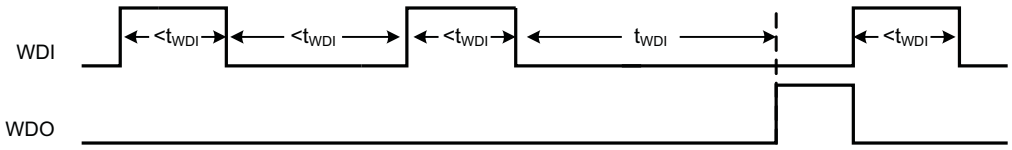


Figure 25. Timing of GPIOs Configured for Watchdog Timer Operation

DATA AND ERROR LOGGING TO FLASH MEMORY

The UCD9090-Q1 can log faults and the number of device resets to flash memory, which also stores peak voltage measurements for each rail. To reduce stress on the flash memory, the device starts a 30-second timer if a measured value exceeds the previously logged value, and writes only the highest value from the 30-second interval from RAM to flash.

Flash memory can store multiple faults, and accessing the faults over PMBus helps to debug power-supply bugs or failures. Each logged fault includes:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

Flash memory also stores the total number of device resets. One can reset the value using PMBus.

With the brownout function enabled, the device only logs the run-time clock value, peak monitor values, and faults to flash on detection of a power-down. The device stores its run-time clock value across resets or power cycles unless the brownout function is disabled, in which case the run-time clock returns to zero after each reset.

It is also possible to update and calibrate the UCD9090-Q1 internal run-time clock via a PMBus host. For example, a host processor with a real-time clock could periodically update the UCD9090-Q1 run-time clock to a value that corresponds to the actual date and time. The host must translate the UCD9090-Q1 timer value back into the appropriate units, based on the usage scenario chosen. See the REAL_TIME_CLOCK command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for more details.

BROWNOUT FUNCTION

The user can enable the UCD9090-Q1 to turn off all nonvolatile logging until a brownout event is detected. A brownout event occurs if V_{CC} drops below 2.9 V. In order to enable this feature, the user must provide enough local capacitance to deliver up to 80 mA (consider additional load based on GPOs sourcing external circuits such as LEDs) for 5 ms while maintaining a minimum of 2.6 V at the device. If using the brownout circuit (Figure 26), then place a Schottky diode so that it blocks the other circuits that are also powered from the 3.3-V supply.

With this feature enabled, the UCD9090-Q1 saves faults, peaks, and other log data to SRAM during normal operation of the device. On detection of a brownout event, the device copies all data from SRAM to Flash. Use of this feature allows the UCD9090-Q1 to keep track of a single run-time clock that spans device resets or system power down (rather than resetting the run-time clock after device reset). Use of this feature can also improve the UCD9090-Q1 internal response time to events, because the device disables Flash writes during normal system operation. This is an optional feature which one can enable using the MISC_CONFIG command. For more details, see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*.

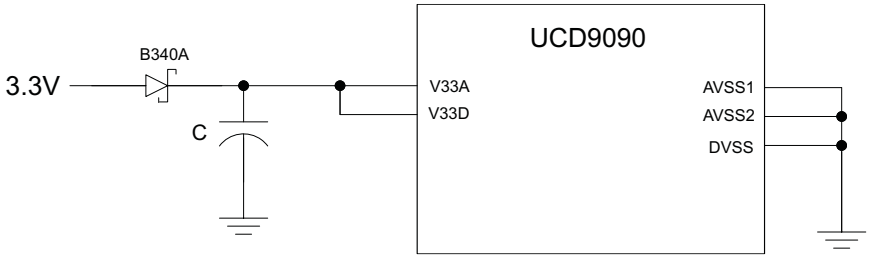


Figure 26. Brownout Circuit

PMBUS ADDRESS SELECTION

Two pins are allocated to decode the PMBus address. At power up, the device applies a bias current to each address-detect pin, and the internal 12-bit ADC captures the voltage on that pin. Calculate the PMBus address as follows.

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of eight addresses as shown in Table 9. The MIN and MAX VOLTAGE RANGE (V) define the address bins. Each bin is a constant ratio of 1.25 from the previous bin. This method maintains the width of each bin relative to the tolerance of standard 1% resistors.

Table 9. PMBus Address Bins

ADDRESS BIN	RPMBus PMBus RESISTANCE (kΩ)
Open	—
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
Short	—

A low impedance (short) on either address pin that produces a voltage below the minimum voltage causes the PMBus address to default to address 126 (0x7E). A high impedance (open) on either address pin that produces a voltage above the maximum voltage also causes the PMBus address to default to address 126 (0x7E).

Address 0 is not used because it is the PMBus general-call address. This device or any other device that shares the PMBus with it cannot use addresses 11 and 127, because TI reserves those for manufacturing programming and test. TI recommends not using address 126 for any devices on the PMBus, because this is the address to which the UCD9090-Q1 defaults in case of a short or open on the address lines. Table 10 summarizes which PMBus addresses can be used. Specific devices have other SMBus or PMBus addresses assigned to them. For a system with other types of devices connected to the same PMBus, see the SMBus device address assignments table in Appendix C of the latest version of the System Management Bus (SMBus) specification. The SMBus specification is available for download at http://smbus.org/specs/smbus20.pdf.

Table 10. PMBus Address Assignment Rules

Address	STATUS	Reason
0	Prohibited	SMBus general address call
11	Avoid	Causes conflicts with other devices during program flash updates
12	Prohibited	PMBus alert response protocol
126	For JTAG use	Default value; may cause conflicts with other devices
127	Prohibited	Used by TI manufacturing for device tests

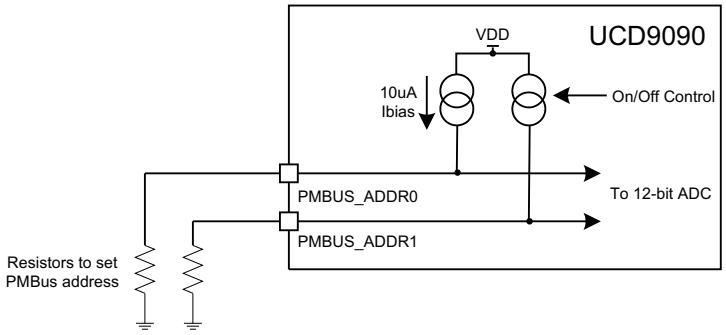


Figure 27. PMBus Address-Detection Method

CAUTION

TI recommends not selecting address 126 (0x7E) as a permanent PMBus address for any given application design. Leaving the address in default state as 126 (0x7E) enables the JTAG and does not allow using the JTAG-compatible pins (27–30) as GPIOs. The UCD9090-Q1 runs at 10% slower frequency with JTAG enabled to ensure best JTAG operation.

DEVICE RESET

- The UCD9090-Q1 has three different reset mechanisms:
  - RESET1 as determined by the voltage on the supply pin (V_{33D})
  - RESET2 as determined by the voltage on the RESET pin
  - RESET2 by a soft-reset command issued over PMBus

The UCD90160 has an integrated power-on reset (POR) circuit which monitors the supply voltage, V_{33D}. When V_{33D} is less than V_{RESET} (2.4-V maximum), the device is in the RESET1 state, and when V_{33D} is greater than V_{RESET}, the device exits the RESET1 state.

As V_{33D} increases above approximately 2.6 V, the device begins an initialization routine which includes a flash error-log integrity check. Normally, the duration of this initialization routine is approximately 20 ms (t_{INIT} in Figure 28). If the flash error-log integrity check fails, the initialization routine can last for approximately 200 ms. At the end of the initialization routine, the device begins normal operation as defined by the device configuration. During the initialization routine, one considers the device to be in the RESET2 state.

It is possible to force the device into the RESET2 state by an external circuit connected to the RESET pin (hard reset) while the device is operating within the recommended supply voltage range. A voltage less than V_{IL} for longer than t_{RESET} places the device in RESET2 and a voltage greater than V_{IH} on the RESET pin allows the initialization routine to start. It is also poslsible to force the device into RESET2 by issuing the soft-reset command (SendByte 0xDB) over PMBus. After processing of the self-clearing soft-reset command, the initialization routine begins.

The description of the state of the GPIO pins during RESET1 and RESET2 is as follows:

- All GPIO: During RESET1, these may sink or source current when approximately 0.7 V < V_{33D} < V_{RESET}.
- FPWM GPIO: During RESET2, these pins sink current.
- Other GPIO: During RESET2, these pins behave as inputs (HiZ).

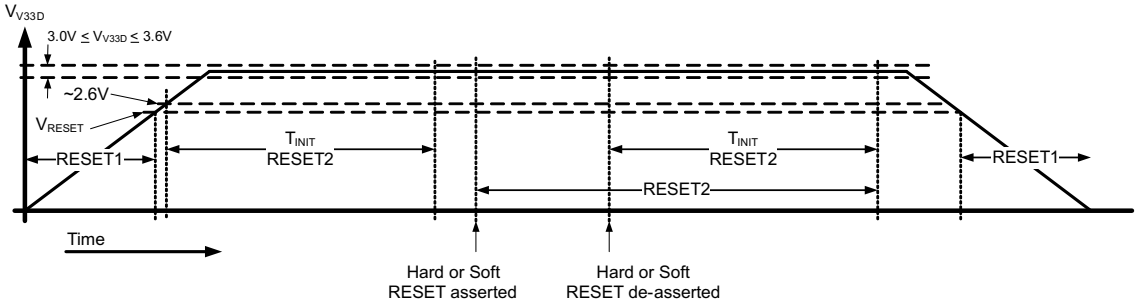


Figure 28. UCD9090-Q1 RESET1 and RESET2 Behavior

For cases where GPIO behavior during supply ramp-up might affect system circuitry, the designer may add a small filter capacitor to the GPIO to help filter the behavior. Use a 100-Ω to 200-Ω series resistor between the GPIO pin and the filter capacitor to limit the GPIO current. To avoid erroneous noise on the RESET pin, use a 10-kΩ pullup resistor (from RESET to 3.3 V) and a 1000-pF capacitor (from RESET to AVSS).

DEVICE CONFIGURATION AND PROGRAMMING

From the factory, the device contains the sequencing and monitoring firmware. Its configuration is also such that all GPOs are high-impedance (except for FPWM/GPIO pins 10–17, which it drives low), with no sequencing or fault-response operation. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that can be selected from the *Fusion GUI* Help menu, for full UCD9090-Q1 configuration details.

After the user has designed a configuration file using *Fusion GUI*, there are three general device-configuration programming options:

1. A host microcontroller can program devices in-circuit by using PMBus commands over I^2C (see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*). Each parameter write replaces the data in the associated memory (RAM) location. After the device receives all the required configuration data, it transfers that data to the associated nonvolatile memory (data flash) by issuing a special command, STORE_DEFAULT_ALL. This method is how the *Fusion GUI* normally reads and writes a device configuration.
2. The *Fusion GUI* (Figure 29) can create a PMBus or I^2C command script file which the I^2C master can use to configure the device.

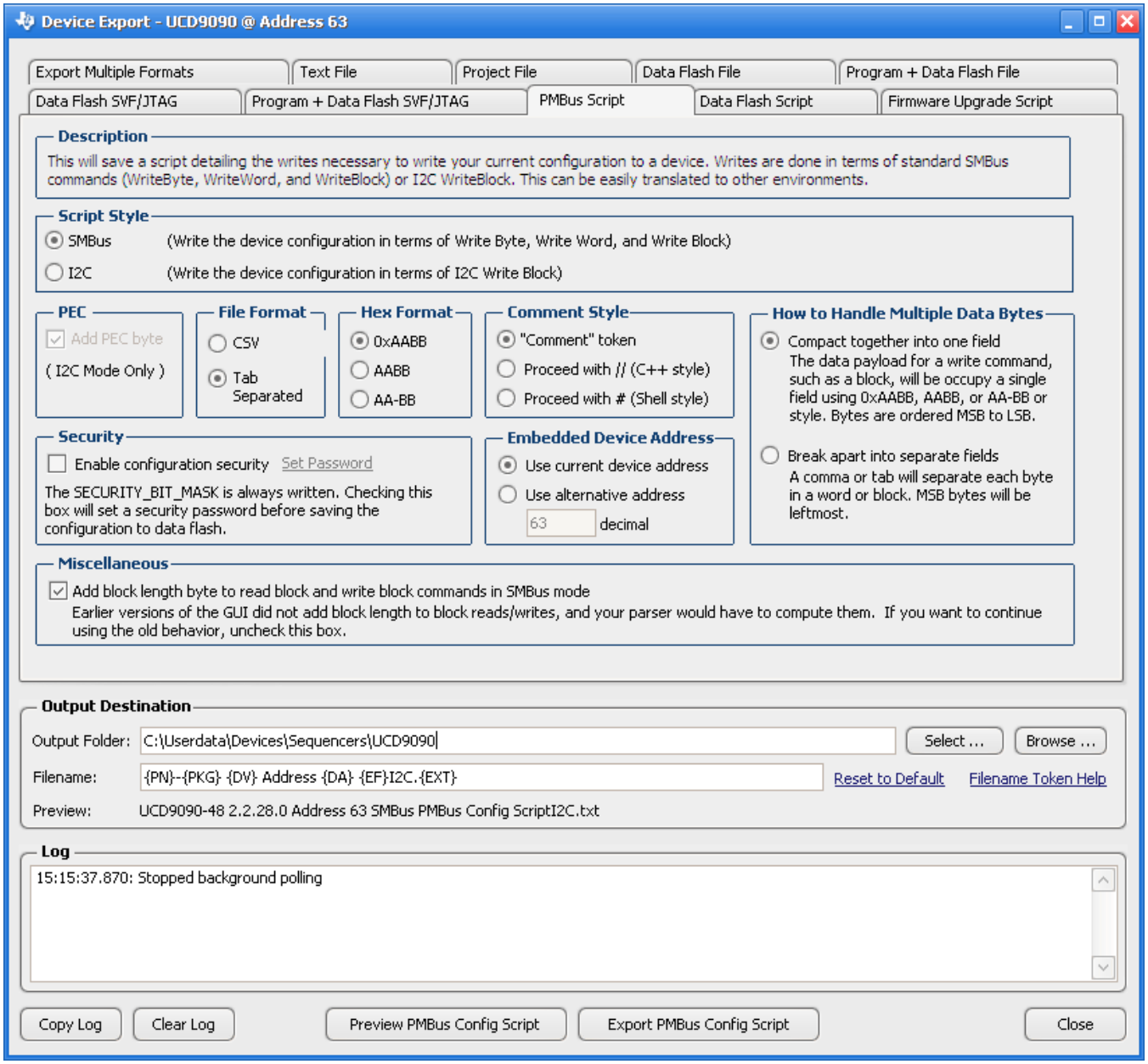


Figure 29. Fusion GUI PMBus Configuration Script Export Tool

3. Another in-circuit programming option is for the *Fusion GUI* to create a data flash image from the configuration file (Figure 30). Export of the configuration files can be in Intel hex, serial vector format (SVF), or S-record. Download the image file to the device using I^2C or JTAG. The *Fusion GUI* tools are usable on-board if the *Fusion GUI* can gain ownership of the I^2C bus on the target board.

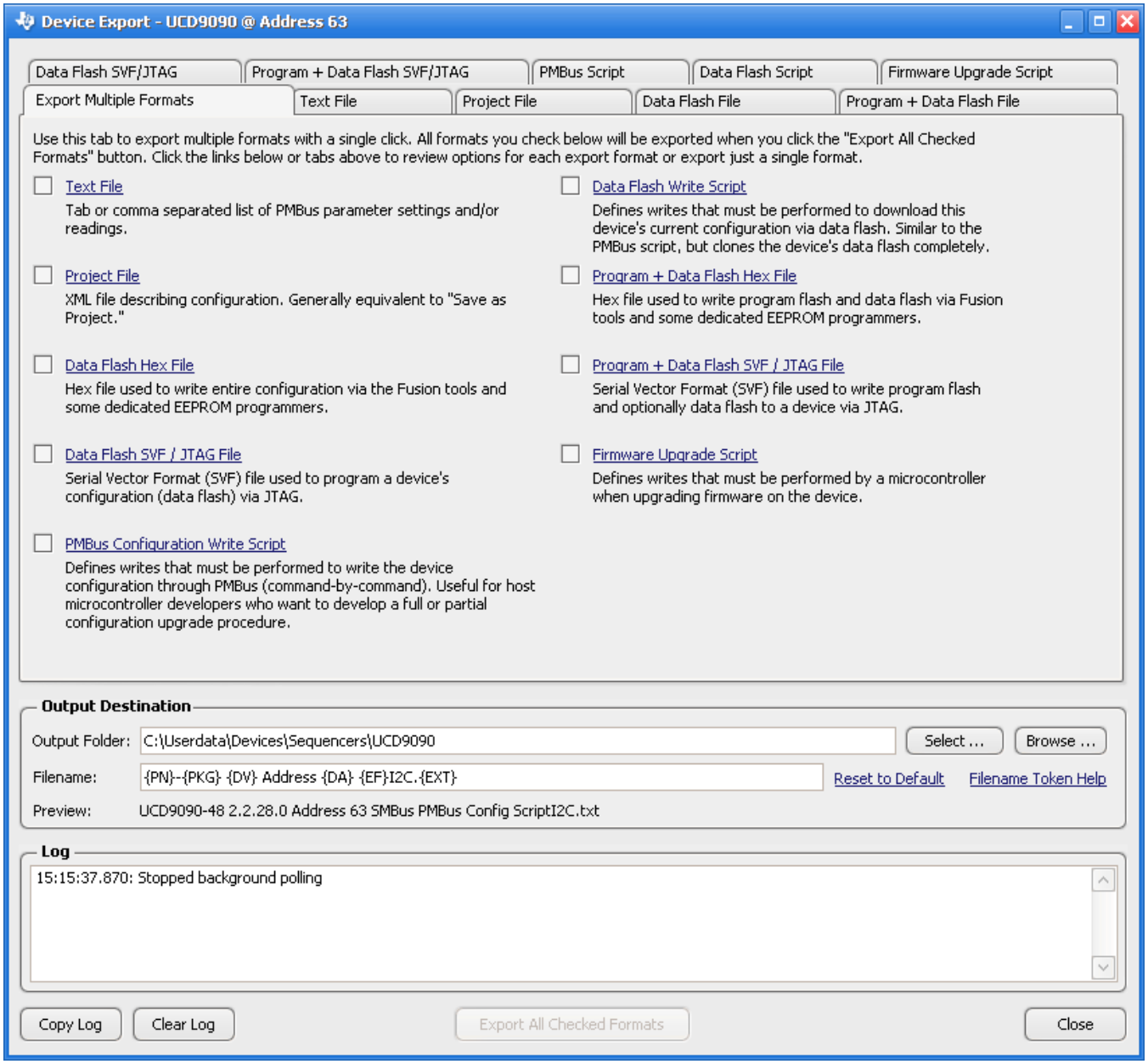


Figure 30. Fusion GUI Device Configuration Export Tool

For small runs, use a ZIF socketed board with an I^{2}C header with the standard Fusion GUI or manufacturing GUI. One can use the TI evaluation module for the UCD90xxx 64-pin sequencer and system-health monitor (UCD90SEQEVM64-650) for this purpose. The *Fusion GUI* can also create a data flash file that a dedicated device programmer can then load into the UCD9090-Q1.

To configure the device over I^{2}C or PMBus, one must power the UCD9090-Q1. The PMBus clock and data pins must be accessible with pullup resistors between 1 kΩ and 2 kΩ pulling them high to the same V_{DD} supply that powers the device. Take care not to introduce additional bus capacitance (<100 pF). One can use a gang programmer via JTAG or I^{2}C to write the user configuration to data flash before installing the device in the circuit. To use I^{2}C, multiplex the clock and data lines or have a socket assign the device addresses. The *Fusion GUI* tools are usable for socket addressing. A user can also do pre-programming using a single-device test fixture.

Table 11. Configuration Options

	Data Flash via JTAG	Data Flash via I²C	PMBus Commands via I²C
Off-Board Configuration	Data flash export (.svf type file)	Data flash export (.srec or hex type file)	Project file I²C/PMBus script
	Dedicated programmer	Fusion tools (with exclusive bus access via USB to I²C adapter)	Fusion tools (with exclusive bus access via USB to I²C adapter)
On-Board Configuration	Data flash export	Fusion tools (with exclusive bus access via USB to I²C adapter)	Fusion tools (with exclusive bus access via USB to I²C adapter)
	IC		

The advantages of off-board configuration include:

- Does not require access to device I²C bus on board
- Once soldered on board, full board power is available without further configuration.
- Can be partially reconfigured once the device is mounted.

Full Configuration Update While in Normal Mode

Although TI recommends performing a full configuration of the UCD9090-Q1 in a controlled test setup, there may be times which required updating the configuration while the device is in an operating system. Updating the full configuration based on methods listed in DEVICE CONFIGURATION AND PROGRAMMING section while the device is in an operating system can be challenging, because these methods do not permit the UCD9090-Q1 to operate as required by application during the programming. During described methods, the GPIOs may not be in the desired states ,which can disable rails that provide power to the UCD9090-Q1. To overcome this, the UCD9090-Q1 has the capability to allow full configuration update while still operating in normal mode.

Updating the full configuration while in normal mode consists of disabling data-flash write protection, erasing the data flash, writing the data-flash image, and resetting the device. There is not a requirement to reset the device immediately, but note that the UCD9090-Q1 continues to operate based on the previous configuration with fault logging disabled until reset. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that is selectable from the *Fusion GUI* Help menu, for details.

JTAG INTERFACE

One can use the JTAG port for production programming, and also use four of the six JTAG pins as GPIOs during normal operation. See the *Pin Functions* table at the beginning of the document and Table 4 for a list of the JTAG signals and the names of those which can be used as GPIOs. The JTAG port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. This device does not support boundary scan. The UCD9090-Q1 runs at 10% slower frequency while the JTAG is enabled to ensure best JTAG operation.

The JTAG interface can provide an alternate interface for programming the device. Being disabled by default allows enabling the GPIO pins with which JTAG is multiplexed. There are two conditions which enable the JTAG interface:

- On power-up, if the data flash is blank. This condition allows JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction.
- When address 126 (0x7E) is detected at power up. A short to ground or an open condition on either address pin generates address 126 (0x7E), which enables JTAG mode.

The UCD9090-Q1 system clock runs at 90% of nominal speed while in JTAG mode. For this reason, it is important not to leave the UCD9090-Q1 in JTAG mode for normal application operation.

The Fusion GUI can create SVF files (See theDEVICE CONFIGURATION AND PROGRAMMING section) based on a given data flash configuration, and which one can used to program the desired configuration by JTAG. For a Boundary Scan Description Language (BSDL) file that supports the UCD9090-Q1, see the product folder in www.ti.com.

There are many JTAG programmers in the market, and they all do not function the same. If planning to use JTAG to configure the device, confirm that the available JTAG tools can reliably configure the device before committing to a programming solution.

INTERNAL FAULT MANAGEMENT AND MEMORY ERROR CORRECTION (ECC)

The UCD9090-Q1 verifies the firmware checksum at each power up. If the checksum does not match, then the device waits for I^2C commands but does not execute the firmware. The device also verifies its configuration checksum at power up. If it does not match, the factory default configuration is loaded. This results in asserting the PMBALERT# pin and setting a flag in the status register. The error-log checksum validates the contents of the error log to ensure no corruption in that section of flash.

There is an internal firmware watchdog timer. If it times out, the device resets so that if the firmware program is corrupted, the device goes back to a known state. This is a normal device reset, so all of the GPIO pins are open-drain and the FPWM pins are driven low while the device is in reset. Checks are also done on each parameter that is passed, to make sure it falls within the acceptable range.

Error-correcting code (ECC) is used to improve data integrity and provide high-reliability storage of data-flash contents. ECC uses dedicated hardware to generate extra check bits for the user data being written into the flash memory. This adds an additional six bits to each 32-bit memory word stored into the flash array. These extra check bits, along with the hardware ECC algorithm, allow for detection and correction any single-bit error when reading the data flash.

APPLICATION INFORMATION

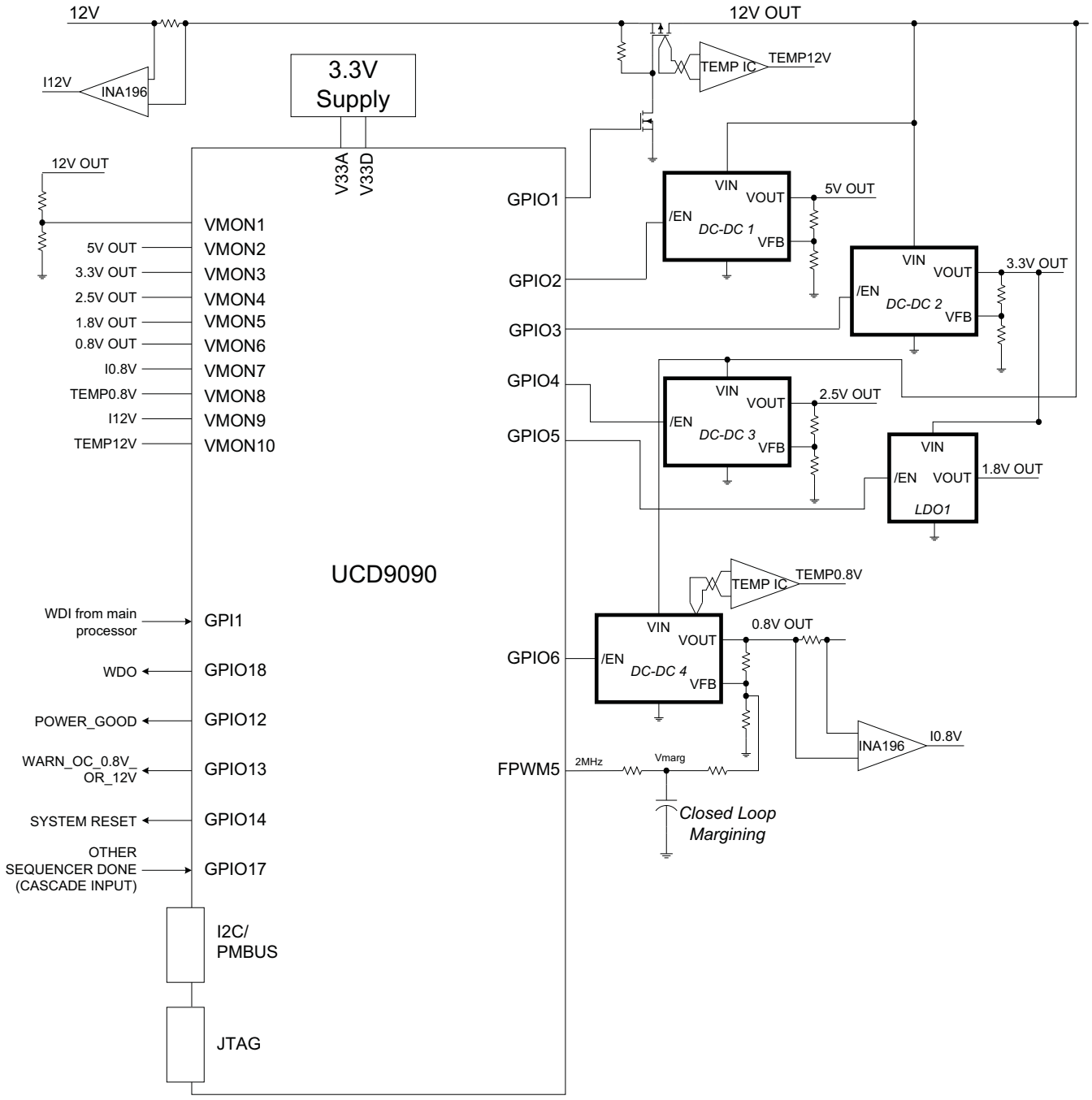


Figure 31. Typical Application Schematic

NOTE

Figure 31 is a simplified application schematic. Simplifying the schematic entailed omission of voltage dividers such as the ones placed on the VMON1 input. All VMONx pins configured to measure a voltage that exceeds the 2.5V ADC reference must have a voltage divider.

Layout Guidelines

The thermal pad provides a thermal and mechanical interface between the device and the printed circuit board (PCB). Connect the exposed thermal pad of the PCB to the device V_{SS} pins and provide at least a 4 × 4 pattern of PCB vias to connect the thermal pad and V_{SS} pins to the circuit ground on other PCB layers.

For supply-voltage decoupling, provide power-supply pin bypass to the device as follows:

- 0.1-µF, X7R ceramic in parallel with 0.01-µF, X7R ceramic at pin 35 (BPCAP)
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pin 33 (V_{33D})
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pin 34 (V_{33A})

Depending on use and application of the various GPIO signals used as digital outputs, one may desire some impedance control to quiet fast signal edges. For example, using the FPWM pins for fan control or voltage margining configures the pin as a digital *clock* signal. Route these signals away from sensitive analog signals. It is also good design practice to provide a series impedance of 20 Ω to 33 Ω at the signal source to slow fast digital edges.

Estimating ADC Reporting Accuracy

The UCD9090-Q1 uses a 12-bit ADC and an internal 2.5-V reference (V_{REF}) to convert MON pin inputs into digitally reported voltages. The least significant bit (LSB) value is $V_{LSB} = V_{REF}/2^N$ where N = 12, resulting in a VLSB = 610 µV. The error in the reported voltage is a function of the ADC linearity errors and any variations in VREF. The total unadjusted error (E_{TUE}) for the UCD9090-Q1 ADC is ±5 LSB, and the variation of VREF is ±0.5% between 0°C and 125°C and ±1% between –40°C and 125°C. V_{TUE} calculates as $V_{LSB} \times E_{TUE}$. The total reported voltage error is the sum of the reference-voltage error and V_{TUE}. At lower monitored voltages, V_{TUE} dominates reported error, whereas at higher monitored voltages, the tolerance of V_{REF} dominates the reported error. Calculate reported error using Equation 3, where REFTOL is the tolerance of V_{REF}, V_{ACT} is the actual voltage being monitored at the MON pin, and V_{REF} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = \left(\frac{1+REFTOL}{V_{ACT}}\right) \times \left(\frac{V_{REF} \times E_{TUE}}{4096} + V_{ACT}\right) - 1 \quad (3)$$

From Equation 3, for temperatures between 0°C and 125°C, if V_{ACT} = 0.5 V, then RPT_{ERR} = 1.11%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 0.64%. For the full operating temperature range of –40°C to 125°C, if VACT = 0.5V, then RPT_{ERR} = 1.62%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 1.14%.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCD9090QRGZRQ1	PREVIEW	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD9090Q	

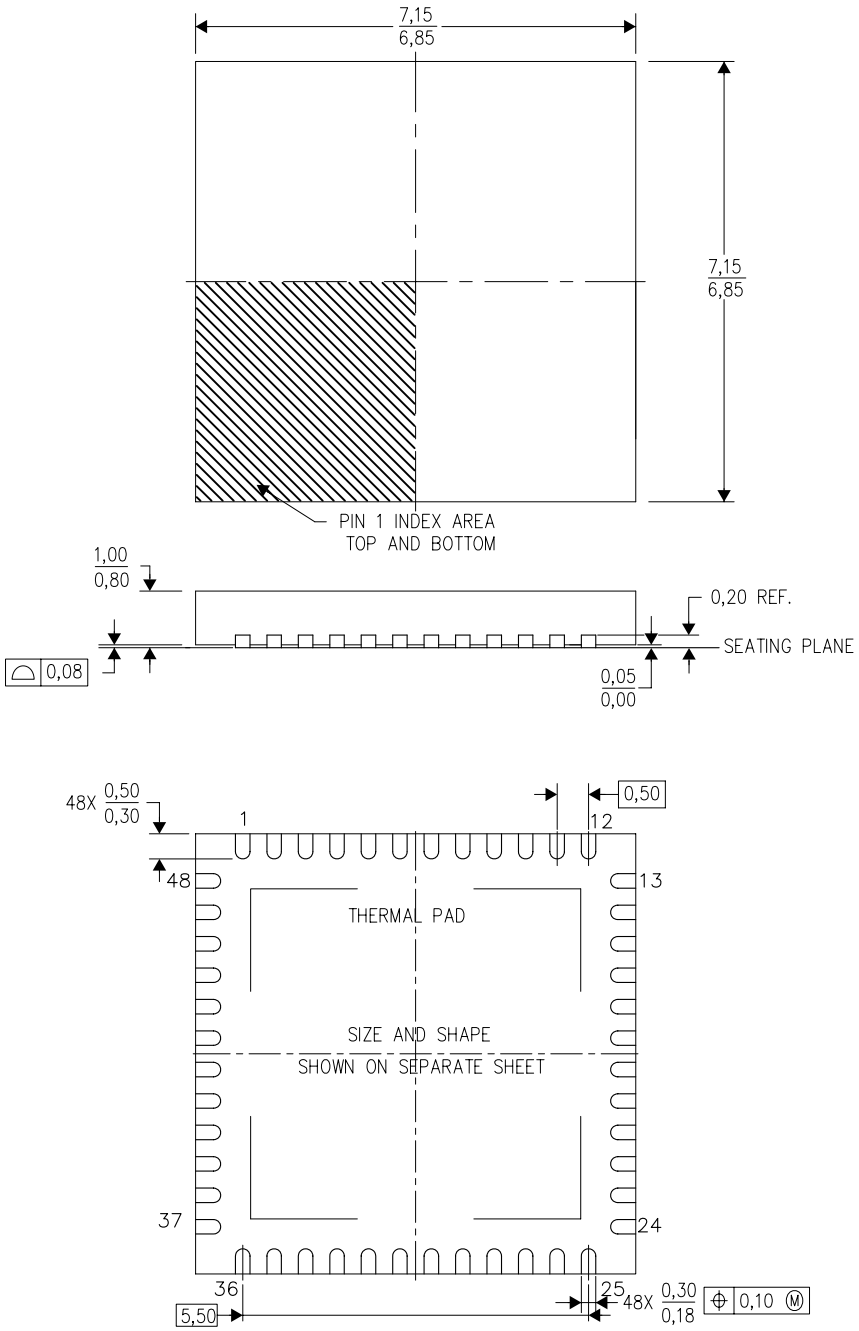
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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