# High-Current, Synchronous Buck Power Stage

**Check for Samples: UCD74120**

## FEATURES

- **Integrates Synchronous Buck Driver and NexFET™ Power MOSFETS for High Power Density and High Efficiency**
- **25-A Output Current Capability for DSP and ASIC**
- **4.7-V to 14-V Input Voltage Range**
- **Operational up to 2 MHz Switching Frequency**
- **Built-In High-Side Current Protection**
- **DCR Current Sensing for Overcurrent Protection and Output Current Monitoring**
- **Voltage Proportional to Load Current Monitor Output**
- **Tri-state PWM Input for Power Stage Shutdown**
- **UVLO Housekeeping Circuit**
- **Integrated Thermal Shutdown**
- **40-Pin, 5 mm x 7 mm, PQFN PowerStack™ Package**

## APPLICATIONS

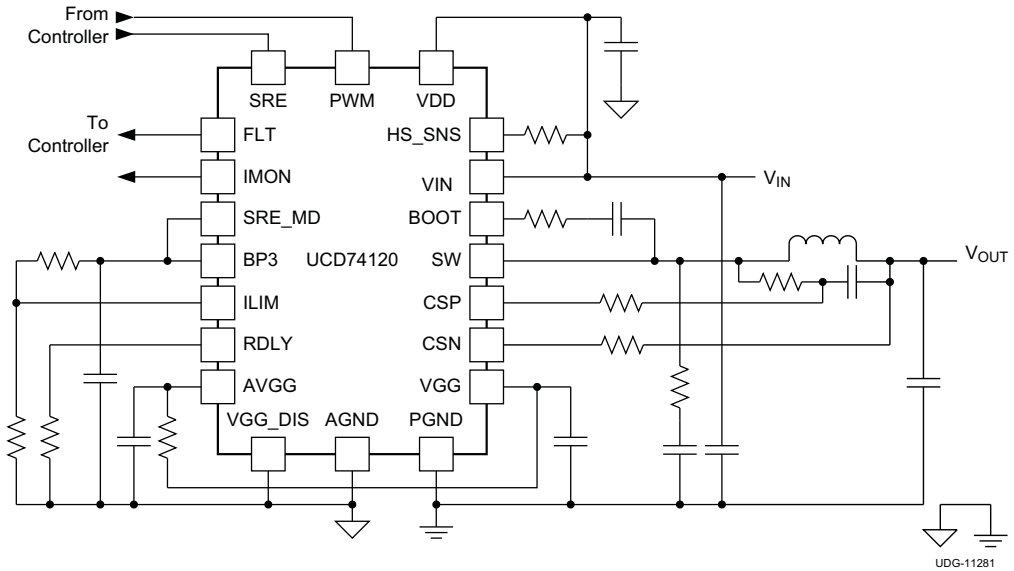
- **Digital or Analog POL Power Modules**
- **High Power Density DC-DC Converters for Telecom and Networking Applications**

## DESCRIPTION

UCD74120 is a multi-chip module integrating a driver device and two NexFET power MOSFETs into a thermally enhanced compact, 5 mm × 7 mm, QFN package. A 25-A output current capability makes the device suitable for powering DSP and ASIC. The device is designed to complement digital or analog PWM controllers. The PWM input of the driver device is 3-state compatible. Two driver circuits provide high charge and discharge current for the high-side N-channel FET switch and the low-side N-channel FET synchronous rectifier in a synchronous buck converter.

Output current is measured and monitored by a precision current sensing amplifier that processes the voltage present across an external current sense element. The amplified signal is available for use by the PWM controller on the IMON pin. On-board comparators monitor the voltage across the high-side switch and the voltage across the external current sense element to safeguard the power stage from sudden high-current loads. Blanking delay is set for the high-side comparator by a single resistor in order to avoid false reports coincident with switching edge noise. In the even of a high-side fault or an overcurrent fault, the high-side FET is turned off and the fault flag (FLT) is asserted to alert the PWM controller.

## APPLICATION DIAGRAM




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET, PowerStack are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| TEMPERATURE RANGE | PINS | PACKAGE | ORDERING NUMBER |
|---|---|---|---|
| –40°C to 125°C | 40 | RVF | UCD74120RVF |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Voltage range | VDD, VIN | –0.3 | 16 | V |
| | SW DC | –1 | 16 | V |
| | SW Pulse < 400 ns, E = 20 µJ | –2 | 20 | V |
| | SW Pulse < 64 ns | –5 | 22 | V |
| | SW Pulse < 40 ns | –7 | 25 | V |
| | VGG, AVGG (Externally supplied) | –0.3 | 7 | V |
| | BOOT DC | –0.3 | 23 | V |
| | BOOT Pulse (SW at 20 V < 400 ns) | –0.3 | 27 | V |
| | BOOT Pulse (SW at 22 V < 64 ns) | –0.3 | 29 | V |
| | BOOT Pulse (SW at 25 V < 40 ns) | –0.3 | 32 | V |
| | ILIM, VGG_DIS, IMON, FLT | –0.3 | 3.6 | V |
| | CSP, CSN, RDLY, PWM, SRE, SRE_MD | –0.3 | 5.6 | V |
| | HS_SNS | –0.3 | 16 | V |
| Temperature | $T_J$ | –40 | 150 | °C |
| | $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | UCD74120 PQFN (RVF) 40-PIN | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 28.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 15.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.1 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 0.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDD, VIN | | 4.7 | | 14 | V |
| VGG, AVGG | Externally supplied gate drive voltage | 4.6 | | 6.5 | V |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## ELECTROSTATIC DISCHARGE (ESD) PROTECTION

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Human body model (HBM) | | 1.5 | | kV |
| Charge device model (CDM) | | 500 | | V |

## ELECTRICAL CHARACTERISTICS

$T_J$ = –40°C to 125°C, $V_{VDD}$, $V_{VIN}$ = 12 V, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| $V_{VIN}$<br>$V_{VDD}$ | Input supply voltage range | | 4.7 | | 14 | V |
| $I_{VDD}$ | Supply current | Not switching, PWM = LOW | | 8 | 10 | mA |
| **GATE DRIVE UNDER-VOLTAGE LOCKOUT** | | | | | | |
| $V_{GG-ON}$ | UVLO on voltage | | | 4.4 | 4.6 | V |
| $V_{GG-OFF}$ | UVLO off voltage | | 4.1 | 4.3 | | V |
| $V_{GG-HYS}$ | UVLO hysteresis voltage | | | 80 | | mV |
| **VGG SUPPLY GENERATOR** | | | | | | |
| $V_{GG}$ | Output voltage | $V_{VIN}$ = 12 V, $I_{GG}$ = 50 mA | 5.3 | 6.0 | 6.8 | V |
| $V_{DO}$ | Dropout voltage, $V_{VDD} – V_{GG}$ | $V_{VIN}$ = 4. 7V, $I_{GG}$ = 50 mA | | | 350 | mV |
| **BP3 REGULATOR** | | | | | | |
| $V_{BP3}$ | Output voltage | $V_{VIN}$ = 12 V, $I_{BP3}$ = 2 mA | 3.0 | 3.2 | 3.3 | V |
| **DIGITAL INPUT SIGNALS (PWM, SRE)** | | | | | | |
| $V_{IH-PWM}$ | Positive-going input threshold voltage | | | 1.8 | 2.1 | V |
| $V_{IL-PWM}$ | Negative-going input threshold voltage | | 0.8 | 0.9 | | V |
| PWM | Input voltage hysteresis, ($V_{IH} – V_{IL}$) | | | 0.9 | | V |
| $V_{IH-SRE}$ | Positive-going input threshold voltage | | | 1.5 | 1.7 | V |
| $V_{IL-SRE}$ | Negative-going input threshold voltage | | 0.9 | 1.0 | | |
| SRE | Input voltage hysteresis, ($V_{IH} – V_{IL}$) | | | 0.45 | | V |
| $I_{PWM}$ | Input current | $V_{PWM}$ = 5 V | | 140 | | µA |
| | | $V_{PWM}$ = 3.3 V | | 70 | | |
| | | $V_{PWM}$ = 0 V | | –63 | | |
| $I_{SRE}$ | Input current | $V_{SRE}$ = 5 V | | 190 | | µA |
| | | $V_{SRE}$ = 3.3 V | | 12 | | |
| | | $V_{SRE}$ = 0 V | | –330 | | |
| $t_{HLD-R}$ (1) | tri-state hold-off time | $V_{PWM}$ transition from 0 V to 1.65 V, time until low-side drive falls to 0 V | 450 | 600 | 750 | ns |
| **OUTPUT CURRENT LIMIT (ILIM)** | | | | | | |
| $R_{ILIM-IN}$ (1) | ILIM input impedance | | | 250 | | kΩ |
| $V_{ILIM}$ | ILIM set point range | | 0.5 | | 3 | V |
| $V_{FLT-HI}$ | FLT output high level | $I_{LOAD}$ = –2 mA | 2.7 | 3.3 | | V |
| $V_{FLT-LO}$ | FLT output low level | $I_{LOAD}$ = 2 mA | | 0.1 | 0.6 | V |
| $t_{FAULT-FLT}$ (1) | Fault detection time. Delay until FLT asserted | $V_{ILIM}$ = 1.5 V, ($V_{CSP}$ - $V_{CSN}$) = 20 mV, $V_{CSN}$ = 1.8 V | | 350 | 475 | ns |
| $t_{DLY}$ (1) | Propagation delay from PWM to reset FLT | PWM falling to FLT falling after a current limit event is cleared. PWM pulse width ≥ 100 ns | | 85 | 200 | ns |
| **CURRENT SENSE BLANKING (RDLY, HS_SNS)** | | | | | | |
| $I_{RDLY}$ | RDLY source current | 8.06 kΩ resistor from RDLY to AGND | | 90 | | µA |
| $R_{RDLY}$ (1) | RDLY resistance range | | 5.00 | 8.06 | 25.00 | kΩ |
| $t_{BLANK}$ | HS_SNS blanking time | $R_{RDLY}$ = 8.06kΩ. From SW rising to HS fault comparator enabled. | 110 | 125 | 140 | ns |
| $I_{OCH}$ | Overcurrent threshold for high-side FET | $T_J$ = 25°C, ($V_{BOOT} – V_{SW}$) = 5.5V | | 50 | | A |

(1) Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

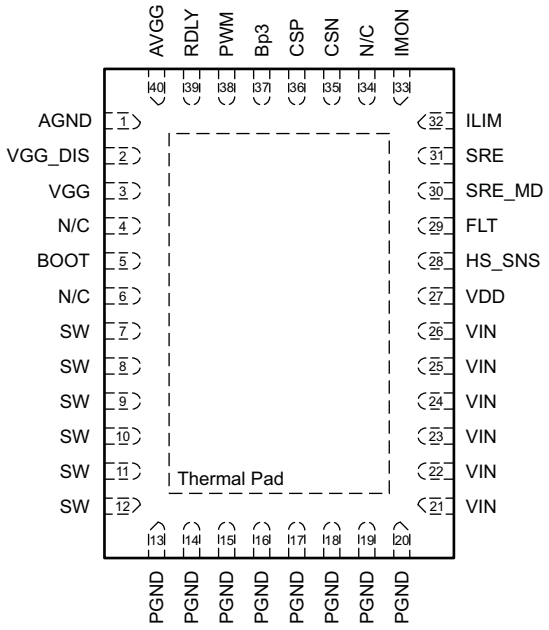
$T_J$ = –40°C to 125°C, $V_{VDD}$, $V_{VIN}$ = 12 V, all parameters at zero power dissipation (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT SENSE AMPLIFIER (IMON, CSP, CSN)** | | | | | | |
| $V_{IMON}$ | IMON voltage at no load | CSP = CSN = 1.8V | 0.46 | 0.50 | 0.54 | V |
| $R_{CS-IN}$ (2) | Input impedance | Differential, ($V_{CSP}$ - $V_{CSN}$) | | 100 | | kΩ |
| $G_{CS}$ | Closed loop DC gain | ($V_{CSP}$ - $V_{CSN}$) = 10 mV, 0.5 V ≤ $V_{CSN}$ ≤ 3.3 V | 48 | 50.2 | 52.4 | V/V |
| | | Gain with 2.49 kΩ resistors in series with CSP, CSN | 45.0 | 47.0 | 49.2 | |
| VCM (2) | Input common mode voltage range | $V_{CM}$ maximum is limited to ($V_{VGG}$ – 1.2 V) | –0.3 | | 5.3 | V |
| $V_{IMON(min)}$ | Minimum IMON voltage | $V_{CSP}$ = 1.2 V; $V_{CSN}$ = 1.3 V, $I_{IMON}$ = –250 µA | | 0.1 | 0.15 | V |
| $V_{IMON(max)}$ | Maximum IMON voltage | $V_{CSP}$ = 1.3 V; $V_{CSN}$ = 1.2 V, $I_{IMON}$ = 500 µA | 3.0 | 3.2 | 3.3 | V |
| SR (2) | Sampling rate | | | 5 | | Msps |
| **OUTPUT STAGE** | | | | | | |
| $R_{HI}$ | High side device resistance | $T_J$ = 25°C, $V_{BOOT}$ – $V_{SW}$ = 5.5 V | | 4.5 | 6.5 | mΩ |
| $R_{LO}$ | Low side device resistance | $T_J$ = 25°C | | 1.9 | 2.7 | |
| **BOOTSTRAP DIODE** | | | | | | |
| $V_F$ | Forward voltage | Forward bias current 20 mA | | 0.4 | | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{TSD-R}$ (2) | Rising threshold | | 155 | 165 | 175 | °C |
| $T_{TSD-F}$ (2) | Falling threshold | | 135 | 145 | 155 | ºC |
| $T_{TSD-HYS}$ (2) | Hysteresis | | | 20 | | ºC |

(2) Ensured by design. Not production tested.

## DEVICE INFORMATION

**RVF PACKAGE**
**40 PINS**
**(TOP VIEW)**




The thermal pad is also an electrical ground connection.

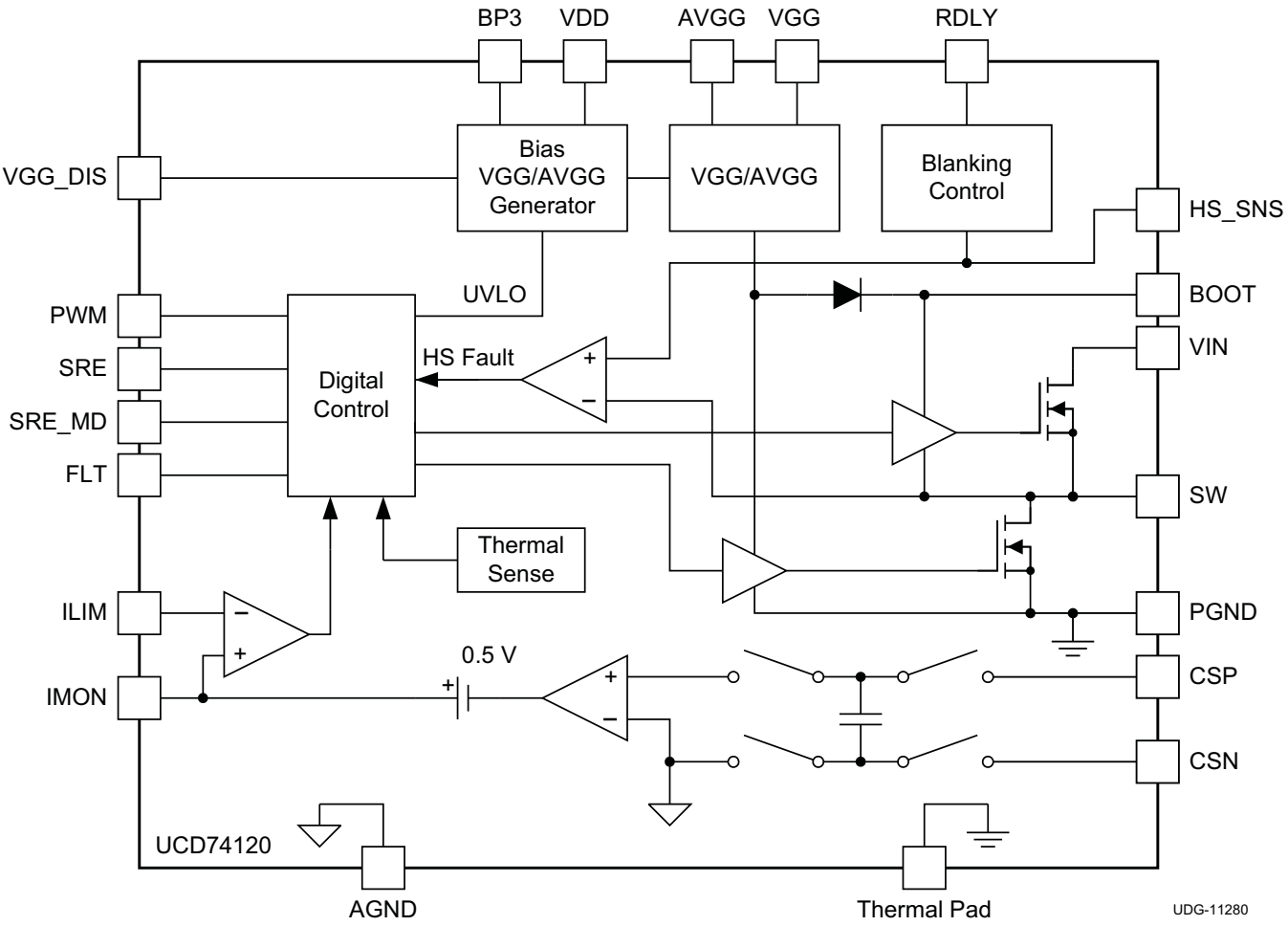
### PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 1 | | Analog ground return for all circuits except the low-side gate driver. The analog ground and power ground should be connected together at one point, near the AGND pin. |
| AVGG | 40 | I/O | Voltage supply to internal control circuitry. Connect a low ESR bypass ceramic capacitor of 100 nF or greater from this pin to AGND. Also a resistor of 1Ω to 2 Ω must be connected between VGG and this pin. |
| BOOT | 5 | I/O | Floating bootstrap supply for high side driver. Connect the bootstrap capacitor between this pin and the SW node. The bootstrap capacitor provides the charge to turn on the high-side FET. A low ESR ceramic capacitor of 220 nF or greater from this pin to SW must be connected. |
| BP3 | 37 | O | Output bypass for the internal 3.3V regulator. Connect a low ESR bypass ceramic capacitor of 1 µF or greater from this pin to AGND. |
| CSN | 35 | I | Inverting input of the output current sense amplifier and current limit comparator. |
| CSP | 36 | I | Non-inverting input of the output current sense amplifier and current limit comparator. |
| FLT | 29 | O | Fault Flag. The FLT signal is a 3.3V digital output which is asserted high when an overcurrent, over-temperature, or UVLO fault is detected. After an overcurrent event is detected, the flag is reset low on the falling edge of the next PWM pin, provided the overcurrent condition is no longer detected during the on-time of the PWM signal. For UVLO and over-temperature faults, the flag is reset when the fault condition is no longer present. |
| HS_SNS | 28 | I | A 2-kΩ resistor must be connected from this pin directly to the drain of the high-side FET. |
| ILIM | 32 | I | Output current limit threshold set pin. The voltage on this pin sets the fault threshold voltage on the IMON pin. The nominal threshold voltage range is 0.5 V to 3.0 V. When V(IMON) exceeds V(ILIM), the FLT pin is asserted and the high-side gate pulse is truncated. |
| IMON | 33 | O | Current sense linear amplifier output. The output voltage level on this pin represents the average output current. V(IMON) = 0.5 V + 50.2(V(CSP) – V(CSN)). |

## PIN FUNCTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| N/C | 4 | | Not internally connected. |
| | 6 | | |
| | 34 | | |
| PGND | 13 | | Power ground pins. These pins provide a return path for low-side FET and the low-side gate driver. |
| | 14 | | |
| | 15 | | |
| | 16 | | |
| | 17 | | |
| | 18 | | |
| | 19 | | |
| | 20 | | |
| PWM | 38 | I | PWM input. This pin is a digital input capable of accepting 3.3 V or 5 V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE mode is high, this pin controls both gate drivers. When SRE mode is low, this pin only controls the high-side driver. This pin can detect when the input drive signal has switched to a high impedance (tri-state) mode. When the high impedance mode is detected, both the high-side gate and low-side gate signals are held low. |
| RDLY | 39 | I | Requires a resistor to AGND for setting the current sense blanking time for the high-side current sense comparator and output current limit circuitry. |
| SRE | 31 | I | Synchronous rectifier enable or low-side input. This pin is a digital input capable of accepting 3.3V or 5V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE mode is high, this signal, when low, disables the synchronous rectifier FET. The low-side gate signal is held off. When SRE mode is high, this signal, when high, allows the low-side gate signal to function according to the state of the PWM pin. When SRE mode is low, this pin is a direct input to the low-side gate driver. |
| SRE_MD | 30 | I | Synchronous rectifier enable mode select pin. When pulled high to BP3, the high-side and low-side gate drive timing is controlled by the PWM pin. Anti-cross-conduction logic prevents simultaneous application of high-side and low-side gate drive. When pulled low to AGND, independent operation of the high-side and low-side gate is selected. The high-side gate is directly controlled by the PWM signal. The low-side gate is directly controlled by the SRE signal. No anti-cross-conduction circuitry is active in this mode. This pin should not be left floating. |
| SW | 7 | I/O | Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high side FET driver. |
| | 8 | | |
| | 9 | | |
| | 10 | | |
| | 11 | | |
| | 12 | | |
| VDD | 27 | I | Input voltage to internal driver circuitry and control circuitry. Connect a low ESR bypass ceramic capacitor of 100 nF or greater from this pin to AGND. |
| VGG | 3 | I/O | Gate drive voltage supply. When VGG_DIS is low, VGG is generated by an on-chip linear regulator. Nominal output voltage is 6.4 V. When VGG_DIS is high, an externally supplied gate voltage can be applied to this pin. Connect a 4.7-µF, low-ESR, ceramic capacitor from this pin to PGND. |
| VGG_DIS | 2 | I | VGG disable pin. When pulled high to BP3, the on-chip VGG linear regulator is disabled. When disabled, an externally supplied gate voltage must be connected to the VGG pin. Connect this pin to AGND to use the on-chip regulator. |
| VIN | 21–26 | I | Power input to the high-side FET. |
| Thermal Pad | | | Power Pad for better thermal performance. It is also connected to PGND internally. |

## BLOCK DIAGRAM



# DETAILED DESCRIPTION

## Introduction

The UCD74120, a power stage for synchronous buck converter with current measurement and fault detection capabilities makes it an ideal partner for digital power controllers. This device incorporates two high-current gate drive stages, two high performance NexFET power MOSFETS and sophisticated current measurement circuitry that allows for the monitoring and reporting of output load current. Two separate fault detection blocks protect the power stage from excessive load current or short circuits. On-chip thermal shutdown protects the device in case of severe over-temperature conditions. Detected faults immediately truncate the power conversion cycle in progress, without controller intervention, and assert a digital fault flag (FLT). An on-chip linear regulator supplies the gate drive voltage. If desired, this regulator can be disabled and an external gate drive voltage can be supplied. Mode selection pins allow the device to be used in synchronous mode or independent mode. In synchronous mode, the high-side and low-side gate timing is controlled by a single PWM input. Anti-cross-conduction dead-time intervals are applied automatically to the gate drives. In independent mode, the PWM and SRE pins directly control the high-side and low-side gate drive signals. Independent mode automaticly disables dead-time logic. When operating in synchronous mode, the use of the low-side FET can be disabled under the control of the SRE pin. Disablling the low-side FET facilitates start-up into a pre-bias voltage and is can reduce power consumption at light loads in some applications.

## PWM Input (PWM)

The PWM input pin accepts the digital signal from the controller that represents the desired high-side FET on-time duration. This PWM input accepts 3.3-V logic levels and 5-V input levels. The SRE mode pin sets the behavior of the PWM pin. When the SRE mode pin is asserted high, the device enters synchronous mode. In synchronous mode,PWM input signal controls the timing of both the high-side gate drive and the low-side gate drive. When PWM is high, the high-side gate drive (HS Gate) is on and the low-side gate drive is off. When PWM is low, the high-side gate drive is off and the low-side gate drive is on. Automatic anti-cross-conduction logic monitors the gate to source voltage of the FETs to verify that the proper FET is turned OFF before the other FET is turned ON. When the SRE mode pin is asserted low, the device enters independent mode. In independent mode, the PWM input controls the high-side gate drive only. When PWM is high, the high-side gate drive is ON. In independent mode, the SRE pin directly controlls the low-side FETs. No anti-cross-conduction logic is active in independent mode. The user must ensure that the PWM and SRE signals do not overlap.

PWM input signal can detect when the device has entered a tri-state mode. When tri-state mode is detected, both the high-side and low-side gate drive signals remain OFF. To support this tri-state mode, the PMW input pin has an internal pull-up resistor of approximately 50-kΩ connected to the 3.3 V input. It also has a 50-kΩ pull-down resistor to ground. During normal operation, the PWM input signal swings below 0.8 V and above 2.5 V. If the source driving the PWM pin enters a tri-state or high impedance state, the internal pull-up/pull-down resistors tend to pull the voltage on the PWM pin to 1.65 V. If the voltage on the PWM pin remains within the 0.8 V to 2.5 V tri-state detection range for longer than the tri-state detection hold-off time ($t_{HLD\_R}$), then the device enters tri-state mode and turns both gate drives OFF. This behavior occurs regardless of the state of the SRE mode and SRE pins. When exiting tri-state mode, PWM should first be asserted low. Asserting the PWM pin low ensures that the bootstrap capacitor is recharged before attempting to turn on the high-side FET.

The logic threshold of this pin typically exhibits 900 mV of hysteresis to provide noise immunity and ensure glitch-free operation of the gate drivers.

## Synchronous Rectifier Enable Input (SRE)

The SRE (synchronous rectifier enable) pin is a digital input with an internal ,10-kΩ, pull-up resistor connected to the 3.3-V input. It can accept 3.3-V logic levels and 5-V logic levels. The SRE mode pin sets the behavior of the SRE pin. When the SRE mode pin is asserted high, the device enters synchronous mode. In synchronous mode, the input, when asserted high, enables the operation of the low-side synchronous rectifier FET. The PWM input controls the state of the low-side gate drive signal. When the SRE pin is asserted low while in synchronous mode, the low-side FET gate drive is remains low, maintaining the FET OFF. While remaining OFF, current flow in the low-side FET is restricted to its intrinsic body diode. When the SRE mode pin is asserted low, the device is placed in independent mode. In this mode, the state of the low-side gate drive signal follows the state of the SRE signal. It is completely independent of the state of the PWM signal. No anti-cross-conduction logic is active in independent mode. The user must ensure that the PWM and SRE signals do not overlap.

The logic threshold of this pin typically exhibits 450 mV of hysteresis to provide noise immunity and ensure glitch-free operation of the low-side gate driver.

## SRE Mode (SRE_MD)

The SRE mode pin is a digital input that accepts 3.3-V logic levels and levels up to 5-V. This pin establishes the operational mode on the device. When asserted high, the device enters synchronous mode. In synchronous mode, the PWM input controls the behavior of both the high-side and low-side gate drive signals. When asserted low, this pin configures the device for independent mode. In independent mode, the PWM pin controls the high-side FET and the SRE pin controls the low-side FET. The SRE mode pin should be tied permanently high or low depending on the power architecture being implemented. It should not be switched dynamically while the device is in operation. This pin can be tied to the BP3 pin to permanently operate in synchronous mode.

## Input Voltage for Internal Circuits (VDD)

The VDD pin supplies power to the internal circuits of the device. An internal linear regulator that provides the $V_{VGG}$ gate drive voltage conditions the input power. A second regulator that operates off of the $V_{VGG}$ rail produces an internal 3.3-V supply that powers the internal analog and digital functional blocks. The BP3 pin provides access for a high frequency bypass capacitor on this internal rail. The VGG regulator produces a nominal output of 6.4 V. The undervoltage lockout (UVLO) circuitry monitors the output of the VGG regulator. The device does not attempt to produce gate drive pulses until the VGG voltage is above the UVLO threshold. This delay ensures that there is sufficient voltage available to drive the power FETs into saturation when switching activity begins.

## Voltage Supply for Gate Drive and Internal Control Circuitry (VGG and AVGG)

The VGG pin is the gate drive voltage for the high-current gate drive stages. The AVGG pin is the voltage supply to internal control circuitry. The on-chip regulator can supply the voltage internally on the VGG pin, or the user can supply the voltage externally. When using the internal regulator, the VGG_DIS pin should be tied low. When using an external source for VGG, the VGG_DIS pin must be tied high. The device draws current from the VGG supply in fast, high-current pulses. Connect a 4.7-µF ceramic capacitor between the VGG pin and the PGND pin as close as possible to the package.

Connect a resistor with a value between 1 Ω and 2 Ω between the AVGG pin and the VGG pin. Connect a low-ESR bypass ceramic capacitor of 100 nF or greater between the AVGG pin and AGND.

Whether the voltage is internally or externally supplied, UVLO circuitry monitors the voltage on the VGG pin. The voltage must be higher than the UVLO threshold before power conversion can occur. Note that the FLT pin is asserted high when $V_{VGG}$ is below the UVLO threshold.

## VGG Disable (VGG_DIS)

The VGG_DIS pin, when asserted high, disables the on-chip VGG linear regulator. When tied low, the VGG linear regulator derives the VGG supply from $V_{IN}$. Permanently tie the VGG_DIS pin high or low depending on the power architecture being implemented. The VGG_DIS pin should not be switched dynamically while the device is in operation.

## Switching Node (SW)

The SW pin connects to the switching node of the power conversion stage. It acts as the return path for the high-side gate driver. When configured as a synchronous buck stage, the voltage swing on SW normally traverses from below ground to well above $V_{IN}$. Parasitic inductance in the high-side FET and the output capacitance ($C_{OSS}$) of both power FETs form a resonant circuit that can produce high frequency ( > 100 MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than $V_{IN}$. Ensure that no peak ringing amplitude exceeds the absolute maximum rating limit for the pin.

In many cases, connecting a series resistor and capacitor snubber network from the switching node to PGND can dampen the ringing and decrease the peak amplitude. Make allowances for snubber network components during the layout of the printed circuit board. If testing reveals that the ringing amplitude at the SW pin exceeds the limit, then populate the snubber components.

Placing a BOOT resistor with a value between 5 Ω and 10 Ω in series with the BOOT capacitor slows down the turn-on of the high-side FET and can help to reduce the peak ringing at the switching node as well.

## Bootstrap (BST)

The BST pin provides the drive voltage for the high-side FET. A bootstrap capacitor connects this pin to the SW node. Internally, a diode connects the BST pin to the VGG supply. In normal operation, when the high-side FET is off and the low-side FET is on, the SW node puills to ground and, thus, maintains one side of the bootstrap capacitor at ground potential. The internal diode connected to VGG clamps the other side of the bootstrap capacitor . The voltage across the bootstrap capacitor at this point is the magnitude of the gate drive voltage available to switch-on the high-side FET. The bootstrap capacitor should be a low-ESR ceramic type, with a recommended minimum value of 0.22 µF. The recommended minimum voltage rating is 16 V or higher.

## Current Sense (CSP, CSN)

The CSP and CSN pins are the input to the differential current sense amplifier. The current sense positive (CSP) pin connects to the non-inverting input, the current sense negative (CSN) connects to the inverting input. This amplifier allows the device to monitor and measure the output current of the power stage. The circuitry can be used with a discrete, low value, series current sense resistor, or can make use of the popular inductor DCR sense method.

Figure 1 illustrates the DCR method of current sensing, showing a series resistor and capacitor network added across the buck stage power inductor. When the value of L/DCR is equal to RC, then the *voltage* developed across the capacitor, C, is a replica of the voltage waveform the *ideal current* would induce in the dc resistance (DCR) of the inductor. This method does *not* detect changes in current due to changes in inductance value caused by saturation effects. The value used for C should be between 0.1 µF and 2.2 µF. This maintains low impendence of the sense network, which reduces its susceptibility to noise pickup from the switching node. The trace lengths of the CSP and CSN signals should be kept short and parallel. To aid in rejection of high frequency common-mode noise, a series 2.49-kΩ resistor should be added to both the CSP and CSN signal paths, with the resistors being placed close to the pins at the package. This small amount of additional resistance slightly lowers the current sense gain.

Select power inductors with the lowest possible DCR in order to minimize losses. Typical DCR values range between 0.5 mΩ and 5 mΩ. With a load current of 25 A, the voltage presented across the CSP and CSN pins ranges between 12.5 mV and 125 mV. Note that this small differential signal is superimposed on a large common mode signal that is the dc output voltage, which makes the current sense signal challenging to process.

The UCD74120 uses switched capacitor technology to perform the differential to single-ended conversion of the sensed current signal. This technique offers excellent common mode rejection. The differential CSP-CSN signal is amplified by a factor of 47 and then a fixed 500-mV pedestal voltage is added to the result. The IMON pin senses this signal.

When using inductors with DCR values of 1.5 mΩ or higher, it may be necessary to attenuate the input signal to prevent saturation of the current sense amplifier. Add of resistor R2 as shown in Figure 2 to provide attenuation.

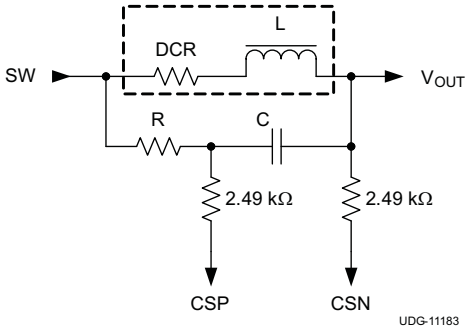



**Figure 1. DCR Current Sense**

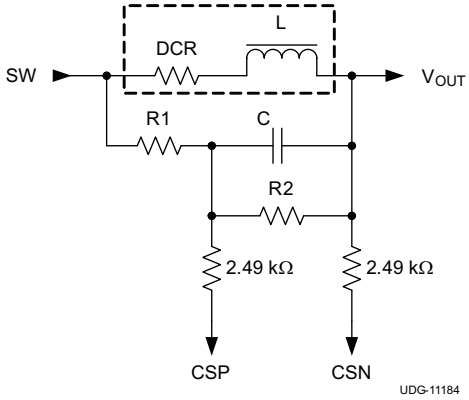



**Figure 2. Attenuating the DCR Sense Signal**

The amount of attenuation is equal to R2/(R1 + R2). The equivalent resistance value to use in the L/DCR = RC formula is the parallel combination of R1 and R2. Thus, when using the circuit shown in Figure 2,

$$\frac{L}{DCR} = \frac{C \times R1 \times R2}{(R1 + R2)} \quad (1)$$

## Current Monitor (IMON)

The IMON pin signal is a voltage proportional to the output current delivered by the power stage. Equation 2 describes the voltage magnitude when using the circuit shown in Figure 1 and reflects the gain reduction caused by the series 2.49-kΩ resistors.

$$V(I_{OUT}) = 0.5 + 47 \times DCR \times I_{LOAD} \quad (2)$$

If the calculated value of $V_{IMON}$ at maximum load exceeds 2.5 V, then the circuit of Figure 2 should be used. When using the circuit shown in Figure 2, the modified Equation 3 describes the voltage on IMON.

$$V(I_{OUT}) = 0.5 + 47 \times DCR \times I_{LOAD} \times \left(\frac{R2}{R1 + R2}\right) \quad (3)$$

In either case, the output voltage is 500 mV at no load. Current that is sourced to the load causes the IMON voltage to rise above 500 mV. Current that is forced into the power stage (sinking current) is considered *negative* current and causes the IMON voltage to fall below 500 mV. The usable dynamic range of the IMON signal is approximately 100 mV to 3.1 V. Note that this signal swing could exceed not only the maximum range of an analog to digital converter (ADC) that may be used to read or monitor the IMON signal, but also the maximum programmable limit for the fault OC threshold. For example, the UCD92xx family of digital controllers has maximum limit of 2.5 V for the ADC converter and 2.0 V for the fault overcurrent threshold, even though the input pin can tolerate voltages up to 3.3 V.

The device internally feeds the IMON voltage ($V_{IMON}$) to the non-inverting input of the output overcurrent fault comparator. Set the overcurrent threshold to approximately 150% of the rated power stage output current plus one half of the peak-to-peak inductor ripple current. This setting requires that the IMON signal remain within its linear dynamic range at this threshold load current level. This requirement may force the use of the attenuation circuit of Figure 2. Note that the IMON voltage (that goes to the output overcurrent fault comparator) is held during the blanking interval set by the resistor on the RDLY pin. This means that the IMON pin does not reflect output current changes during the blanking interval, and that a fault is not flagged until the blanking interval terminates.

## Current Limit (ILIM)

The ILIM pin feeds the inverting input of the output overcurrent fault comparator. The voltage applied to this pin sets the overcurrent fault threshold. When the voltage on the $I_{MON}$ pin exceeds the voltage on this pin, athe device flags a fault . The voltage on this pin can be set by a voltage divider, a DAC, or by a filtered PWM output. The usable voltage range of the ILIM pin is approximately 0.6V to 3.1V. This represents the linear range of the IMON signal for sourced output current. When using a voltage divider to set the threshold, add a small (0.01-µF) capacitor to BP3 to improve noise immunity.

### Blanking Time (RDLY)

The RDLY pin sets the blanking time of the high-side fault detection comparator. A resistor to AGND sets the blanking time according to the following formula, where $t_{BLANK}$ is in nanoseconds and RDLY is in kΩ. Do not use a value greater than 25 kΩ for the RDLY resistor.

$$R_{RDLY} = \frac{(t_{BLANK} - 54.4)}{8.76} \quad (4)$$

To calculate the nominal blanking time for a given value of resistance, use Equation 5.

$$t_{BLANK} = 8.76 \times R_{RDLY} + 54.4 \quad (5)$$

The blanking interval begins on the rising edge of SW. During the blanking time the high-side fault comparator remains OFF. A high-side fault flags when the voltage drop across the high-side FET exceeds the threshold set by the HS_SNS pin. Blanking is required because the high amplitude ringing that occurs on the rising edge of SW would otherwise cause false triggering of the fault comparator. The required amount of blanking time is a function of the high-side FET, the PCB layout, and whether or not a snubber network is being used. A value of 100 ns is a typical starting point. An $R_{RDLY}$ of 8.06 kΩ provides 125 ns of blanking. Maintains a blanking interval as short as possible, consistent with reliable fault detection. The blanking interval sets the minimum duty cycle pulse width where high-side fault detection is possible. When the duty-cycle of the PWM pulses are narrower than the blanking time, the high-side fault detection comparator is held off for the entire on-time and is, therefore, blind to any high-side faults.

Internally, a 90-µA current source supplies the RDLY. When using the default value of 8.06 kΩ, the voltage measured on the RDLY pin is approximately 725 mV.

### Fault Flag (FLT)

The digital output fault flag (FLT) pin assertes when the device detects a significant fault. It alerts the host controller to an event that interrupts power conversion. The device holds the FLT pin low during normal operation.

When a fault is detected, the FLT pin asserts high (3.3 V). There are four events that can trigger the FLT signal:

- output overcurrent
- high-side overcurrent
- undervoltage lockout (UVLO)
- thermal shutdown

The Fault Behavior section describes the operation of the device during fault conditions. When asserted in response to an overcurrent fault, the FLT signal resets to low at the falling edge of a subsequent PWM pulse, provided no faults are detected during the on-time of the pulse. If the fault is still present, the flag remains asserted. When asserted in response to an UVLO or thermal shutdown event, the FLT pin automatically de-asserts when the UVLO or thermal event has passed. If the on-time of the PWM pulse is less than 100 ns, then more than one pulse may be required to reset the flag.

### 3.3-V BP Regulator (BP3)

The BP3 pin provides a connection point for a bypass capacitor that quiets the internal 3.3-V voltage rail. Connect a 1-µF (or greater) ceramic capacitor from this pin to analog ground. Do not draw current from this pin. The BP3 pin is not intended to be a significant source of 3.3-V input voltage. However, the user can design an application that includes 3.3-V source for an ILIM voltage divider and a tie point for the SRE mode pin. Limit the current drawn 100 µA or less.

### Fault Behavior

When faults are detected, the device reacts immediately to minimize power dissipation in the FETs and protect the system. The type of fault influences the behavior of the gate drive signals.

Immediately after a thermal shutdown fault occurs, the device forces both high-side gate and low-side gate low. They remain low (regardless of the state of the PWM and the SRE pin) for the duration of the thermal shutdown.

A UVLO fault occurs when the voltage on the VGG pin is less than the UVLO threshold. During this time, the device drives both the high-side gate and low-side gate to low, regardless of the state of the PWM the and SRE pins. The fault automatically clears when $V_{VGG}$ rises above the UVLO threshold.

When the device detects either a high-side fault or an output overcurrent fault, the FLT pin asserts high, and the device immediately pulls both gate signals to low. During a high-side fault, the device issues a high-side gate pulse with each incoming PWM pulse. If the fault is still present, the high-side gate signal again truncates. This behavior repeats on a cycle-by-cycle basis until the fault clears or the PWM input remains low. Figure 3 illustrates this behavior

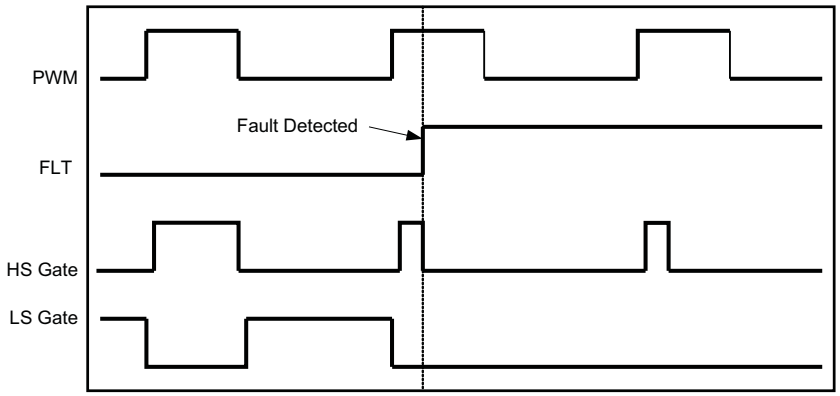



**Figure 3. High-side Overcurrent Fault Response**

When the device detects a high-side fault and output overcurrent fault concurrently, then it immediately turns OFF and holds OFF both FET drives. If the output overcurrent fault remains present at the next PWM rising edge, then the device issues no high-side gate pulsecontinue to be hold both gates OFF. Unlike the high-side fault detection circuitry, the output overcurrent fault circuitry does not reset on a cycle-by-cycle basis. The output current must fall below the overcurrent threshold before switching resumes.

## FLT Reset

With the exception of a UVLO fault or a thermal shutdown fault, subsequent PWM pulses clears the FLT flag, after it is asserted. The device clears the FLT flag at the falling edge of the next PWM pulse, provided a fault condition is not asserted during the entire on-time of the PWM pulse. If the device detects a fault during the on-time interval, the FLT pin remains asserted. Figure 4 illustrates this behavior.

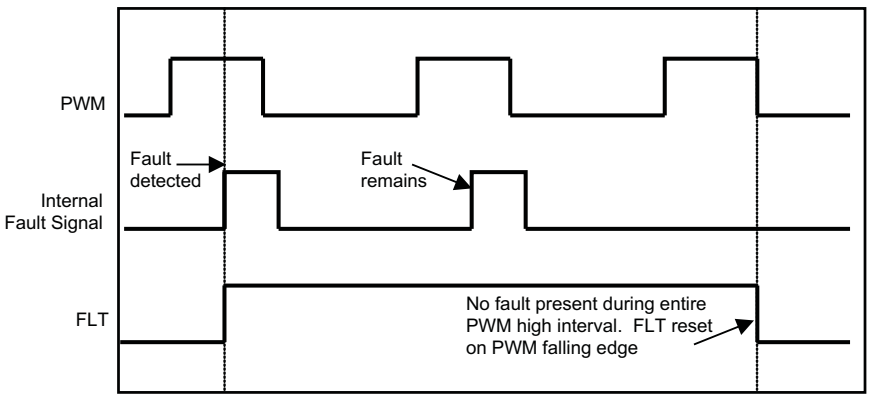



**Figure 4. FLT Reset Sequence**

Whenever the voltage on the VGG pin is below the UVLO falling threshold (as at the time of initial power-up for example) the FLT pin asserts. When the voltage on the VGG pin rises above the UVLO rising threshold, the device clears the FLT automatically. This feature permits the FLT pin to be used as a *power not good* signal at initial power-up to signify that there is insufficient gate drive voltage available to permit proper power conversion. When FLT goes low, it is an indication of *gate drive power good* and power conversion can commence. After initial power-up, the assertion of the FLT flag indicates that power conversion has stopped or has been limited by a fault condition.

### Thermal Shutdown

If the junction temperature exceeds approximately 165°C, the device enters thermal shutdown. The device asserts the FLT pin and turns OFF both gate drivers. When the junction temperature cools by approximately 20°C, the device exits thermal shutdown. The FLT flag resets immediately after exiting thermal shutdown.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| UCD74120RVFR | ACTIVE | LQFN | RVF | 40 | 3000 | Pb-Free (RoHS Exempt) | CU NIPDAU | Level-2-260C-1 YEAR | |
| UCD74120RVFT | ACTIVE | LQFN | RVF | 40 | 250 | Pb-Free (RoHS Exempt) | CU NIPDAU | Level-2-260C-1 YEAR | |

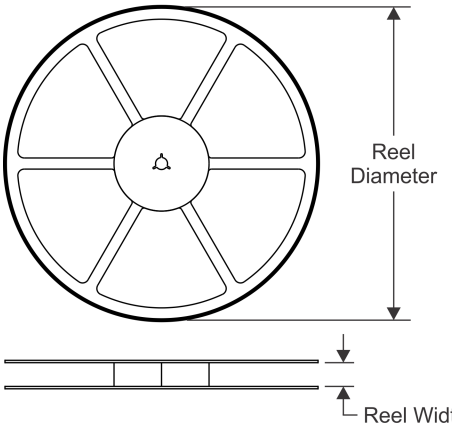
**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

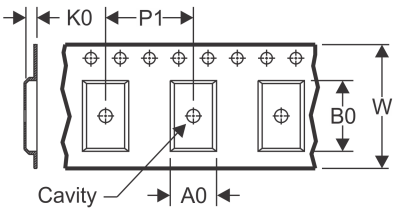
**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

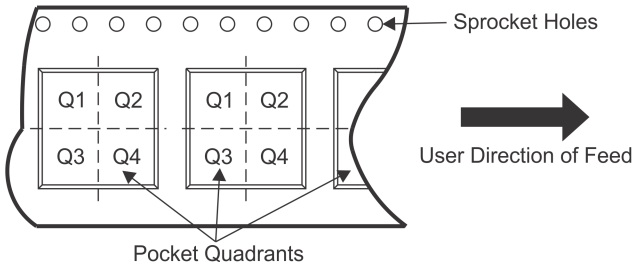



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

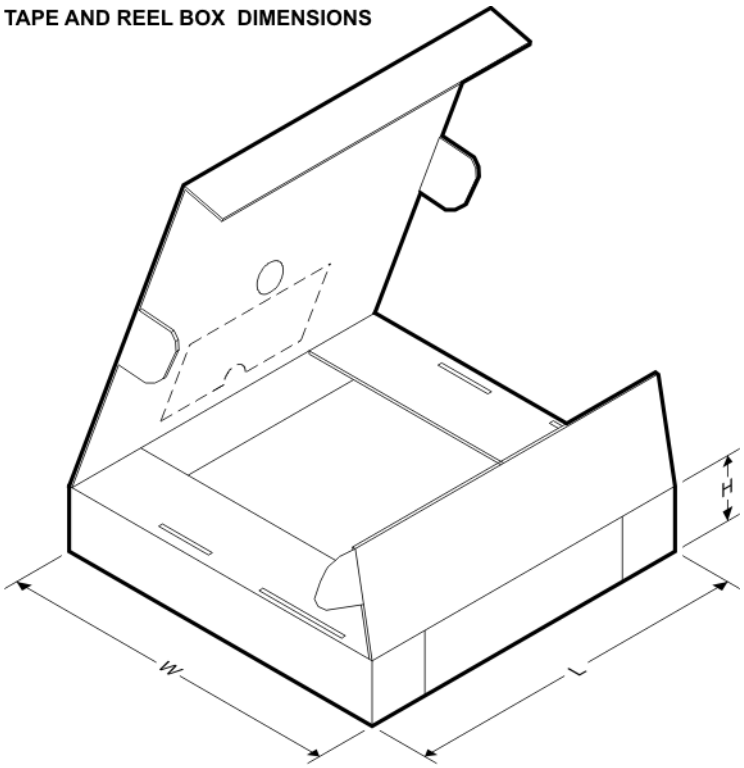
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD74120RVFR | LQFN | RVF | 40 | 3000 | 330.0 | 16.4 | 5.35 | 7.35 | 1.7 | 8.0 | 16.0 | Q1 |
| UCD74120RVFT | LQFN | RVF | 40 | 250 | 180.0 | 16.4 | 5.35 | 7.35 | 1.7 | 8.0 | 16.0 | Q1 |

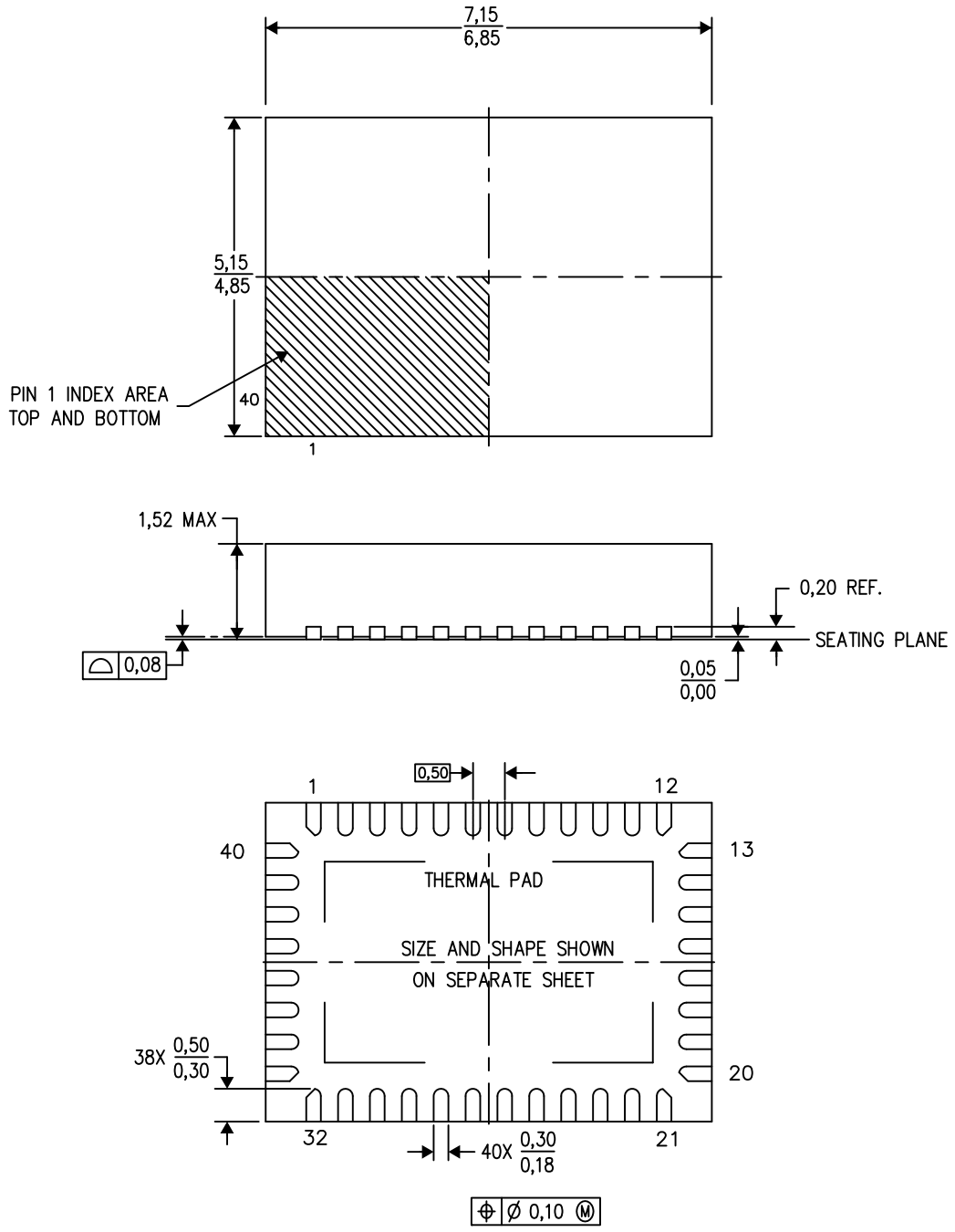
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCD74120RVFR | LQFN | RVF | 40 | 3000 | 367.0 | 367.0 | 38.0 |
| UCD74120RVFT | LQFN | RVF | 40 | 250 | 210.0 | 185.0 | 35.0 |

RVF (R–PLQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




4211383/C 04/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

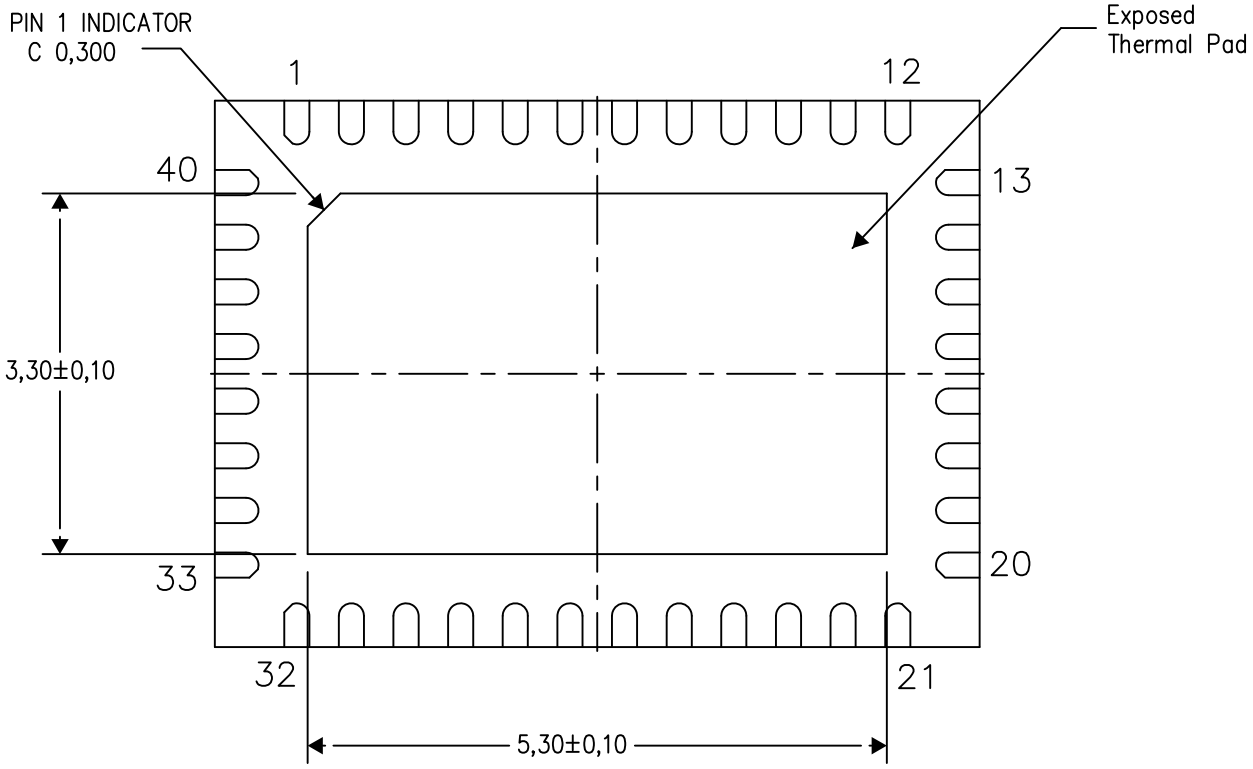
RVF (R–PLQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



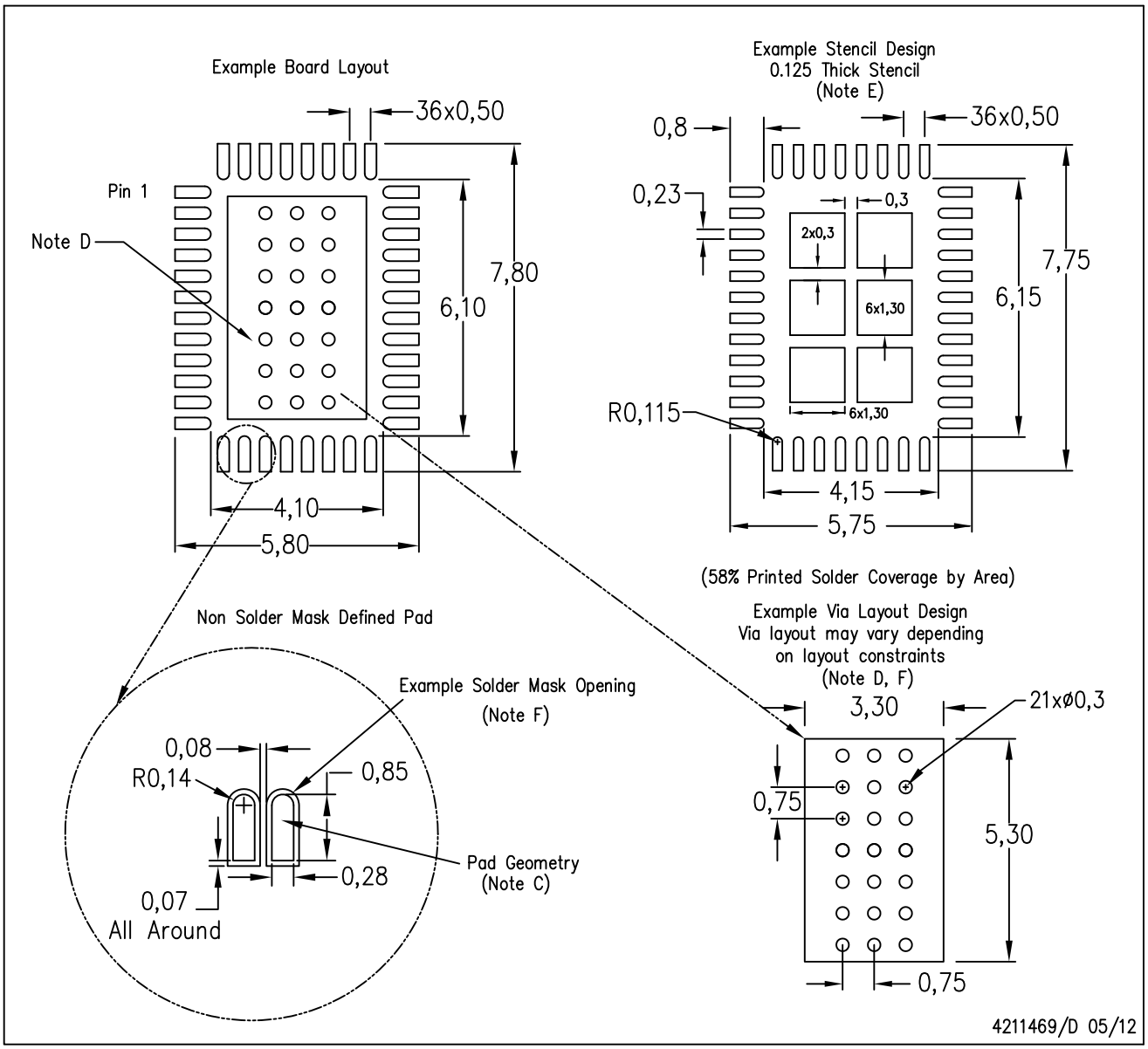

Bottom View

Exposed Thermal Pad Dimensions

4211460/D 05/12

NOTE: All linear dimensions are in millimeters

RVF (R–PLQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265