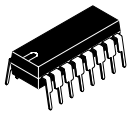


SLUS347A – MAY 1995 – REVISED APRIL 2003

9-LINE 3 TO 5 VOLT SCSI ACTIVE TERMINATOR, REVERSE DISCONNECT

FEATURES

- **Complies with SCSI, SCSI–2 and SPI–2 Standards**
- **2.7-V to 5.25-V Operation**
- **1.8-pF Channel Capacitance during Disconnect**
- **0.5-μA Supply Current in Disconnect Mode**
- **110-Ω/2.5-kΩ Programmable Termination**
- **Completely Meets SCSI Hot Plugging**
- **–400-mA Sourcing Current for Termination**
- **+400-mA Sinking Current for Active Negation Drivers**
- **Trimmed Termination Current to 4%**
- **Trimmed Impedance to 7%**
- **Current Limit and Thermal Shutdown Protection**

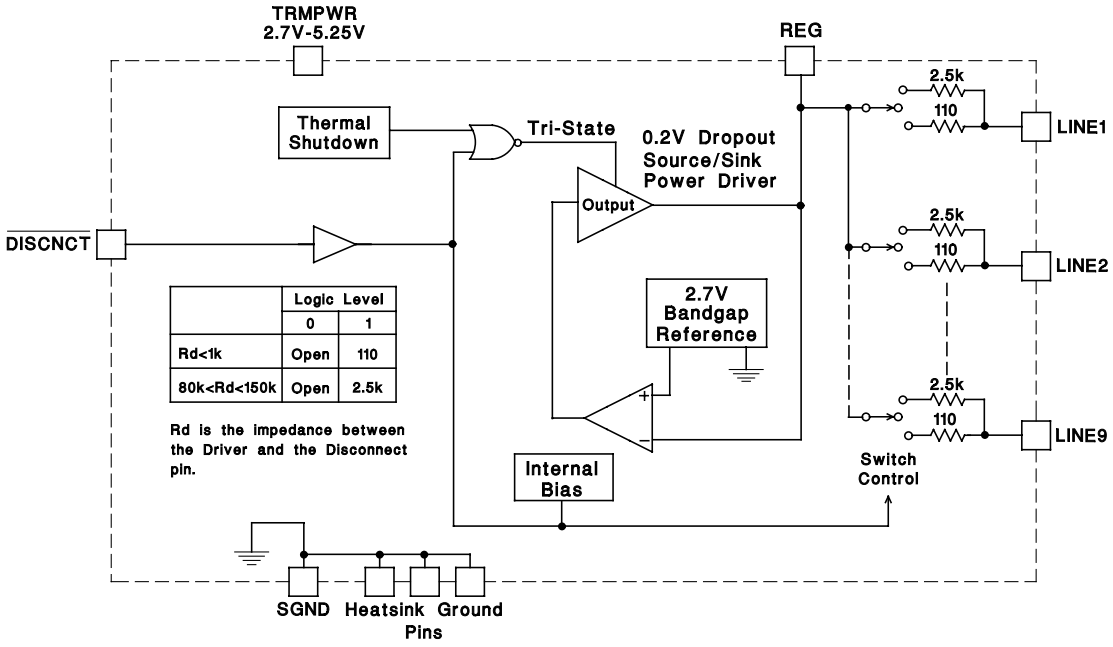
DESCRIPTION

The UCC5606 provides 9 lines of active termination for a small computer systems interface (SCSI) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UCC5606 is ideal for high performance 3.3-V SCSI systems. The key features contributing to such low operating voltage are the 0.1-V drop out regulator and the 2.7-V reference. During disconnect the supply current is typically only 0.5 μA, which makes the device attractive for battery powered systems.

The UCC5606 is designed with an ultra-low channel capacitance of 1.8 pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

BLOCK DIAGRAM



UDG–94067–1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The UCC5606 can be programmed for either a 110-Ω or 2.5-kΩ termination. The 110-Ω termination is used for standard SCSI bus lengths and the 2.5-kΩ termination is typically used in short bus applications. When driving the TTL compatible $\overline{\text{DISCNCT}}$ pin directly, the 110-Ω termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when low. When the $\overline{\text{DISCNCT}}$ pin is driven through an impedance between 80 kΩ and 150 kΩ, the 2.5-kΩ termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when driven low.

The power amplifier output stage allows the UCC5606 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5606 is pin-for-pin compatible with Unitrode's other 9-line single-ended SCSI terminators, except that $\overline{\text{DISCNCT}}$ is now active low, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5606 is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0 V or open.

Internal circuit trimming is utilized, first to trim the 110-Ω termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the maximum SCSI specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16-pin narrow body SOIC, 16-pin N and 24-pin TSSOP.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

	UCC5606	UNIT
TRMPWR voltage	7	V
Signal line voltage	0 to 7	
Regulator output current	0.6	A
Storage temperature, T_{stg}	–65 to 150	°C
Operating junction temperature, T_J	–55 to 150	
Lead temperature (soldering, 10 sec.)	300	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
TRMPWR voltage	2.7		5.25	V
Signal line voltage	0		5	V
Disconnect input voltage	0		TRMPWR	°C

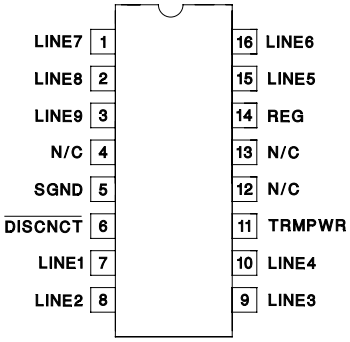
ORDERING INFORMATION

T_A	DISCONNECT STATUS	PACKAGED DEVICE†		
		DIL–16 (N)	SOIC–16 (DP)	TSSOP–24 (PWP)
0°C to 70°C		UCC5606N	UCC5606DP	UCC5606PWP

† The LQFP packages are available taped and reeled. Add TR suffix to device type (e.g. UCC5606PWPTR) to order quantities of 2,500 devices per reel.

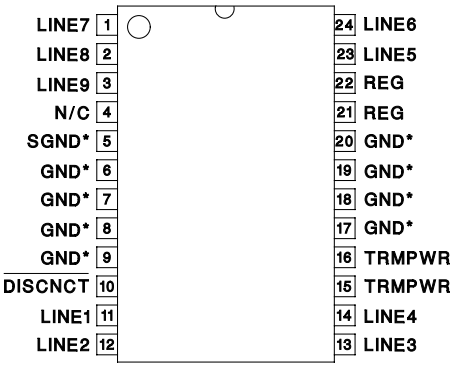
CONNECTION DIAGRAM

DIL–16 (Top View)
N Package



SOIC–16 (Top View)
DP Package

TSSOP–24 (Top View)
PWP Package



NOTE: GND* serves as a heat sink ground which must be tied to a large copper area or the grounding plate.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, $\overline{\text{DISCNCT}}$ = 3.3 V, $R_{DISCNCT}$ = 0 Ω, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr supply current	All termination lines = open		1	2	mA
	All termination lines = 0.2 V		210	218	
Power down mode	$\overline{\text{DISCNCT}}$ = 0 V		0.5	5.0	µA
Output Section (110 ohms – Terminator Lines)					
Terminator impedance		102.3	110.0	117.7	Ohms
Output high voltage	TRMPWR = 3 V (1)	2.5	2.7	3.0	V
Max output current	V_{LINE} = 0.2 V, T_J = 25°C	–22.1	–23.0	–24.0	mA
	V_{LINE} = 0.2 V	–21	–23	–24	
	V_{LINE} = 0.2 V, T_J = 25°C (1) TRMPWR = 3 V,	–20.2	–23.0	–24.0	
	V_{LINE} = 0.2 V, TRMPWR = 3 V (1)	–19	–23	–24	
	V_{LINE} = 0.5 V			–22.4	
Output leakage	$\overline{\text{DISCNCT}}$ = 0 V, TRMPWR = 0 V to 5.25 V		10	400	nA
Output capacitance	$\overline{\text{DISCNCT}}$ = 0 V, DP package (2)		1.8	2.5	pF
Output Section (2.5 kΩ – Terminator Lines) ($R_{DISCNCT}$ = 80 kΩ)					
Terminator impedance		2.0	2.5	3.0	kΩ
Output high voltage	TRMPWR = 3 V (1)	2.5	2.7	3.0	V
Max output current	V_{LINE} = 0.2 V	–0.7	–1.0	–1.4	mA
	V_{LINE} = 0.2 V, TRMPWR = 3 V (1)	–0.6	–1.0	–1.5	
Output leakage	$\overline{\text{DISCNCT}}$ = 0 V, TRMPWR = 0 to 5.25 V		10	400	nA
Output capacitance	$\overline{\text{DISCNCT}}$ = 0 V, DP package (2)		1.8	2.5	pF

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, $\overline{\text{DISCNCT}}$ = 3.3 V, $R_{DISCNCT}$ = 0 Ω, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
Regulator output voltage	5.25 V > TRMPWR > 3 V	2.5	2.7	3.0	V
Drop-out voltage	All termination lines = 0.2 V		0.1	0.2	
Short circuit current	V_{REG} = 0 V	–200	–400	–800	mA
Sinking current capability	V_{REG} = 3 V	200	400	800	
Thermal shutdown	(2)		170		°C
Thermal shutdown hysteresis	(2)		10		
Disconnect Section					
Disconnect threshold	$R_{DISCNCT}$ = 0 kΩ to 80 kΩ	0.8	1.5	2.0	V
Input current	$\overline{\text{DISCNCT}}$ = 3.3 V		30	50	µA

NOTES: 1. Measuring each termination line while other eight are low (0.2 V).
2. Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{DISCNCT}}$	7	I	Taking this pin low causes the 9 channels to become high impedance and the chip to go into low power mode. In short laptop buses an 80-kΩ to 150-kΩ resister to TERPWR terminates the bus at 2.5 kΩ. Less than 110 Ω to TERPWR enables the terminator.
GND	9		Ground reference for the device
LINE1 TO LINE9	4	I	110-Ω termination channels
REG	9	I	Output of the internal 2.7-V regulator
TRMPWR	4		Power for the device
GND*			Heat sink ground, must be tied to a large copper area or the grounding plate.

APPLICATION INFORMATION

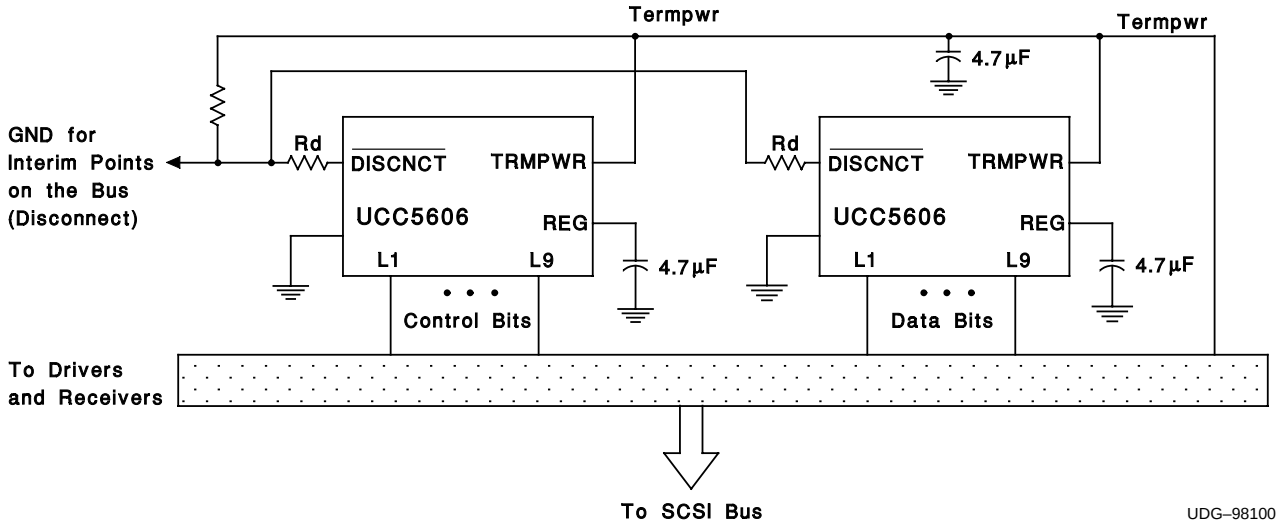


Figure 1. Typical SCSI Bus Configurations Utilizing two UCC5606 Devices

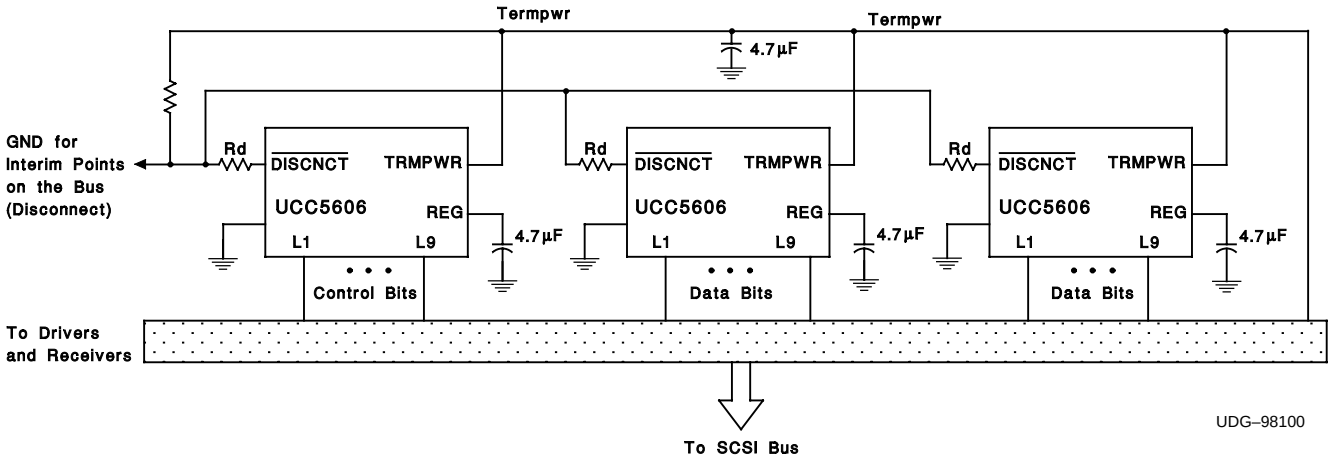


Figure 2. Typical Wide SCSI Bus Configurations Utilizing three UCC5606 Devices

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC5606DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606DPTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606DPTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606J	OBSOLETE		UTR	16		TBD	Call TI	Call TI
UCC5606PWP	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606PWPG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606PWPTR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5606PWPTRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

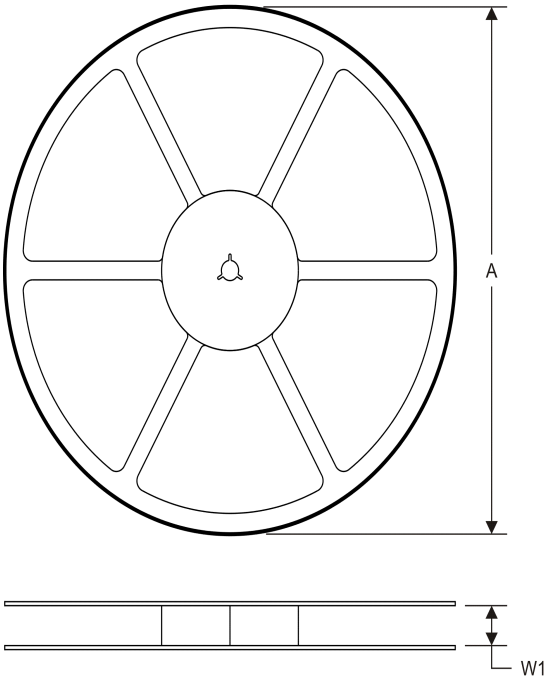
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

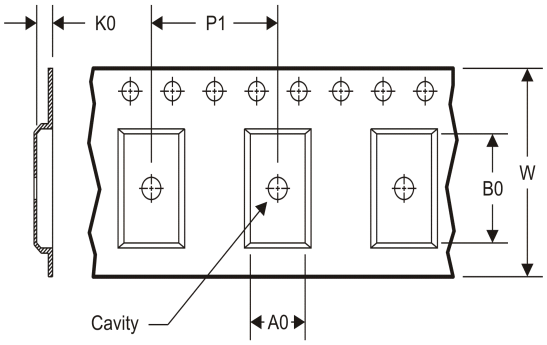
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



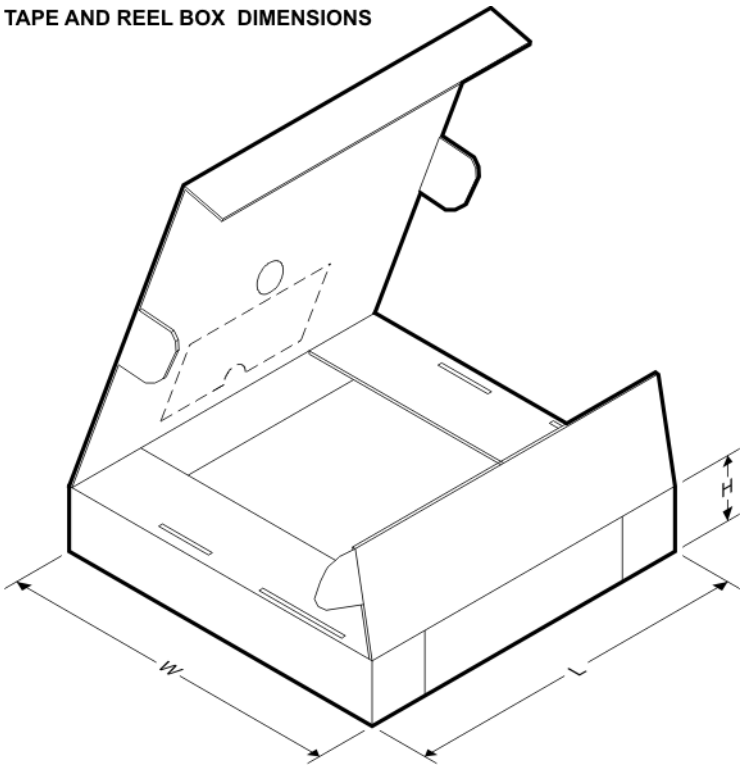
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5606DPTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC5606PWPTR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

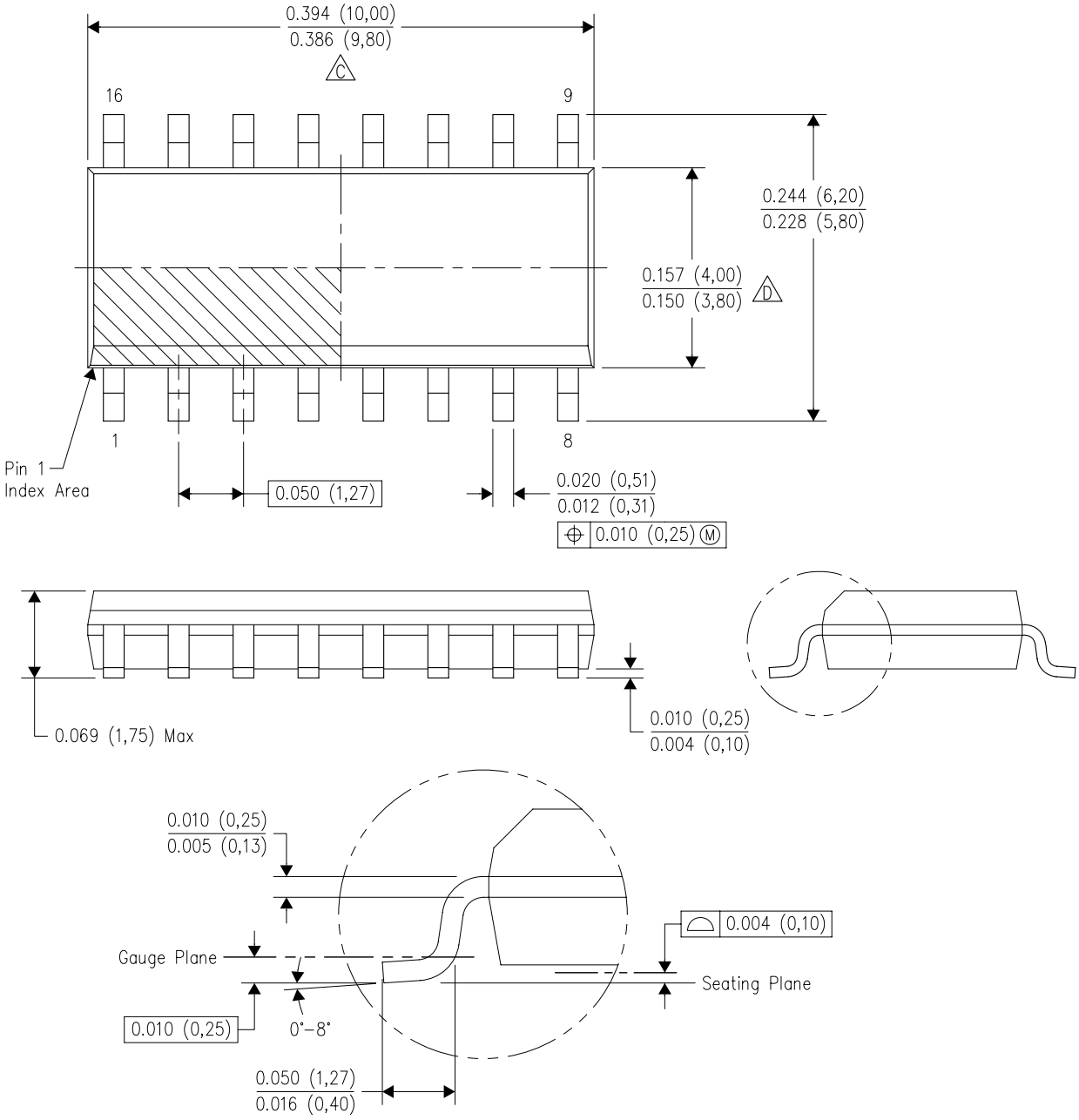
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

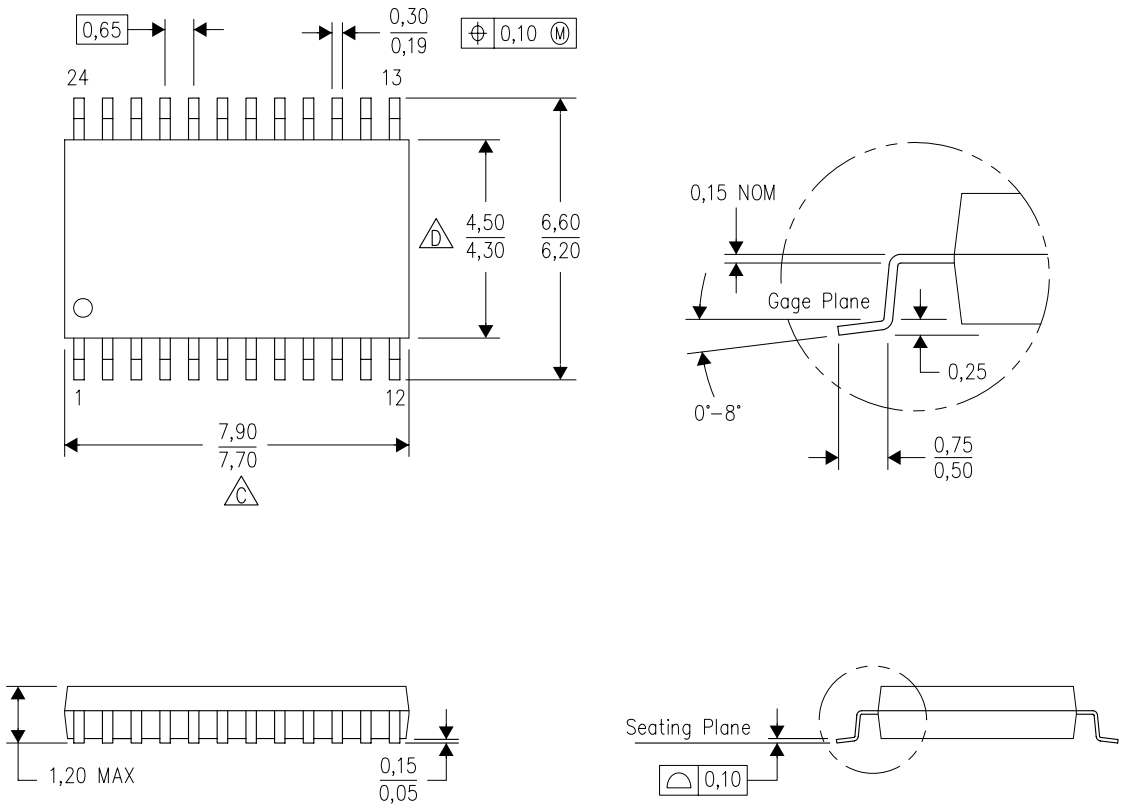
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5606DPTR	SOIC	D	16	2500	367.0	367.0	38.0
UCC5606PWPTR	TSSOP	PW	24	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

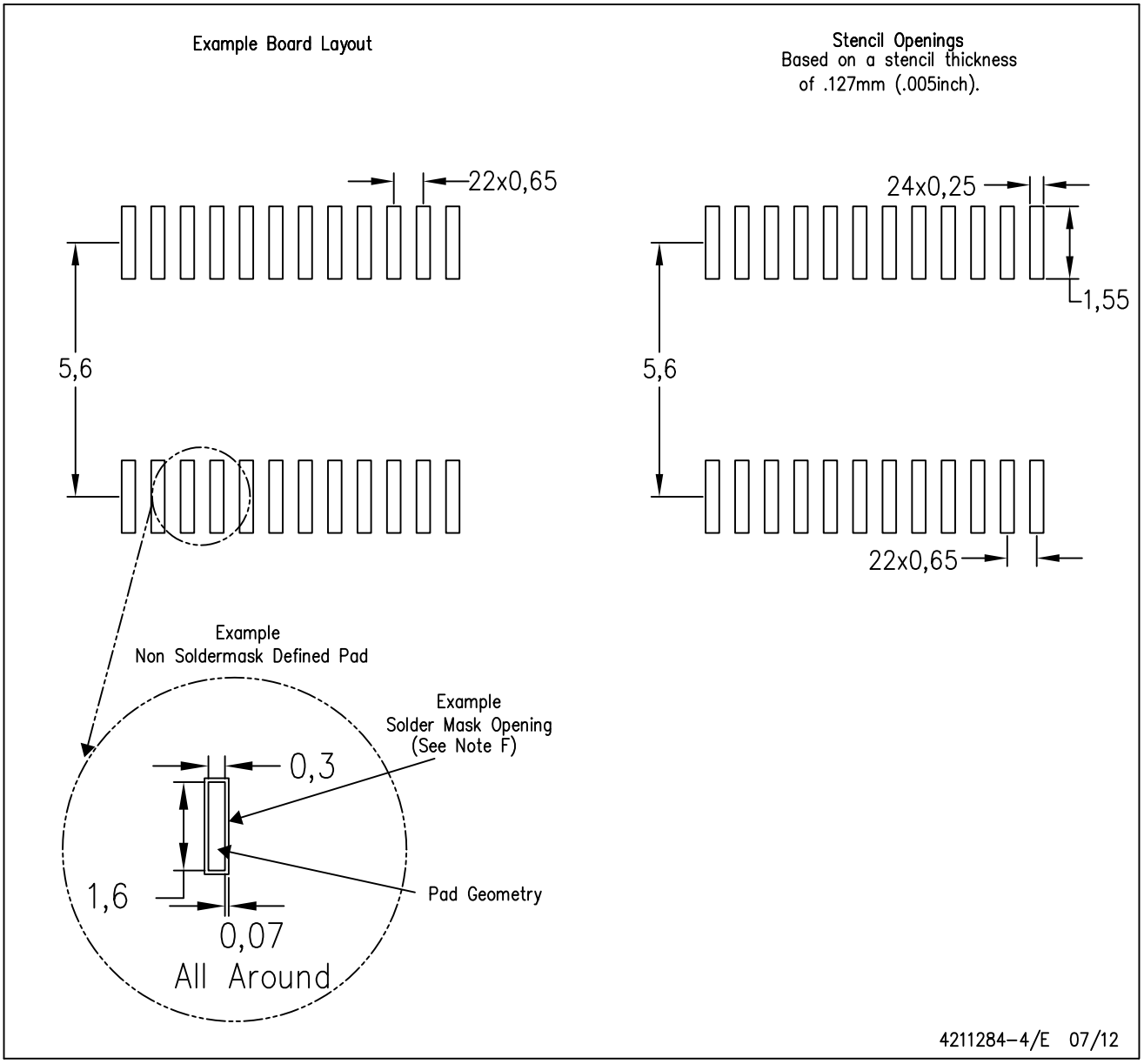
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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